Controlling the Input Impedance of Constant Power Loads

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***Abstract*—Power electronic circuits often regulate load power and present a constant power load (CPL) to the utility or other electrical source. Because CPLs exhibit a negative incremental input impedance, they pose stability concerns in both DC and AC systems. This paper presents a power converter for a constant power LED lighting load that mitigates these stability concerns by presenting a controllable input impedance to the electrical source. The use of an energy buffer allows the converter to control input power to resemble a resistive load over short times, while still delivering constant output power. Experimental results demonstrate that the converter exhibits a resistive input impedance at frequencies over 0.5 Hz while maintaining constant power to the LED load.**

I. Introduction

Constant power loads (CPLs) are becoming major power consumers on the electric grid. For example, actively controlled components of HVAC systems can demand constant power from the utility over certain time intervals, as can uninterruptible power supplies. Another example can be found in LED lighting. The energy savings projections from LED use versus traditional lighting technologies are the force behind LEDs replacing other technologies altogether [1], [2]. LED lighting can feature drivers designed to keep the light intensity impervious to fluctuations in voltage supply, which is done by commanding constant output power. This prevents the lamp from producing noticeable and annoying flickering. The consequence, however, is that if there is a decrease in voltage, the power converter responds by increasing the current draw. Thus, this CPL presents a negative incremental input impedance, which can cause instability in both DC and AC systems [3]–[6]. This paper presents the application of an electronic energy buffer for LED lighting in order to maintain constant output conditions while relaxing constant power input demands over short time intervals.

The presented converter, a switched-mode power supply, consists of two cascaded stages separated by an energy buffer. The boost step-up stage ensures that the lamp input mimics a resistive load over short transients, while the buck step-down stage implements aggressive feedback control to provide constant power to the LEDs for flicker-free light. A capacitor between the two stages buffers short-term input and output power imbalances with active control of the converter power flow accomplished with a combination of analog and digital methods. This paper presents the converter by describing the design from an energy flow standpoint and presenting test results and performance data of the prototype lamp.

Mathematical Notation

- Large signal DC quantities are denoted by capital letters, e.g. Y_{in}.
- Constant quantities or parameters are also denoted by capital letters.
- A small signal quantity is denoted by a hatted lowercase letter, e.g. $\hat{y}_{in}$.
- A total quantity, comprised of both large signal and small signal quantities, is denoted by a lowercase letter, e.g. $y_{in} = Y_{in} + \hat{y}_{in}$.

II. Energy Balance

Different load types present different input impedances to the electrical source. A resistive load, e.g. an incandescent lamp, follows Ohm's law so that the load's power p_r relates to its resistance R and the supplied voltage v as

$$p_r = \frac{v^2}{R}. \tag{1}$$

A CPL consumes constant power P_{cpl}, and the supplied voltage and load current i follow an inverse relationship:

$$P_{cpl} = iv. \tag{2}$$

Consider these two loads with the same nominal voltage and current operating point V_0 and I_0, respectively. For resistive loads, the incremental admittance is $\frac{I_0}{V_0}$. For CPLs, noting that $P_{cpl} = I_0 V_0$, the incremental admittance is $-\frac{I_0}{V_0}$. Since the CPL has an inverse I-V characteristic, its incremental admittance is negative. A load that exhibits a negative incremental impedance can destabilize a DC or AC system. For DC systems, stability criteria can determine the level of CPL penetration which will cause instabilities [4], [5]. In AC systems, CPLs generally interface through either a passive or active rectifier. This complicates the stability analysis due to the nonlinear characteristics of rectifiers. However, under certain scenarios, there are methods that can be applied to determine the stability criteria [7]–[10]. In general, decreasing the dominance of CPLs tends to stabilize an AC system.

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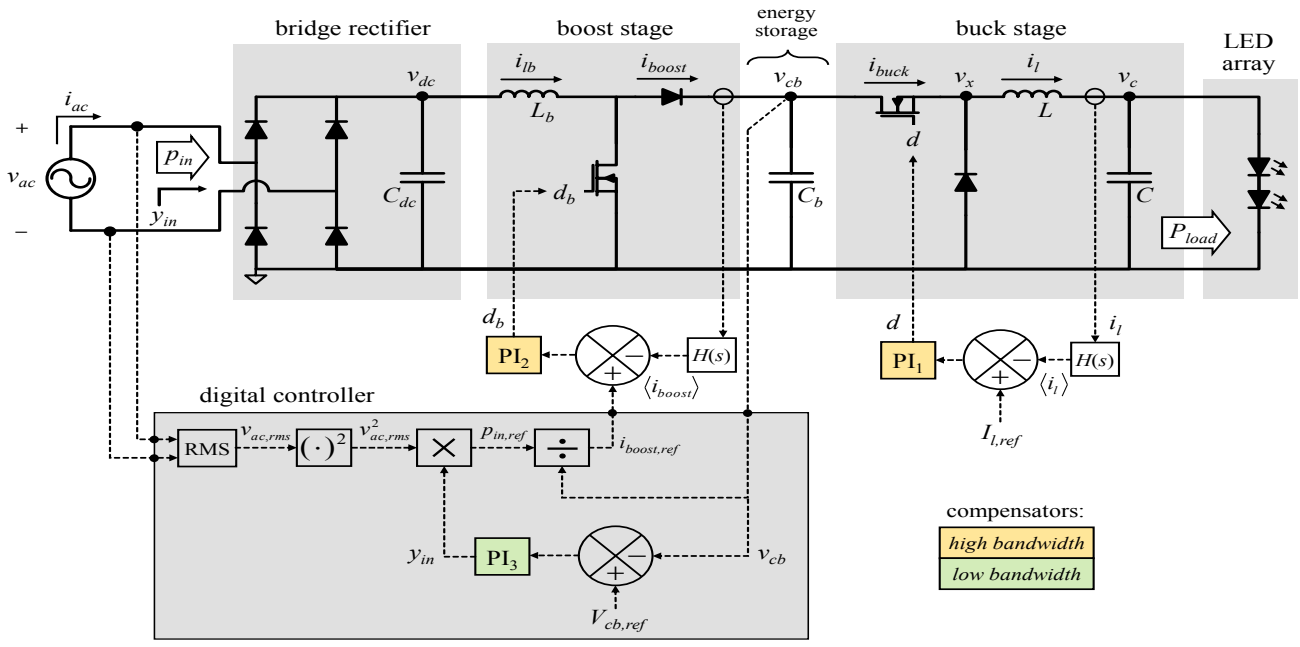

Figure 1: Overall energy buffer circuit and control scheme.

A. AC Power to Rectified Loads

Loads with single-phase passive bridge rectifiers draw distorted current waveforms from the AC system if power factor correction is not implemented. This makes it difficult to determine the rectified load's AC impedance. However, it is useful to consider the AC and DC power in estimating this impedance. From the distorted AC current drawn by a passively rectified load, the active power p_{ac} can be determined from the RMS of the in-phase fundamental current $i_{d,\,rms}$, while the reactive power q_{ac} can be determined from the RMS of the quadrature fundamental current $i_{q,\,rms}$:

$$p_{ac} = v_{ac,\,rms}\, i_{d,\,rms}, \quad \text{and} \quad q_{ac} \;\; = v_{ac,\,rms}\, i_{q,\,rms}. \quad (3)$$

The harmonic content in the current contributes no active power since it is all orthogonal to the AC voltage. Thus, neglecting diode losses in the rectifier, the DC power p_{dc} provided to the rectified load equals the AC active power p_{ac}. Since these terms are interchangeable and ultimately describe the overall input power, they are referred to as p_{in}.

In this way, the component of AC impedance contributing to active power can be determined if the impedance and power of the DC system following the rectifier is known. More thorough techniques have been developed to determine the AC impedance of rectified loads, but they require specific operating conditions. Bing and Sun et al. developed an impedance mapping method to determine the AC impedance from the DC impedance, as well as stability criteria [11]–[13]. However, their method assumes continuous current through the rectifier diodes.

In this paper, we simplify this analysis by considering power flow. That is, we can ensure that the converter is indeed resembling a resistive input impedance if its active power resembles the relationship in (1). For an AC system, this can be interpreted as the active power vs. the voltage RMS:

$$p_{in} = \frac{v_{ac,\,rms}^2}{R}. \quad (4)$$

B. Energy Buffer Circuit

To ensure the relationship (4), the input power p_{in} must be allowed to vary. However, if we intend for the load to always consume some constant power P_{load}, then the converter must be capable of buffering short-term input and output power imbalances. An energy buffer, implemented in this paper with a capacitor, accomplishes this. Other storage elements and methods can also be used. For example, reference [14] discusses a parallel multi-converter system, using batteries and fuel cells as main and parallel sources. A ripple power port is discussed in [15] that manages energy storage in converters with a DC and an AC port. In general, any energy storage element can be used so long as it can sustain a power flow imbalance for the desired amount of time.

Figure 1 presents the energy buffer circuit The boost stage at the front end steps up the rectified input voltage to maintain the energy storage capacitor C_b charged. The buck stage at the output regulates power to the load. For the application of an LED power converter, the load is an LED array. The array consumes constant power P_{load} due to a high bandwidth feedback controller in the output buck stage. This produces flicker-free lighting that is impervious to input voltage fluctuations. However, the overall input power p_{in} is allowed to vary via a high bandwidth controller in the boost stage, which is designed to present a resistive converter input impedance. The

imbalance in input and output power is absorbed by C_b, and its voltage v_{cb} determines how much energy remains stored in the energy buffer. A third feedback loop is implemented digitally as a discrete-time PI controller. It acts at low bandwidth to ensures that over large time scales, the energy storage capacitor C_b remains charged to its steady-state value.

III. Average Model Feedback Design

Circuit averaging is a powerful tool for modeling and analyzing the stability of switched converters [16]–[18], and the use of linearized small signal models further simplify the analysis. Classical control design methods are then used to determine controller gains for stable and desired performance.

Both stages of the converter operate at a switching frequency of $f_{sw} = 80$ kHz. The DC circuit input voltage v_{dc} is the output of the passive rectifier, and is approximated as 160 V during the design process, though the completed converter is designed to operate over a wide range of input voltages. The boost stage maintains a nominal voltage of 200 V on the energy buffer capacitor C_b, while the buck stage regulates the LED array load to the operating point of 65 V, 85 mA.

A. Topology Overview

The buck stage operates in continuous conduction mode (CCM), allowing for the switching duty ratio to not depend on the load [19]. The boost stage is intentionally designed to operate in discontinuous conduction mode (DCM) to occupy less space and improve efficiency by using a smaller inductor L_b. This also allows greater control over the current flowing into the boost capacitor i_{boost} [20], [21]. This is useful in order to command the converter input power at a high bandwidth.

The capacitor C_b is both the output capacitor for the boost stage, and the energy buffer storage element. A larger C_b allows the converter to sustain an imbalance in input and output power for longer durations, but is also physically larger and/or more expensive. Two parameters related to the extent of an input voltage disturbance help to determine an appropriate size for C_b, the relative drop in input voltage δ_v, and the voltage drop duration t_{drop}. These parameters are the amount the input voltage decreases as a percentage, and for how long, respectively. The converter input power p_{in} is the power provided to C_b by the boost stage. The buck stage draws power P_{load} from C_b. Then the net power p_{cb} into C_b is

$$p_{cb} = p_{in} - P_{load}. \tag{5}$$

Under steady state operation and neglecting lossless, the input power matches the load power ($p_{in} = P_{load}$), and there is no net power into C_b. However, for the input to behave as a resistive load with an admittance Y_{in}, p_{in} should depend on $v_{ac,rms}$ as

$$p_{in} = v_{ac,rms}^2 Y_{in}. \tag{6}$$

Then, to reconcile that $p_{in} = P_{load}$ when there is no input voltage drop, i.e. when $\delta_v = 0$,

$$p_{in} = (1 - \delta_v)^2 P_{load}. \tag{7}$$

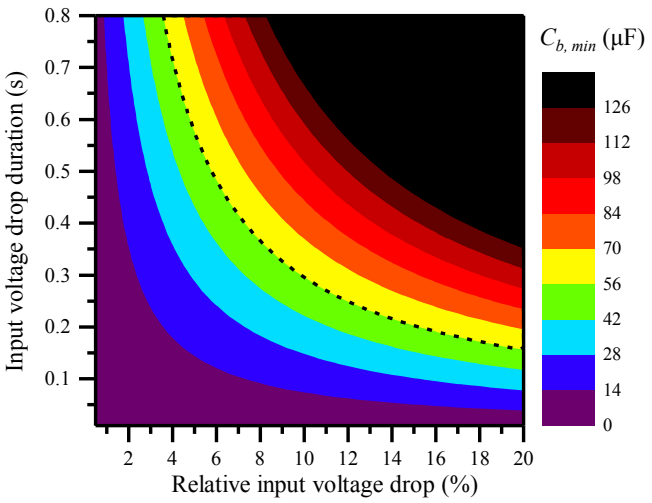

Figure 2: Minimum C_b for various voltage drop parameters δ_v and t_{drop}.

Then from (5) and (7), for an input voltage drop decrease lasting t_{drop} seconds, the capacitor acting as the energy buffer must provide E_{eb} energy to the load.

$$E_{eb} = -\left((1 - \delta_v)^2 - 1\right) P_{load}\, t_{drop} \tag{8}$$

The capacitor voltage v_{cb}, which is $V_{cb} = 200$ V in steady state, will decrease as it provides energy to the load. However, the diode in the boost stage prevents the output voltage from falling below the peak input voltage. If v_{cb} drops to this value, then the boost stage will no longer operate as intended. Therefore, we constrain that v_{cb} may not decrease below $V_{ac,pk} = 170$ V, the maximum voltage at the input, equal to the peak input AC voltage. The maximum energy $E_{eb,\,max}$ that C_b can provide to the load is then

$$E_{eb,\,max} = \frac{1}{2} C_b \left(V_{cb}^2 - V_{ac,pk}^2\right). \tag{9}$$

Substituting (8) into (9) and solving for C_b describes the minimum capacitor needed,

$$C_{b,\,min} = \frac{2\left(1 - (1 - \delta_v)^2\right) P_{load}\, t_{drop}}{\left(V_{cb}^2 - V_{ac,pk}^2\right)}. \tag{10}$$

Figure 2 provides the minimum C_b needed corresponding to a range of values for δ_v and t_{drop} according to (10). For the converter design described in this paper, we chose a capacitor C_b sized 56 µF to provide enough storage to completely buffer a 5% input voltage drop for up to 0.5s. Table I provides values for the converter's passive components along with the corresponding nominal operating characteristics. The resistance R is the incremental resistance of the nonlinear LED array at the operating point.

B. Buck Stage Feedback Design

The buck stage is a self-contained circuit designed to behave as a CPL. This is done by maintaining a constant current on the

inductor L through a high bandwidth feedback controller [22], [23]. This control scheme is shown in the buck stage of Fig. 1. The high bandwidth compensator PI_1 has a proportional gain K_1, and an integral gain to proportional gain ratio α_1. Acting as a CPL, flicker-free lighting is produced, but the buck stage presents a negative incremental input impedance to the output of the boost stage.

C. Boost Stage Feedback Design

The boost stage is designed to provide a resistive converter input impedance. The switching duty ratio in this stage dictates the average diode current i_{boost}. This allows control over the input power since by neglecting switching losses, this is equal to the power into the boost capacitor, i.e.

$$p_{in} = i_{boost} v_{cb}. \tag{11}$$

The boost stage mimics a resistive load by drawing power proportional to the stage input voltage squared, i.e.

$$p_{in} = v_{dc}^2 \, Y_{in}, \tag{12}$$

where Y_{in} is the input admittance. Then, substituting (11) into (12) and solving for i_{boost} gives

$$i_{boost,ref} = \frac{v_{dc}^2 \, Y_{in}}{V_{cb}}. \tag{13}$$

This is the desired average diode current needed to present a resistive input impedance. If the controller is able to track this quantity, then the input impedance will be resistive. This control scheme is shown within the boost stage in Fig. 1.

The high bandwidth compensator PI_2 has a proportional gain K_2, and an integral gain to proportional gain ratio α_2. With the compensator gains shown in Table I, the controller can track $i_{boost,\,ref}$ as desired, at frequencies up to 100 Hz.

D. Energy Buffer Feedback Design

A third control loop is used to keep the energy buffer charged to 200 V. In fact, there is an inherent instability caused by the previous two control loops. The buck stage draws a constant P_{load} from the capacitor, while the boost stage provides $v_{dc}^2 Y_{in}$ power to the capacitor. The net power into the boost capacitor is then

$$p_{cb} = v_{dc}^2 Y_{in} - P_{load}. \tag{14}$$

If the input and output power are not balanced and $p_{cb} \neq 0$, then v_{cb} will either increase or decrease without bound. This balance is not guaranteed from the input voltage alone, so adding a controller that adjusts the converter input admittance y_{in} can ensure v_{cb} settles to 200 V in the long term. This control loop has a relatively low bandwidth to preserve the favorable resistive input impedance that the previous control loops achieve. The controller bandwidth determines the frequencies at which the converter's input resembles either a CPL or a resistor.

This feedback loop is implemented as a discrete-time PI controller using a PSoC microcontroller with a sampling rate of 7.2 kHz. It can be approximated as a continuous PI controller since it operates with a low bandwidth relative to the sampling rate. The PI compensator outputs y_{in}. The reference current $i_{boost,ref}$, which depends on y_{in}, is then computed and sent as an analog signal to the boost stage controller to command i_{boost} in order to present resistive input impedance. This control scheme is shown in the digital controller of Fig. 1. The low bandwidth compensator PI_3 has a proportional gain K_3, and an integral gain to proportional gain ratio α_3. It is expressed as $K_3 C_3(s)$, where $C_3(s)$ is

$$C_3(s) = \frac{s + \alpha_3}{s}. \tag{15}$$

Because this controller operates at frequencies lower than either of the previous control loops, the low-frequency approximations of the two high bandwidth control loops can be used to simplify the analysis. The buck stage is replaced with an ideal CPL, and the boost diode current i_{boost} is replaced by an ideal tracking of the reference current $i_{boost,\,ref}$ from (13). That is,

$$i_{buck} = \frac{P_{load}}{v_{cb}}, \quad \text{and} \quad i_{boost} = \frac{v_{dc}^2 \, y_{in}}{v_{cb}}. \tag{16}$$

The buck stage input current i_{buck} only depends on v_{cb}. Its linear approximation in terms of the constant B_4 is

$$\hat{i}_{buck} = \underbrace{\frac{-P_{load}}{V_{cb}^2}}_{B_4} \hat{v}_{cb}. \tag{17}$$

From (16), i_{boost} is a function of three variables. The linear approximation in terms of the constants B_1, B_2, and B_3 is

$$\hat{i}_{boost} = \underbrace{\frac{V_{dc}^2}{V_{cb}}}_{B_1} \hat{y}_{in} + \underbrace{\frac{-V_{dc}^2 Y_{in}}{V_{cb}^2}}_{B_2} \hat{v}_{cb} + \underbrace{\frac{2 V_{dc} Y_{in}}{V_{cb}}}_{B_3} \hat{v}_{dc}. \tag{18}$$

The current i_{lb} is $v_{dc} \, y_{in}$, and so its linear approximation is

$$\hat{i}_{lb} = V_{dc} \, \hat{y}_{in} + Y_{in} \hat{v}_{dc}. \tag{19}$$

These approximations are shown in the small signal feedback loop diagram in Fig. 3. A perturbation reference of zero implies that the controller aims to always eliminate any perturbation in v_{cb}, thereby maintaining it at 200 V.

The capacitor voltage is described in the Laplace domain by

$$\hat{v}_{cb} = \frac{1}{s \, C_b} (\hat{i}_{boost} - \hat{i}_{buck}). \tag{20}$$

The $\hat{v}_{dc}$ to $\hat{v}_{cb}$ transfer function is

$$\frac{\hat{v}_{cb}}{\hat{v}_{dc}} = \frac{B_3}{sC_b - B_2 + B_4 + B_1 K_3 C_3(s) H(s)}, \tag{21}$$

which can be rearranged to canonical form for root locus analysis as

$$\frac{\hat{v}_{cb}}{\hat{v}_{dc}} = \frac{\frac{B_3}{sC_b - B_2 + B_4}}{1 + K_3 \frac{B_1 C_3(s) H(s)}{sC_b - B_2 + B_4}}. \tag{22}$$

A minimum compensator gain $K_{3,\,min} = 5 \times 10^{-9}$ is needed for marginal stability, and there is in fact a negative stability

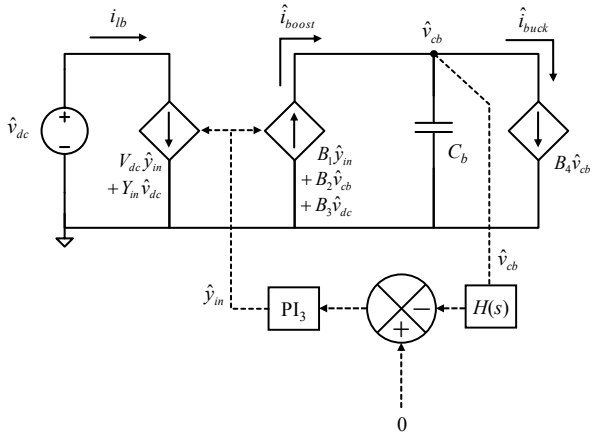

Figure 3: Linearized small signal boost capacitor feedback loop.

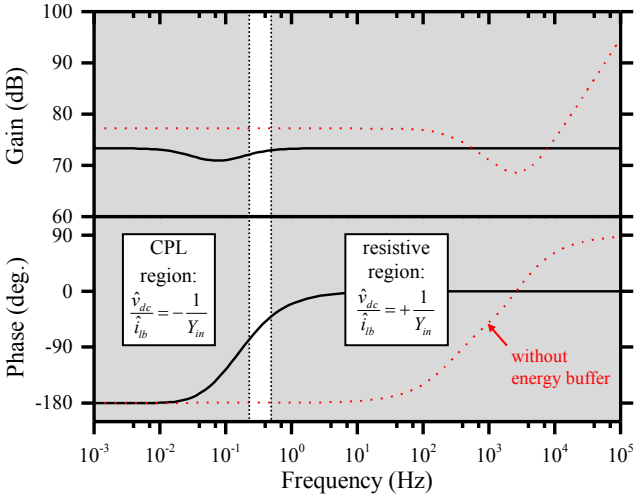

Figure 4: Bode plot of overall converter small signal input impedance. Note that the curve is 'resistive' at frequencies above 0.5 Hz, and that below 0.2 Hz, the curve exhibits -180 degrees of phase, a negative resistance.

gain margin. A gain $K_3 = 0.5 \times 10^{-6}$ is used to maintain resistive input impedance at frequencies above 0.5 Hz.

The overall input impedance is found by substituting the PI controller output $\hat{y}_{in}$ into (19), i.e.

$$\hat{i}_{lb} = V_{dc}\left(-K_3 H(s) C_3(s)\,\hat{v}_{cb}\right) + Y_{in}\hat{v}_{dc}. \tag{23}$$

Then, dividing (23) by $\hat{v}_{dc}$ and substituting the transfer function (21) reveals the incremental input admittance,

$$\frac{\hat{i}_{lb}}{\hat{v}_{dc}} = \frac{-V_{dc}B_3K_3H(s)C_3(s)}{sC_b - B_2 + B_4 + B_1K_3C_3(s)H(s)} + Y_{in}. \tag{24}$$

The inverse of (24) is the incremental input impedance. The limits at low and high frequencies are

$$\lim_{s\to 0}\frac{\hat{v}_{dc}}{\hat{i}_{lb}} = -\frac{V_{dc}}{I_{lb}}, \quad \text{and} \quad \lim_{s\to\infty}\frac{\hat{v}_{dc}}{\hat{i}_{lb}} = \frac{V_{dc}}{I_{lb}}. \tag{25}$$

From the nominal operating point values from Table I, this corresponds to a 73 dB gain with $-180°$ and $0°$ phases, respectively. Figure 4 shows the incremental impedance Bode plot and compares it with the incremental impedance if the energy buffer were not in use (shown in red). At frequencies above 0.5 Hz, the impedance magnitude is as desired, with a resistive $0°$ phase. In the long term, the converter's input must present a negative incremental impedance to maintain the nominal charge in the boost capacitor. However, with the energy buffer and the presented control techniques, this is only present for frequencies under 0.2 Hz. The energy buffer increases the bandwidth of resistive input impedance by three decades compared to the input impedance of the CPL buck stage alone. The complete controller gains used in the design in order to produce this performance are shown in Table I.

TABLE I
OPERATING POINT, PASSIVE COMPONENTS, AND COMPENSATOR GAINS

Parameter	Value	Unit	Parameter	Value	Unit
T_{sw}	12.5	µs	C_b	56	µF
P_{load}	5.53	W	L	6.8	mH
V_{dc}	160	V	C	2	µF
V_{cb}	200	V	R	100	Ω
V_c	65	V	K_1		1
I_{lb}	34.5	mA	α_1		5000
I_{boost}	27.6	mA	K_2		0.7
D_b	0.102		α_2		2×10^4
D	0.325		K_3		0.5×10^{-6}
L_b	1.5	mH	α_3		0.2

IV. Test Setup and Measurements

Ultimately this converter would be integrated into the LED bulb, however for design and testing purposes we assembled the converter using two external PCBs. One board contains the buck stage and the other contains the boost stage and a microcontroller for digital control. Figure 5 shows these PCBs inside an insulating housing.

A PSoC microcontroller digitally implements the control loop from Sec. III-D and calculates and commands the reference current $i_{boost,ref}$ needed to present the input admittance y_{in}. In terms of the RMS of the AC input voltage $v_{ac,\,rms}$, the current i_{boost} needed to present an input admittance y_{in} is

$$i_{boost,\,ref} = \frac{v_{ac,\,rms}^2\, y_{in}}{v_{cb}}. \tag{26}$$

The PSoC measures v_{cb} and the AC input voltage to determine and output $i_{boost,ref}$.

In order to test the converter, a test setup is used that allows an arbitrary AC high voltage to be delivered as an input to the device while voltage, current, and luminous output measurements are recorded. A high bandwidth light intensity sensor is contained in an enclosure placed over the test lamp, ensuring consistent illuminance measurements across various tests.

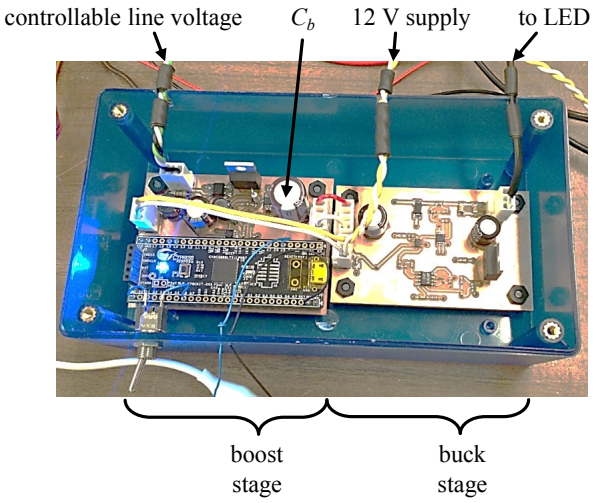

Figure 5: Energy buffer power converter and connections.

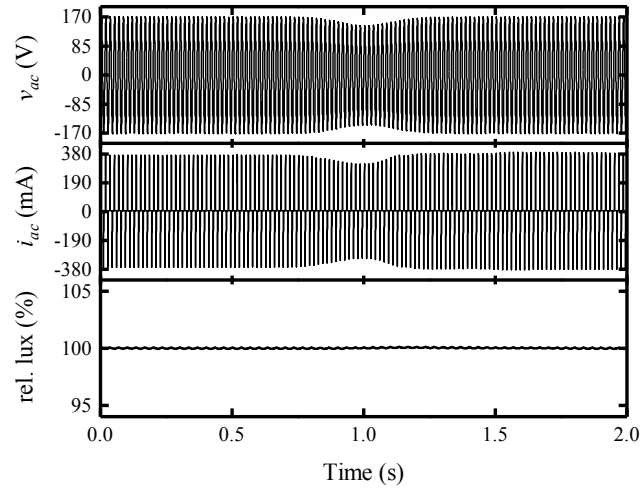

Figure 6: Measured AC voltage and current during a 15% dip in input voltage lasting 0.5 seconds. The response resembles that of a resistive load, and the light output is steady with imperceptible flicker.

A. Input Current and Power

A voltage dip fluctuation can be simulated by modulating the AC waveform by a Gaussian function. Figure 6 shows input measurements during a 15% input voltage dip lasting approximately 0.5s, along with the AC input current and luminous output. The current waveform resembles that of a resistive load since it follows a direct relationship to the input voltage. Simultaneously, the light sensor measures no significant light output fluctuations. This shows that the output continues to consume constant power as intended.

Plotting RMS or average quantities helps clarify the portrayed information. Average AC power is computed by moving average, and dividing this power by $v_{ac,\,rms}$ gives the in-phase current fundamental RMS, denoted by $i_{d,\,rms}$.

For a short 15% input voltage dip, the input current for four

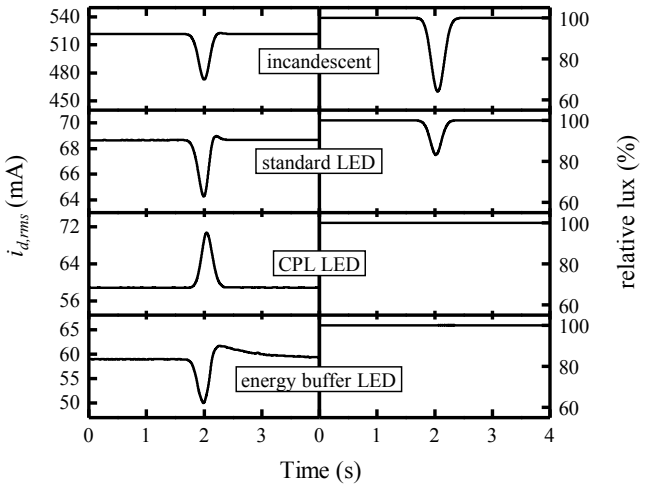

Figure 7: Response of various loads (as indicated) to a 15% dip in input voltage lasting 0.5 seconds. The input current on the vertical axis is expressed as the RMS of the in-phase fundamental current. Only the CPL and energy-buffered CPL produce steady light output with imperceptible flicker.

different lamps is compared in Fig. 7. The incandescent bulb is the best resemblance of an ideal resistive load. However, with no energy buffer, its light output is highly susceptible to the input voltage fluctuation. A standard LED bulb also exhibits resistive input impedance, but the lack of an energy buffer again results in a luminance drop. The lamp labeled "CPL LED" is the presented power converter with the boost stage shut down. In this way, the energy buffer is not active and so the input resembles a CPL since current increases during the dip in voltage. However, the light output is consistent. Finally, the presented power converter with an energy buffer exhibits favorable characteristics for both measures; Its input resembles a resistive load, and its light output is consistent and flicker free.

V. Conclusions

This paper has presented a power converter with an energy buffer that drives a CPL to power an LED load while presenting a resistive input impedance. A switched-mode power supply is implemented with cascaded boost and buck converters. The output buck stage implements high bandwidth feedback control on the load to produce high quality, consistent lighting that rejects fluctuations in input voltage. However, this creates a negative incremental input impedance. This poses a stability concern, so a boost stage is added and implements active control over the converter input power. This allows the converter to appear as a resistive load. The boost stage output capacitor acts as an energy buffer, allowing momentary power imbalances between the input and output power. The converter can be used to power other types of CPLs, and be tailored to meet the input impedance needs required by the distribution system.

ACKNOWLEDGMENT

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