DC Distributed Systems Stabilization and Performance Improvement Using Small-Signal Voltage Injection

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***Abstract*—In this paper, we introduce a method to eliminate the impact of constant power loads (CPLs) on dc distributed systems. A CPL, in small-signal sense, resembles a negative resistance that is connected to its source. The negative resistance interacts with the source output impedance, leading to instability or degrading the dynamic performance at the dc-bus. The proposed method injects the bus-voltage oscillations into the control loop of the source-converter using a high-pass filter. The filter suppresses the dc quantity of the bus-voltage, while passing the high-frequency oscillations. Thus, the operating point of the source-converter is not modified, while the dynamic performance is improved. A prototype dc distributed system was analytically analyzed, simulated, and experimentally tested in order to validate the effectiveness of the proposed controller.**

I. INTRODUCTION

A dc distributed power system is formed by installing two switching-mode regulators in series [1], as shown in Fig. 1. This configuration of delivering dc power is highly efficient, and flexible [2], [3]. Therefore, dc distributed systems (DPSs) are the base for modern satellite, aircraft, and automobile industries [4], [5]. However, DPSs are vulnerable to dynamic performance degradation or voltage instability problems, which arise due to impedance interaction between the source and load converters [6]–[11]. Many criteria [12]–[14] were proposed to eliminate the impedance interaction by assuming the source output impedance (Z_o) is pre-defined, consequently, the load-converter is designed accordingly [15]. Moreover, others proposed in [16] methods to ensure proper dynamic performance by connecting a damping-circuit to the dc-bus. The criteria and damping-circuits are not optimal solutions for modern applications (e.g., electric vehicles) because they reduce the modularity, efficiency, and power-density of DPSs. These drawbacks are tackled by shaping Z_o and/or the load input impedance (Z_{in}) using novel control techniques; these solutions are referred to as active damping methods (ADMs) [17]. The proposed ADMs in the scientific literature can be criticized for their 1) compatibility with specific dc-dc converters such as [18], [19], 2) ability to stabilize a DPS while the dynamic performance is not optimized such as [20], [21], and 3) compromising the power-density of DPSs as in [22]. Therefore, we propose a novel method that addresses the above-mentioned critiques of ADMs by injecting the high-frequency oscillations of the dc-bus voltage into the source-converter control loop. The method is independent of the source-converter type, and it guarantees highly improved dynamic performance. Since the output voltage and a high-pass filter are used to improve the dynamic performance of DPSs, the efficiency and power-density of DPSs are not affected. The effectiveness of the controller was proven using lab experiments, simulations, and analytical analyses.

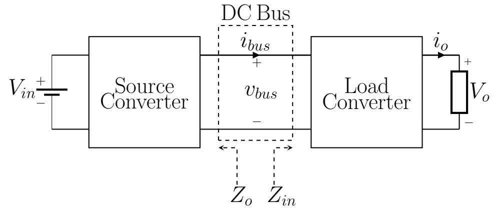

Fig. 1. Two-converters distributed power system.

II. STABILITY AND DYNAMIC PERFORMANCE OF DPSS

The stability of dc distributed systems can be evaluated by representing the source and load converters by their Thevenin and Norton forms [23], respectively, as shown in Fig. 2a. Thus, the dc-bus-voltage (v_{bus}) can be expressed as

$$\tilde{v}_{bus} = \frac{\tilde{v}_s - Z_o\tilde{i}_{bus}}{1 + Z_oY_{in}} = \frac{\tilde{v}_s - Z_o\tilde{i}_{bus}}{1 + Z_o/Z_{in}} \tag{1}$$

where $\tilde{v}_s$ is the Thevenin-equivalent voltage of the source, $\tilde{i}_{bus}$ is the bus current, i_l is the load current, and Y_{in} is the admittance of the load system (i.e., $Y_{in} = 1/Z_{in}$). The bus-voltage will be unstable if (1) has a pole in the right-half-plane (RHP). An unstable pole will occur if an impedance overlap occurred within the bandwidth of the load-converter controller (ω_{BW}) [12], [24], as demonstrated in Fig. 2b for $\omega_{BW} = 1 \times 10^4 rad/sec$. On the other hand, the dynamic performance can be highly deteriorated if $|Z_o/Z_{in}|$ is close to

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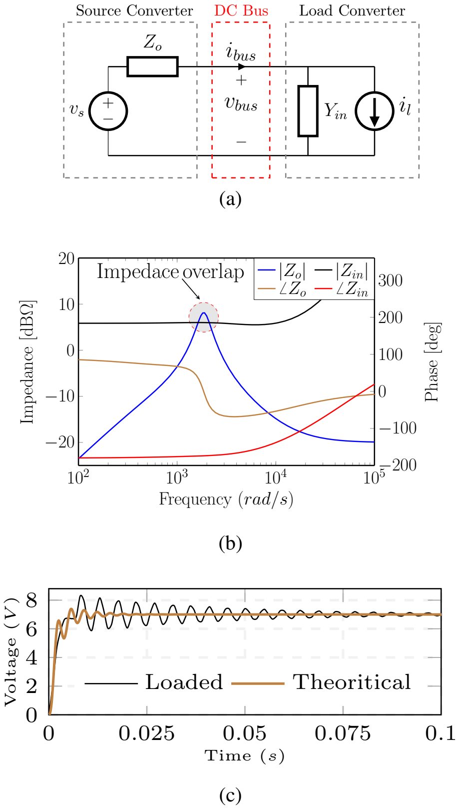
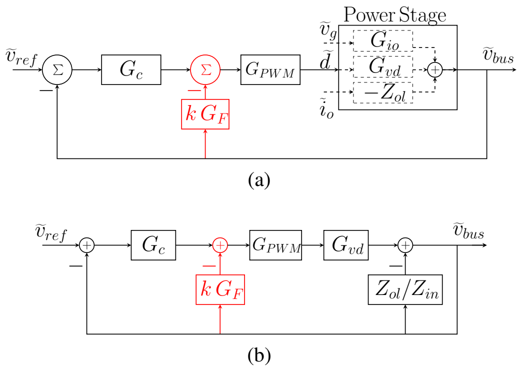


(a)

(b)

(c)

Fig. 2. A distributed power system (a) modeling, (b) typical impedance overlap, (c) loaded response.



(a)

(b)

Fig. 3. The proposed controller representation for (a) unloaded, (b) loaded models.

unity [25]–[27]. For example, Fig. 2c compares the theoretical response of a source-converter with its loaded response.

III. THE PROPOSED CONTROLLER

. We propose a controller, for the source-converter, that improves the dynamic performance of DPSs. The controller utilizes the oscillations of the dc-bus voltage using a high-pass filter, as show in Fig. 3a. The filter eliminates the dc component of the dc-bus, so the steady-state operating point is not changed, and the dynamic performance is improved. The bus-voltage, using the proposed controller, can be expressed as

$$\begin{aligned}\widetilde{v}_{bus} =& \widetilde{v}_{ref}\frac{T}{1+T+k\,G_f G_{pwm} G_{vd}} \\ &-\widetilde{i}_{bus}\frac{Z_{ol}}{1+T+k\,G_f G_{pwm} G_{vd}} \\ &+\widetilde{v}_g\frac{G_{io}}{1+T+k\,G_f G_{pwm} G_{vd}}\end{aligned} \tag{2}$$

where

$$T = G_c G_{vd} G_{pwm} \tag{3}$$

$\widetilde{v}_{ref}$ is the reference of the bus-voltage, T is the voltage loop gain, G_c is the controller transfer function, G_{vd} the control-to-output voltage transfer function, G_{pwm} is the pulse width modulation gain, G_f is the high-pass filter transfer function, k is a constant, $\widetilde{i}_{bus}$ is the bus current, $\widetilde{v}_g$ is the input voltage, G_{io} is the input-to-output voltages transfer function, and Z_{ol} is the open-loop source output impedance. The closed-loop output impedance (Z_o) is shown in red in (2). The source-converter is assumed to be fed from an ideal voltage source, hence, $\widetilde{v}_g$ is neglected hereinafter. According to (2), Z_o can be reduced by increasing k, and the dynamic performance can be expected by analyzing the loaded model of the source-converter, as shown in Fig. 3b. For the loaded model, the bus current ($\widetilde{i}_{bus}$) can be represented by $\widetilde{v}_{bus}/Z_{in}$. Thus, the dynamic response of the system can be evaluated using

$$\frac{\widetilde{v}_{bus}}{\widetilde{v}_{ref}} = \frac{T}{1+L_m} \tag{4}$$

where

$$L_m = T + \frac{Z_{ol}}{Z_{in}} + k\,G_f\,G_{pwm}\,G_{vd} \tag{5}$$

L_m is the induced voltage loop gain of the source-converter. Applying the Nyquist criterion to L_m reveals the relative stability margins, while the dominant poles of (4) dictates the settling time. According to (4), the relative stability margins and the settling time are controlled by the selection of the filter corner frequency (ω_F) and k. Hence, their selection methods are explained next.

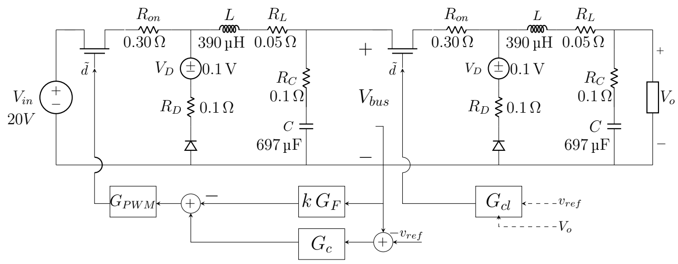


Fig. 4. The prototype DPS parameters.

IV. SELECTING THE PROPOSED CONTROLLER PARAMETERS

Selecting ω_F and k is demonstrated using the prototype that is shown in Fig. 4, whose output voltage (V_o), bus-voltage

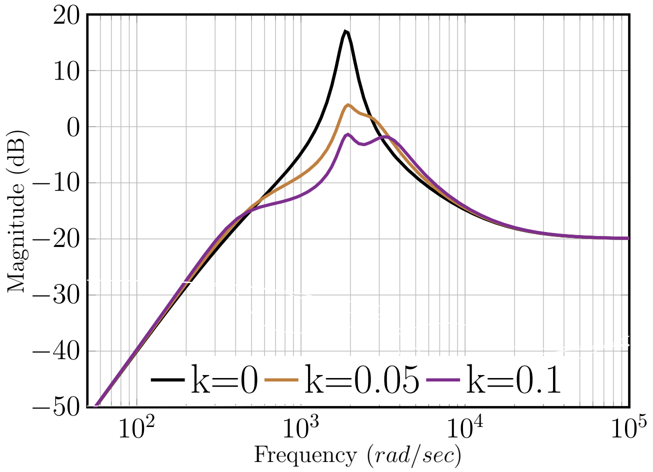


Fig. 5. Analysis of source output impedance (Z_o) subject to different k values.

(V_{bus}), output power (P_o), G_{pwm}, source controller (G_c), and load controller (G_{cl}) are listed in [28]. Each converter was standalone stable, however, integrating the system destabilized the voltage at the dc-bus due to an impedance overlap as illustrated in [28]–[30]. ω_F should be selected to allow the oscillations to pass. The oscillation frequency can be examined using the location of the unstable poles, which occurred at ($1 \pm 1310i$) for the prototype. As a consequence, the oscillation frequency is expected to be $1310 rad/sec$ ($\approx$ 208 Hz), so we selected ω_F to be 1×10^3 rad/sec ($\approx$ 159 Hz). After selecting ω_F, k is crucial to ensuring stability and improving the dynamic performance of DPSs. It is capable of reducing Z_o according to (2). In addition, k determines the relative stability margins and the location of the dominant poles of (4). Thus, the dynamic response is characterized by k. Fig. 5 shows that $|Z_o|$ decreases as k increases. Therefore, $|Z_o/Z_{in}|$ can be ensured to less than unity by increasing k. The stability margins are determined by applying the Nyquist criterion to L_m, as shown in Fig. 6. The system was unstable for $k = 0$, while the stability margins improved for $k = 0.05$ and $k = 0.1$. Moreover, the dominant poles for $k = 0.1$ were ($-242.5 \pm 355.4i$), and they were ($-383.2 \pm 382.4i$) for $k = 0.05$. Thus, the settling time for $k = 0.05$ should be shorter than the settling time of $k = 0.1$.

V. SIMULATIONS AND EXPERIMENTS

In order to verify the efficacy of the proposed controller, the prototype was simulated using PLECS Standalone package. The responses of the system to $k = 0$, $k = 0.05$, and $k = 0.1$ are demonstrated in Fig. 7. Fig. 7a shows that the system was unstable for $k = 0$, and the oscillation frequency was 200 Hz. Fig. 7b and Fig. 7c depict that the system was stable with different settling times. The settling time for $k = 0.05$ was $0.013\,s$, while it was $0.03\,s$ for $k = 0.1$. Hence, the impact of the poles location is verified. The simulation results were verified using lab experiments, where Fig. 8 shows the

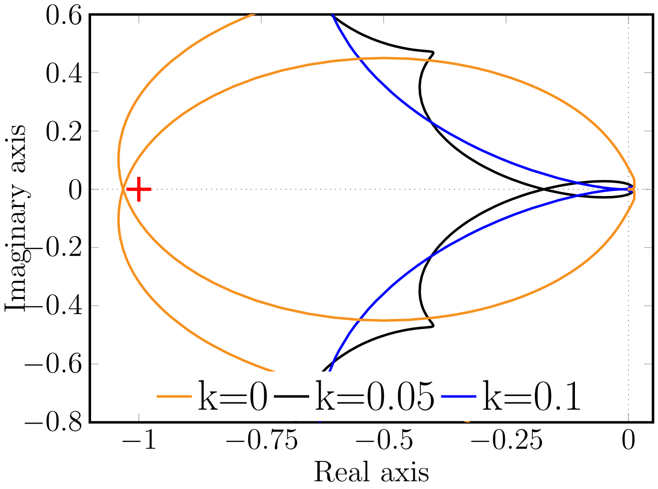
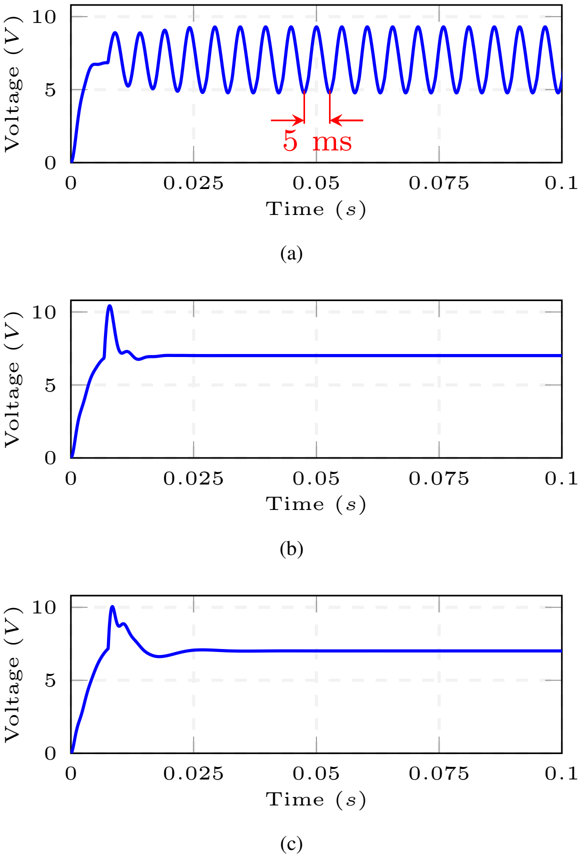


Fig. 6. Analysis of the relative stability margins subject to different k values.



(a)

(b)

(c)

Fig. 7. Simulation results for (a) $k = 0$, (b) $k = 0.05$, and (c) $k = 0.1$.

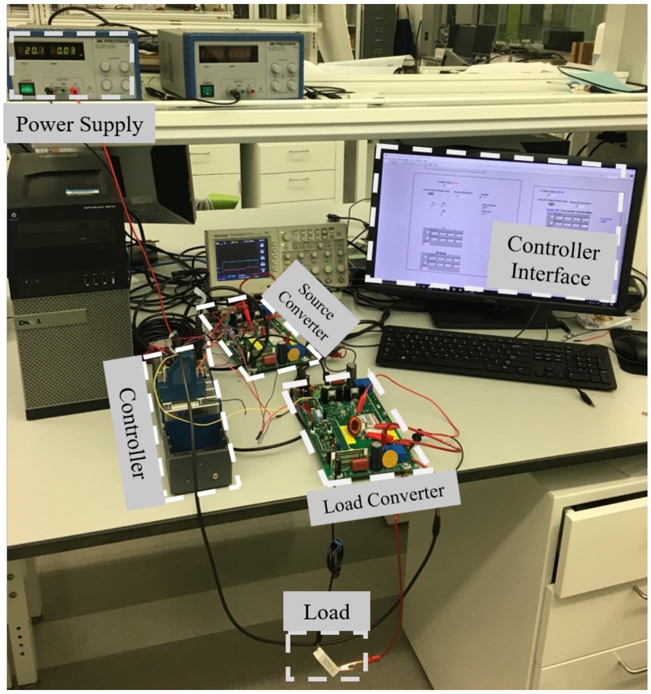
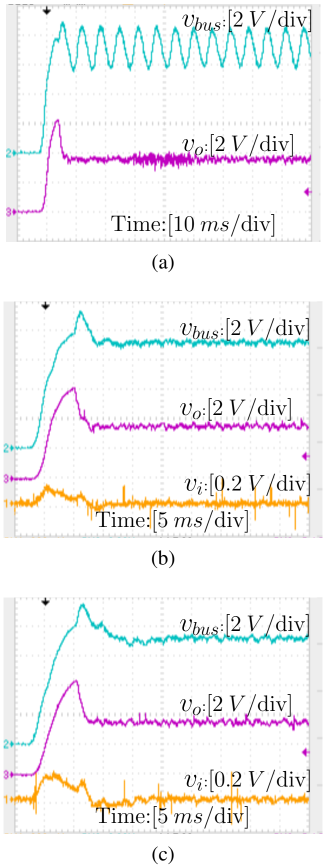


Fig. 8. Test Bench.

experimental setup. Fig. 9a shows the instability of the bus-voltage using $k = 0$, where v_{bus} denotes the bus-voltage, and v_o denotes the output voltage of the load-converter. Despite the instability of v_{bus}, v_o was stable because the frequency of oscillation falls within the load controller bandwidth [7], [31]. Fig. 9b and Fig. 9c show the responses to $k = 0.05$, and $k = 0.1$, respectively. v_i denotes the injected voltage oscillations to the source controller. The settling time to $k = 0.05$ was shorter than the settling time to $k = 0.1$, so the analyses and simulations results were matched. Moreover, the ability of the controller to respond for load changing was verified. The load-converter was supplying half of its rated load, then the remaining half was connected. v_{bus} became unstable at full load for $k = 0$, as shown in Fig. 10a. In contrast, Fig. 10b depicts a highly improved dynamic response for $k = 0.05$.

VI. CONCLUSION

This paper introduced a novel controller to stabilize and to improve the dynamic performance of dc distributed power systems. The controller utilizes the voltage oscillation that occurs at the dc-bus in order to eliminate the impact of CPLs on the dynamic performance of DPSs. A prototype DPS was thoroughly analyzed in order to validate the controller effectiveness using analytical analyses, simulations, and lab experiments. All of the outcomes were in agreement of proving the effectiveness of the proposed controller. The future work will focus on selecting ω_F and k adaptively, while the most optimum dynamic performance is guaranteed.



(a)

(b)

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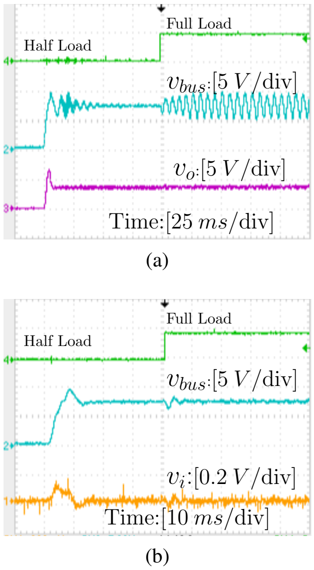
Fig. 9. Experimental results for (a) $k = 0$, (b) $k = 0.05$, (c) $k = 0.1$.



(a)

(b)

Fig. 10. The response for stepping-up the load for (a) $k = 0$, (b) $k = 0.05$.

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