Lifetime-based Power Routing of Smart Transformer with CHB and DAB Converters

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***Abstract*—Smart Transformers (ST) are a potential solution for installing intelligent nodes in the electrical distribution grid, which can provide DC connectivity and are capable of providing grid services the traditional low-frequency transformers was not able to provide. However, the reliability of STs is one of the main challenges, limiting its application. To improve the reliability of STs, it is proposed to control the power in a modular ST architecture in order to control the remaining lifetime of its building blocks. Therefore, unequal power sharing through the cells based on the remaining useful lifetime, known as power routing, has been proposed for different converter topologies. However, existing literature has not investigated the impact of power routing on the ST on a system level. This paper focuses on the design and implementation of lifetime-based power routing control based on virtual resistances tailored for an ST consisting of Cascaded H-bridge (CHB) and Dual-Active Bridge (DAB) converters.**

I. Introduction

The paradigm shift from fossil fuels to green-technologies in the energy production has altered the conventional power system network with higher share of renewable energy sources and electric vehicle charging stations. This has posed challenges in the electrical distribution network with spatially distributed generations and bidirectional power flow. The ST is one promising solution to address the power flow flexibility while catering the requirements of changing grid scenarios [1]–[3]. However, expected lower reliability is one of the key challenges of the ST compared with the conventional low-frequency transformer.

The power electronic devices and capacitors contribute to the major failures in converter systems [4]. The paper focuses on the failures due to semiconductors. The power cycling of the devices resulting in thermal cycles is considered to be the crucial factor for the aging of devices. The existing literature mainly focuses on device level and converter level reliability by actively controlling the thermal cycles by different methods such as switching frequency control, active gate drivers and modulation techniques [5]–[7]. For improving the reliability of a modular converter system comprising of many cells, the aging of the cells can be actively controlled by unequal sharing of the power depending on the remaining useful life of each module and thereby the system failure can be delayed [8]–[10]. However, the system level reliability study of a modular power converter system is scarce in the existing literature. This work presents the impact of unequal power sharing on the reliability of the power electronic converters on a system level. The design and implementation of a reliability oriented system level design of the ST with the power routing strategy is investigated in this paper.

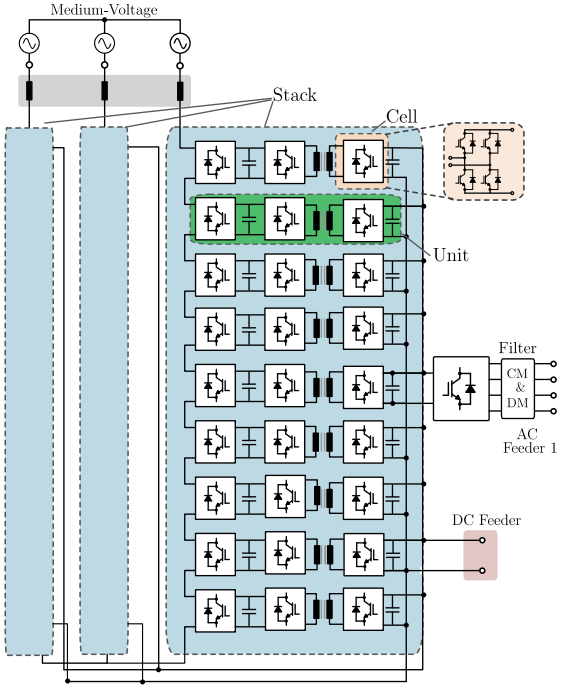

Fig. 1: ST topology with CHB and DAB.

Since the unequal power sharing for increased reliability has different effects on different topologies, implementation of power routing for the ST consisting of various topologies is challenging. The paper proposes a virtual resistance based lifetime based control for the modular ST comprising of CHB converter cells and DAB cells as shown in Fig. 1.

The section II introduces the concept of power routing to increase the reliability of ST. Topology and the design of the lifetime-based power routing controller (PRC) is explained in section III. The simulation results are discussed in section IV. The section V shows the experimental validation of the proposed strategy and finally a conclusion is drawn in section VI.

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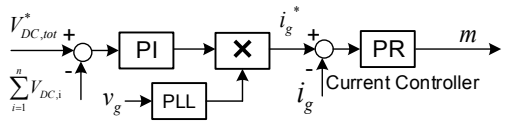


Fig. 2: CHB control scheme.

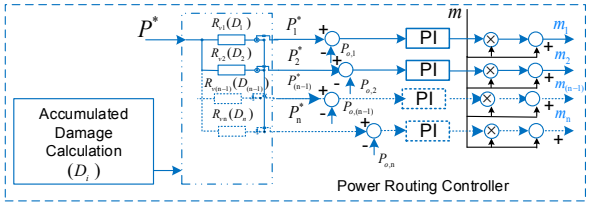


Fig. 3: Power routing controller.

II. Power Routing for Increased Reliability

One of the main challenges of the ST is the reliability and availability compared to the traditional low-frequency transformer with expected lifetimes of 60 - 80 years. Therefore, a modular system with the capability to monitor the health of components is proposed. When a component fails, the corresponding cell is sent back for maintenance and replaced. Consequently, the ST is composed of modules with different ages. According to the aging of the cells, the power is distributed among the cells to delay the processed-power dependent failures. The highly aged cells process less power compared to the new ones and therefore the power dependent aging can be controlled. This is illustrated in Fig. 4.

The junction temperature fluctuations influence the aging and deterioration of the power modules as expressed in (1). Here, N_f denotes the number of thermal cycles to failure depending on the thermal swing ΔT, average junction temperature $T_{j,av}$ and the device dependent parameters a_1, a_2 and a_3. The parameter $a_2 \approx 5$ makes N_f highly sensitive to junction temperature variations [12].

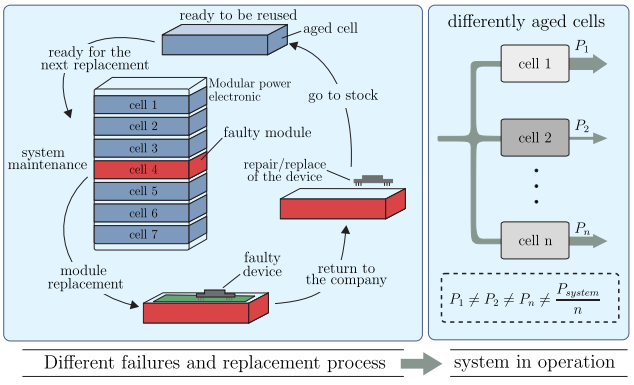


Fig. 4: Replacement cycle in the repairable modular ST and uneven loading based on remaining estimated lifetime [11].

$$N_f = a_1 (\Delta T)^{a_2} \cdot e^{\frac{a_3}{T_{j,av}+273°C}} \quad (1)$$

The thermal cycles lead to fatigue and leads to bond-wire liftoff. For fatigue analysis, Miner's rule can be applied to calculate the accumulated damage using [13]

$$D_{acc} = \sum \frac{N_i}{N_{fi}} \quad (2)$$

where D_{acc} is the accumulated damage, N_i the number of cycles and N_{fi} the durability of the i-th stress range. When the accumulated damage becomes 1, the device fails. It is assumed that the damage accumulates linearly.

III. Topology and Controller Structure

A potential three-stage configuration of the ST is shown in Fig. 1. The CHB connects the Medium Voltage AC (MVAC) to Medium Voltage DC (MVDC) and DAB converts the MVDC to Low Voltage DC (LVDC) with medium frequency transformer isolation. This section focuses on the controller design for CHB and DAB of the ST with the capability to route the power based on the remaining useful lifetime (RUL). The Fig. 1 shows the ST topology with CHB and DABs comprising of n units. Here, one CHB cell along with a DAB is considered as one unit.

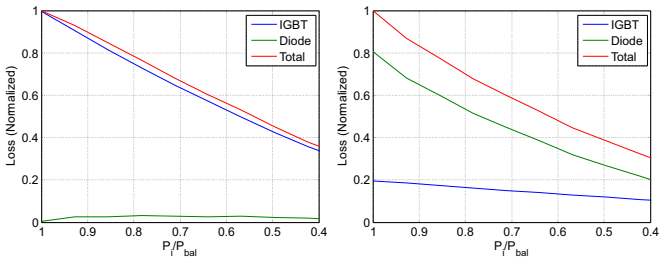
A. Control Scheme for CHB and DAB

The CHB rectifier stage controls and shapes the input ac current and controls the total MVDC-link voltage. The control scheme for CHB is shown in Fig. 2. The current and voltage control is achieved through cascaded controller structure with Proportional-Resonant (PR) controller and Proportional-Integral (PI) controller respectively [14]. The Fig. 3 shows the control scheme for power routing using the CHB. The modulation index, m, produced by the PR controller is given to a PI-based Power Modulator to achieve different power flow through the DC-links of CHB. The power reference, P_i^*, for each of the DC-links is computed through a power routing algorithm based on virtual resistors.

A control scheme with output and input voltage control is adopted for the DAB. The input MVDC-link voltages are balanced by the DAB, which is critical for the stability while processing unequal power through each H-bridge of the CHB. For the output LVDC-link voltage control, a PI voltage controller is designed using pole-zero cancellation technique [15].

B. Impact of Power Routing on CHB and DAB topology

Power routing strategy has been implemented on the CHB in [9]. It is evident that the total losses of the power semiconductors do not vary much with unequal power sharing for the CHB. For the selected IGBT in [9], even 80% unloading of on cell leads to only $\approx 5\%$ decrease in the total losses. In general, since the H-bridges in a CHB are connected in series, the



(a) (b)

Fig. 5: Loss distribution of the power semiconductors in DABs of the ST (a) Unloaded cell primary side H-bridge (b) Unloaded cell secondary side H-bridge.

power routing has limited effect on the device losses. However, the loss distribution among the IGBTs and diodes is influenced by power routing resulting in $\approx 20\%$ change in losses for 80% unbalance [9].

To evaluate the effect of unbalanced power sharing on the semiconductor loss distribution in DABs, a simulation study is done in SIMULINK. The diode and IGBT losses of the primary and secondary side H-bridges of DAB are analyzed from full load to 40% of full load condition. The results for the primary (MVDC) and secondary (LVDC) active bridges are shown in Fig 5(a) and (b) respectively. The IGBT losses on primary side and diode losses on secondary side dominate the total losses due to the power flow from MV to LV stage. The loss variation for unloading can be approximated as a linear function for simplicity. Therefore, by varying the power sharing ratio among the DABs, the device losses can be effectively influenced and consequently their junction temperatures and the aging.

C. Lifetime based power routing with virtual resistor

To conduct a lifetime analysis of the ST, a simplified electro-thermal model of a seven level CHB connected to three DABs are modeled in MATLAB. The model consist of electrical equations of CHB and DAB along with thermal models of the semiconductor switches and the heatsink for calculating the junction temperature of each device. The simplified model shortens the simulation time of electro-thermal circuits drastically, making lifetime studies of the order of many years feasible to be simulated within reasonable time.

First, the CHB and DAB are described with their electrical equations. Considering phase shift modulation for DAB cell i, the power handled is given by

$$P_i = \frac{m_{dab,i} V_{dc,i}^2 D_i (1 - D_i) T_{sw}}{2 L_i} \tag{3}$$

where P_i is the power processed by DAB cell i, $m_{dab,i}$ is the modulation index of DAB_i,$V_{dc,i}$ is the MVDC link voltage, L_i is the leakage inductance and T_{sw} is the switching time period. Depending on the operating power, duty cycle D_i is calculated and subsequently the primary $i_{prim,i}$ and secondary currents $i_{sec,i}$ through the switches are also calculated [16]. The

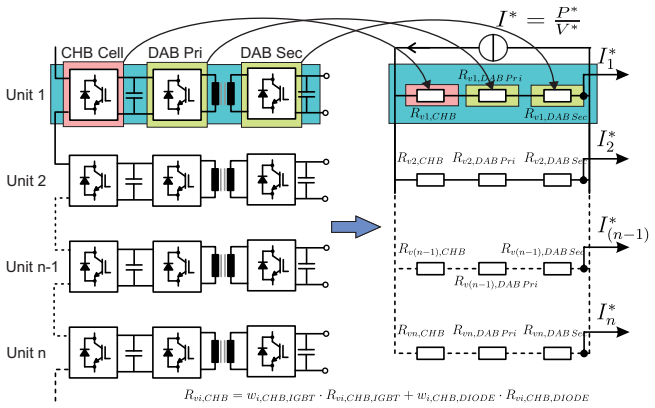


Fig. 6: Equivalent circuit design of virtual resistor based power routing in the ST with CHB and DAB.

conduction loss for the switches are calculated with knowing their on-state resistance value r_{on} and the switching losses, turn on $P_{sw-on,i}$ and turn off $P_{sw-off,i}$ losses, from their turn-on E_{on} and turn-off E_{off} energies and using the equations (4) and (5) respectively.

$$P_{sw-cond,i} = 4(i_{prim,i}^2 \cdot r_{on-pri,i} + i_{sec,i}^2 \cdot r_{on-sec,i}) \tag{4}$$

$$P_{sw-off,i} = 4 f_{sw} (E_{off-pri,i} + E_{off-sec,i}) \tag{5}$$

The turn on losses for each DAB cell $P_{sw-on,i}$ depends on the Zero Voltage Switching condition and are calculated accordingly [16]. Finally, the total losses $P_{sw,i}$ for the given operation point can be computed by (7)

$$P_{sw,i} = P_{sw-cond,i} + P_{sw-on,i} + P_{sw-off,i} \tag{6}$$

Similarly, the electrical equations of CHB is used to compute the devices losses for the given operating point [17].

The thermal model consists of the thermal impedance of junction to case, case to heatsink and heatsink to ambient represented by a Cauer network. The junction temperature T_{jun} of the device can be calculated from

$$T_{jun}(t) = Z_{th,jun-amb}(t) * P_{loss}(t) + T_{amb}(t) \tag{7}$$

The junction temperature measurement from the cells are used to calculate the accumulated damage (D_i) using rainflow counting algorithm and Miner's rule [13]. When the accumulated damage reaches unity, the power module attains it's End of Life (EOL). Based on the accumulated damages of the semiconductor modules, the power distribution is changed to delay the power dependent failures. The virtual resistance R_{vi}, $i \varepsilon [1,n]$ is defined as function of the accumulated damage of the respective units. The scheme for the implementation of the power routing controller is shown in Fig. 3.

Therefore, the higher the value of virtual resistance, the lower the power processed through each unit. For the implementation of power routing, the converters are not oversized and when the system is operated under full load, the converters

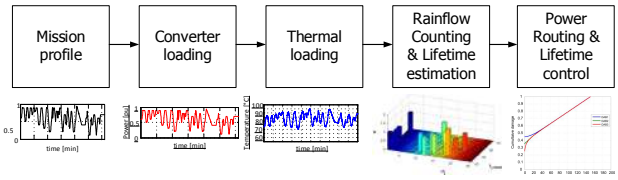


Fig. 7: Lifetime control block diagram with power routing.

Symbol	Description	Value
e (rms)	Grid voltage (rms)	$230V,\ 50Hz$
L_g	Filter inductance (MV side)	$3.8mH$
$V_{DC,1} = V_{DC,2}$	DC-link voltage reference	$250V$
V_0	DC-link voltage (LV side)	$240V$
n	MFT turn ratio	$1:1$
$f_{sw,CHB}$	Switching frequency of the CHB	$3kHz$
$f_{sw,DAB}$	Switching frequency of the DAB	$12kHz$

TABLE I: System parameters

process their rated power. The power routing strategy is active only during the partial load operation. The design of the virtual resistance for the CHB-DAB topology is illustrated graphically in Fig. 6. The accumulated damages for each H-bridges of CHB and DAB can be calculated from the junction temperature measurements and the virtual resistance can be modeled as a function of accumulated damage. For simplicity, a proportional relationship is considered (8):

$$R_{vi,CHB/DAB} \propto D_{i,CHB/DAB} \tag{8}$$

A weighted average of the virtual resistances of CHB and DAB modules in one power path is considered for the total virtual resistance calculation as expressed in (9).

$$R_{vi} = w_{i,CHB,IGBT} \cdot R_{vi,CHB,IGBT} + w_{i,CHB,DIODE} \cdot R_{vi,CHB,DIODE} + w_{i,DAB} \cdot max(R_{vi,DABPri}, R_{vi,DABSec}) \ , i \varepsilon [1,n] \tag{9}$$

The weighting factors are calculated from the slope of the normalized loss vs. power unbalance ratio for CHB and QAB. Thus the impact of power routing on the different topologies are also considered to optimize the overall system reliability. The total loss for the same power for both the active bridges of DAB (primary and secondary) are similar as shown in Fig. 5. Therefore, the power routing strategy has similar impact on both the bridges. The maximum virtual resistance value among the two-bridges is chosen for calculation (9) because both bridges process the same power and the bridge with higher virtual resistance is expected to fail first. For the CHB, however, power routing has relatively little impact on the total losses. But the loss distribution among IGBTs and diodes can be affected by routing the power. For the power flow from MVAC to MVDC, the diodes are more stressed than IGBTs. The damage accumulation of both IGBTs and diodes are considered for CHB. The functional block diagram of the power routing control for lifetime control is shown in Fig. 7.

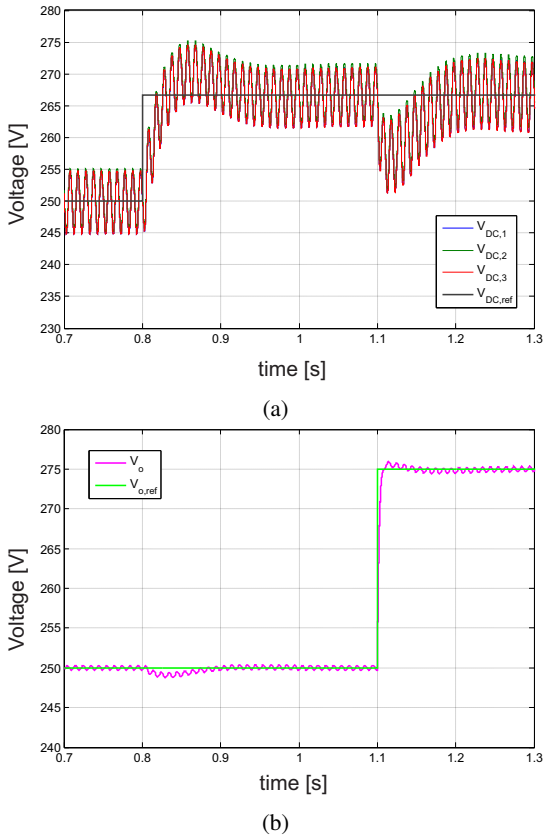


Fig. 8: (a) Dynamic behavior of CHB capacitor voltages $V_{DC,1-3}$ (b) Dynamic behavior of DAB output voltage V_o.

IV. Simulation Results

The simulation results comprises of two parts: a) Validation of the control algorithm with simulation and b) Validation of the impact of the virtual resistance based power routing on the lifetime of ST.

A. Validation of Control Algorithm

To validate the performance of CHB and DAB control algorithm with power routing controller, a simulation model of the ST is developed as described in section III. The controller controls the output LVDC voltage while maintaining the CHB capacitor voltages to their reference values. The power routing controller should be able to load the DABs with unequal power according to their references without changing the output voltage and CHB capacitor voltages. The controller has been validated with simulation for the system parameters given in the table I. Fig. 8 (a) shows the dynamic behavior of CHB voltage control for a step change in the CHB DC link reference voltage $V_{DC,ref}$ at 0.8 s. At 1.1 s, the CHB DC link voltages have a perturbation due to the step change of DAB output voltage reference $V_{o,ref}$. Fig. 8 (b) validates the performance of DAB voltage controller and it is shown that the output voltage V_o follows the reference $V_{o,ref}$ and remains stable even during the reference voltage $V_{DC,ref}$ change in the CHB.

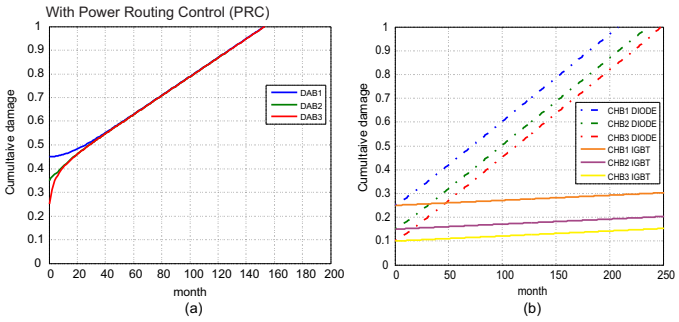


Fig. 9: Cumulative damage vs. time with PRC (a) For the DABs (b) For the CHB.

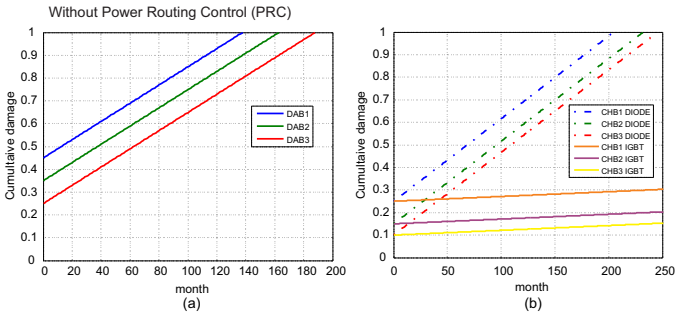


Fig. 10: Cumulative damage vs. time without PRC (a) For the DABs (b) For the CHB.

B. *Validation of the impact of power routing on lifetime*

To validate the effect of virtual resistor based power routing on the lifetime of ST, an electro-thermal model of the ST comprising of CHB and DAB with IGBTs and diodes along with the heatsink is developed as described in section III. Mission profile of a grid is given as the input and based on the junction temperature calculation, the accumulated damages are evaluated with rainflow counting. The power sharing between the units of ST are dynamically changed according to the virtual resistor model developed in section III. For the proof of concept, results of three units comprising of three CHB cells connected to three DABs are shown in Fig. 9 and Fig. 10. Fig. 9 (a) and (b) shows the accumulated damage variation of the cells over time with the proposed virtual resistance Power Routing Control (PRC) for the DABs and CHB respectively. The accumulated damage of the DABs converge over time, resulting in the failure of the system at a single point in time even though they have different initial accumulated damages. The progression of the accumulated damage of the system without PRC for the DABs and CHB is shown in Fig. 10 (a) and (b) respectively. It illustrates that one of the cells fails earlier than the others resulting in the total system failure. In order to analyse the results more vividly, the RUL of the DAB and CHB with and without power routing are illustrated in the bar-graphs Fig. 11 (a) and (b) respectively. Without power routing, the system fails at 137^{th} month when the first DAB fails whereas the power routing extends RUL of system

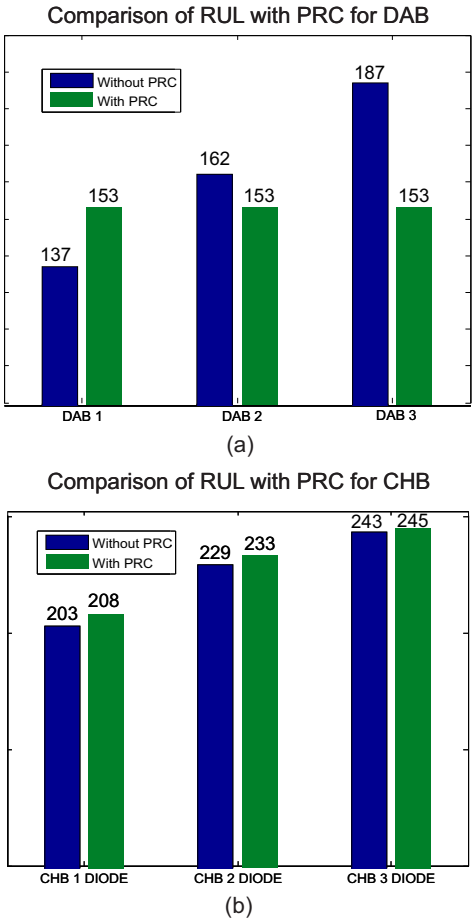


Fig. 11: (a) RUL of DAB with and without PRC (b) RUL of CHB with and without PRC.

by 16 months. There is an increase in the RUL of the CHB with actively sharing the power between diode and IGBTs as depicted in Fig. 11 (b). To sum up, the PRC strategy results in the overall lifetime extension on a system level even though the lifetime of some healthy module is decreased compared to normal operation. Moreover, the results confirm that PRC strategy has different impacts on CHB and DAB as expected.

V. Experimental Results

To validate the proposed power routing control strategy, a small scale prototype of a five level CHB connected to two DABs has been developed as illustrated in Fig. 13. The H-bridges of CHB and DAB are made with open-module DP25H1200T101616 from Danfoss to facilitate direct junction temperature measurements. High speed infrared thermal camera is used to obtain the thermal image of the open module as shown in Fig. 16. The camera is controlled by an automatic positioning system for fast and accurate measurements. The setup is controlled by the dSPACE SCALEXIO system. The parameters of the experimental setup is summarized in Table I.

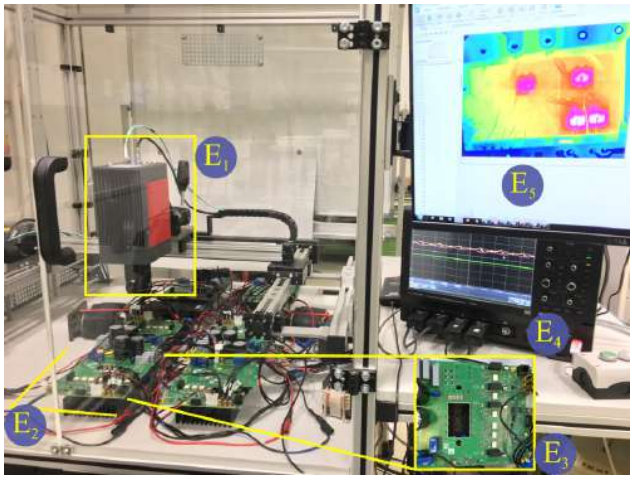


Fig. 12: The experimental setup (E_1 - High Speed Thermal Camera, E_2 - CHB and DABs, E_3 - Open Module, E_4 - Oscilloscope, E_5 - Thermal image.

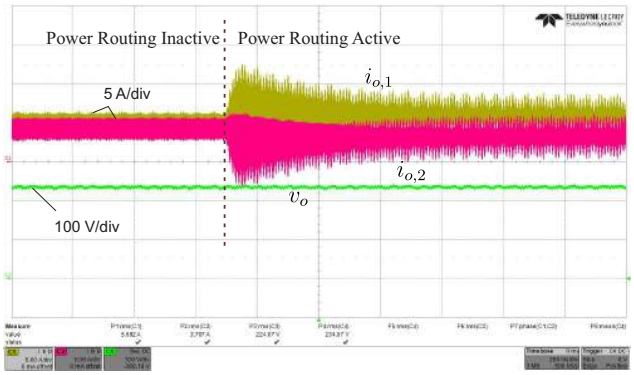


Fig. 13: ST with and without power routing showing the output current of both DAB, ($i_{o,1-2}$) and the output voltage (v_o).

Functioning of the power routing controller along the overall control system is tested by changing the power distribution. The overall power processed by the system is kept constant at $P_n = 2.2\,kW$ and the power references of the DABs are changed to $P_{DAB,1} = 1.45\,kW$ and $P_{DAB,2} = 0.75\,kW$ from equal power sharing. The output currents of DAB,1 ($i_{o,1}$) and DAB,2 ($i_{o,2}$) along with voltage across the load resistor (v_o) are shown in Fig. 13. When the power references are changed, $i_{o,1}$ and $i_{o,2}$ change accordingly while v_o stays constant as expected. The DC-link voltages of the CHBs are controlled and kept equal to the reference value, even with the unequal power sharing. The Fig.14 (a) and (b) show the output currents of DABs and the output voltage clearly for both equal and unequal power sharing respectively. This validates the proper functioning of the control scheme developed in section III.

The temperature change in the primary side of the DAB in both modules are measured during the equal and unequal power sharing. The results of the high speed infrared camera measurement for DAB cell 1 showing the temperature of the IGBTs is shown in Fig. 15. The results show a difference

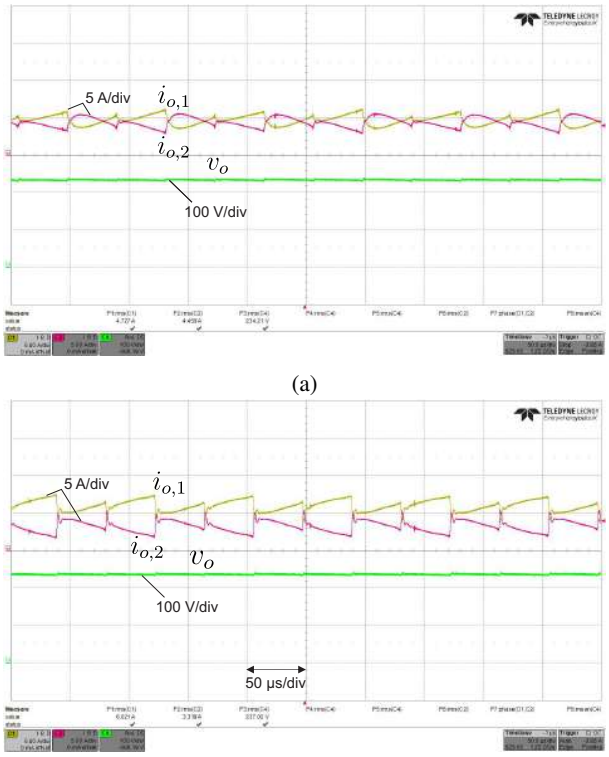


Fig. 14: (a) The output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) for equal power sharing (b) The output currents of both DABs ($i_{o,1-2}$) and the load voltage (v_o) for unequal power sharing.

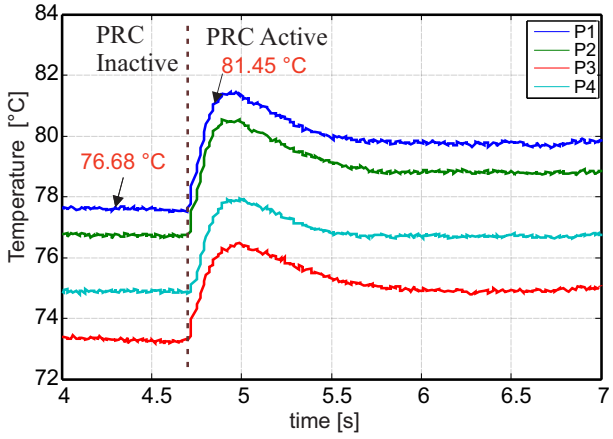
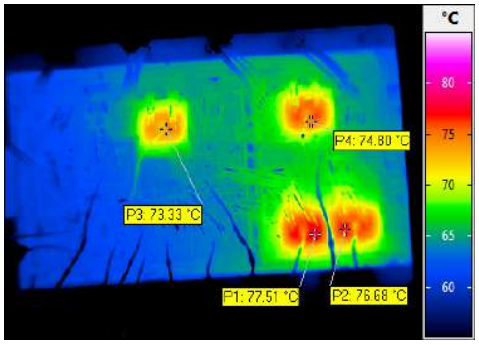
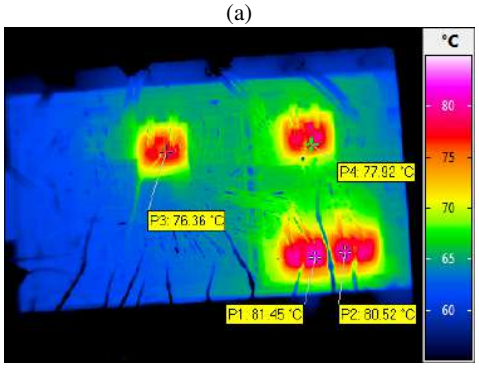


Fig. 15: Variation of primary side IGBT junction temperatures of the DAB cell 1 for a step change of $\approx 21\%$ increase in power.

of $\approx 4\,^{\circ}C$ in the junction temperature for 350 W change of the power applied for 5 s. The junction temperature of the DAB cell 2 has reduced by $\approx 4^{\circ}C$. The heat-sink has lower thermal resistance since the converter is designed for a higher nominal power (20 kW) which results in the smaller difference



(a)



(b)

Fig. 16: Junction temperature measurement of primary side IGBTs of DAB cell 1 (a) during nominal power operation (b) with power routing control active with 21 % power unbalance.

in temperature for a power change of 350 W. The objective of the experiment is validate the working of the designed power routing controller and the effect on the junction temperature and consequently the aging. Fig. 16 (a) and (b) shows the thermal image of the open modules showing the temperature distribution without and with power routing control respectively. It is clear that the power routing controller can influence the junction temperature of the modules and thereby the stress on the semiconductors in different cells of the ST.

VI. Conclusion

For applications requiring very high reliability such as the ST, advanced control strategies are necessary to increase the lifetime. The design and the implementation of the controller scheme for unequal sharing of power based on lifetime of the power modules for the ST is presented in this paper. The impact of power routing on different converter topologies is investigated and is considered for the design of the virtual resistors for the ST. Analytical results show an increase of $\approx 12\%$ increase in the lifetime of the system with the proposed power routing strategy. The proof of concept of the designed control scheme is shown experimentally on a small-scale prototype with open IGBT modules. The effect of the power routing controller on the junction temperature of the ST is measured experimentally to validate the concept. The experimental results show that the control strategy can be used to actively control the lifetime of ST.

Acknowledgment

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