Power Rectifier Based on Open-end Converter with Floating Capacitor Under Non-Sinusoidal and Unbalanced Input

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***Abstract*—This work studies a three-phase power rectifier which consists on an open-end converter composed of two three-phase three-leg converters (converters A and B). Converter A has a floating capacitor on its dc-link. On the other hand, converter B processes power and has a dc load connected to its dc-link capacitor. The voltage ratio considered is 2:1 to maximize the number of levels symmetrically spaced. A level-shifted PWM strategy is presented and dc-link control strategies are proposed for both converters A and B. The dc-link floating capacitor is controlled by means of the common mode voltage, keeping the PWM levels, and it is performed by a PI controller. Additionally, scenarios with non-sinusoidal and unbalanced grid voltages are discussed. It is shown that it is possible to use the maximum capability of the converter A in the compensation of harmonics and negative sequence. Finally, simulation and experimental results are shown to validate the strategies and scenarios presented.**

I. INTRODUCTION

Static ac-dc power converters, also known as rectifiers, are used in many industrial and commercial applications, such as adjustable-speed drives (ADS), uninterruptible power supplies (UPS), interface with renewable power sources such as solar photovoltaic (PV) systems and wind energy conversion systems (WECS), battery energy storage systems (BESS), battery charging for electrical vehicles, and power supplies for telecommunication systems [1], [2].

The classical passive three-phase diode bridge is a cheap and simple solution for ac-dc power conversion [3], [4]. Nevertheless, their power absorbed from the ac source has poor quality because of injected current harmonics and low power factor [1]. For applications where energy quality is of great concern, it is demanded at least a current total harmonic distortion (THD) lower than 5% and a power factor greater than 95% [5]. Hence, the need to employ three-phase active rectifier circuits rises. In this scenario, many solutions can be found in the literature [6]–[9]. If the solid-state rectifier is bidirectional, it provides not only currents with lower THD, but also allows power factor correction (PFC), greatly enhancing the quality of the power absorbed from the ac source.

On the other hand, multilevel converters allow to increase the voltage and power capability of the conversion system, and at the same time they enhance the power quality by generating an ac multilevel voltage with low weighted THD (WTHD) and ac currents with even lower THD compared to conventional two-level converter alternatives [10], [11]. There are several types of multilevel converters, but in general they can be classified into three main groups found in the literature: i) Neutral Point Clamped (NPC) converters, ii) Flying Capacitor (FC) converters, and iii) Cascaded H-Bridge (CHB) converters [12]–[14].

Open-end configurations are frequently seen in the literature applied to electrical machines drivers, as seen in [15]–[19]. They allow to feed the machine with multilevel voltages by using conventional two-level converters without additional injection transformers. Though many dc sources are required in some cases, it is possible to save these sources by replacing them for floating dc-link capacitors [15]–[20]. On the other hand, the floating capacitor control limits the converter modulation index. To use the converter in its full voltage capability, the cell with floating capacitor may be used to compensate harmonics [21]. Although the most observed application of these multilevel converters is as inverters, ac-dc applications are also possible for the machine operating as generator, or even if the ac source is the electrical grid. In this last case, the open-end configuration is formed in the secondary winding of a three-phase transformer whose primary is connected to the grid.

Hence, in this paper the power rectifier shown in Fig. 1 is studied. The converter is composed of two three-leg three-phase converters (converters A and B) series connected with the grid in an open-end arrangement. Converter A has a floating capacitor on its dc-link and may provide reactive power, compensate for harmonic content or negative-sequence component. On the other hand, converter B processes power and feeds a dc load connected to its dc-link. The control of the floating capacitor imposes constraints to the system modulation index (m_a). However, under non-sinusoidal or unbalanced input, the converter may achieve higher modulation indexes by using converter A to generate voltage harmonic content or negative-sequence component. Details regarding the PWM strategy and the floating capacitor regulation techniques are given. Simulation and experimental results are presented to validate the analysis.

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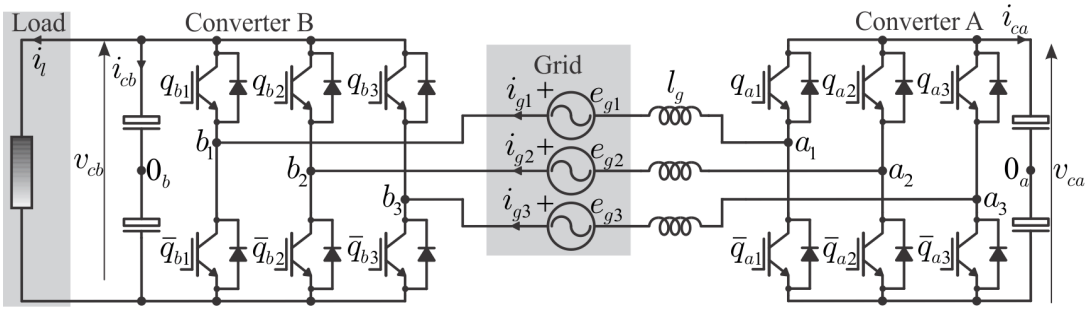


Fig. 1. Open-end three-phase power rectifier studied (6LC).

II. CONVERTERS MODEL

The model of the converter is described in this section. Henceforward, $j = \{1, 2, 3\}$, denoting each of the three phases of the system. The grid is modelled as a three-phase source with a series coupling inductor (l_g). The system model is derived from the equivalent circuit shown in Fig. 2 and applying Kirchhoff's laws. Then, (1) presents the current dynamic equation per phase, where i_{gj} are the currents, v_{bj0} and v_{aj0} are the pole voltages of converters B and A, respectively, e_{gj} are the grid voltages and v_{0ba} is the voltage between converter B and converter A dc-link midpoints (0_a and 0_b), that is, the common-mode voltage.

$$l_g \frac{di_{gj}}{dt} = v_{bj0} - v_{aj0} - e_{gj} - v_{0ba}. \quad (1)$$

Besides that, it is important to define the multilevel resultant pole voltage (v_{baj}) and the rectifier resultant ac voltages (v_{gj}). These are shown in (2) and (3).

$$v_{baj} = v_{bj0} - v_{aj0}, \quad (2) \qquad v_{gj} = v_{baj} - v_{0ba}. \quad (3)$$

From the states of the switches (opened or closed) it is possible to determine the converters pole voltages v_{bj0} and v_{aj0}. In this way, (4) and (5) present the pole voltages, considering the state of the switches (q_{bj} and q_{aj}) binary variables with the value 1 representing the closed state and 0 the opened state.

$$v_{aj0} = (2q_{aj} - 1)\frac{v_{ca}}{2} \quad (4) \qquad v_{bj0} = (2q_{bj} - 1)\frac{v_{cb}}{2} \quad (5)$$

where v_{ca} and v_{cb} are the dc-link voltages for converters A and B, respectively.

Finaly, considering a three-phase grid which might contain unbalanced or non-sinusoidal voltages, the common-mode voltage (v_{0ba}) is described in (6).

$$v_{0ba} = \frac{\sum_{j=1}^{3} v_{baj}}{3} - \frac{\sum_{j=1}^{3} e_{gj}}{3} \quad (6)$$

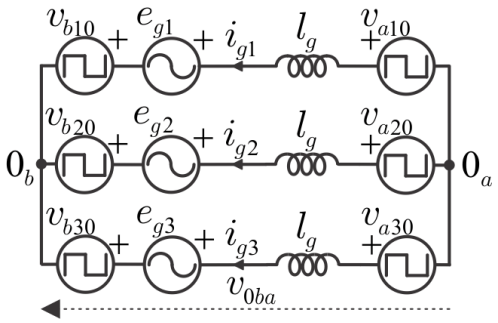


Fig. 2. Converter 6LC equivalent circuit.

III. PWM STRATEGY

This section aims to explain the pulsewidth modulation (PWM) strategy implementation for the studied rectifier. On this section, the superscript "*" denotes reference variables. Additional details on the PWM inplementation can be found at [22]. It is considered a level-shifted PWM strategy (LSPWM), first presented in [23]. On this approach, the reference multilevel resultant pole voltages (v^*_{baj}) are compared to level-shifted carriers ($v_{\Delta 1}$, $v_{\Delta 2}$ and $v_{\Delta 3}$) to generate the gating signals for the power switches to synthesize the average reference voltage. A voltage controller will provide reference voltages for the resultant converter. From (3) it is possible to derive the expression for the reference voltage v^*_{abj}, shown in (7).

$$v^*_{baj} = v^*_{gj} + v^*_{0ba} \quad (7)$$

where v^*_{gj} is the rectifier resultant ac reference voltage set by the controller and v^*_{0ba} is the reference common-mode voltage.

In order to respect the voltage generation limits, the reference common-mode voltage (v^*_{0ba}) is calculated from a maximum ($v^*_{0ba\,\max}$) and a minimum ($v^*_{0ba\,\min}$) values by (8). The limits $v^*_{0ba\,\max}$ and $v^*_{0ba\,\min}$ are defined by (9) and (10).

$$v^*_{0ba} = \mu_{ab} v^*_{0ba\,\max} + (1 - \mu_{ab}) v^*_{0ba\,\min} \quad (8)$$

$$v^*_{0ba\,\max} = \frac{v^*_{ca}}{2} + \frac{v^*_{cb}}{2} - max\{v^*_{g1}, v^*_{g2}, v^*_{g3}\} \quad (9)$$

$$v^*_{0ba\,\min} = \frac{-v^*_{ca}}{2} + \frac{-v^*_{cb}}{2} - min\{v^*_{g1}, v^*_{g2}, v^*_{g3}\} \quad (10)$$

where v_{ca}^* and v_{cb}^* are the reference values for the dc-link voltages. The apportioning factor μ_{ab} is defined by the dc-link voltage controller of converter A, and it must satisfy $0 \leq \mu_{ab} \leq 1$.

Then, the PWM technique algorithm, in sequence, consists of:

- Acquire v_{gj}^* from the voltage controller;
- Calculate $v_{0ba\,\max}^*$ and $v_{0ba\,\min}^*$ from (9) and (10);
- Set μ_{ab} in a value between 0 and 1;
- Determine v_{0ba}^* from (8);
- Determine v_{baj}^* from (7);
- Locate the reference v_{baj}^* and choose the right carrier ($v_{\Delta 1}$, $v_{\Delta 2}$ or $v_{\Delta 3}$)

The considered dc-link voltage ratio is 2:1 ($v_{cb}^* = 2v_{ca}^*$), which provides maximum number of levels symmetrically spaced with three carriers, as shown in Fig. (3).

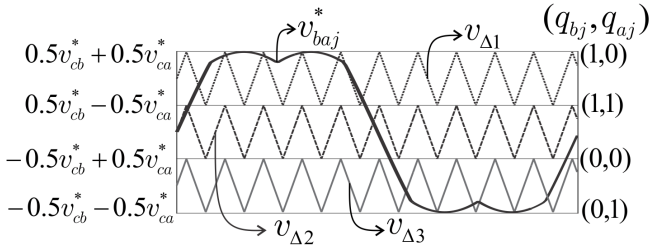


Fig. 3. LSPWM explanation. Triangular carriers disposition.

IV. CONTROL STRATEGY

This section describes the proposed control strategy for the studied converter. A block diagram of the control strategy is presented in Fig. 4. The control dc-link of converter B is accomplished by a cascaded control. In this way, a PI controller provides the current reference amplitude (I_g^*). The current phase is given by a power-based PLL (PLL block), whose model is presented at [24], to synchronize the grid currents with the grid voltages. Hence, two resonant controllers (R_{es}), presented at [25], control the ac currents. These controllers output are the converter reference voltages (v_{g1}^* and v_{g2}^*). Only two currents are controlled (i_{g1} and i_{g2}) because it is a three wire system, that is, $i_{g3} = -i_{g1} - i_{g2}$. Then, to guarantee balanced currents $v_{g3}^* = -v_{g1}^* - v_{g2}^*$.

The reference currents of the controllers R_{es} must be sinusoidal and balanced. Also, the resonant controllers have harmonic terms, in order to eliminate harmonic content from the current, even if the source voltage contains significant harmonic components. These characteristics guarantee that the converter current will be sinusoidal and balanced.

Converter A dc-link voltage is controlled by means of the common-mode voltage (v_{0ab}) which is manipulated by the apportioning factor μ_{ab}. Therefore, a PI controller evaluates the dc-link voltage error ($v_{ca} - v_{ca}^*$) and returns a value for μ_{ab}. It is important to emphasize that both the controller output and its integrator must be limited to assure that $0 \leq \mu_{ab} \leq 0.5$.

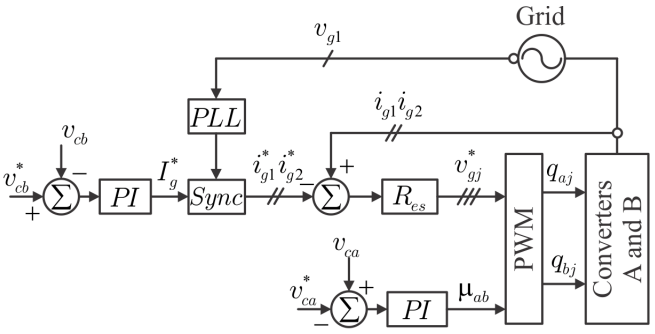


Fig. 4. Converters dc-link control block diagram.

The floating capacitor voltage control presented achieves a steady-state value for μ_{ab}, leading to a nearly constant value. This, in a steady-state situation generate pole voltages with low disturbances and eliminate the disturbances that a hysteresis-based algorithm would cause on both dc-link voltages. Additionally, the floating capacitor voltage control algorithm does not require further measurements, such as current ones. It requires only the measurement of the converter A dc-link voltage (v_{ca}). This feature allows the reduction of sensors if the same topology is used for applications that does not require current control, for example, DVR or inverter.

Although the floating capacitor imposes a limit to the modulation index in a balanced sinusoidal operation, in a situation in which there are voltage harmonics or negative-sequence component in the grid voltage, the converter may operate in higher modulation index values. For example, considering a voltage ratio of 2:1, the maximum modulation index achieved considering only the fundamental component would be $m_a = 0.72$. In this situation, if the grid voltage have, for example, 28% of fifth harmonic component in addition with the previous voltage value, it would be possible to achieve modulation index $m_a = 1$, reaching a higher output voltage without increasing the dc-link voltages.

An unbalanced voltage scenario would also be tolerated by the proposed converter control. Situations in which there are negative-sequence components in the grid voltage, increasing voltage in one phase and decreasing voltage in other phases would not disturb the floating capacitor voltage control whereas the reference voltage does not exceed the maximum voltage possible for the topology.

These characteristics are possible because the current control maintains the converter currents sinusoidal and balanced. Hence, negative-sequence and harmonic voltage components produce no mean active power.

V. THD AND SEMICONDUCTOR LOSSES EVALUATION

To evaluate the performance of the converter on the proposed scenarios, three parameters are presented in this section: Total Harmonic Distortion (THD), Semiconductor losses and mean switching frequency. The studied topology (6LC) is compared to the conventional three-phase three-leg converter (3LC) shown in Fig. 5. The semiconductor losses are based

on the thermal module of PSIM software. For all simulations in this section it is considered coupling inductor $l_g = 7$ mH, the load is purely resistive and has a power rated of 3 kW. The scenarios analysed have dominant switching losses and the conducting losses remains nearly constant.

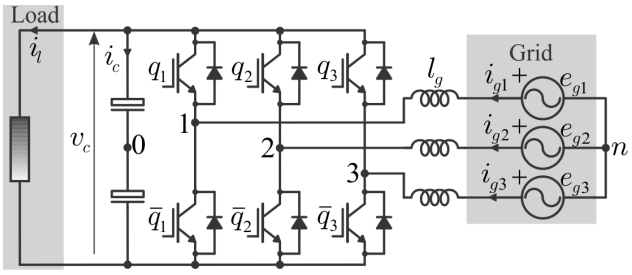


Fig. 5. Conventional three-leg power rectifier (3LC) used for comparison with studied topology.

A. Scenario 1: sinusoidal and balanced

This section presents results considering a grid voltage amplitude of 220 V RMS. For both converters it is considered the maximum voltage achieved, so for the studied 6LC converter it is used $m_a = 0.72$ and for the conventional 3LC it is used $m_a = 1.0$. In table I, it is presented the weighted total harmonic distortion (WTHD) results. Even with a lower modulation index, the 6LC topology presents a lower WTHD compared with the 3LC.

In table II it is shown the semiconductor losses and current THD, where F_Δ is the triangular carriers frequency, P_{swit} are the switching losses, P_{cond} are the conducting losses and P_{tot} are the total losses. For a same carrier frequency, the losses on the 6LC converter are 0.03 % higher than in the 3LC, although the current THD on the 6LC is lower. To compare the two converters with the same current THD, the carriers frequency of the 6LC converter was decreased to 3 kHz. In this configuration, the losses in the 6LC topology are 49 % lower than in the 3LC.

Although the 6LC converter has more legs, it has lower losses because its switches have lower voltage and lower switching frequency. Besides, the switches with higher voltage (q_{bj}) have the lower switching frequency. This can be noticed at table III, where F_{qj}, F_{qbj} and F_{qaj} are the mean switching frequencies and the subtitles inform the switch considered.

TABLE I
WTHD FOR BALANCED SINUSOIDAL SCENARIO. CARRIERS FREQUENCY $F_\Delta = 10$ kHz, VOLTAGE $V_g = 220$ V RMS, $\mu_{ab} = 0.5$

Topology	WTHD (%)
3LC	0.46
6LC	0.13

B. Scenario 2: non-sinusoidal

On this scenario, the voltage of the scenario 1 was increased with 28 % of 5th harmonic component, therefore, both converters 6LC and 3LC have $m_a = 1$. The grid voltages fundamental component amplitude is 220 V RMS. Table IV presents the losses in this scenario. For a 10 kHz carriers frequency, the losses on the converter 6LC are 58 % lower than in the 3LC. To make the THD of both topologies equal, the carriers frequency for the 6LC topology was decreased to $F_\Delta = 6.6$ kHz. On this scenario, the losses on the converter 6LC are 67 % lower than in the 3LC. As it can be seen in table V, the addition of the 5th harmonic component increased the mean switching frequency of the converter 3LC to its maximum (10 kHz) and decreased the switching frequency of the topology 6LC.

TABLE II
SEMICONDUCTOR LOSSES FOR SINUSOIDAL AND BALANCED SCENARIO. TOTAL POWER $P = 3$ kW, VOLTAGE $V_g = 220$ V RMS AND $\mu_{ab} = 0.5$

Topology	$F_\Delta(k\text{Hz})$	P_{swit}(W)	P_{cond}(W)	P_{tot}(W)	THD(%)
6LC	10	60.1	23.8	83.9	2.8
3LC	10	68.9	12.4	81.3	9.3
6LC	3	17.1	23.6	41.2	9.3

TABLE III
MEAN SWITCHING FREQUENCY FOR SINUSOIDAL AND BALANCED SCENARIO. TOTAL POWER $P = 3$ kW, VOLTAGE $V_g = 220$ V RMS AND $\mu_{ab} = 0.5$

Topology	$F_\Delta(k\text{Hz})$	$F_{qj}(k\text{Hz})$	$F_{q_{bj}}(k\text{Hz})$	$F_{q_{aj}}(k\text{Hz})$
6LC	10	-	1.73	9.73
3LC	10	7.06	-	-
6LC	3	-	2.9	0.54

TABLE IV
SEMICONDUCTOR LOSSES FOR SCENARIO WITH WITH 28% OF FIFTH HARMONIC. TOTAL POWER $P = 3$ kW, VOLTAGE $V_g = 220$ V RMS AND $\mu_{ab} = 0.5$

Topology	$F_\Delta(k\text{Hz})$	P_{swit}(W)	P_{cond}(W)	P_{tot}(W)	THD(%)
6LC	10	61.6	23.8	85.4	4.4
3LC	10	191.7	11.9	203.6	10.0
6LC	6.6	42.5	24.4	66.9	10.0

TABLE V
MEAN SWITCHING FREQUENCY FOR SCENARIO WITH 28% OF FIFTH HARMONIC. TOTAL POWER $P = 3$ kW, VOLTAGE $V_g = 220$ V RMS, $\mu_{ab} = 0.5$ AND $m_a = 1$

Topology	$F_\Delta(k\text{Hz})$	$F_{qj}(k\text{Hz})$	$F_{q_{bj}}(k\text{Hz})$	$F_{q_{aj}}(k\text{Hz})$
6LC	10	-	1.44	9.73
3LC	10	10	-	-
6LC	6.6	-	1.03	6.41

C. Scenario 3: unbalanced

On this scenario, the voltage of scenario 1 was increased with 28 % of negative-sequence component, therefore, both converter 6LC and 3LC have $m_a = 1$, at least for one phase. The grid voltages positive-sequence component amplitude is 220 V RMS. Table VI presents the losses on this scenario. For a 10 kHz carriers frequency, the losses on the converter 6LC are 54 % lower than in the 3LC. To make the THD of both topologies equal, the carriers frequency for the 6LC topology

was decreased to $F_\Delta = 3$ kHz. On this scenario, the losses on the converter 6LC are 78 % lower than in the 3LC. The switching frequency in the different phases do not vary despite the unbalanced reference voltages. As in scenario 2, converter 3LC has the mean switching frequency at its maximum value (10 kHz), while the switching frequency does not change on the 6LC [table VII].

TABLE VI
SEMICONDUCTOR LOSSES FOR SCENARIO WITH 28% OF NEGATIVE-SEQUENCE. TOTAL POWER $P = 3$ kW, VOLTAGE $V_g = 220$ V RMS, $\mu_{ab} = 0.5$ AND $m_a = 1$

Topology	F_Δ(kHz)	P_{swit}(W)	P_{cond}(W)	P_{tot}(W)	THD(%)
6LC	10	70.3	23.9	94.2	3.4
3LC	10	191.8	12.0	203.8	11
6LC	3	21.1	23.7	44.8	11

TABLE VII
MEAN SWITCHING FREQUENCY FOR SCENARIO WITH 28% OF NEGATIVE-SEQUENCE. TOTAL POWER $P = 3$ kW, VOLTAGE $V_g = 220$ V RMS, $\mu_{ab} = 0.5$ AND $m_a = 1$

Topology	F_Δ(kHz)	F_{qj}(kHz)	$F_{q_{bj}}$(kHz)	$F_{q_{aj}}$(kHz)
6LC	10	-	1.43	9.86
3LC	10	10	-	-
6LC	3	-	0.43	2.91

VI. SIMULATION RESULTS

This section presents the simulation results obtained. Some parameters are the same for all simulations of this section. They are: grid voltage fundamental component (60 Hz) amplitude of 220 V RMS, coupling inductor $l_g = 7$ mH, PWM carriers frequency $F_\Delta = 10$ kHz and dc-link capacitors of 9.4 μF. In all simulations it was used a resistive dc load.

Steady-state simulation results are presented in Fig. 6 considering a sinusoidal and balanced scenario. The converter generates 4 levels on voltages v_{baj} and up to 13 levels on the on the phase voltages v_{gj}. On Fig. 6(a) there are only 11 levels on the voltage v_{g1} due to the modulation index ($m_a = 0.72$).

In Figs. 7 and 8, simulation results for non-sinusoidal and unbalanced grid voltages are shown, respectively. The grid voltage was added, for the first scenario, with 28% of 5th harmonic component, and for the second, 28% of negative-sequence component. On these unbalanced and non-sinusoidal scenarios, the converter was able to generate a voltage whose amplitude ($m_a = 1.0$) was higher than the generation limit in a balanced voltage scenario ($m_a = 0.72$). It is important to notice that although the grid voltages may have harmonics or be unbalanced, the control maintains the currents sinusoidal and balanced [Figs. 6(b), 7(b) and 8(c)].

A load transitory from 880 W to 5250 W is presented in Fig. 9. It is possible to observe the action of both control loops in order to maintain the dc-link voltages tracking their reference values [Fig. 9(a)]. It is valid to observe that after the transitory, μ_{ab} stabilizes at a different value [Fig. 9(c)] as well as the grid currents amplitude [Fig. 9(b)] which increases to supply the additional load power demanded.

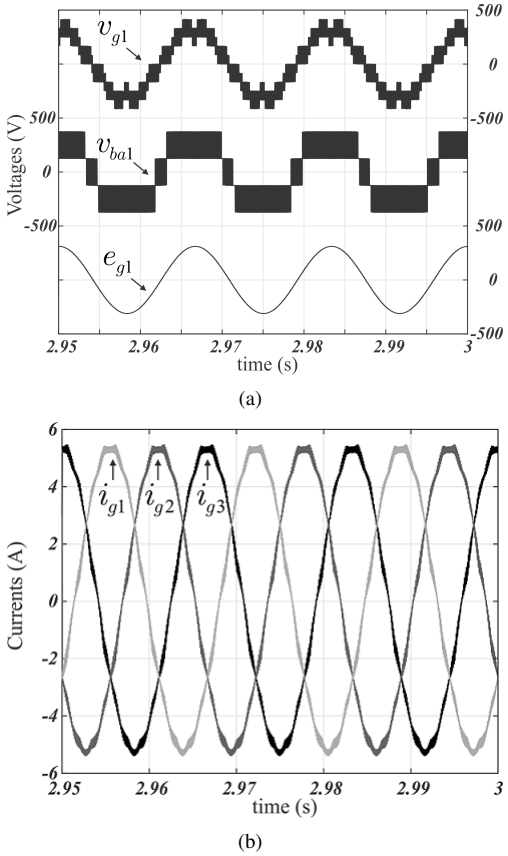


Fig. 6. Sinusoidal and balanced simulation results for a load with 5 kW and $m_a = 0.72$. (a) Rectifier resultant ac voltage (v_{g1}), multilevel resultant pole voltage (v_{ba1}) and grid voltages (e_{g1}). (b) Grid currents (i_{gj}).

VII. EXPERIMENTAL RESULTS

Experimental results were taken using SEMIKRON IGBT (insulated gate bipolar transistor) modules SKM50GB123D and drivers SKHI23. Control and PWM modulation was accomplished by digital signal processor (DSP) TMS320F28335. It has been considered dc-link voltages $v^*_{ca} = 30$ V and $v^*_{cb} = 60$ V, modulation index $m_a = 0.68$, coupling inductor $l_g = 7$ mH, dc-link capacitors $C_a = C_b = 2200$ μF, PWM carriers frequency $F_\Delta = 10$ kHz and a resistive dc-load with power 120 W.

On Figs. 10 and 11, the grid voltages are sinusoidal and balanced. Converter B low switching frequency can be observed on Fig. 10(a). On the other hand, converter A has pole voltage with higher switching frequency. Besides, the high power factor developed can be observed on Figs. 10(b) and 10(c), that show the currents with low distortion and the grid voltages in-phase with its currents. An increase on the power load from 120 W to 150 W is presented on Fig. 11. On this situation, the grid currents increase to provide more power to the load [Fig. 11(a)]. Also, Converter B dc-link voltage has a decrease of 16 % and returns to its reference value within 100 ms [Fig. 11(b)].

Additionally, scenarios with harmonic and negative se-

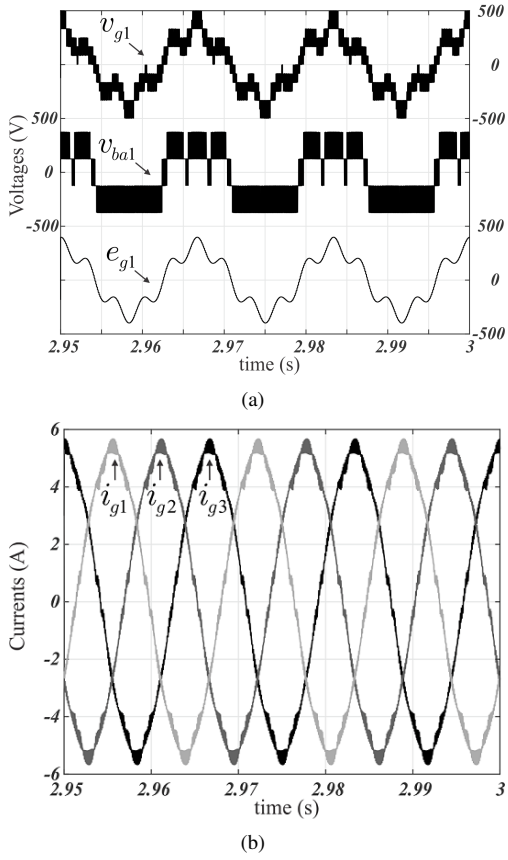


Fig. 7. Non-sinusoidal balanced simulation results for a load with 5 kW and $m_a = 1$. Rectifier resultant ac voltage (v_{g1}), multilevel resultant pole voltage (v_{ba1}) and grid voltages (e_{g1}) .(b) Grid currents (i_{gj}).

quence are presented on Fig. 12. The addition of 5th harmonic to the grid voltages does not increases converter B switching frequency, which can also be observed on Fig. 12(a). Also, on Fig. 12(b), output PWM voltages with unbalanced grid voltages are shown.

VIII. CONCLUSION

In this work, it was studied a three-phase open-end power rectifier with one floating dc-link capacitor (6LC). Situations with unbalanced and non-sinusoidal grid voltages were discussed. On these scenarios, the floating capacitor control was not disturbed and the converter was capable of reaching its maximum amplitude voltage, using the floating capacitor converter to compensate harmonic and negative-sequence components.

The 6LC converter performance has been compared to a conventional topology (3LC). In the three scenarios considered, the studied converter presented lower THD and mean switching frequency considering the same carriers frequency compared to the 3LC. Also, the 6LC obtained lower semiconductor losses considering the same current THD compared to conventional 3LC topology. In both scenarios with disturbances on the grid voltage, the improvement in the performance from 3LC to 6LC was especially higher because

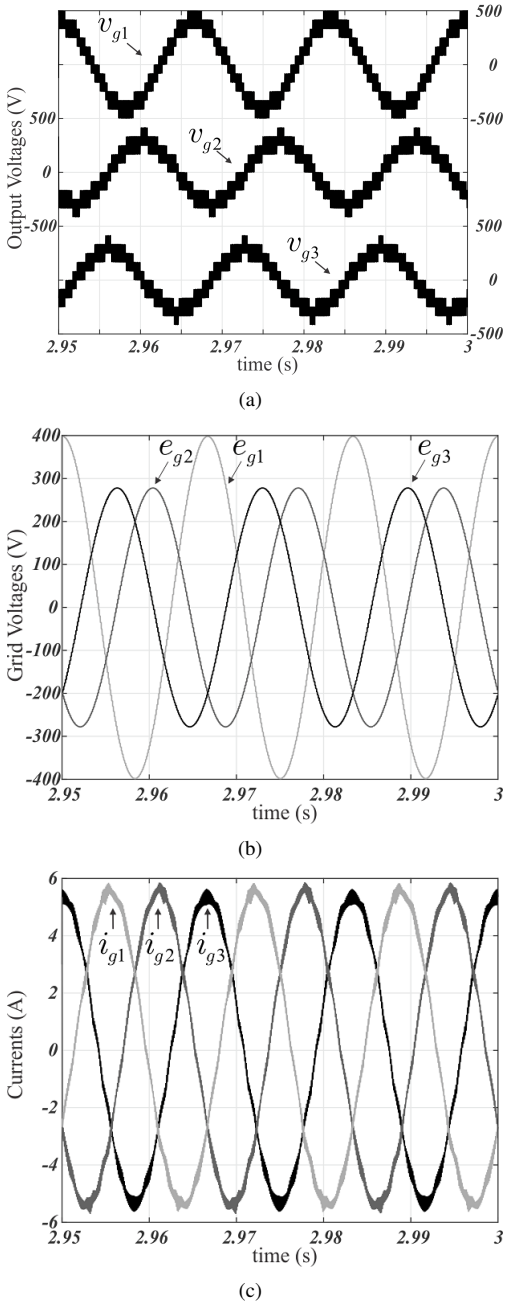
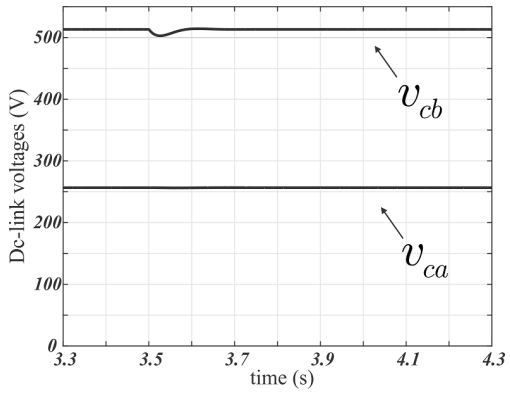


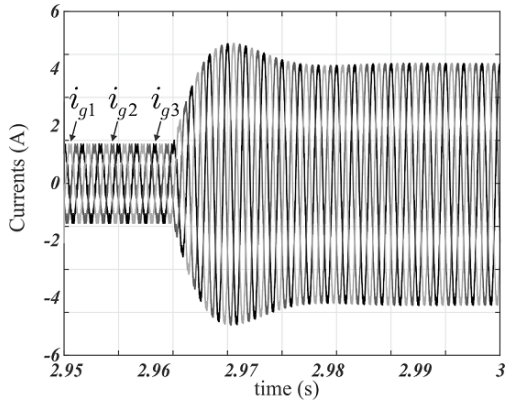
Fig. 8. Unbalanced scenario simulation (28% of negative-sequence component). Load with 5 kW and $m_a = 0.72$ (a) Rectifier resultant ac voltage (v_{gj}). (b) Grid voltages (e_{gj}. (c) Currents (i_{gj}).

the addition of harmonics and negative sequence increased the switching frequency of 3LC converter and increased the modulation index on the 6LC. Also, these disturbances did not increased the mean switching frequency on the 6LC converter switches.

The outcomes validated the theoretical expectations of the studied system. Indeed, simulation and experimental results have been obtained with great accordance.



(a)



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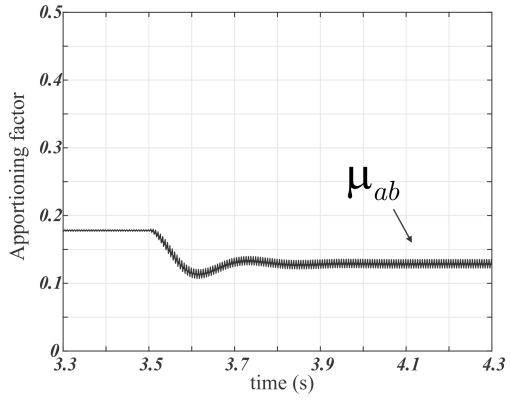
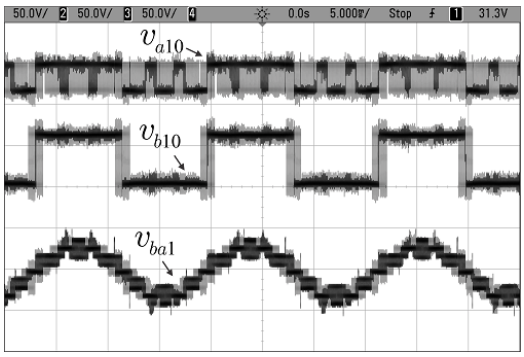
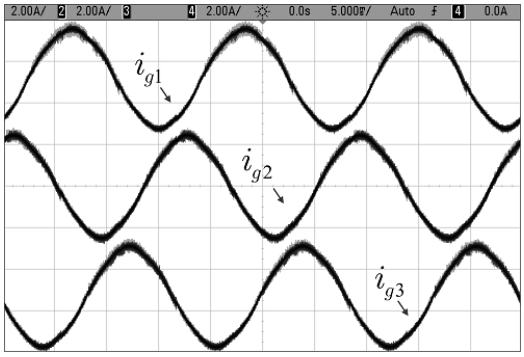


(c)

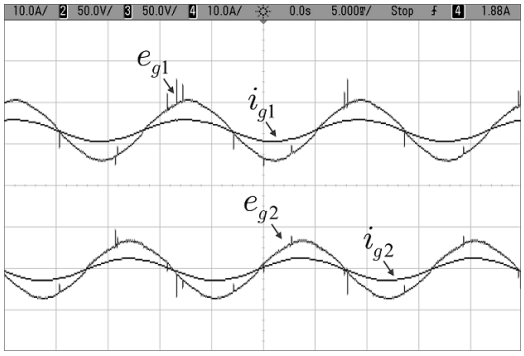
Fig. 9. Simulation results. Load transitory from 880 W to 5250 W with $m_a = 0.7$. (a) Converter B dc-link voltage (v_{cb}) and Converter A dc-link voltage (v_{ca}). (b) Grid currents (i_{gj}). (c) Apportioning factor (μ_{ab}).



(a)



(b)



(c)

Fig. 10. Experimental results. Steady-state sinusoidal balanced scenario. (a) Rectifier resultant ac voltage and pole voltages (v_{gj}, v_{bj0} and v_{aj0}). (b) Currents (i_{gj}). (c) Grid voltages (e_{gj}) and currents(i_{gj})

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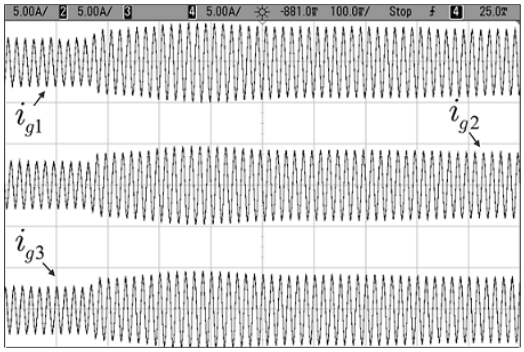
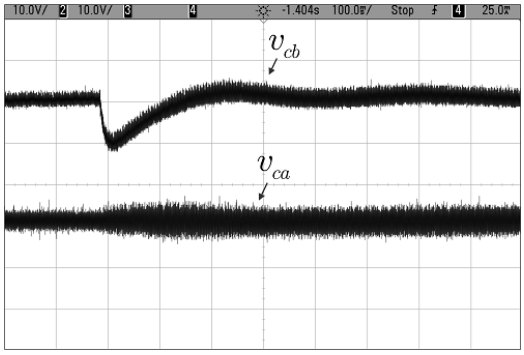
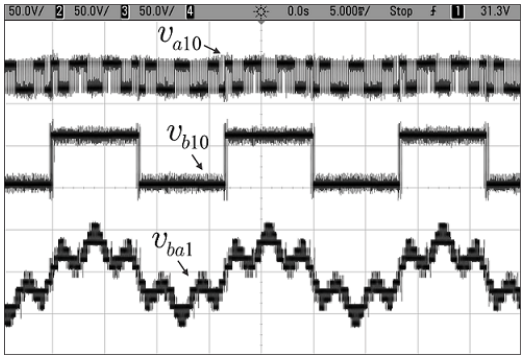


(a)

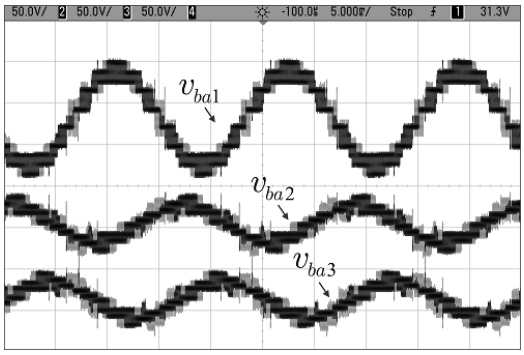


(b)

Fig. 11. Experimental results. Load transient from 120 W to 150 W. (a) Currents (i_{gj}). (b) Dc-link capacitor voltages (v_{ca} and v_{cb}).



(a)



(b)

Fig. 12. Experimental results. (a) Non-sinusoidal scenario voltages (v_{g1}, v_{b10} and v_{a10}). (b) Unbalanced scenario rectifier resultant ac voltages (v_{gj}).

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