Adaptive Dead Time Synchronous Rectification Control for High Efficiency LLC Resonant Converter

SangCheol (Caprio) Moon
Industrial and Offline Power Division
ON Semiconductor
Bucheon, Republic of Korea
caprio.moon@onsemi.com

ChengSung Chen
Industrial and Offline Power Division
ON Semiconductor
Hsinchu, Taiwan
jeff.chen@onsemi.com

DongJin Park
Industrial and Offline Power Division
ON Semiconductor
Bucheon, Republic of Korea
dongjin.park@onsemi.com

***Abstract*— In low output voltage and high output current LLC resonant converter applications, a synchronous rectification (SR) is essential component for high efficiency and high power density. In the conventional SR control method, instantaneous drain voltage sensing method is widely used because it shows very simple control algorithm. However, the method has disadvantage against stray inductances in MOSFET package and PCB pattern. The stray inductances induce premature turn-off of SR gate and large SR dead time. Since the body diode conduction time is increased, the system efficiency is decreased in the conventional method. To compensate the stray inductance effect and increase system efficiency, an adaptive dead time control method is proposed. In the proposed control method, SR dead time is regulated to predetermined dead time target regardless of the stray inductances by using present drain voltage information and previous cycle dead time information. To verify the validity of the proposed control method, 240W prototype is built and experimented with the proposed controller which is implemented with 0.35-μm BCDMOS technology.**

Keywords—LLC Converter, Synchronous Rectification

I. INTRODUCTION

Among many resonant type converters, a LLC resonant converter has been the most popular topology since this topology has many advantages over other resonant topologies; it can regulate the output over entire load condition with a relatively small switching frequency variation, it can achieve zero voltage switching (ZVS) for the primary side switches and zero current switching (ZCS) for the secondary side rectifiers. In the LLC resonant converter, rectifier diodes are typically used to obtain DC output voltage from the transformer secondary side winding. The conduction loss of a diode rectifier contributes significantly to the overall power losses in the LLC resonant converter; especially in low voltage and high current output applications such as 200 ~ 300 W adapter power supplies. Because the conduction loss of a rectifier is proportional to the product of its forward-voltage drop and the forward conduction current. In addition, to handle the temperature of the diode rectifier, large size heatsink is also required. On the other hand, in synchronous rectification (SR) which replaces rectifier diodes as MOSFETs with a small on resistance R_{DS_ON}, the forward-voltage drop of the synchronous rectifier can be lower than that of the diode rectifier so that the rectifier conduction loss is dramatically decreased. Consequently, the heatsink for the rectifier can be reduced. It is good for higher power density.

In the conventional SR control method, instantaneous drain-source voltage sensing type is widely used due to simplicity. Before SR gate is turned on, SR body diode conducts as normal diode rectifier. Once the body diode starts conducting, the drain-source voltage drops below the turn-on threshold voltage which triggers the turn-on of the SR gate. Then the drain-source voltage is determined by the product of R_{DS_ON} and instantaneous SR current. When the drain-source voltage reaches the turn-off threshold voltage as SR current decreases to near zero, SR gate is turned off. If the turn off threshold is set as close as possible to zero, the turn off dead time can be minimized in this control method.

However, in the practical system, the stray inductances of MOSFET package and PCB pattern prevent exact drain-source voltage sensing at SR turn-off instant. The typical stray inductance of the MOSFET packages are summarized in Fig. 1 and the stray inductance effect is described in Fig. 2 and Fig. 3. If there is no stray inductance, V_{DS} becomes opposite sine-wave which follows SR current shape when SR gate is turning on in Fig. 2. However, in case with stray inductance as shown in Fig. 3, offset voltage $V_{LS}(t)$ is induced by:

$$V_{LS}(t) = -L_{Stray} \times \frac{di_{SR}}{dt} \tag{1}$$

on the stray inductance. This induced voltage makes drain-source sensing voltage of MOSFET larger than the product of R_{DS_ON} and instantaneous SR current when SR current decreases. It results in premature turn-off of SR gate and large dead time as shown in Fig. 3. As a result, the conduction loss increases.

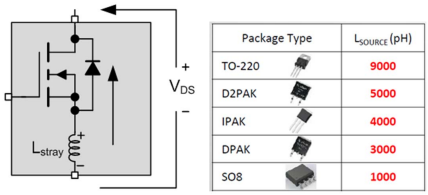


Fig. 1. Stray inductance of MOSFET package

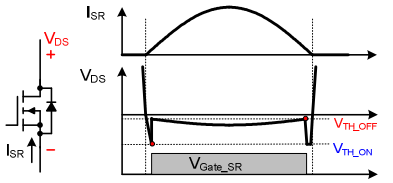


Fig. 2. SR current and gate waveform without L_{stray}

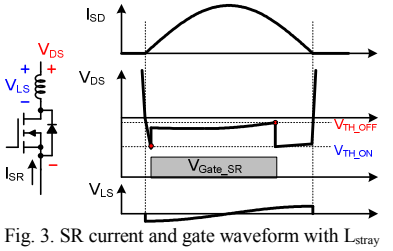


Fig. 3. SR current and gate waveform with L_{stray}

To overcome the stray inductance effect and increase SR turn-on time, [1] and [2] proposed adaptive synchronous rectifier driving scheme. However, those control methods are only based on previous cycle on-time and dead time information. In that case, SR inversion current which makes huge drain voltage spike may occur during fast load transient with large frequency variation.

To solve this problem and compensate the induced offset voltage by stray inductance, this paper proposes an adaptive dead time control method which can achieve higher efficiency with better transient characteristic.

II. Analysis of The Proposed Adaptive Dead Time Control Method

A. System Block Diagram

Fig. 4 shows the system block diagram of the proposed control method. To make explanation easy, LLC control and GATE2 control methods are not described. SR gate turn-on method is the same with the conventional control method. When V_{D1} is decreased and lower than V_{TH_ON} by body diode conduction of $M1$, gate signal V_{G1} becomes high and SR gate is turned on.

On the other hand, when SR gate is turned off, V_{SAW} signal is utilized. When V_{SAW} is higher than turn-off threshold voltage V_{TH_OFF}, SR gate is turned off as below equation:

$$\begin{aligned} V_{SAW} &\geq V_{TH\_OFF} \\ V_{D1} + V_{Comp} &\geq V_{TH\_OFF} \end{aligned} \tag{2}$$

where, V_{Comp} is compensation voltage. Rearranging (2), SR gate is turned off when the V_{D1} is higher than virtual turn-off threshold voltage $V_{TH\_OFF\_V}$ as below:

$$\begin{aligned} V_{D1} &\geq V_{TH\_OFF} - V_{Comp} \\ V_{D1} &\geq V_{TH\_OFF\_V}. \end{aligned} \tag{3}$$

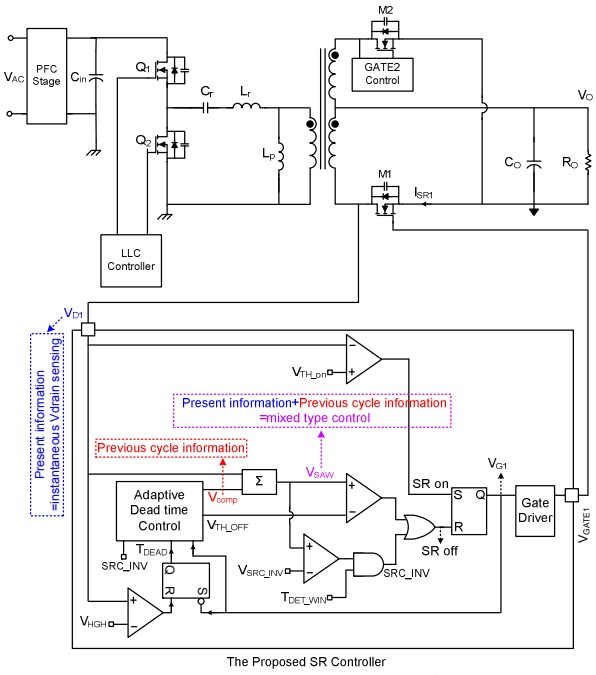


Fig. 4. Stray inductance of MOSFET package

In V_{SAW}, the drain sensing voltage V_{D1} which has present information is combined with an internal compensation voltage V_{Comp} which has previous cycle dead time information to compensate the stray inductances. Since V_{SAW} signal has both present information and previous cycle information, the proposed control method becomes mixed type control which can provide better transient characteristic and low conduction loss. In steady state, V_{SAW} is compared with V_{TH_OFF} to minimize the dead time and maximize the SR conduction time. During load transient, especially from heavy load to light load condition, V_{SAW} can be compared with current inversion detection threshold voltage V_{SRC_INV} within detection window time T_{DET_WIN} which is 0%~50% of previous cycle SR conduction time. If V_{SRC_INV} is set slightly lower than zero voltage, it can turn off SR faster than V_{TH_OFF} comparator during transient to prevent inversion current. Once SRC_INV is triggered, adaptive dead time control parameters are reset in the adaptive dead time control block.

In the adaptive dead time control block, V_{Comp} is generated by previous cycle SR dead time T_{DEAD} which is measured from V_{G1} falling edge to where V_{D1} is higher than drain high threshold voltage V_{HGH}. If the dead time is larger than the dead time regulation target t_{TARGET} as shown in Fig. 5, the virtual turn-off threshold voltage $V_{TH\_OFF\_V}$ is increased by decreasing V_{Comp} in the next switching cycle. Then T_{DEAD} can be closed to t_{TARGET} as described in Fig. 6. On the contrary, when the dead time T_{DEAD} is smaller than t_{TARGET} as shown in Fig. 7, $V_{TH\_OFF\_V}$ is decreased by increasing V_{Comp} in the next switching cycle. If V_{Comp} is saturated to maximum value or minimum value, V_{TH_OFF} is also adaptively changed in accordance with V_{Comp} saturation level.

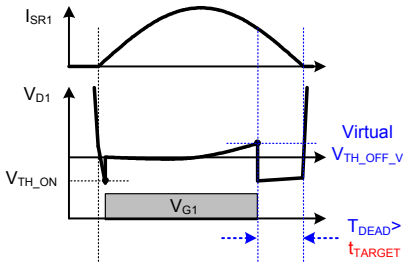


Fig. 5. $T_{DEAD} > t_{TARGET}$

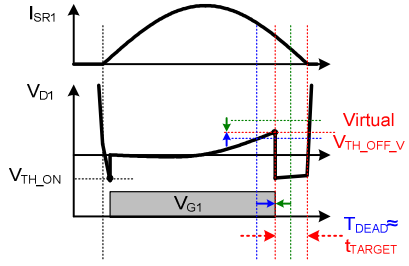


Fig. 6. $T_{DEAD} \fallingdotseq t_{TARGET}$

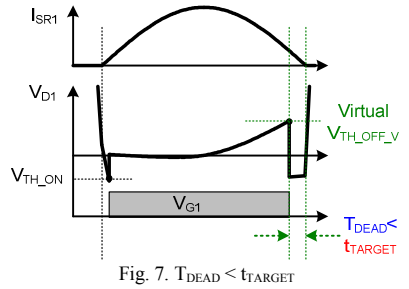


Fig. 7. $T_{DEAD} < t_{TARGET}$

B. Adaptive Dead Time Control

Fig. 8 and Fig. 9 illustrate the proposed adaptive dead time control block diagram and control algorithm, respectively. When the control algorithm starts, V_{Comp} and V_{TH_OFF} are generated with initial value. If T_{DEAD} is smaller than t_{TARGET}, up/down flag *UP1* of a *COMP_CNT* counter becomes high. So, the counter is set as a up counter. Then if the counter is not saturated by maximum value, which means *HSAT* is low, at next rising edge of V_{G1}, *COMP_CNT* is updated by:

$$COMP\_CNT = COMP\_CNT(n-1)+1. \qquad (4)$$

Then, the controller check updated COMP_CNT whether maximum value or not. Finally, digital to analog converter *DAC1* generates V_{Comp} according to *COMP_CNT[4:0]*. If *HSAT* is high in previous cycle and UP1 is high, SR latch *SR1* is reset. Then, up/down flag *UP2* of a *OFF_CNT* counter becomes low and the counter is set as a down counter. As a result, *OFF_CNT* is updated by:

$$OFF\_CNT = OFF\_CNT(n-1)-1. \qquad (5)$$

At the same time, digital to analog converter *DAC2* decreases V_{TH_OFF} and clears HSAT signal. This makes virtual turn-off threshold voltage $V_{TH\_OFF\_V}$ decrease and dead time increase.

On the other hand, if T_{DAED} is larger t_{TARGET}, up/down flag *UP1* of a *COMP_CNT* counter is set to low. Then if the counter is not saturated by minimum value, which means *LSAT* is low, *COMP_CNT* is decreased at next rising edge of V_{G1} by :

$$COMP\_CNT = COMP\_CNT(n-1)-1. \qquad (6)$$

After then, updated *COMP_CNT* is verified with minimum value signal. Finally, V_{Comp} is decreased by digital to analog converter *DAC1* output *COMP_CNT[4:0]*. If *LSAT* is high in previous cycle and UP1 is low, SR latch *SR1* becomes set. Then, up/down flag *UP2* of a *OFF_CNT* counter goes high and the counter is set as a up counter and *OFF_CNT* is calculated by:

$$OFF\_CNT = OFF\_CNT(n-1)+1. \qquad (7)$$

At a result, V_{TH_OFF} is increased by digital to analog converter *DAC2* output, and clears *LSAT* signal. It makes virtual turn-off threshold voltage $V_{TH\_OFF\_V}$ increase and dead time decrease.

Therefore, the proposed adaptive dead time control method provides dead time regulation at around t_{TARGET} in the steady state regardless of the stray inductance. It induces lower conduction loss of SR MOSFET and can achieve higher efficiency when compared to the conventional SR control method. In addition, since the proposed control method uses instantaneous drain voltage information within current inversion detection window time, SR gate can be turned off properly during load transient. It can provide excellent transient characteristic without SR inversion current.

Fig. 10 shows simulation result of V_{Comp} and V_{TH_OFF} changes with soft load transient. When the output load is increased, induced offset voltage $V_{LS}(t)$ by stray inductance is also increased due to steep I_{SR1} slope. It induces SR dead time T_{DEAD} increases. Therefore, the proposed adaptive dead time control algorithm operates with (6) and (7). The system goes stead state at 12ms and T_{DEAD} is regulated with t_{TARGET} again. After then, the output load is decreased, the proposed control resumes operation. Then, V_{Comp} and V_{TH_OFF} is controlled by (4) and (5).

When the output load is changed severely as shown in Fig. 11, the current inversion detection is triggered to prevent

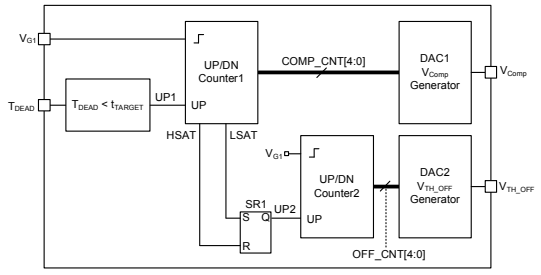


Fig. 8. Adaptive Dead Time Contrl Block

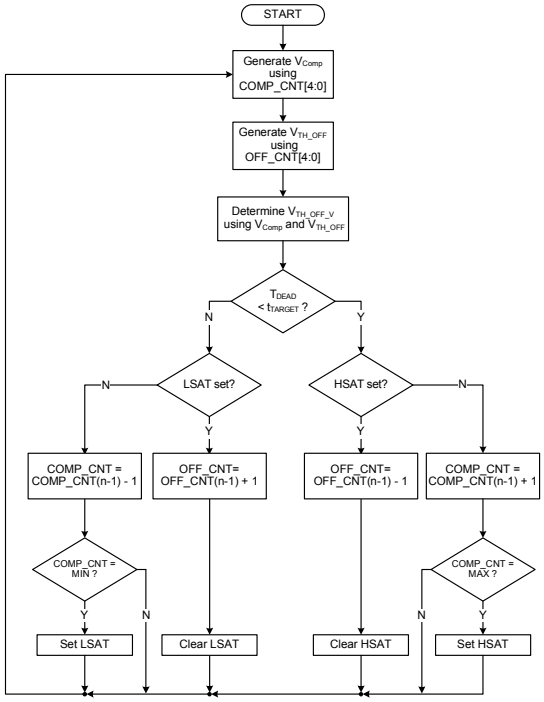


Fig. 9. Adaptive dead time control algorith

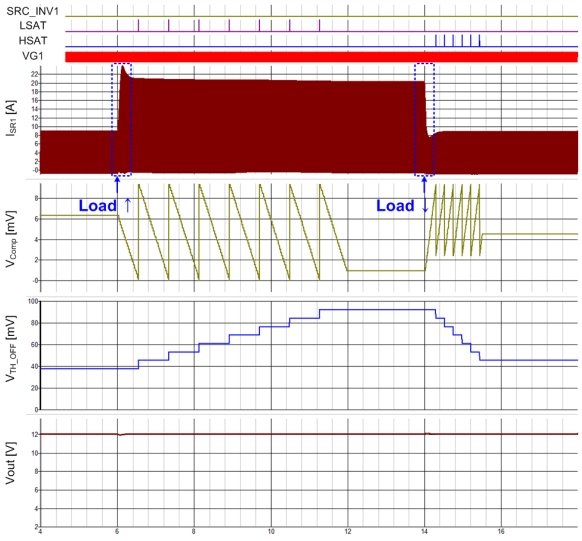


Fig. 10. Simulation Results when load changes softly

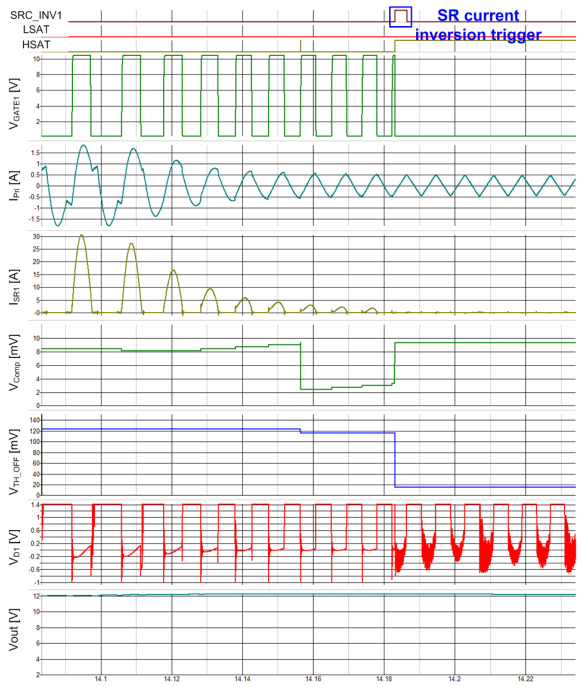


Fig. 11. Simulation Results when load changes severely

reverse current and turn-off SR gate immediately. Then V_{Comp} and V_{TH_OFF} parameters are reset. It helps fast load transient.

III. Design Considerations

To operates the proposed adaptive dead time control method and design LLC system with the synchronous rectification, the compensation voltage step size, the virtual turn-off threshold voltage trajectory and light load operation need to be considered.

A. Compensation Voltage V_{Comp} Step Size

In the proposed adaptive dead time control method, V_{Comp} step size should be properly selected for stable operation. If too small V_{Comp_Step} is designed, the virtual turn-off threshold voltage $V_{TH\_OFF\_V}$ range becomes narrow in (3). It results in undefined control range in steady state operation as shown in Fig. 12. When the output load is set to the undefined range, the proposed control method repeatedly increases and decreases V_{TH_OFF} between V_{TH_OFF1} and V_{TH_OFF2} to regulate SR dead time to t_{TARGET}. Therefore it may induce the output current oscillation and audible noise. To avoid this unstable operation, V_{Comp_Step} needs to have relatively large value to make overlap range between $V_{TH\_OFF\_V2}$ range and $V_{TH\_OFF\_V1}$ range as shown in Figure 13. Therefore, V_{Comp} step size is recommended as small as value satisfying :

$$V_{TH\_OFF2} - V_{TH\_OFF1} < V_{Comp\_MAX} - V_{Comp\_MIN} = N \times V_{Comp\_Step} \quad (8)$$

where, N is total number of step of V_{Comp}.

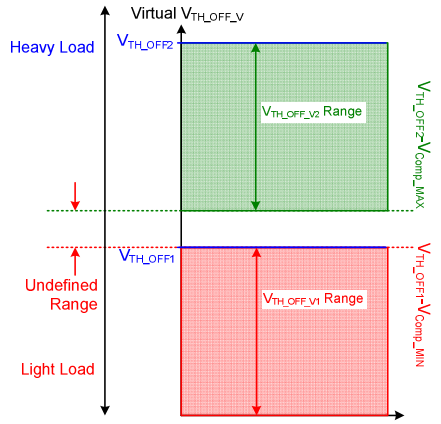


Fig. 12. Virtual $V_{TH\_OFF\_V}$ range with small V_{Comp_Step}

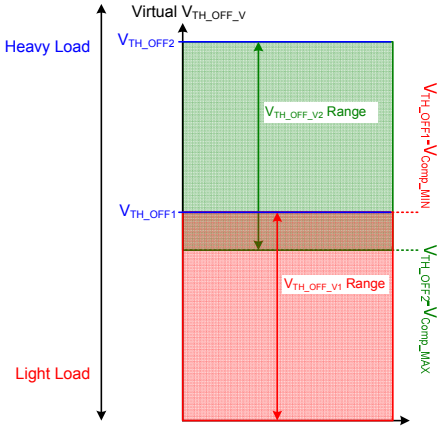


Fig. 13. Virtual $V_{TH\_OFF\_V}$ range with large V_{Comp_Step}

B. Virtual Turn-off Threshol Voltage $V_{TH\_OFF\_V}$ Trajectory

When V_{TH_OFF} is changed by *LSAT* or *HSAT* high, V_{Comp} should be set or reset to proper value which provides soft transition from V_{TH_OFFN} to $V_{TH\_OFFN\pm1}$. If it is not considered, the SR dead time jumping may happen. It can induce the output current oscillation.

In case of the output load increase, V_{Comp} should be reset to maximum value at V_{TH_OFF} one step increasing, if V_{Comp_Step} is satisfied with (8). When $V_{TH\_OFF\_V}$ equals to (V_{TH_OFF1} - V_{Comp_MIN}), $V_{TH\_OFF\_V}$ is slightly cutback to (V_{TH_OFF2} – V_{Comp_MAX}). As a result, $V_{TH\_OFF\_V}$ follows blue line trajectory and shows soft transition as shown in Fig. 14.

When the output load is decreased, V_{Comp} needs to set to optimized value satisfying:

$$V_{TH\_OFF2} - V_{Comp\_MAX} < V_{TH\_OFF1} - V_{Comp\_StepK} \quad (9)$$

where, V_{Comp_StepK} is the value of set at V_{TH_OFF} decreasing. $V_{TH\_OFF\_V}$ decreasing trajectory is illustrated in Fig. 15. When $V_{TH\_OFF\_V}$ is decreased to (V_{TH_OFF2} – V_{Comp_MAX}), $V_{TH\_OFF\_V}$ becomes ($V_{TH\_OFF1} - V_{Comp\_StepK}$) for better $V_{TH\_OFF\_V}$ transition. After then, $V_{TH\_OFF\_V}$ is determined by the adaptive dead time control algorithm.

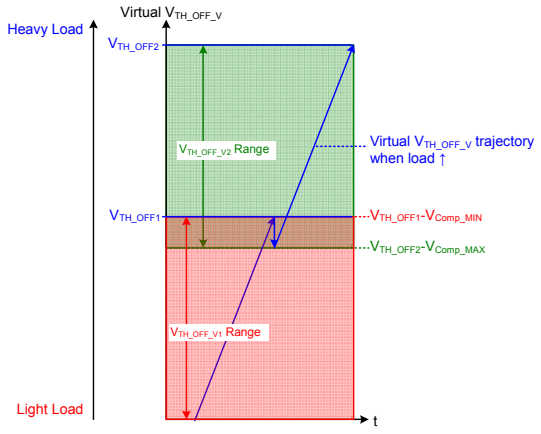


Fig. 14. Virtual $V_{TH\_OFF\_V}$ trajectory when load increases

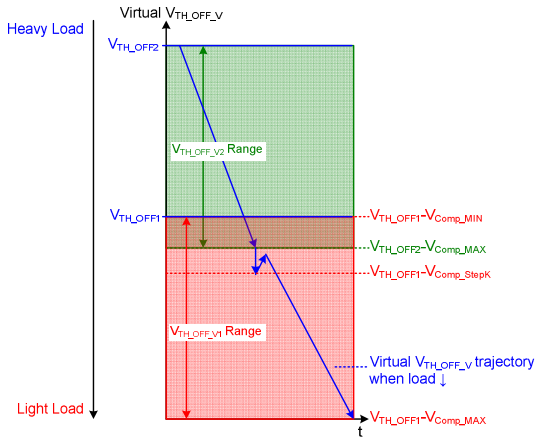


Fig. 15. Virtual $V_{TH\_OFF\_V}$ trajectory when load decreases

C. Light Load Operation

In LLC resonant converter, light load operation with the synchronous rectifier is quite different from the conventional diode rectifier due to large output capacitance of SR MOSFET. To control SR in light load condition, it is important to understand light load condition behavior. For the light load operation analyze, the switching period is subdivided into 5 modes. The main equivalent circuits for operation modes are shown in Fig. 16. operational waveforms in light load condition is depicted in Fig. 17.

Mode 1 ($t_0 \sim t_1$): *Mode 1* begins at t_0 when the primary switch Q_1 is turned off. An equivalent circuit is shown in Fig. 16 (a). In this mode, C_{OSS1} and $C_{OSS}SR1$ are charged, and C_{OSS2} and $C_{OSS}SR2$ are discharged by the resonant current I_{Lr}. In addition, the magnetizing inductor voltage V_{Lp} increases in this mode. When the transition of drain voltages (V_{DS1}, V_{DS2}, V_{SR1DS}, V_{SR2DS}) is completed, this mode ends. In the practical LLC resonant converter system, the transition of V_{DS1} and V_{DS2} may end earlier than that of V_{SR1DS} and V_{SR2DS}. Zero voltage switching (ZVS) of Q_2 and M_2 can be guaranteed during this mode.

Mode 2 ($t_1 \sim t_2$): When *Mode 1* ends, the body diodes of Q_2 and M_2 are conducted. The resonant inductor voltage V_{Lr} is still determined by the resonant capacitor voltage V_{Cr} and V_{Lp}. However, since V_{Cr} is not larger enough to build up I_{Lr} and most of the V_{Cr} applies to L_p, the LLC converter cannot transfer power to the secondary side and the secondary SR current I_{SR2} decreases with a slope of $n^2*(V_o+V_F)/L_p$. In the secondary side, body diode of M_1 is turned off so that I_{SR1} is added to I_{SR2} at t_1. It results in sudden increase of I_{SR2} which is called as capacitive current spike at t_1. In addition, in this mode, V_{SR2DS} becomes $-V_F$ at t_1. It generates turn-on signal of M_2. However, the turn-on signal should be ignored, because there is no power transfer from the primary side until I_{Lr} build-up. If the turn-on signal is not prevented, abnormal turn-on happen at t_3 as shown in Fig. 18. The mis-trigger signal induces inversion current of M_2 from the output capacitor. *Mode 2* ends when Q_2 is turned on

Mode 3 ($t_2 \sim t_3$): In this mode, I_{Lp} decreases with the same slope of that of *Mode 2* until I_{SR2} becomes zero. In the primary side V_{Cr} is charged by I_{Lp}. The equivalent circuit is shown in Fig. 16 (c).

Mode 4 ($t_3 \sim t_4$): In the primary side, since V_{Lp} is not clamped by the output voltage any more, V_{Cr} is divided into V_{Lp} and V_{Lr} with their inductance ratio:

$$V_{Lp} = V_{Cr} \cdot L_p / (L_r + L_p) \tag{10}$$

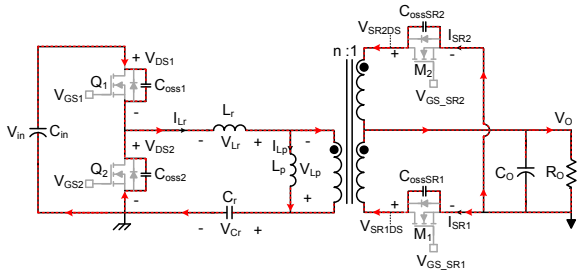
$$V_{Lr} = V_{Cr} \cdot L_r / (L_r + L_p) . \tag{11}$$

In addition, C_r is gradually charged by I_{Lp}. In the secondary side, since I_{SR2} is zero at t_3, sub-resonance starts between $C_{OSS}SR1$ and $C_{OSS}SR2$, L_r, and L_p. the sub-resonance period $T_{sub\text{-}res}$ can be calculated by:

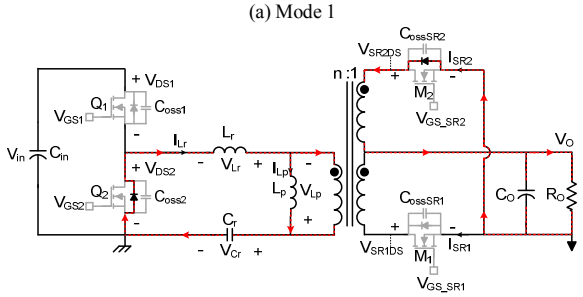
$$T_{sub-res} = 2\pi\sqrt{(L_r \parallel L_p) \cdot n^2 (C_{OSS}SR1 + C_{OSS}SR2)} . \tag{11}$$

As a result, V_{SR2DS} oscillates as shown in Fig. 17 and I_{Lr} cannot transfer power to the secondary side until V_{Lp} becomes $n*(V_o+V_F)$. Finally, when V_{Lp} reaches $n*(V_o+V_F)$, V_{Lp} is clamped by $n*(V_o+V_F)$ and I_{Lr} builds up and I_{SR2} increases. Therefore, V_{GS_SR2} should be turned on after the sub-resonance ends to prevent the inversion current in Fig. 18.

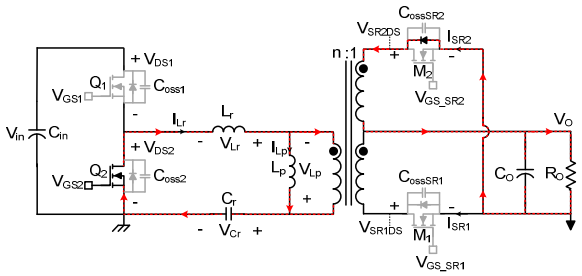
Mode 5 ($t_4 \sim t_5$): After t_{ON_DLY} finishes, M_2 is turned on so that V_{SR2DS} is determined by product of R_{DS_ON} of M_2 and instantaneous SR current I_{SR2}. When V_{SR2DS} is higher than turn-off threshold voltage V_{TH_OFF}, M_2 is turned off and this mode ends. In this mode, to guarantee stable operation under light load condition, t_{ON_DLY} is should be set at t_4 which can be varied with the output load condition.



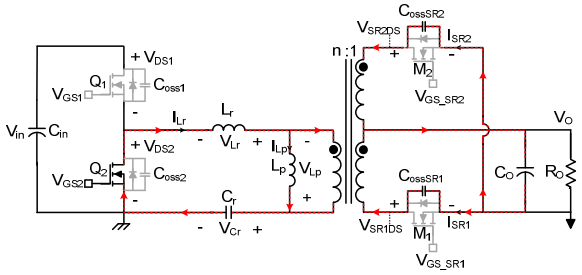
(a) Mode 1



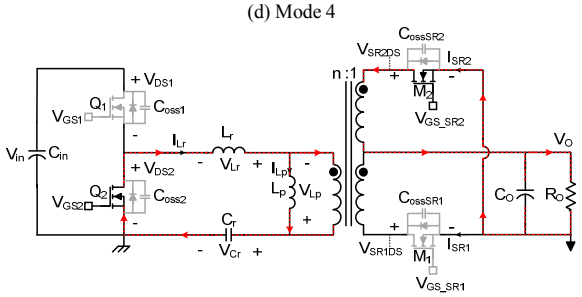
(b) Mode 2



(c) Mode 3



(d) Mode 4



(e) Mode 5

Fig. 16. Equvalent circuits in light load condition

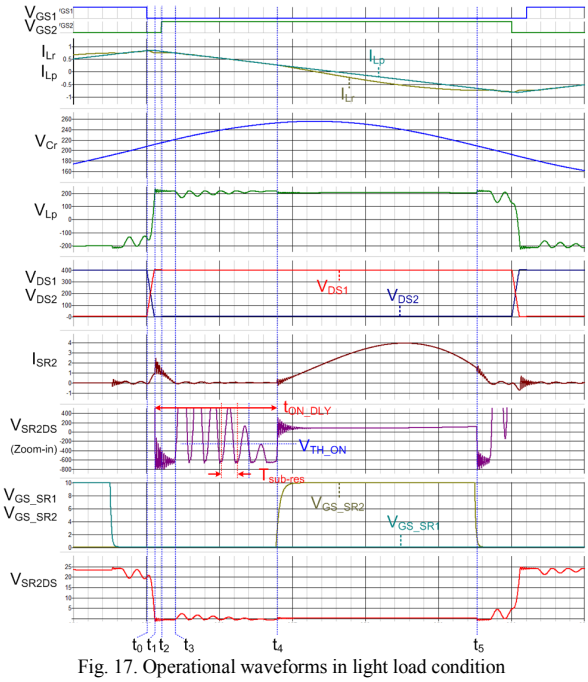


Fig. 17. Operational waveforms in light load condition

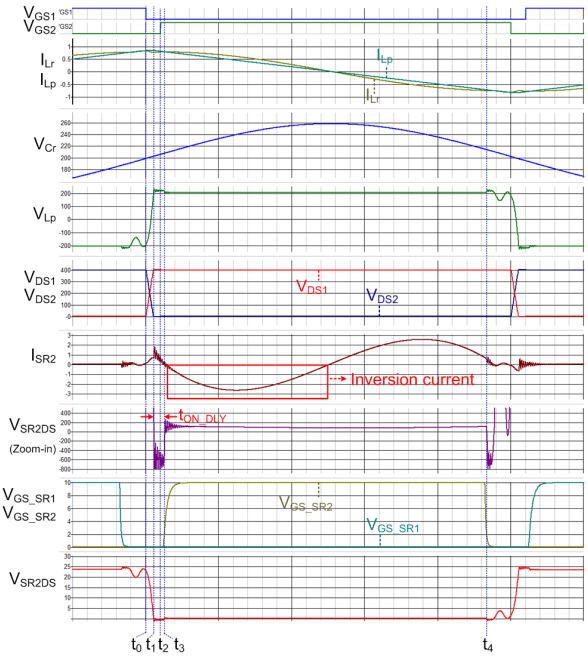


Fig. 18. Current inversion waveform with SR mis-triggering

IV. The Experimental Results

A prototype for 240W power supply system, which is configured boost PFC and LLC resonant converter with the proposed controller, is built and experimented on to verify the validity of the proposed control method as shown in Fig. 19. The proposed control method is implemented with 0.35-μm BCDMOS technology. Two SR drivers and the proposed control method operate independently for two SR MOSFETs. In the system specifications as shown in Table I, the input voltage is 220Vac, the output voltage is 19.5V and the maximum output current is 12.3 A. The operating frequency f_s of LLC resonant converter is 105 kHz under full load condition. In the resonant tank design, the resonant inductance and magnetizing inductance are 80 μH and 650 μH, respectively, and the resonant capacitance is 33 nF. In the adaptive dead time control, the dead time target t_{TARGET} is 230 ns in heavy load condition and 280 ns in light load condition.

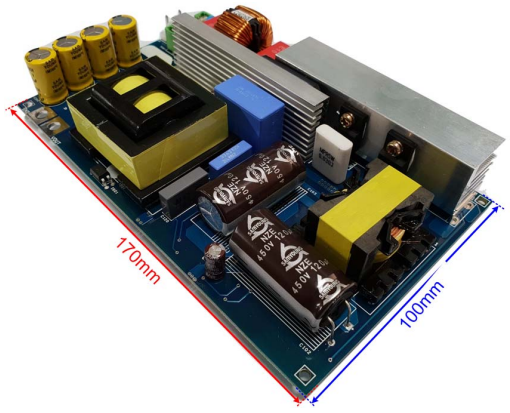


Fig. 19. The prototype of the proposed system verification board

TABLE I. SYSTEM SPECIFICATIONS

Parameters	Value
Input voltage V_{in}	230 Vac
Output voltage V_o	19.5 V
Output current I_o	12.3 A
Output Power P_o	240 W
Switching frequency f_s @ full load condition	105 kHz
Resonant inductance L_r	80 µH
Magnetizing inductance L_m	650 µH
Resonant capacitance C_r	33 nF
LLC transformer turns ratio	31 : 3
Dead time target t_{TARGET} @ heavy load condition	230 ns
Dead time target t_{TARGET} @ light load condition	280 ns

Fig. 20 shows experimental waveforms of the proposed adaptive dead time control method under full load condition. The dead time T_{DAED} is measured from GATE1=2V falling to V_{D1}=0.8V rising. Maximum T_{DEAD} is 258ns and minimum T_{DEAD} is 202ns. It verifies T_{DEAD} is regulated at around 230ns of t_{TARGET}. In Fig. 21, the proposed control method is also verified under light load condition. In this condition, t_{TARGET} is increased to 280ns for safe operation. Since the output current falling slope is reduced, the induced voltage of the stray inductance, which is determined by (1), is also decreased when compared with that of heavy load condition. It may induces larger dead time variation. Therefore, larger t_{TARGET} may be required in a system. In the proposed system, it operates well with 280ns of t_{TARGET} under light load condition.

Fig. 22 and Fig. 23 are steady state operation under heavy load and light load conditions, respectively. In heavy load condition operation, the primary current I_{pri} shows above resonance operation. In this condition, turn-on is triggered by the drain sensing voltage V_{D1} with body diode conduction, and turn-off is determined by the proposed adaptive dead time control method. Thus, the turn-on time is maximized with t_{TARGET} as can be seen in Fig. 22. In the light load condition, the proposed control method also operates well.

Fig. 24 shows the output load on/off waveforms. The output load is repeatedly changed between 0A to 10A and the load on/off frequency is 1 kHz. When the output load is decreased to 0A, SR GATE1 and GATE2 are stopped without delay. On the other hand, when the output load is increased to 10A, there is wake-up delay to resume IC operation. Under this severe load transient condition, the proposed control method is also verified to have stable operation.

Fig. 25 measured the efficiency comparison with the conventional SR control method which has the constant turn-off threshold level without the stray inductance compensation. The result shows the proposed control method is higher efficiency than that of the conventional control method. In the full load condition, the proposed control method shows 0.2% point higher than that of the conventional controller. The efficiency difference increases as load decreases. In 2A load condition, the proposed control method shows 2.5% point higher efficiency.

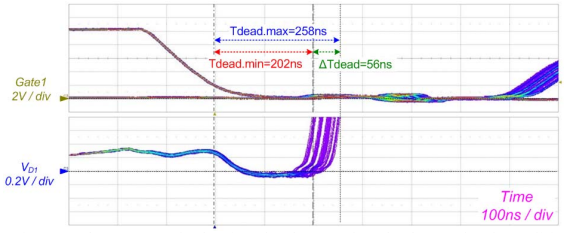


Fig. 20. The proposed adaptive dead control under heavy load condition

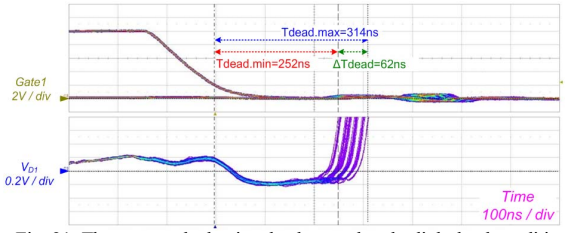


Fig. 21. The proposed adaptive dead control under light load condition

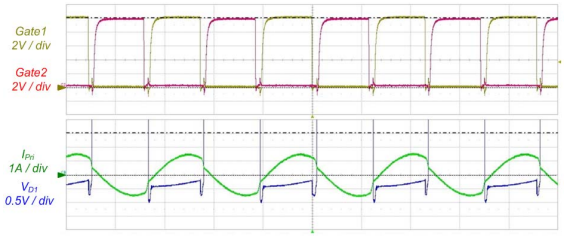


Fig. 22. SR waveforms under heavy load condition

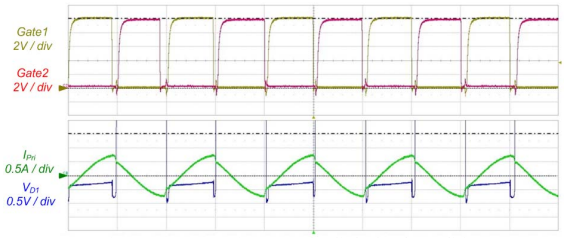


Fig. 23. SR waveforms under light load condition

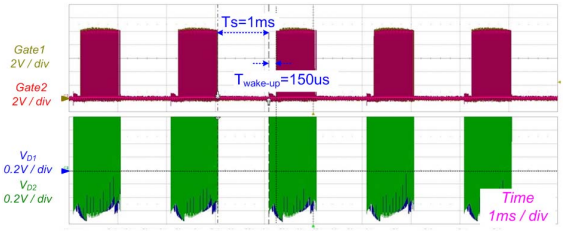


Fig. 24. SR waveforms under load on/off

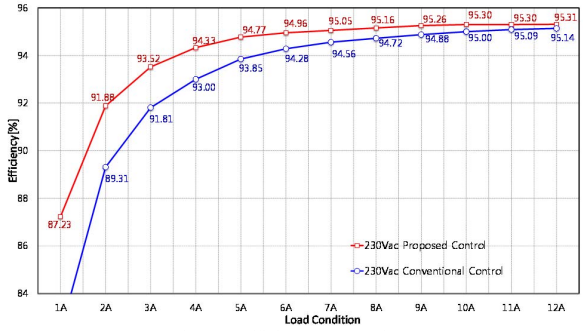


Fig. 25. Efficiency comparison

V. CONCULUSION

In this paper, a novel adaptive dead time control method for LLC synchronous rectification has been proposed to maximize SR conduction time and the system efficiency. In the proposed control method, instantaneous drain voltage information and previous cycle dead time information are used for SR dead time regulation and better transient characteristic. The compensation voltage and turn-off threshold voltage control algorithm for compensating the stray inductance of MOSFET package and PCB pattern is discussed in Section II with flow chart. Design considerations of the compensation voltage is explained with the virtual turn-off threshold voltage trajectory when the output load is changed. In addition, the requirement regarding light load SR operation is discussed in Section III. To verify the proposed adaptive dead time control method, 240W prototype was experimented with the proposed controller which is implemented with 0.35-μm BCDMOS technology. In the result, the proposed control method shows dead time regulation at around dead time target which provides maximum SR conduction time under heavy and light load conditions. In the transient characteristic, the proposed controller well follows load on and off condition without any problem. Finally, the proposed control method proved higher efficiency compared to that of the conventional control method. Therefore, the proposed control method can be a good candidate for high efficiency LLC synchronous rectification control method.

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