Accelerated Low Gate Count Parameter Identification for Integrated Switched-Mode Power Supplies with Digital Control

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***Abstract*—Parameter identification in digital switched-mode power supplies (SMPS) enables new features in terms of design, diagnostics, and autotuning. It is beneficial for plug and play solutions, which allow to choose practically any inductor or capacitor for the SMPS meeting the application, cost and quality requirements. Parameter identification enables indication of component failure cases and adaption to unwanted parameter variations due to production tolerances, aging, and temperature changes. This paper proposes an identification concept for inductance and capacitance, the most influential parameters in SMPS. It allows for autotuning during startup and operation. The SMPS parameters are identified with very short identification time (85 µs during startup / 2 µs during operation), low gate count (8778 gates), small output voltage perturbations (0.4 % of the nominal output voltage), and high identification accuracy (max. 5 % deviation for inductance / max. 13 % deviation for capacitance). Experimental results are shown for a variable input voltage (3-6 V), 6.3 V output voltage, 1 A digitally controlled boost converter with 500 kHz switching frequency.**

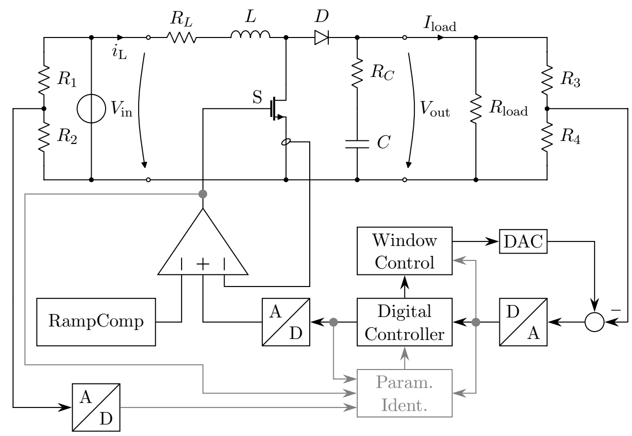

Fig. 1. Proposed mixed-signal peak current mode controlled boost converter with parameter identification.

I. Introduction

Digital control is well suited for various adaptive and sophisticated controls improving the transient behavior of SMPS [1]–[5]. Accurate knowledge of the SMPS parameters is required for proper functionality in these controls. Unfortunately, the SMPS parameters, such as the inductor and the output capacitor, are not well-known due to production tolerances and they vary over life-time due to temperature variations and aging. Besides, accurate identification of the SMPS parameters is necessary for plug and play solutions, which allow to choose any inductor and capacitor in order to meet the application, cost and quality requirements. Thus, many applications greatly benefit from an identification of the actual SMPS parameters.

Existing solutions propose identification by intentionally introducing oscillations, in particular, relay based identification [6], [7] and limit cycling based identification [8]. In [9], [10] the frequency response of the SMPS is evaluated. [4] proposes direct tuning of the control crossover frequency and phase margin. In those concepts, output voltage disturbances are applied continuously, interacting control loops are added, and complex sets of equations are solved at the expense of extensive hardware overhead. Further, open loop operation or duty cycle freeze are required and the desired crossover frequency needs to be specified a priori. In boost converters, although autotuning is offered, this requires a worst case approach, as the maximum crossover frequency is dependent on varying parameters, including the inductance. The identification times are long, during startup (>1 ms) and operation (>15 ms). In most applications, this is not reasonable, as the output voltage is permanently disturbed in operation. Also, startup time is limited, e.g. in automotive applications typically only 1 ms is available before regular operation (including soft-start output voltage ramp up, which already takes ∼0.5 ms).

This work presents a parameter identification concept for SMPS yielding results within less than 85 µs in startup and 2 µs in operation, which is 12x (startup) / 7000x (operation) shorter than prior art. The identification including an autotuning with eight predefined controller configurations is implemented with a relatively low overall digital hardware effort of 8778 NAND gate equivalents. It operates with a small output voltage perturbation of 0.4 % of the nominal value. In contrast to prior art, the presented concept enables autotuning in current mode controlled converters and avoids a priori worst case crossover frequency specification. The concept is well suited

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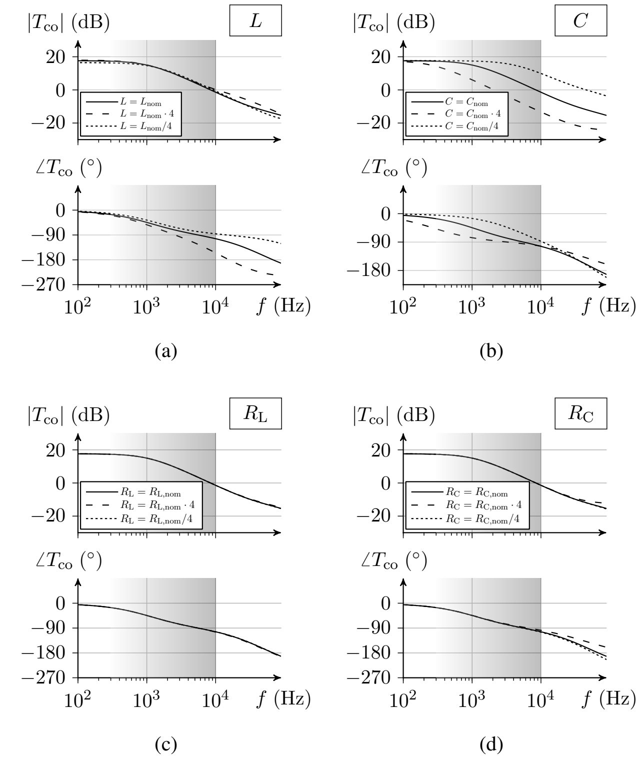

Fig. 2. Bode plots of a boost converter with variation of (a) the inductance L, (b) the capacitance C, (c) the inductor series resistance R_L, and (d) the capacitor series resistance R_C.

for plug and play solutions, and applications with limited startup time. As the values of capacitance and inductance are actually determined, they can be used for advanced control concepts [3], [5], whose control success strongly relies on these values.

Section II explains, why accurate inductance and capacitance identification is important in SMPS. The proposed identification concept is introduced in Section III. Experimental results are shown in Section IV. The proposed identification concept is compared to prior art in Section V.

II. Identification Strategy

The proposed identification concept is exemplary presented for a peak current mode controlled boost converter, Fig. 1. It can be applied to various other converter topologies.

Figure 2 demonstrates the influence of the variation of different parameters on the control-to-output transfer function T_{co} of a boost converter in comparison to nominal parameters. The most relevant part of the transfer function, the typical crossover frequency range, is shaded in gray. Inductance variations (a) may lead to negative phase shift in the crossover frequency range, which endangers control stability. Capacitance variations (b) influence the magnitude and consequently, move the crossover frequency, which impacts control stability and may slow down the control. In contrast, the transfer function is neither greatly affected from variations of (c) the inductor series resistance R_L nor of (d) the capacitor series resistance R_C.

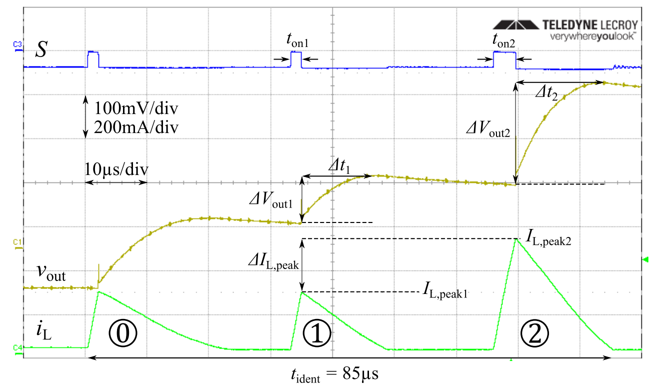

Fig. 3. Output voltage v_{out}, inductor current i_L, and switch control signal S during startup identification for $L = 22\,\mu H$, $C = 22\,\mu F$, and $V_{in} = 3.5\,V$.

In conclusion, Fig. 2 proves that apart from the operating parameters (V_{in}, I_{load}), the inductance and the capacitance dominate the transfer function in the frequency range of interest, while other SMPS parameters are of minor influence. Consequently, accurate inductance and capacitance identification is most important in SMPS for stable and fast control.

III. Proposed Identification Concept

The proposed concept is composed of an initial startup and an in-operation identification procedure.

A. Startup Identification

The switch control signal S, inductor current i_L, and output voltage V_{out} of the startup identification are shown in Fig. 3. The basic idea is to evaluate the inductor current ramp up while the switch is turned on:

$$L = V_L \cdot \frac{t_{on}}{I_{L,peak}} \tag{1}$$

Therefore, a peak inductor current $I_{L,peak}$ is set by the controller which leads to the ramp up. Inductor current measurement, digital-to-analog conversion, and comparator (see Fig. 1) may contribute to peak inductor current offset errors. In order to compensate for these offset errors the inductor current is ramped up twice (① and ②). Consequently, the calculation of the inductance L considers the difference of two peak inductor current values ($\Delta I_{L,peak} = I_{L,peak2} - I_{L,peak1}$), eliminating any offset errors:

$$L = V_L \cdot \frac{t_{on2} - t_{on1}}{\Delta I_{L,peak}} \tag{2}$$

The inductor voltage V_L is approximately equal to the input voltage V_{in}. But, the switch on-resistance $R_{DS,on}$ causes a voltage drop and therefore, influences the inductor current rising slope. Consequently, the inductor voltage behavior is described by a complex differential equation, which requires extensive hardware for solving. In order to yet obtain an accurate identification result, the switch on-resistance voltage drop is compensated by consideration of the average voltage drop:

$$V_{\mathrm{L}} = V_{\mathrm{in}} - R_{\mathrm{DS,on}} \cdot \frac{I_{\mathrm{L,peak2}} + I_{\mathrm{L,peak1}}}{2} \tag{3}$$

The inductor current starts from 0 A in the two identification ramp ups (①and ②) as the output voltage is easily increased through the first inductor current ramp up (⓪) due to the low load in startup. Thus, the diode D blocks once the inductor current has ramped down as the output voltage is higher than the input voltage of the converter. Consequently, the inductor current start value is equal and independent of the load for the subsequent identification ramp up.

When the switch is turned off, the inductor current is delivered to the output capacitor and the load. In good approximation, the inductor current is triangle shaped and its average value (minus I_{load}) supplies the capacitor:

$$I_{\mathrm{C}} = \frac{I_{\mathrm{L,peak}}}{2} - I_{\mathrm{load}} \tag{4}$$

The charging of the output capacitor leads to an increase of the output voltage ΔV_{out} until the inductor current equals the load current. This point in time can be determined with the standard output voltage measurement, as in this instant the output voltage stops increasing and starts decreasing.

$$\Delta V_{\mathrm{out}} = \frac{I_{\mathrm{C}}}{C} \cdot \Delta t = \frac{I_{\mathrm{L,peak}}/2 - I_{\mathrm{load}}}{C} \cdot \Delta t \tag{5}$$

By charging the output capacitor two subsequent times, (5) loses the load dependent term. Consequently, the need for an additional measurement of the load current is avoided. By changing (5) and considering the double charging, the capacitance identification formula becomes:

$$C = \frac{\Delta I_{\mathrm{L,peak}}}{2 \cdot (\frac{\Delta V_{\mathrm{out2}}}{\Delta t_2} - \frac{\Delta V_{\mathrm{out1}}}{\Delta t_1})} \tag{6}$$

The capacitor identification relies on a linear decrease of the inductor current. Any parasitic resistance in the inductor current path may cause a slight nonlinearity in this decrease. A more precise capacitance identification is achievable with increased output voltage. Thus, the resistive voltage drop becomes negligible compared to the inductor voltage drop and reduces the nonlinearity. Beside the reason mentioned above, that is why the first inductor current ramp-up (⓪) is applied in order to increase the output voltage for identification.

Window concept ADCs are proposed for the analog-to-digital conversion in SMPS with digital control. The output voltage varies over a wide voltage range when applying the parameter identification. As standard window concept ADCs convert the output voltage solely around the setpoint of the control, which is zero before operation, they are not suitable. Full-range ADCs get around this problem, but are expensive.

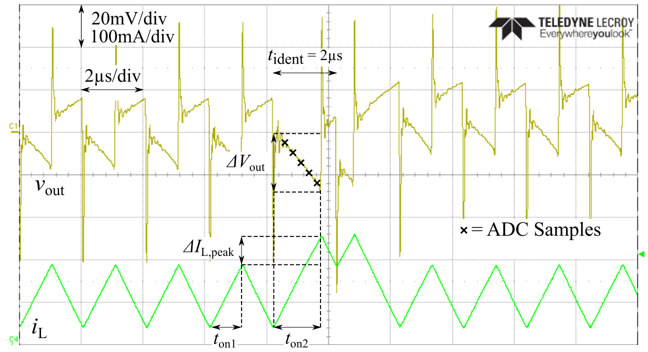

Fig. 4. Output voltage v_{out} and inductor current i_{L} for the in-operation identification with $L = 22\,\mu\mathrm{H}$, $C = 22\,\mu\mathrm{F}$, $V_{\mathrm{in}} = 3.5\,\mathrm{V}$, and $I_{\mathrm{load}} = 250\,\mathrm{mA}$.

TABLE I
BOOST CONVERTER PARAMETERS

Boost Converter Plant	
Input Voltage V_{in}	3-6 V
Output Voltage V_{out}	6.3 V
Load Current I_{load}	0-1 A
Range of Inductors L	3.3 µH - 41 µH
Range of Capacitors C	10 µF - 37 µF
Switching Frequency f_{sw}	500 kHz
Switch On-Resistance $R_{\mathrm{DS,on}}$	0.5 Ω
Compensation Ramp $V_{\mathrm{comp,pp}}$	0.2 V
Live-Tracking Window Analog-to-Digital Converter	
Output Voltage Resolution	7 mV (6 bit)
Sampling Rate	500 kSps / 4 MSps
Digital-to-Analog Converter	
Output Voltage Resolution	5 mV (10 bit)
Conversion Rate	500 kHz
Input-Voltage ΔΣ Analog-to-Digital Converter	
Input Voltage Resolution	5 mV (12 bit)
Sampling Rate	100 kSps

Therefore, the use of a live-tracking window ADC is recommended, which tracks the output voltage over a wide operation range maintaining window concept operation [11].

B. *In-Operation Identification*

The inductance is identified by manipulating the controller output with a known offset $\Delta I_{\mathrm{L,peak}}$ from one to the next switching period, Fig. 4. Consequently, the inductor current increases to a new peak current, accompanied by a duty cycle increase. If a ramp compensation preventing subharmonic oscillations is used, its impact on the peak inductor current has to be considered. The on-time difference helps determining the inductance value:

$$L = V_{\mathrm{L}} \cdot \frac{t_{\mathrm{on2}} - t_{\mathrm{on1}}}{\Delta I_{\mathrm{L,peak}}} \tag{7}$$

The inductor voltage V_{L} equals the input voltage V_{in} with compensation of the switch on-resistance voltage drop. Thus, it is chosen according to (3).

TABLE II
COMPARISON OF IDENTIFICATION METHODS

	[4]	[6]	[9]	[10]	**This Work**
Identification Method	In-Operation	Startup	Startup & In-Operation	In-Operation	**Startup & In-Operation**
Identification Time	20 ms*	1 ms	120 ms*	15 ms	**85 µs / 2 µs**
Dig. HW (#NANDs)	12.3 k	18 k	28.1 k**	12.8 k***	**8.8 k**
V_{out} Perturbation	±0.4 %	n/a	±3 %	±0.3 %	**±0.4 %**
Identification Error	$\Delta f_c/f_c$=0.6 % $\Delta\varphi_R/\varphi_R$=2.5 %	$\Delta f_c/f_c$=3.7 % $\Delta\varphi_R/\varphi_R$=22 %	n.r.	$\Delta f_c/f_c$=12.5 % $\Delta\varphi_R/\varphi_R$=14.5 %	**$\Delta L/L$=5 % $\Delta C/C$=13 %**

*Continuous identification, estimated from figure. **Additional: 10 k memory ***Additional: 2x32-bit multipliers.

When the switch in a boost converter is turned on, the load current is provided from the output capacitor. The output voltage decreases linearly as shown in Fig. 4 and the capacitance can be calculated according to:

$$C = \frac{I_{\mathrm{load}}}{dV_{\mathrm{out}}/dt} \quad (8)$$

The load current of current mode controlled converters can be determined from the controller output [12]. For identification, multiple output voltage samples are recorded to determine the output voltage-time derivative, Fig. 4. This determination might be inaccurate due to the limited ADC resolution. In this case, a linear regression algorithm helps improving the accuracy. Any high-frequency output voltage disturbances are eliminated by the low-pass filter characteristics of the input stage of the ADC.

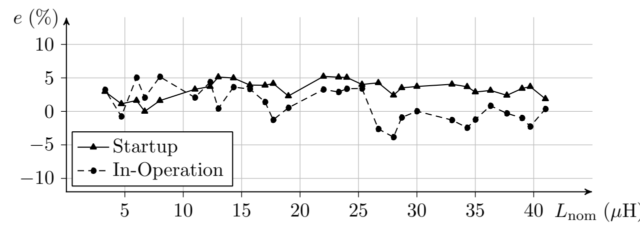

Fig. 5. Relative identification error for different inductors.

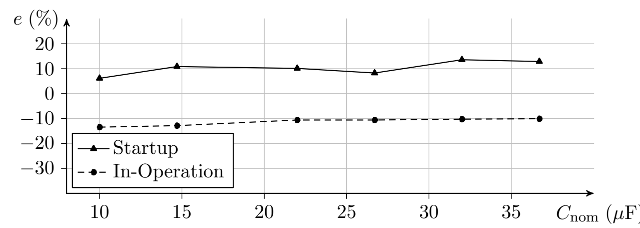

Fig. 6. Relative identification error for different capacitors.

IV. EXPERIMENTAL VERIFICATION

The identification concept is applied to a boost converter, which is shown in Fig. 1. Its operating parameters are summarized in Table I. The integrated control loop is composed of a live-tracking window-concept ADC (standard operation: 500 kSps, identification: 4 MSps), an input voltage $\Delta\Sigma$ ADC, and an integrated DAC for current mode control. ADCs, DAC, current sensing, PWM generation including compensation ramp, gate driver and low-side switch are available as an ASIC, fabricated in a 180 nm BCD technology. The digital part is implemented in a Xilinx Spartan-6 FPGA.

Figure 3 shows the measurement of the output voltage V_{out}, the inductor current i_{L}, and the switch control signal S for $L = 22\,\mu\mathrm{H}$ and $C = 22\,\mu\mathrm{F}$ when applying the startup identification scheme. For the in-operation identification, the measurement of the output voltage V_{out} and the inductor current i_{L} are shown exemplary for the same inductor and capacitor in Fig. 4.

The identification concept was further tested with multiple capacitors and inductors, which were inserted in the boost converter. Their capacitance and inductance was measured in impedance analyzer reference measurements with $f_{\mathrm{stimulus}} = 10\,\mathrm{kHz}$, $I_{\mathrm{bias}} = 0\,\mathrm{A}$ for the inductor, and $V_{\mathrm{bias}} = 6.3\,\mathrm{V}$ for the capacitor, respectively. The relative identification errors for the inductor and capacitor identification are shown in Figures 5 and 6, respectively. The maximum identification error is 5 % for the inductance and 13 % for the capacitance.

The identification error of the capacitance in startup mainly results from the voltage dependency of the used MLCC capacitors. The higher the operating voltage is, the smaller is their capacitance. In the reference measurement, the capacitance was measured at 6.3 V, which is the nominal output voltage of the boost converter. The identification voltage is well below (depending on the input voltage). Consequently, a compensation of the voltage dependency of the used capacitor according to its data sheet enables a more accurate identification. Also, the capacitor is dependent on the operating frequency. With higher operating frequency, the capacitance becomes smaller. During operation, the identification scheme is applied at high frequency. The capacitance reference measurement was conducted at the control crossover frequency, which is lower. As a result, the identified capacitance is lower as its reference value. Thus, the in-operation identification accuracy can be improved by considering the capacitors frequency characteristics.

V. COMPARISON

Table II compares the proposed identification concept to state-of-the-art parameter identification concepts. This work achieves similar or even better hardware count, output voltage perturbation, and maximum identification error. The main improvement of the presented concept is the short identification time. It yields results within less than 85 µs in startup and 2 µs in operation, respectively. Typical identification times in the other concepts are in the range of 1 ms up to 120 ms. Thus, the presented concept enables use in applications with only limited identification time. Unlike [4], [6], [10], this work combines a startup and in-operation parameter identification. As an additional advantage, it does not need an open loop configuration or duty cycle freeze. The identification allows for autotuning in current mode controlled converters, which was not published before.

VI. CONCLUSION

A startup and in-operation parameter identification concept without continuous disturbance of the output voltage is presented. It enables autotuning and health monitoring, which are of particular interest in SMPS for optimum performance and prevention of control instability. The concept for identification of the inductance and the capacitance is exemplary applied to a variable input voltage (3-6 V), 6.3 V output voltage boost converter. Compared to prior art, the identification time of the presented concept is 12x shorter during startup and 7000x shorter in operation. Consequently, it allows for use in applications with limited startup time, and the most influential parameters can be identified with lower hardware effort, enabling cost savings. The proposed identification concept ensures proper regulation in advanced controls and supports an advanced plug and play approach for passive L and C components in SMPS.

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