A Wide Input and Output Voltage Range Battery Charger Using Buck-Boost Power Factor Correction Converter

A.V.J.S.Praneeth, *Student Member, IEEE* and Sheldon S Williamson, *Senior Member, IEEE*
Advanced Storage Systems and Electric Transportation (ASSET) Laboratory
Smart Transportation Electrification and Energy Research (STEER) Group
UOIT-Automotive Center of Excellence (UOIT-ACE)
Department of Electrical, Computer, and Software Engineering
University of Ontario Institute of Technology,Canada
E-mail ID: Jaya.Av@uoit.net, Sheldon.Williamson@uoit.ca

***Abstract*—In both battery operated electric vehicles (EVs) and plug-in-hybrid electric vehicles (PHEVs), a two-stage converter connects the input grid voltage to the battery pack whose voltage varies from 100-500 V, depending on the vehicle size and range. A universal charger, which can address this wide range of battery pack voltages, is suitable for all vehicle architectures. This requirement is achieved by varying the AC/DC converter output voltage using the concept of variable dc link voltage, which is one of the challenges in battery chargers for attaining universal output voltages. This paper mainly focuses on analysis and operating modes for a interleaved boost cascaded-by buck(IBCBB) converter suitable for a power factor correction (PFC) converter. The designed control structure provides a wide degree of control freedom to operate even if the V_{DC}/V_{max} (output voltage to peak of Input) less than 0.5. The design considerations for selection of components is also addressed in the paper. Moreover, the proposed converter is validated on the experimental setup and the results are presented in the paper. In addition, a two-stage universal battery charger with wide input and output voltage is been simulated and presented in the paper.**

***Index Terms*—AC-DC power converters, battery chargers, energy storage, power electronics, transportation**

I. Introduction

On-board chargers for electric and hybrid electric vehicles is an indication of the new era in field of power electronics for the automotive industry. Lack of fast charging infrastructure deploys the automotive manufactures with on-board battery chargers, which are feasible of charging from household power sockets. A considerable range of literature is available on the topologies, power levels and stages of the chargers for electric and hybrid electric vehicles [1]-– [3]. Fig.1 shows the typical layout of the battery chargers with a feature of isolation accepting the wide input voltages. A front-end active power factor correction (PFC) converter is required at the input to maintain high power quality. In most PFC applications, a boost converter with or without interleaved topology is preferred in order to provide a dc output voltage that is greater than its peak ac line voltage [4]. At low line AC voltages, drawbacks such as more stress on switches, a bulky inductor and a huge input

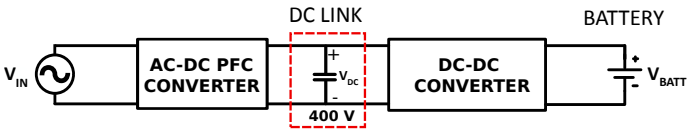


Fig. 1: Two-stage layout of battery chargers

current ripple will appear in the boost converter. Researchers in [5]– [8] investigated the various PFC topologies to mitigate the problems. However, it showed up some improvements in the efficiency but the structure of the boost PFC category remains the same. The output of PFC converter when connected to a high frequency DC-DC converter provide the output voltage to various batteries with a minimum voltage of 200 V. There are few electric vehicles having the DC battery operating voltage less than or equal to 150 V (48 V system, 72 V,96 V,144 V). In such a low output voltage conditions, the battery charger manufactures are employed with a high frequency step-down transformer in the DC-DC converters, which restricts the output voltage range limits, weight of the transformers and efficiency with limited ZVS [9]– [12].

The voltage fed DC-DC converter is inherently a buck converter whose output voltage is less than the input. The desired maximum voltage is attained by varying the high frequency transformer. One of the attractive solution to attain universal charger without influencing much on the magnetics of high frequency transformers is the step up or step down of the PFC output voltage. For a universal charger to operate at worldwide voltage range, conventional converters such as buck-boost, SEPIC and CUK converter can fulfill the requirements but have the disadvantage of stress and bulky size [13]-– [14]. To have a low stress level in the device, a combination of buck and boost with two switches is proposed in [15]– [17]. The benefits of two switch converters is the ability to have a direct energy transfer path between the source and load to minimize the effect of using passive components.

This paper proposes a two-switch configuration based interleaved boost cascaded-by buck PFC converter. The detailed design analysis and operation of a proposed converter in dif-

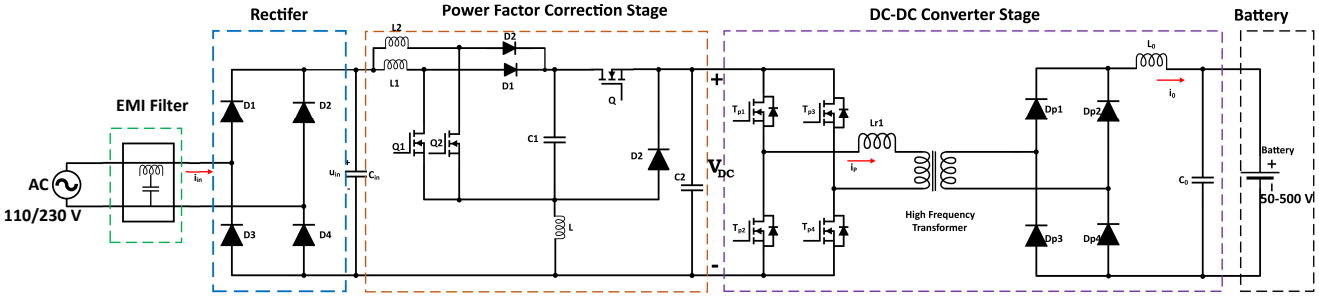


Fig. 2: Proposed Interleaved boost cascaded-by buck PFC converter based on-board battery charger

ferent modes are discussed in the paper. The proposed control structure with voltage and current control loops maintains the universal output voltages and high input power quality. The parameters of the converter are derived and the proof-of concept hardware set-up with results are presented in this paper. Finally, the proposed variable DC link PFC voltage is simulated with a Phased shifted DC-DC converter to have a universal chargers with wide output voltage range.

II. Analysis and Operation of the Proposed PFC Converter

The above circuit shown in Fig.2 is schematic of two-stage on-board battery charger. It consists of an power factor correction converter in two-switch topology configuration and an isolated DC-DC converter. The proposed PFC converter consists of a cascaded combination of the interleaved boost with a buck converter. The inductors L_1,L_2 at the input provides a non-pulsating current which can be easily controlled to maintain the power quality. Interleaved combination at input also provides the reduced ripple content in the input current. The converter is operated in the continuous conduction mode (CCM) with a boost configuration formed with the switches Q_1, Q_2 and diode D_1 D_2. An LC filter is paired either at the input or the output side of the converter based on operating mode which provides non-pulsating currents to source and load. The converter controls the buck switch Q and diode D based on the input and output voltages. The output voltage of the converter is represented as V_{DC} which can be controlled to a value either above or below of the peak value of input voltage V_{max}. Fig.3 shows the rectified universal input voltage applied to converter whose output voltage (V_{DC}) selected is greater than the peak of input voltage V_{max} enabling the boost operation with controlling switches Q_1 and Q_2 with a duty ratio of d_1 and d_2 turning the buck switch Q on continuously. If the output voltage at the converter is selected lesser than the peak of the input voltage V_{max} the converter operates in both boost and buck modes. In interval [0,t_1] the converter operates in boost mode controlling Q_1 and Q_2 as shown in switching states and from [t_1, $\frac{T_s}{4}$] in buck mode of operation with duty ratio of d_{Bu} and it repeats for next quarter cycle. The switching pattern of the converter during buck and boot modes of operation is showed in Fig.3. The overall gain of the converter is given as

$$M = \frac{d_{Bu}}{1 - d_{Bo}} \tag{1}$$

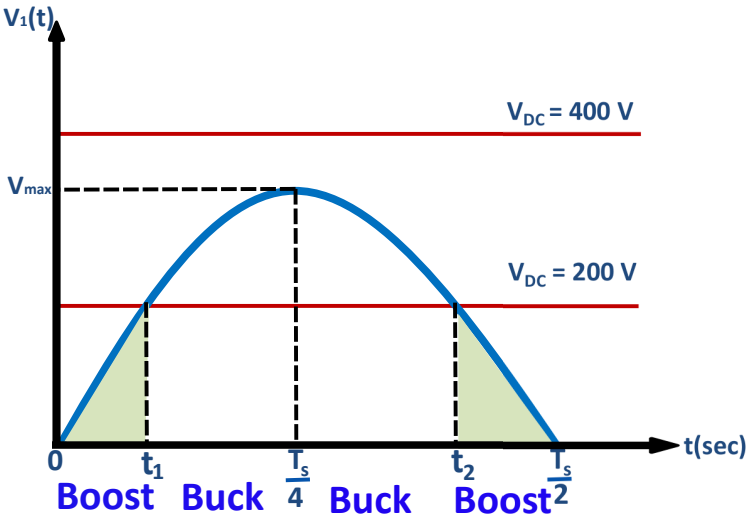
The duty ratio for the boost mode of operation is defined as d_{Bo} with the duty ratio of the boost switches d_1 and d_2 are maintained 180^0 phase shift between them. The phase shift in the PWM signals generates the ripple current in the inductor in phase opposition which cancels the ripple when they are added up resulting in the reduction of ripple current at the PFC output. In the boost mode of operation the duty ratio of the buck switch is made high $d_{Bu} = 1$, (turned on continuously) and the inductor at input and output provides a continuous current. The overall gain of the converter in boost mode of operation with the duty ratio d_{Bo} is given as $M_1 = \frac{1}{1-d_{Bo}}$. The detailed operating modes of the converter in boost mode is as shown in Fig.4. In mode-(a) the inductors share input current equally and the output capacitor supplies to load. A part of the input current flows to the load through the capacitor C_1 providing a direct path from source to load. In mode-(b) and (c) one of the boost switch is turned off which provides a path for the input current to charge the inductor as well as to supply to load. In mode-(d) the switches are turned off and the input current flows directly to output. Similarly, in the buck mode of operation the converter is operated with a duty ratio of d_2 and the boost switch is turned off making the duty ratio $d_{Bo} = 0$. The overall gain of the converter is given as $M_2 = d_{Bu}$. The cascaded combination of the boost mode and the buck mode implies the product of the gains of converter. The overall gain of converter is given as:

$$M = M_1 \times M_2 = \frac{d_{Bu}}{1 - d_{Bo}} \tag{2}$$

For analysis as shown in Fig.4 the forward voltage drop of the diodes is neglected and the rectified voltage is assumed to be same as the input voltage which is given as

$$V_1(t) = V_{max}|sin\omega t| \tag{3}$$

where V_{max} is the maximum value of rectified input voltage and is given as $V_{max} = \sqrt{2}V_{ac,rms}$.For a ideal PFC rectifier (neglecting losses) the power at input and output is assumed to be constant. For a particular value of the output voltage V_{DC}



Switching States

Q_1	Q_2	Q	Operation
0	1	1	Boost
1	1	1	
0	0	1	
0	1	1	
0	0	0	Buck
0	0	1	

Fig. 3: Rectified input voltage waveform with different possible operating modes and switching states

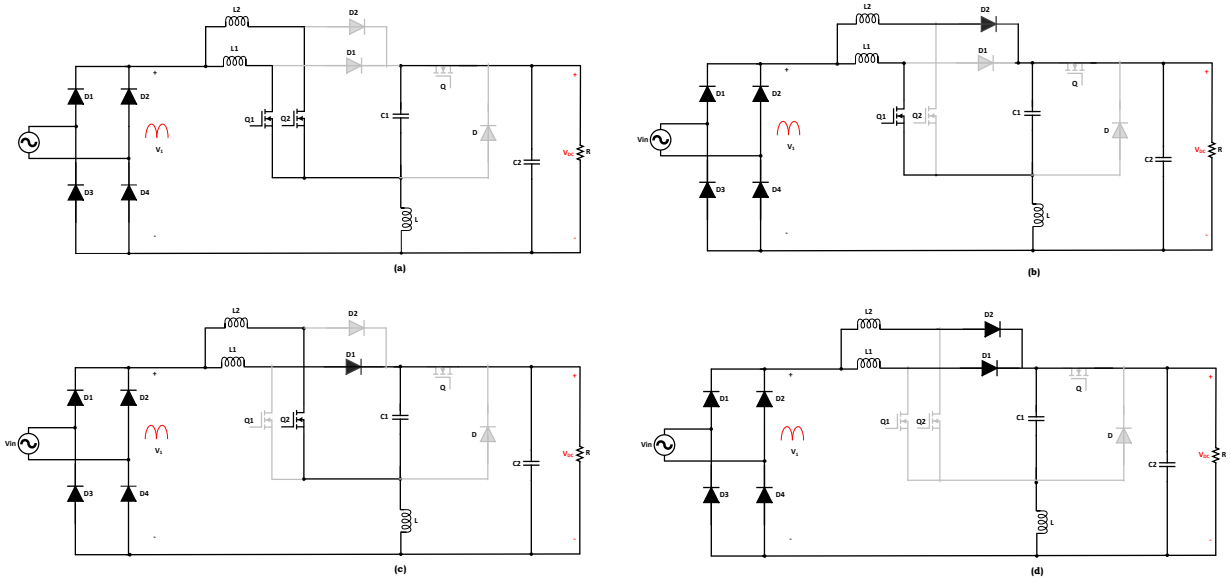


Fig. 4: Operation of the proposed converter in boost mode

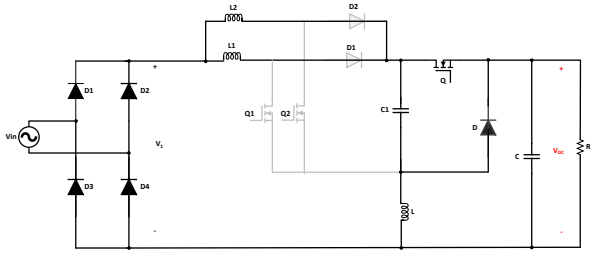


Fig. 5: Operation of the proposed converter in buck mode

the input current i_{in}(t) is proportional to the input voltage $V_1(t)$.

$$\begin{cases} i_{in}(t) = \dfrac{\sqrt{2}V_{ac,rms}}{R_{em}}|sin\omega t| \\ i_{in}(t) = \dfrac{V_1(t)}{R_{em}} \end{cases} \quad (4)$$

where R_{em} is the emulated resistance related to active power P_0 demanded by load. The expression for the input current is given as :

$$I_{in}(t) = \frac{\sqrt{2}P_0}{V_{ac,rms}} sin(\omega t) \quad (5)$$

$$I_{in}(t) = \frac{4P_0}{\pi V_0(1-d_{Bo})} sin(\omega t) \quad (6)$$

A. Design Parameters of PFC converter

The selection of the inductors is assumed under the condition of continuous conduction mode with less effects on current ripple. Let I_1 is the average input current flowing through the inductor L_1 with an peak inductor ripple of ΔI_1 and I_2 is the average input current flowing through the inductor L_2 with an peak inductor ripple of ΔI_2 .

$$I_{in} = I_{L1} + I_{L2} > \Delta I_{L1} + \Delta I_{L2} \quad (7)$$

TABLE I: Parameters of the Proposed Converter

Item	Buck Mode	Boost Mode
Input Voltage V_{in}(rms)	85-265 V	85-265 V
Output PFC Voltage V_{dc}	150, 250 V	400 V
Power Rating	1 kW	1 kW
PFC Switching Frequency f_s	30 kHz	30 kHz
Boost Inductor L_1	3 mH	3 mH
Boost Inductor L_2	3 mH	3 mH
Inductor L	2.52 mH	2.52 mH
Leakage Inductor L_{r1}	2 μH	2 μH
Output Capacitor C_0	10 μF	10 μF
Output filter Inductor L_0	320 μH	320 μH
Capacitor C_1	8 μF	8 μF
PFC CapacitorC_2	950 μF	950 μF
Duty Cycle D	0.266	0.7175
Output Load Resistance R	62.5 Ω	160 Ω

The input current and the peak inductor current ripple is defined as :

$$I_{in} = \frac{V_1}{R_e} > \frac{V_1 \times d_1 T_s}{2L_{in}} \quad (8)$$
$$where L_{in} = L_1 = L_2$$

where R_e is the input resistance of the power converter which can be determined for a given output power.

$$L_{in} > \frac{T_s \times R_e}{2}(1 - \frac{V_{max} sin(\omega t)}{V_{DC}}) \quad (9)$$

similarly in the buck mode the inductance L_2 can be determined from the below equations. For the selection of the capacitance C_1 so that input variations will not effect much on the output voltage voltage. The converter forms a low pass LC filter at input during mode whose frequency is more than the input line frequency.

$$L_p > \frac{(V_{max} sin(\omega t) - V_{DC}) \times V_{DC}^2 \times R_e T_s}{2 \times (V_{max} sin(\omega t))^3} \quad (10)$$

$$L_p = \frac{L_{in} L}{L + L_{in}} \quad (11)$$

The value of inductance L_2 can be determined using the equations (10) and (11). For a given power rating the parameters used in the converter are detailed in Table.I. For the phase shifted ZVS DC-DC converter the standard design guidelines are followed and the parameters derived are shown in Table-I. To have a proper ZVS for the different loads the condition shown in (12) must be satisfied.

$$\frac{1}{2} L_{lk} I_{cri}^2 > \frac{4}{3} C_{mos} V_1^2 + \frac{1}{2} C_{Tr} V_1^2 \quad (12)$$

Here C_{mos} is refered as the drainto source capacitance of the switch and C_{Tr} is the transformer winding capacitance.

III. Experimental Setup and Results

The simulations of the proposed Interleaved boost cascaded-by buck PFC converter were performed in PSIM 11.0.3 with the power ratings of 1 kW. Fig.6 shows the simulation result of the proposed converter configuration with an input voltage of

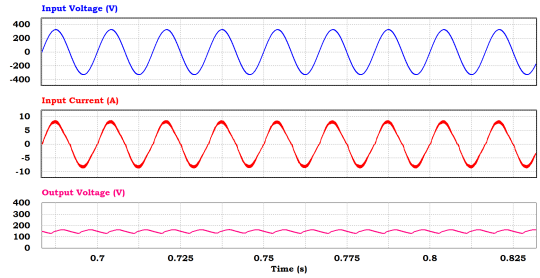


Fig. 6: Simulation results of converter with 150 V output voltage

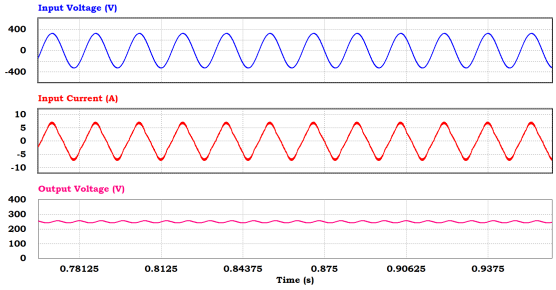


Fig. 7: Simulation results of converter with 250 V output voltage

230 V. The output of converter is at 150 V which is less than the peak of the input voltage and the captured input current is in-phase with input voltage which maintains high power quality. Similarly, Fig.7 shows the simulation result of the proposed converter configuration with an output voltage of 250 V which reaches almost near to the peak of input voltage. The role for operation of the buck converter reduces near the peak voltages giving more operation time for the boost mode. Fig.8 shows the simulation results of converter with output voltage of 400, which is greater than peak of input voltage. The input current observed from the above waveforms Fig.6 to 8 shows the smooth operation providing a high power factor. The control structure proposed for this smooth variation in the DC link voltage is implemented as shown in Fig.9 with a separate set of PI controllers for both the boost and buck modes of operation. As a proof of concept, the experimental set up of the proposed converter is scale down and implemented on a 300 W set-up. Fig.10 shows the experimental setup of the proposed converter and the control algorithm implementation using Launchpad TMS320F28069M. Silicon labs Si-8284 isolated gate drivers

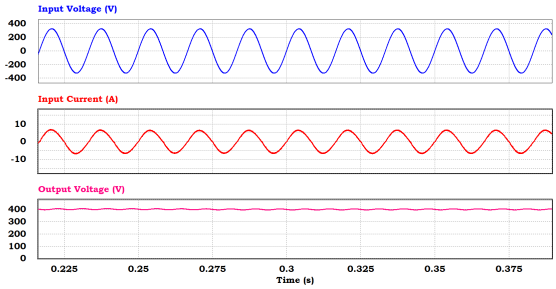


Fig. 8: Simulation results of converter with 400 V output voltage

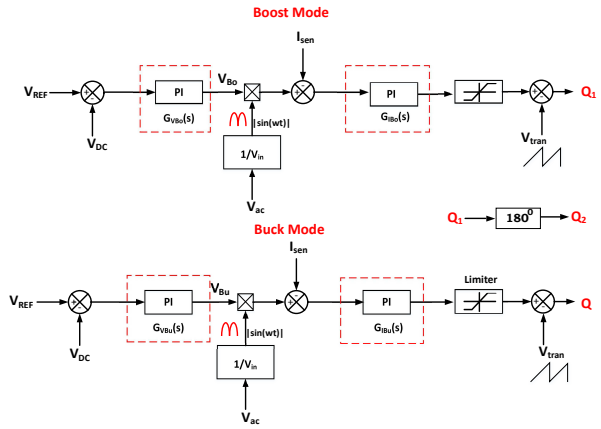


Fig. 9: Implemented control structure for proposed converter

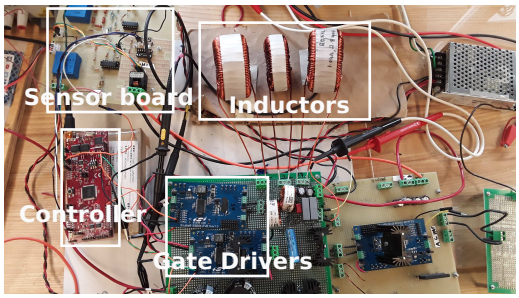


Fig. 10: Experimental setup of the proposed IBCBB PFC converter

with the maximum voltage of 300V are used for Infineon MOSFET switches IXFHG0N50P3 with LV-20P LEM voltage sensors. The gate drivers has with inbuilt protection circuits which can turn-off the gate pulses in abnormal conditions.

A regenerative grid simulator NHR300 is used as a programmable AC source to power up the converter. The components are selected for 1 kW but as a proof-of concept a low voltage is applied to the converter and results are presented in the paper. The Fig.11 shows the boost operation of the proposed converter and Fig.12 shows the buck-boost operation of converter. The closed loop operation is implemented in the TI-Launchpad using fixed point representation. The output voltage observed is above the peak of the input voltage and the current is in-phase relation with the voltage with an observed

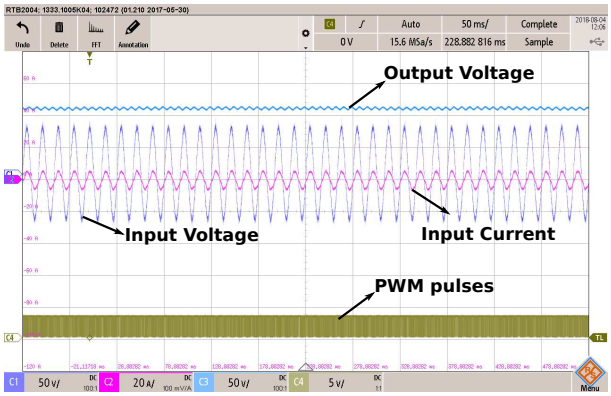


Fig. 11: Experimental results of PFC converter in boost mode

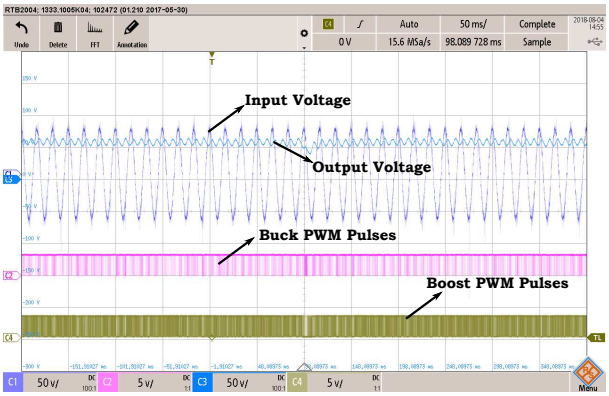


Fig. 12: Experimental results of PFC converter in buck-boost mode

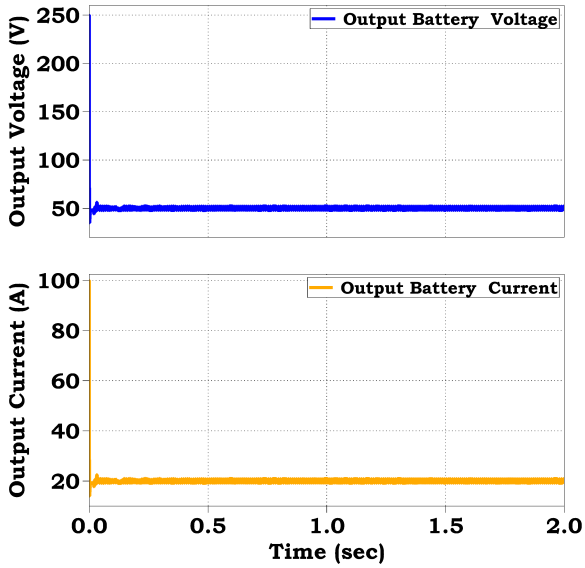


Fig. 13: Output voltage and current of charger at 50 V

power factor of 0.99. To Prove the concept of universal battery charger the above variable DC link voltage is applied to a Phase shifted DC-DC converter. The over all schematic of the above circuit shown in Fig.2 is simulated in PSIM and the results are presented in the paper. The parameters used to create the ZVS are calculated and indicated in the Table.I. For the switch capacitance we have considered the SiC MOSFET C3M0065090D with 900V and 36 A. The output inductor is designed to withstand the maximum current of 20A at lower voltage of 50 V. The maximum voltage seen by the charger is around 500 v to which the selection of the components are made to withstand 1.8 times the operating voltage (rate of chances for voltage spikes).Fig.13 to Fig.15 shows the results of the DC output voltage including the DC-DC converter. A voltage ripple of around 2% and current ripple of around 1.5% is been observed. This paper achieves a wide range of output battery voltages.

IV. Conclusion

This paper proposes a new interleaved boost cascaded-by-buck PFC converter for on-board battery chargers. The

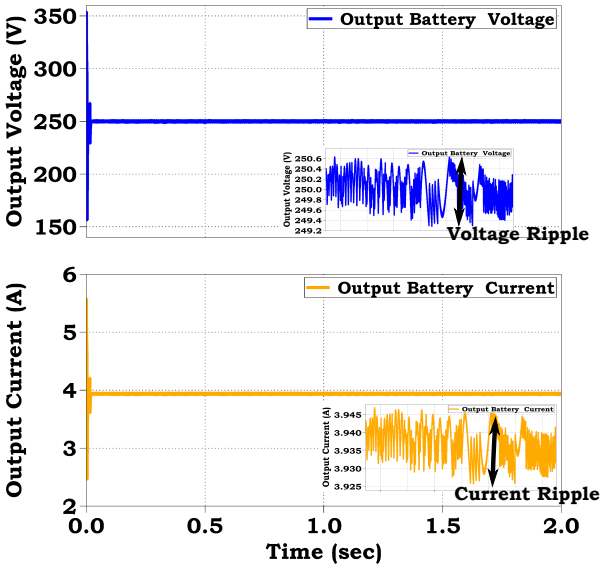


Fig. 14: Output voltage and current of charger at 250 V

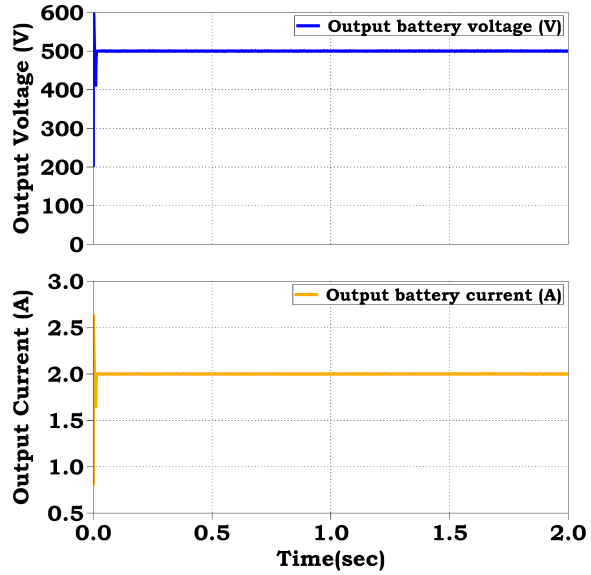


Fig. 15: Output voltage and current of charger at 500 V

proposed PFC converters operates with wide output voltages for universal input voltages. The various modes of operation of the converter are detailed in the paper. Moreover, the converter is operated above and below the peak of the input voltage to provide a wide DC link voltage with smooth input current. The design considerations and the control loop to achieve the wide output voltages is also discussed in the paper. The prototype build of the proposed converter achieves high input power factor of 0.99 and able to operate with both buck and boost modes of operation. The proposed PFC converter is cascaded to a phase shifted DC-DC converter to form a two-stage layout of the battery charger which is simulated and the results are presented to validate the concept of achieving wide output battery voltages with reduced voltage and current ripple.

ACKNOWLEDGMENT

The authors would like to thank Natural Sciences and Engineering Research Council (NSERC), Canada Research Chairs (CRC) Program for funding this project.

REFERENCES

[1] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[2] A. V. J. S. Praneeth and S. S. Williamson, "A review of front end ac-dc topologies in universal battery charger for electric transportation," in *2018 IEEE Transportation Electrification Conference and Expo (ITEC)*, June 2018, pp. 293–298.

[3] S. S. Williamson, A. K. Rathore, and F. Musavi, "Industrial electronics for electric transportation: Current state-of-the-art and future challenges," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 3021–3032, May 2015.

[4] R. W. Erickson and D. Maksimovic´, *Fundamentals of Power Electronics, 2nd ed.*

[5] T. Nussbaumer, K. Raggl, and J. W. Kolar, "Design guidelines for interleaved single-phase boost pfc circuits," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 7, pp. 2559–2573, July 2009.

[6] M. Pahlevaninezhad, P. Das, J. Drobnik, P. K. Jain, and A. Bakhshai, "A zvs interleaved boost ac/dc converter used in plug-in electric vehicles," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3513–3529, Aug 2012.

[7] U. Anwar, R. Erickson, D. Maksimović, and K. K. Afridi, "A control architecture for low current distortion in bridgeless boost power factor correction rectifiers," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2017, pp. 82–87.

[8] F. Musavi, W. Eberle, and W. G. Dunford, "A phase-shifted gating technique with simplified current sensing for the semi-bridgeless ac–dc converter," *IEEE Transactions on Vehicular Technology*, vol. 62, no. 4, pp. 1568–1576, May 2013.

[9] D. S. Gautam, F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "An automotive onboard 3.3-kw battery charger for phev application," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 8, pp. 3466–3474, Oct 2012.

[10] T. Kim, S. Lee, and W. Choi, "Design and control of the phase shift full bridge converter for the on-board battery charger of the electric forklift," in *8th International Conference on Power Electronics - ECCE Asia*, May 2011, pp. 2709–2716.

[11] F. Musavi, M. Edington, W. Eberle, and W. Dunford, "A cost effective high-performance smart battery charger for off-road and neighborhood evs," in *2012 IEEE Transportation Electrification Conference and Expo (ITEC)*, June 2012, pp. 1–6.

[12] H. Wang, S. Dusmez, and A. Khaligh, "Design and analysis of a full-bridge llc-based pev charger optimized for wide battery voltage range," *IEEE Transactions on Vehicular Technology*, vol. 63, no. 4, pp. 1603–1613, May 2014.

[13] R. Zane and D. Maksimovic, "Nonlinear-carrier control for high-power-factor rectifiers based on up-down switching converters," *IEEE Transactions on Power Electronics*, vol. 13, no. 2, pp. 213–221, Mar 1998.

[14] A. M. A. Gabri, A. A. Fardoun, and E. H. Ismail, "Bridgeless pfc-modified sepic rectifier with extended gain for universal input voltage applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4272–4282, Aug 2015.

[15] J. Chen, D. Maksimovic, and R. Erickson, "Buck-boost pwm converters having two independently controlled switches," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230)*, vol. 2, 2001, pp. 736–741 vol.2.

[16] J. Chen, D. Maksimovic, and R. W. Erickson, "Analysis and design of a low-stress buck-boost converter in universal-input pfc applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 320–329, March 2006.

[17] M. O. Badawy, Y. Sozer, and J. A. D. Abreu-Garcia, "A novel control for a cascaded buck–boost pfc converter operating in discontinuous capacitor voltage mode," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 7, pp. 4198–4210, July 2016.