

A High Frequency Power and Area Efficient Charge-Pump-Constant-On-Time Controlled DC-DC Converter Based on Dynamic-Biased Comparator with 50mV Droop and 2 μ s 1% Settling Time for 1.15A/1ns Load Step

Shih-Chieh Hsu
Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan
r06921022@ntu.edu.tw

Ching-Jan Chen
Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan
chenjim@ntu.edu.tw

Chieh-Ju Tsai
Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan
f04943123@ntu.edu.tw

Abstract—This paper presents a novel constant-on-time controlled buck converter IC with charge-pump-synthesized-ripple for compensation. The proposed technique replaces the external ramp generator by a simple charge-pump circuit to alleviate the sub-harmonic instability problem of ripple-based constant-on-time (RBCOT) control. Moreover, it can effectively minimize the size of on-chip resistor and capacitor compared with VIC-based COT. Without using any wide bandwidth analog processing circuitry, this new control scheme achieves small cost of power and area simultaneously under high switching frequency operation. The conventional on-time generator operating at high switching frequency needs a high speed comparator which consumes huge current. To solve this issue, a quadratic bias current reusing on time ramp information is adopted in the modified dynamic-biased comparator. Thus, the average current consumption of comparator is reduced by 58% compared with the traditional constant-biased method in CCM. The circuit is implemented in a 0.18 μ m CMOS process with near 10MHz high switching frequency. For the 1.15A/1ns load step, the simulation result shows near time-optimal transient response with only 50mV droop and 2 μ s 1% settling time.

Keywords—ripple-based constant on-time control IC, charge-pump constant on-time control, dynamic biased comparator

I. INTRODUCTION

Recently, constant-on time (COT) control has been widely used in power management IC to achieve fast transient response, high light-load efficiency, and less component simultaneously [1]-[5]. Fig. 1 shows that the instability and noise-margin issues caused by the small equivalent series resistor (ESR) of output capacitor can be suppressed by injecting a pseudo-ramp for modulation. As shown in Fig. 2, [2]-[5] demonstrate a common circuit implementation based on virtual-inductor-current (VIC) ripple by filtering the phase voltage V_{PHASE} . Nevertheless, the on-chip resistors and capacitors of VIC circuit which occupy large area are hard to be designed.

In recent years, the high switching frequency operation is preferred to shrink inductor and output capacitor size on printed-circuit-board (PCB) and improve the load transient response.

However, the VIC-based COT is not suitable for high speed design due to the use of adder. A novel charge-pump constant-on-time (CPCOT) controlled buck converter is then presented to solve this problem. Without using large RC and wide-bandwidth adder, the external ramp mixing up with reference voltage is directly generated by a charge-pump circuit [6]. Therefore, CPCOT control is more area and power efficient at high speed operation.

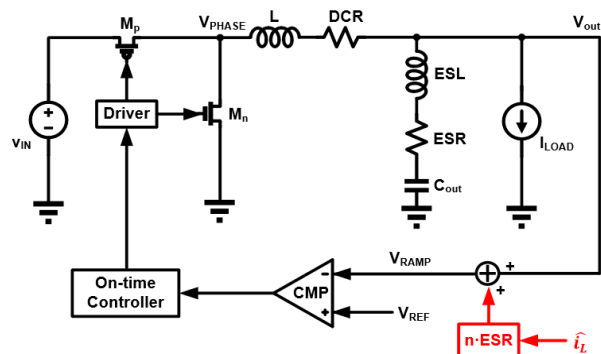


Fig. 1. RBCOT control with pseudo-ramp injection

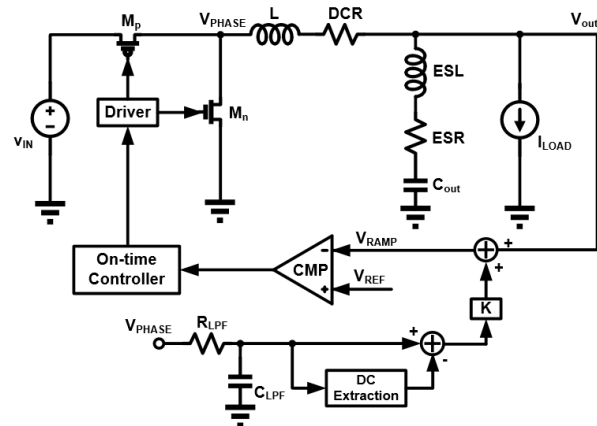


Fig. 2. Circuit diagram of VIC-based COT

II. ISSUES OF VIC-BASED COT AND ILLUSTRATIONS OF PROPOSED CPCOT

To meet the stability criterion of VIC-based COT control [2], the time-constant of low-pass filter should be designed as small as possible to generate adequate VIC ripple. Fig. 3 illustrates the VIC ripple component with different RC time-constant. It is obviously seen that with small RC time-constant, the exponential settling limits VIC ripple component and induces unwanted non-linear modulation. In contrast, using large RC introduces a perfect triangular ripple, but it requires an additional amplifier to enlarge the VIC ripple. Therefore, the VIC-based COT control costs more area and power.

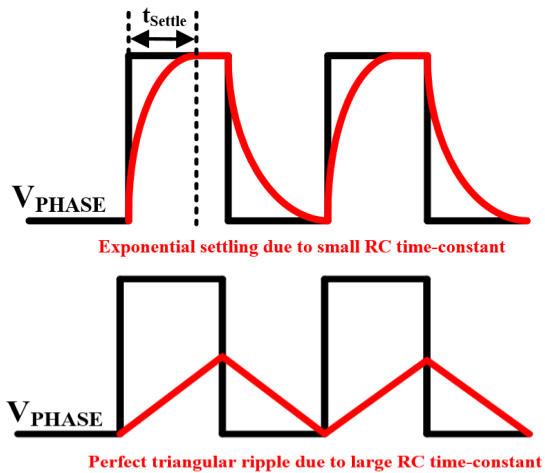


Fig. 3. Waveforms of VIC ripple under different RC time-constant

Fig. 4 demonstrates the intuitive circuit diagram of the proposed CPCOT. The external ramp is generated by a charge-pump circuit. The charge-pump circuit formed by a pair of current sources and switches charges and discharges the capacitor linearly. The rising slope M_{RISE} and the falling slope M_{FALL} of V_{CP} can be derived as (1) and (2), respectively.

$$M_{RISE} = \frac{I_{CP1}}{V_{CP}} \quad (1)$$

$$M_{FALL} = \frac{I_{CP2}}{V_{CP}} \quad (2)$$

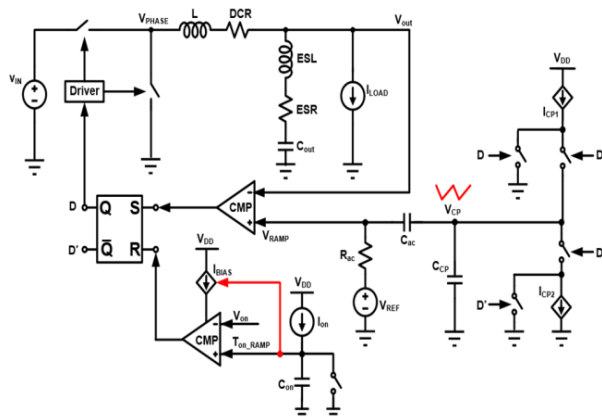


Fig. 4. Circuit diagram of buck converter using the proposed CPCOT scheme

Thus, the ramp signal that determines the stability and control characteristic can be easily generated without exponential settling. In addition, the ramp signal is coupled to reference voltage through a capacitor instead of adding ramp on the output voltage. Therefore, the control scheme is much more suitable for high switching frequency operation than VIC-based COT control. Fig. 5 shows the theoretical waveforms of proposed CPCOT controlled buck converter.

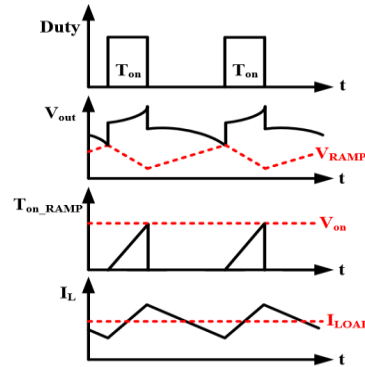


Fig. 5. Steady-state waveforms of CPCOT controlled buck converter

III. PROPOSED DYNAMIC-BIASED COMPARATOR FOR ON-TIME GENERATOR

In high switching frequency design, the comparator inside on-time generator dominates the quiescent power consumption of controller. Consequently, the dynamic-biased technique is developed to bias the comparator efficiently. Fig. 6 shows the concept and waveform of this technique. With applying on-time ramp signal to the bias circuit, the bias current of comparator inside on-time generator can be modulated dynamically.

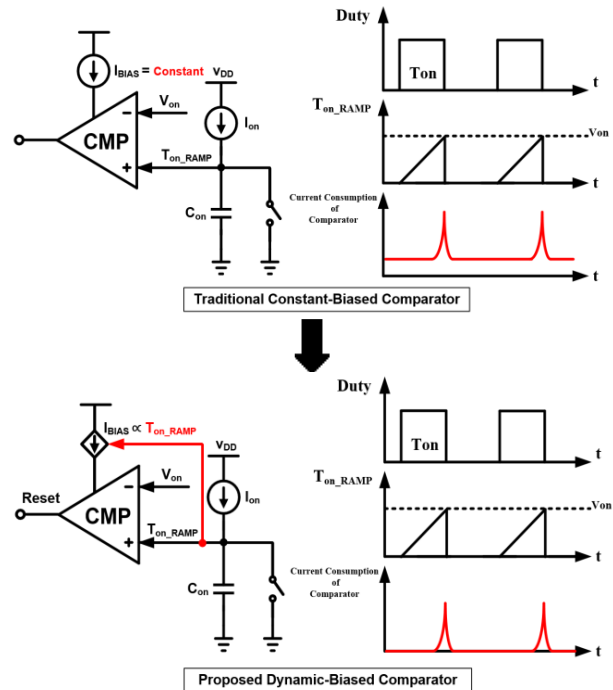


Fig. 6. Concept of dynamic-biased comparator for on-time generator

Fig. 7(b) shows the simulation result of average current consumption of comparator in on-time generator with dynamic-biased technique. There's around 58% current reduction compared with the conventional constant-biased method shown in Fig. 7(a).

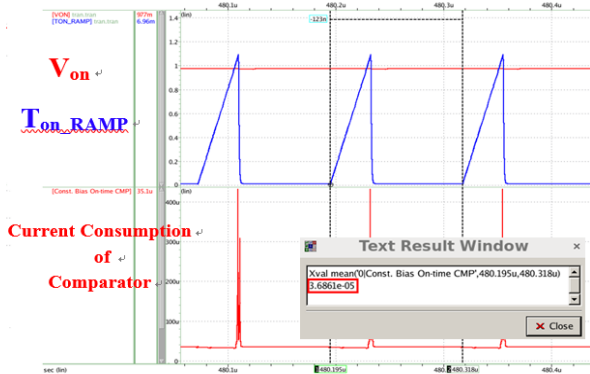


Fig. 7 (a). Average current consumption (36.86uA) of constant-biased on-time comparator in CCM

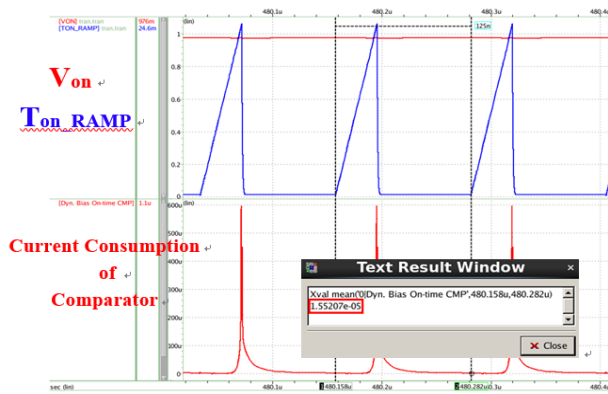


Fig. 7 (b). Average current consumption (15.52uA) of dynamic-biased on-time comparator in CCM

IV. SIMULATION RESULTS

The CPCOT control IC is fabricated in a 0.18um CMOS process for a buck converter with near 10 MHz switching frequency. Fig. 8 shows the chip layout of the control IC. The charge-pump circuit which is used to enhance the effect of the ESR voltage ripple in the feedback occupies only 0.061mm², 5.4% of the chip. Compared with VIC-based COT which uses 0.11mm² low-pass filter for virtual inductor current ripple injection [5], the proposed CPCOT control scheme is much more area-efficient.

SIMPLIS simulations were run for a CPCOT controlled buck converter with the following parameters: $V_{in}=3.3V$, $V_{ref}=1V$, $L=0.33\mu H$, $C_{out}=1.6\mu F$, and $ESR=8m\Omega$. Fig. 9 shows the simulated steady-state waveforms of the constant on-time controlled buck converter with and without charge-pump circuit. From Fig. 9(a), the waveforms show that the traditional RBCOT control method suffers from instability when using low ESR output capacitors, such as ceramic capacitors. By contrast,

Fig. 9(b) shows the stable operation attributed to the charge-pump-synthesized-ripple injection.

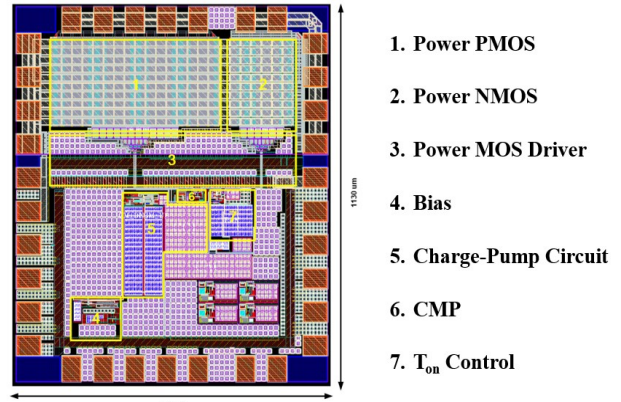
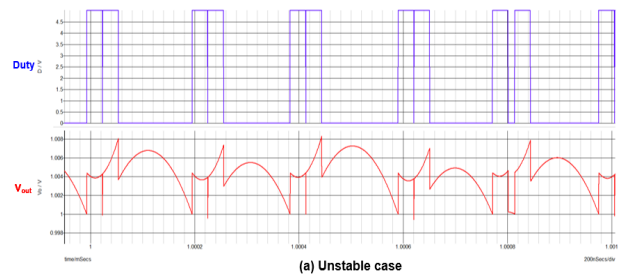
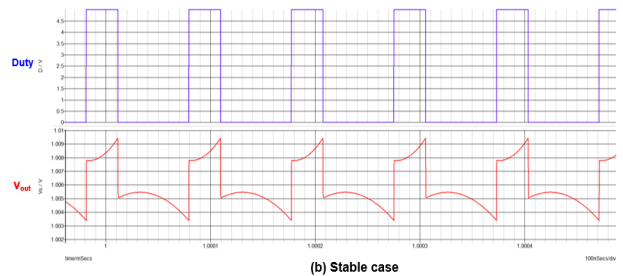


Fig 8. Chip layout of the control IC.



(a) Unstable case



(b) Stable case

Fig. 9. Simulated steady-state output voltage waveforms

As shown in Fig. 10, the full transistor level simulation result demonstrates that the CPCOT controlled buck converter accomplishes near time-optimal transient response with 50mV droop and 2us 1% settling time from 0.1A to 1.25A load step.

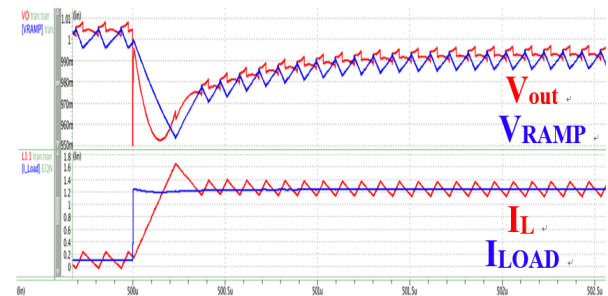


Fig 10. Transient response of buck converter using proposed control

V. CONCLUSION

This paper presents a high switching frequency CPCOT controlled buck converter IC without using large RC and complicated analog adder. Hence, the proposed design is more power and area efficient than the VIC-based COT [2]-[5]. The dynamic-biased comparator is developed to persevere much more quiescent current of controller. The full transistor level simulation results show that more than 50% quiescent current can be reduced after dynamic-biased technique is introduced. For the 1.15A/1ns load step, the simulation result shows near time-optimal transient response with only 50mV droop and 2us 1% settling time.

VI. ACKNOWLEDGEMENT

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