Power Factor Improvement of Flyback PFC Converter Operating at the Light Load

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***Abstract*—We propose a duty-ratio feed-forward controller for flyback power factor correction (PFC) converters operating in discontinuous conduction mode (DCM). For PFC applications, the power factor (PF) of the input current must be high under most load conditions. To improve PF of the flyback converter even under light load, we propose a compensation method for input capacitor current. The proposed controller significantly improves the displacement factor as well as the distortion factor, and therefore flyback PFC converter can achieve the high power quality. Meanwhile, the output voltage of the PFC converter is well regulated. The derivation of the proposed method is presented and effectiveness of the proposed method is demonstrated in experiments with a 100-W rated power prototype.**

***Index Terms*—Single-stage PFC, power factor improvement, total harmonic distortion, capacitor current, feed-forward controller.**

I. Introduction

Power supplies for TV, light emitting diode (LED), and telecom systems operate well below 50 % of their rated power due to redundant design. Recently, the 80 PLUS initiative certifies computer power supply products that meet power factor and efficiency requirements at 10 %, 20 %, 50 %, and 100 % of rated load. Also, the IEC61000-3-2 standard [1] and Energy Star specifications [2] have defined the minimum requirements of external power supplies at 25 %, 50 %, 75 %, and 100 % of full load. Therefore, a light load power factor is becoming more important in the power electronics industry.

Single-stage PFC converter is one of the most promising converter topologies because of its simple structure, a small number of components and high efficiency [3–6]. The flyback converter is usually designed to operate in DCM for low power applications, but it requires relatively a large input capacitor to suppress the input current ripple. Then, this large input capacitor generates a large amount of phase lead to the total input current with respect to grid voltage. To overcome the filter-related current displacement problem, several phase-lead/lag compensation schemes have been developed to increase the displacement factor of power converters. A lagging phase compensation technique has been developed for full-bridge inverters an alternative to proportional-resonant (PR) controllers [7]. Also, the phase leading current of a PFC boost converter was analyzed and a compensator has been designed in the time-domain [8, 9]. The compensator calculated desired feed-forward control input to compensate the effect of the input capacitor, and calculated duty-ratio well compensated the current distortion due to the input capacitor. Recently, the phase lag current of unfolding-type inverters was also analyzed and a compensator has been designed in the time-domain [10]. The compensator well compensated the effect of the output capacitor, and the result is expanded to other unfolding-type inverters. However, no published research has considered compensating for the current of the input capacitor for flyback PFC converters.

In this paper, we analyze the effect of the input capacitor current in the flyback PFC converter. Based on the analysis, we present a new nominal duty that compensates for the effect of the input capacitor current. Thus, the resulting total input current becomes in-phase with the grid voltage. Also, the output voltage of the PFC converter is well regulated. The applicability of this scheme was validated by experiments using a 100-W prototype.

The remainder of this study is organized as follows. Section II describes the operation of the flyback PFC converter and presents the effect of the input capacitor. Section III presents the proposed duty-ratio feedforward controller in the time domain. Section IV describes the experimental results. Section V presents conclusions.

II. Preliminaries and Problem Formulation

Single-stage flyback PFC converter (Fig. 1) consists of a diode bridge connected in series with a flyback converter and a large output capacitor. The flyback PFC converter is designed to operate in discontinuous conduction mode (DCM). It modulates the main switch S_1 with an almost constant duty cycle D_{conv} at switching frequency f_s.

The objective of the PFC converter is to obtain an input current that is synchronized with the sinusoidal input voltage. Assuming lossless operation, the conventional duty-ratio feedforward controller D_{conv} can be obtained as [11]

$$D_{conv} = \frac{\sqrt{2P_o L_m f_s}}{V_{rms}} \tag{1}$$

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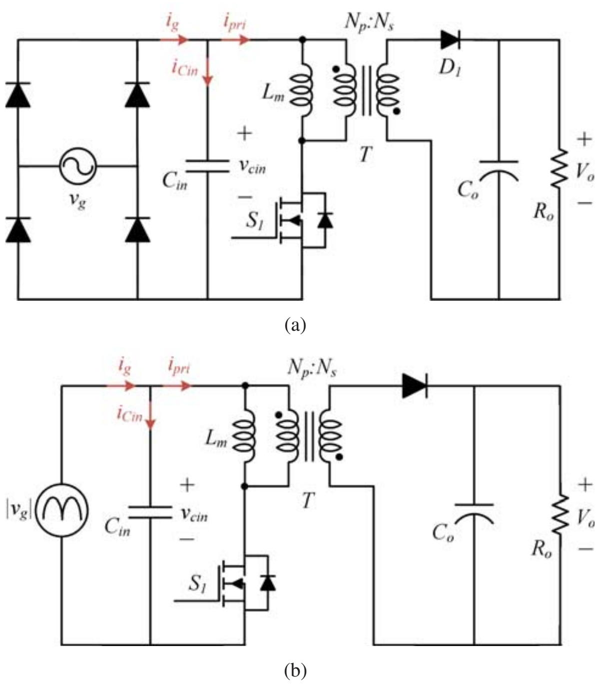


Fig. 1. Schematic diagram of the single-stage flyback PFC converter. (a) Schematic diagram. (b) Equivalent circuit.

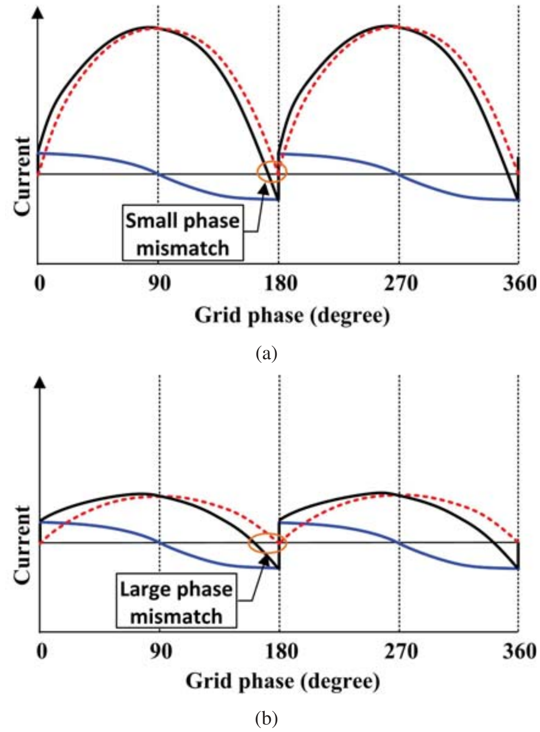


Fig. 2. Total input current (black solid line), primary current (red dashed line) and input capacitor current (blue solid line). (a) Under heavy load. (b) Under light load.

where P_o is a desired average power output, L_m is the magnetizing inductance seen from the primary winding, f_s is the switching frequency, and V_{rms} is the root-mean-square of the input voltage.

Then, the primary current can be represented as

$$i_{pri}(t) = \frac{D_{conv}^2 V_{rms}|\sin(2\pi f_L t)|}{\sqrt{2} L_m f_s} \tag{2}$$

where f_L is the grid frequency.

The total input current $i_g(t)$ is the sum of the primary current $i_{pri}(t)$ and the input capacitor current $i_{Cin}(t)$

$$(i_g(t) = i_{pri}(t) + i_{Cin}(t)). \tag{3}$$

The rectified grid voltage is applied to the input capacitor: $v_{C_{in}}(t) = \sqrt{2}V_{rms}|\sin(2\pi f_L t)|$, so

$$\begin{aligned} i_{Cin}(t) &= C_{in}\frac{dv_{C_{in}}(t)}{dt} \\ &= \begin{cases} 2\sqrt{2}\pi f_L V_{rms} C_{in}\cos(2\pi f_L t) \\ \qquad \text{if} \quad 0 < 2\pi f_L t < \pi \\ -2\sqrt{2}\pi f_L V_{rms} C_{in}\cos(2\pi f_L t) \\ \qquad \text{if} \quad \pi < 2\pi f_L t < 2\pi \end{cases} \end{aligned} \tag{4}$$

where C_{in} represents the input capacitance. Eq. (4) demonstrates that i_{Cin} increases as f_L, V_{rms} or C_{in} increases, but that i_{Cin} is independent of P_o.

When the conventional nominal duty is used, i_{Cin} does not greatly affect the total input current in the heavy load condition, but i_{Cin} occupies a progressively larger portion of the total input current as load decreases, and thereby shifts and distorts the total input current (Fig. 2). To compensate the effect of the input capacitor current, a new duty-ratio feed-forward controller should be developed for flyback PFC converter.

III. Controller design

The main control objective of the flyback PFC converter is to make the grid current become sinusoidal. The inner-loop current controller mainly controls the grid current. Also, flyback PFC converter should have the constant output voltage, which can be controlled by the outer loop controller. When the conventional duty cycle is used at the light load, the power factor decreases due to the effect of the input capacitor. To improve the displacement and distortion power factors, we propose a new duty-ratio feed-forward controller D_{comp} for the flyback PFC converter.

The averaged input capacitor current $\langle i_{C_{in}}(t)\rangle_{T_s}$ over a sampling period T_s. Here, we set the sampling period equal to the switching period. Then, we have

$$\begin{aligned} \langle i_{Cin}(t)\rangle_{T_s} &= \frac{\int_0^{T_s} i_{Cin}(\tau)d\tau}{T_s} \\ &= \frac{C_{in}}{T_s}(|v_{Cin}(T_s)| - |v_{C_{in}}(0)|). \end{aligned} \tag{5}$$

In the discrete time domain, Eq. (5) can be expressed as

$$\langle i_{Cin}(t)\rangle_{T_s} = \frac{C_{in}}{T_s}(|v_{Cin}[k]| - |v_{Cin}[k-1]|), \tag{6}$$

where k is the discrete time index, $v_{Cin}[k]$ is the present input capacitor voltage and $v_{Cin}[k-1]$ is the previously-sampled input capacitor voltage.

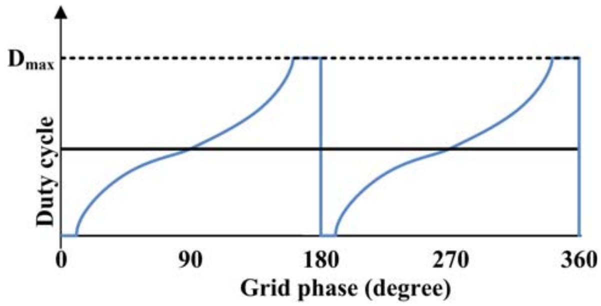


Fig. 3. Proposed feedforward duty cycle (Blue solid line) vs. conventional duty cycle (Black solid line).

The desired average grid current i_g can be represented as

$$\langle i_g(t)\rangle_{T_s} = \frac{\sqrt{2}P_o}{V_{rms}}|\sin(2\pi f_L k T_s)|. \tag{7}$$

Then the compensated primary current should be

$$\langle i_{pri,comp}(t)\rangle_{T_s} = \langle i_g(t)\rangle_{T_s} - \langle i_{Cin}(t)\rangle_{T_s}. \tag{8}$$

Rearranging eq. (2) and using eq. (8), we have the compensated feed-forward duty-ratio

$$D_{comp}(t) = D_{conv}\sqrt{\frac{i_{pri,comp}(t)}{i_{pri}(t)}} \tag{9}$$

The PFC converter cannot generate the negative current due to hardware limitations. Thus, when the compensated current is negative, the control duty is set to zero. When the compensated current is positive, the control duty is set to $D_{comp}(t)$. Since the required control duty is excessively high near the end of every half cycle, the control duty is set to a maximum duty D_{max}. Then, the resulting feed-forward duty-ratio becomes

$$D_{new}(t) = \begin{cases} 0 & \text{if} \quad \langle i_{pri,comp}(t)\rangle_{T_s} < 0. \\ D_{comp}(t), & \text{if} \quad \langle i_{pri,comp}(t)\rangle_{T_s} \geq 0 \\ D_{max}, & \text{if} \quad D_{comp}(t) \geq D_{max} \end{cases} \tag{10}$$

When we use the new nominal duty for the flyback PFC converter (Fig. 3), the capacitor input current can be completely compensated, therefore unity PF can be achieved theoretically.

IV. Experimental setup and results

To verify the feasibility of the proposed compensator for the flyback PFC converter, we conducted experimental tests using a prototype of the converter controlled by a TMS320F28377D digital signal processor. The major parameters for experiments are listed in Table I. The configuration of the flyback converter system is shown in Fig. 4. Inner-loop proportional-integral (PI) controller plus proposed feedforward controlller mainly take the input current control and outer-loop PI controller takes the output voltage control.

When the conventional feed-forward controller was used, the input current was distorted and out of phase with the grid voltage due to the effect of the input capacitor current (Fig. 5(a)). When the proposed feed-forward controller was used, the input current was close to sinusoidal and in phase with the grid voltage (Fig. 5(b)). Moreover, the current distortion near the zero crossing point was diminished. At quarter load, when the conventional nominal duty was used, the input current was

TABLE I
Parameters and components of the prototype.

Parameters	Symbols	Value
Nominal output voltage	V_o	40 V
Grid voltage	v_g	220 V_{rms}
Grid frequency	f_L	60 Hz
Switching frequency	f_s	20 kHz
Rated power	P_o	100 W
Transformer turns ratio	N_p:N_s	61:12
Magnetizing inductance	L_m	1.5 mH
Input capacitance	C_{in}	0.47 μF
Output capacitance	C_o	1000 μF x 2
Components	**Symbols**	**Part number**
Primary switch	S_1	FCH072N60F
Output diode	D_1	MUR820G
Transformer core	T	PQ3535

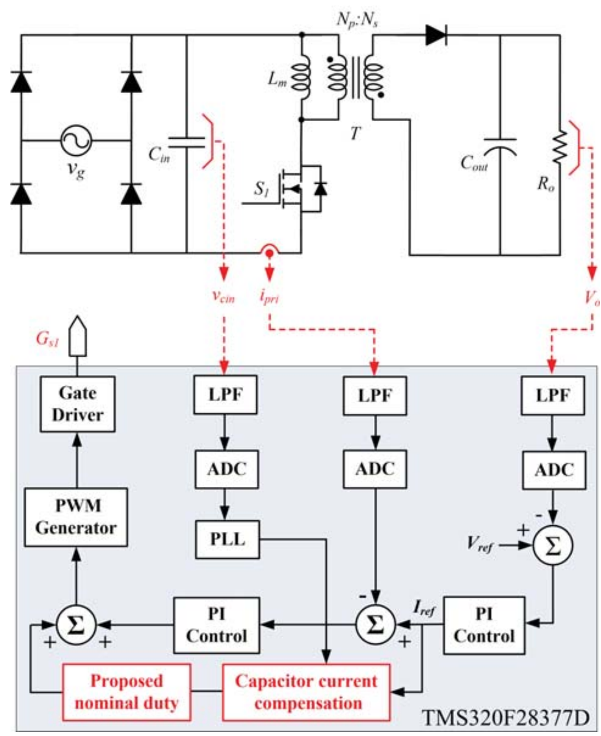
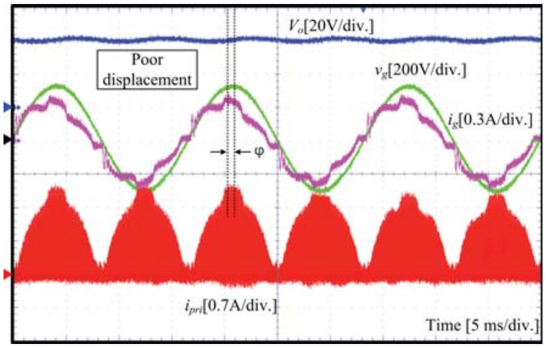
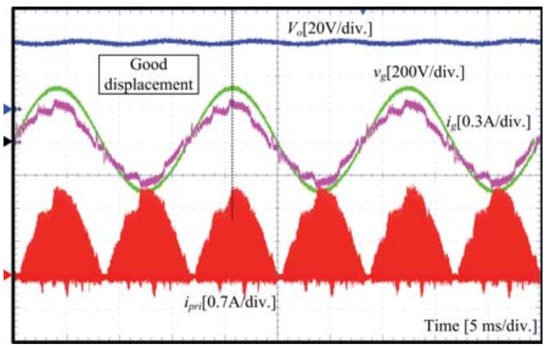


Fig. 4. Configuration of the proposed control system. LPF, ADC, PLL stand for low pass filter, analog-to-digital converter, phase locked loop, respectively.

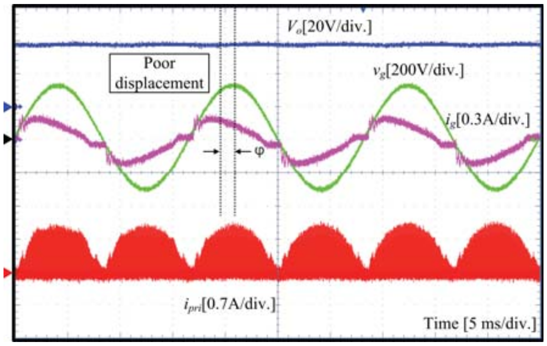


(a)

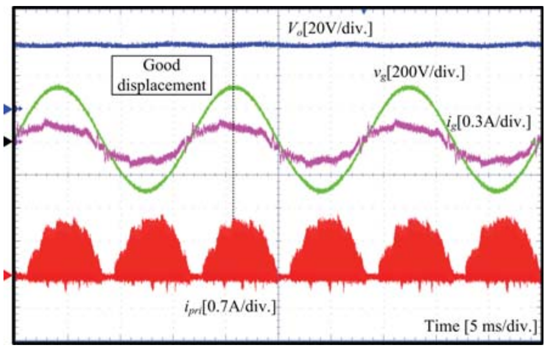


(b)

Fig. 5. Experimental waveforms under half load condition; the grid voltage (green), the grid current (purple), the output voltage (blue) and the primary current (red). (a) When the conventional nominal duty is used. (b) When the proposed nominal duty is used.



(a)



(b)

Fig. 6. Experimental waveforms under quarter load condition; the grid voltage (green), the grid current (purple), the output voltage (blue) and the primary current (red). (a) When the conventional nominal duty is used. (b) When the proposed nominal duty is used.

TABLE II
MEASURED POWER FACTOR (PF) AND TOTAL HARMONIC DISTORTION (THD) AT 40 V OUTPUT VOLTAGE AND 220 VRMS GRID VOLTAGE

Controllers	At half load		At quarter load	
	PF (%)	THD (%)	PF (%)	THD (%)
Conventional one	95.5	11.6	85.9	17.3
Proposed one	98.6	11.2	96.4	17.2

close to sinusoidal, but the phase discrepancy becomes greater than that under half load condition (Fig. 6(a)). When the proposed controller was used, the input current was sinusoidal and in phase with grid voltage (Fig. 6(b)). The PF and the total harmonic distortion (THD) of the total input current under both half load and quarter load are listed in Table II.

V. CONCLUSION

To improve the power factor under the light load, we propose a duty-ratio feed-forward controller for the flyback PFC converter. The flyback PFC converter features step-up/down ability, low cost, and high efficiency. However, it suffers from low power factor and total harmonic distortion under the light load due to the input capacitor effect. The proposed feed-forward controller aims at compensating the phase leaded current caused by the input capacitor. We describe the implementation of the controller, the required compensated current, and the controller structure in detail. We conducted experiments with an 100-W prototype to verify the operation of the proposed feed-forward controller. The proposed feed-forward controller significantly increased the power factor of the converter. Meanwhile, the output voltage of the PFC converter is well regulated.

ACKNOWLEDGMENT

This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (No. 2018R1D1A1B07044999) and in part by the MSIP (Ministry of Science, ICT and Future Planning), Korea, under the "ICT Consilience Creative Program" (IITP-R0346-16-1007) supervised by the IITP (Institute for Information & communications Technology Promotion)"

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