A Distributed Control Architecture for Cascaded H-Bridge Converter

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***Abstract*—Cascaded H-bridge topology has been used in grid-tied converter for battery energy storage system due to its modular structure. To fully utilize the converter's modularity, we propose a hierarchical distributed control architecture that consists of primary control and secondary control. Primary control ensures correct current tracking, but may lead to unequal power output among modules. A distributed secondary control based on consensus algorithm is presented to establish equal power sharing among modules. Further, a carrier phase shift control is implemented to achieve multilevel output voltage and harmonic reduction. Finally, the effectiveness of the presented control strategy is verified through experiments.**

I. Introduction

The increasing penetration of intermittent renewable energy sources, such as wind and solar, leads to numerous challenges for power grid operation. Dispatchable battery energy storage system (BESS) can address many of these issues by balancing out power fluctuation, shaving peak and filling valley in power requirement, increasing reserve capacity of power grid, and etc. It is a cost-efficient technology available today to enhance the grid reliability and the power quality in the face of fluctuating generation [1].

As one of the most popular multilevel topologies, cascaded H-bridge (CHB) topology can effectively integrate BESS into the grid, since it can achieve low harmonics, reduced switching frequency, increased efficiency and etc [2], [3]. Moreover, its inherent modularity makes it easily extensible to a higher number of output voltage levels by increasing the number of H-bridge modules. Also, the modular structure can reduce the voltage stress on the switches and provide more redundancy.

CHB converter operation usually utilizes centralized control since it is easier to realize system control and synchronized modulation [4], [5]. Centralized control approaches requires each H-bridge module to communicate with a central controller via high-speed communication links. The central controller executes all the calculations and sends switching commands to each module at every switching cycle, which increases computation burden of the central controller and makes modularization difficult. Furthermore, the switching noise of high-power converters can negatively affect the quality of communication, which could potentially degrade the controller's performance.

To circumvent the need for central controller and high bandwidth communication, distributed control approaches are preferred. In distributed control strategies, all control and modulation are implemented in the local controllers for each module, named as module controllers. Information is collected and exchanged through a sparse communication network. However, for CHB converter, it is quite challenging to achieve accurate output current regulation and power sharing control among modules without globally coordinating the switching actions of all the semiconductor devices. In [6], a decentralized control method is presented to realize maximum power point tracking for each H-bridge module in PV applications. However, a single module is used to compensate all the transient and reactive power which may limit the converter operating range. To achieve both coordinated output current and power sharing regulation, a method proposed in [7] is to optimize current regulation in module controllers by mitigating current measurement errors and DC voltage mismatches. But module controllers could potentially influence each other since errors and mismatches could not be eliminated completely. In [8]–[10], an LC filter is added to each module so that the output voltage of each module can be controlled independently as an AC signal instead of a pulse signal. The control strategy in [8] utilizes local voltage control along with a virtual droop resistance, but it requires a resistive impedance to connect to

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the grid. In [9] the author proposed a power factor-frequency inverse droop control strategy to generate desired voltage reference. Then, power sharing among modules is realized when all the modules have the same phase angle. However, the method only works for standalone inverter and cannot be applied to grid-tied applications.

In this paper, a hierarchical distributed control architecture for CHB converter is proposed. The proposed architecture consists of two levels, namely primary and secondary control. Primary control guarantees a good current tracking performance and is a decentralized control strategy without the need of any communication. However, the converter operates in an undesired unbalanced state with only primary control, where each module outputs non-uniformed active and reactive power. A secondary control scheme based on distributed consensus algorithm is proposed to generate equal voltage and power output among modules. The proposed secondary control scheme only requires a low bandwidth communication network to share information. The analysis presented in this paper shows that both output current regulation and equal power sharing can be achieved by the proposed hierarchical distributed control architecture. Additionally, a carrier phase shift (CPS) control is implemented to deal with the synchronization issue between module controllers and obtain multilevel output voltage and lower ripple output current. It is noteworthy that though the proposed control scheme is applied for BESS in this paper. it can also be extended to other applications.

The rest of the paper is organized as follows: primary control and secondary control are introduced in Section II and III, respectively. The CPS control is designed in Section IV. Experiment verification is provided in Section V. Section VI concludes the work.

II. Primary Control Scheme

A single phase grid-tied CHB converter with separate DC battery sources and its control block diagram are shown in Fig. 1. It is assumed that there are N H-bridge modules connected in series with a filter inductor L_{f}. The fundamental level of the proposed distributed control architecture is primary control, whose objective is to maintain a stable and accurate current control. The corresponding control scheme is depicted in the primary control part of Fig. 1.

In primary control, one single module, i.e. module 1 in Fig. 1, is named as current control module (CCM) and designed to control the converter output current i_{g}. A digital phase lock loop (PLL) produces a reference sine signal $\sin\hat{\theta}$ that is synchronized with the grid voltage. The output current reference i_{ref} is generated by multiplying the current amplitude reference I^* with the sine signal $\sin\hat{\theta}$. The output current i_{g} is then regulated via a PI or PR controller.

Due to the series topology, all modules share the same output current. Two or more modules trying to control the converter output current at the same time could lead to instability. Therefore, only one CCM is presented while other modules, i.e. module $i(i = 2, 3, \ldots, N)$ in Fig. 1, are controlled in an open-loop manner. These modules are called voltage control

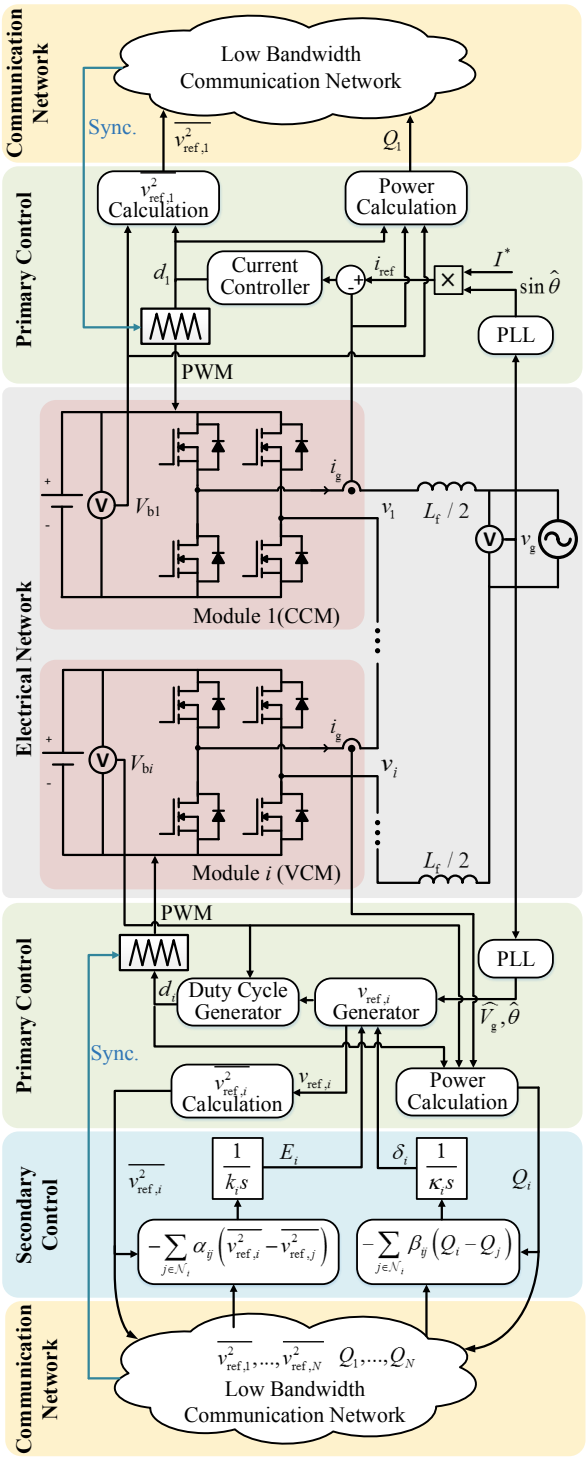
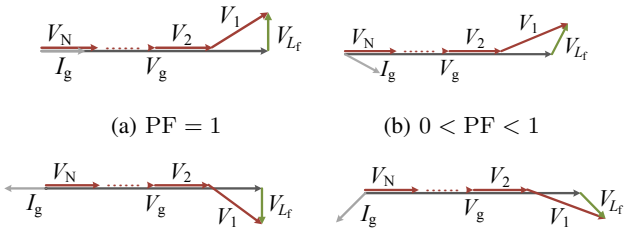


Fig. 1: The topology and distributed control architecture of single phase CHB converter

module (VCM). The reference output voltage of each VCM is designed as $\frac{1}{N}v_{\mathrm{g}}$, where v_{g} represents the grid voltage magnitude. In steady state, all the VCMs' output builds up to a total fundamental AC voltage $\frac{N-1}{N}v_{\mathrm{g}}$. The remained voltage



(a) PF $= 1$ (b) $0 <$ PF < 1

(c) PF $= -1$ (d) $-1 <$ PF < 0

Fig. 2: The voltage vector diagram of different modules with only primary control under different conditions

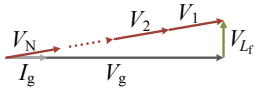


Fig. 3: The voltage vector diagram under balanced condition

$\frac{1}{N}v_g$ and the voltage drop across filter inductance v_{L_f} are compensated by CCM. The desired fundamental component of CCM output voltage in steady state is calculated as:

$$v_1 = \frac{1}{N}v_g + v_{L_f} = \frac{1}{N}v_g + j\omega L_f i_g \tag{1}$$

Fig. 2 shows the voltage vector diagram of different modules with only primary control under different conditions. Fig. 2a shows the nominal operation condition at unity power factor (PF). It can be found that VCMs have the same output voltage in the same phase with grid voltage, and the output voltage of CCM differs due to the existence of filter inductor. If PF changes, the amplitude and phase of the output voltage for CCM change accordingly while the ones of VCMs' remain unchanged, as shown in Fig. 2b-d. VCMs are always aligned with grid voltage and CCM compensates for voltage transients or power variations of the converter. It can be concluded that CCM injects/absorbs different active and reactive power to/from the grid compared with VCMs. Therefore, with only primary control, the output voltage, and thus output power among modules will always be unbalanced. The unbalanced power output can cause battery SOC unbalance, which could result in a reduced utilization of the converter.

To deal with the issue described above, the next level control is required, which is named as secondary control in the proposed hierarchical distributed control architecture. The aim of secondary control is to share the active and reactive power demand equally among modules and maintain balanced operation. That is, the amplitude and phase of the output voltage for each module should be of the same value. The corresponding vector diagram is presented in Fig. 3 and the secondary control scheme with a low bandwidth communication network is detailed in Section III.

III. Secondary Control Scheme For Equal Power Sharing

In this section, the secondary control scheme based on distributed consensus algorithm for the CHB converter is presented. First, we provide a brief introduction to the graph theory and its properties that are going to be used in the subsequent analysis. Then, the secondary control scheme is described in detail and the realization of power sharing among modules is interpreted.

A. Graph Theory and Consensus Algorithm Preliminaries

According to graph theory, a communication network can be depicted by an undirected graph $G = (\mathcal{V}, \mathcal{E})$, with $\mathcal{V} = \{n_1, n_2, \ldots, n_N\}$ being the set of nodes, $\mathcal{E} \subseteq \{(n_i, n_j) \in \mathcal{V} \times \mathcal{V}\}$ being the set of edges in the graph. Define $\mathcal{A}$ as a corresponding $N \times N$ adjacency matrix with $\alpha_{ij} = \alpha_{ji} \geq 0$ and $\alpha_{ii} = 0$, which means that interactions between nodes are mutual. We assume that $\alpha_{ij} = \alpha_{ji} > 0$ if and only if the ith and jth node can communicate directly with each other, i.e., $(n_i, n_j) \subseteq \mathcal{E}$, otherwise $\alpha_{ij} = \alpha_{ji} = 0$. The indices of the nodes that are interconnected to node n_i directly form its neighboring set, denoted by $\mathcal{N}_i = \{j \mid (n_i, n_j) \subseteq \mathcal{E}\}$. If a path between any two nodes exists in a graph, it is called a connected graph.

Furthermore, we assume that each node n_i $(i = 1, 2, \cdots, N)$ of the graph represents an agent that holds a state x_i. To achieve consensus of a multi-agent system (MAS), appropriate algorithms are needed for cooperation among agents, called consensus algorithms [11]. Conventional consensus algorithm describes the dynamics of x_i as

$$\dot{x_i} = -\sum_{j \in \mathcal{N}_i} \alpha_{ij} (x_i - x_j) \tag{2}$$

For a connected graph $G = (\mathcal{V}, \mathcal{E})$, when consensus is achieved, all state variables x_i converge to a common value, i.e., $x_i = x_j$ for all i and $j (i, j = 1, 2, \cdots, N)$ [12].

If an agent acting as a leader is controlled by an external controller without obeying (2), while other agents still obey (2), it will set up a "leader-follower" relationship in consensus algorithm [13]. In this case, with carefully designed control parameters and communication network, the states of overall interconnected network can be controlled by regulating the motion of the leader [14].

B. Secondary Control and Equal Power Sharing

The proposed secondary control exploits the "leader-follower" relationship in consensus algorithm. We use the undirected graph $G = (\mathcal{V}, \mathcal{E})$ to model the communication network of the CHB converter. Every agent represents a module, and the edge depicts the communication channel among modules. And there exists a direct or indirect communication channel among any two modules to ensure a connected graph.

The proposed secondary control scheme is depicted in the secondary control and communication network part of Fig. 1. CCM acts as the leader and controls the converter output current by controlling its output voltage v_1. Whereas VCMs

act as followers and regulate the output voltage using the secondary controller, which can be expressed as

$$v_{\mathrm{ref},i} = \left(\frac{\hat{V}_{\mathrm{g}}}{N} + E_i\right)\sin\left(\hat{\theta} + \delta_i\right) \tag{3a}$$

$$k_i \frac{dE_i}{dt} = -\sum_{j\in\mathcal{N}_i} \alpha_{ij}\left(\overline{v_{\mathrm{ref},i}^2} - \overline{v_{\mathrm{ref},j}^2}\right) \tag{3b}$$

$$\kappa_i \frac{d\delta_i}{dt} = -\sum_{j\in\mathcal{N}_i} \beta_{ij}\left(Q_i - Q_j\right) \tag{3c}$$

where for the ith ($i = 2, 3, \ldots N$) VCM, E_i, δ_i are secondary control variables, k_i, κ_i are positive gains; for any module i ($i = 1, 2, \ldots N$), $v_{\mathrm{ref},i}$ is the open-loop-control reference voltage and $\overline{v_{\mathrm{ref},i}^2}$ is the moving average of $v_{\mathrm{ref},i}^2$, Q_i is the reactive power output; $\hat{V}_{\mathrm{g}}$ and $\hat{\theta}$ are grid voltage amplitude and phase tracked by PLL, respectively. The $N \times N$ matrix $\mathcal{A} = [\alpha_{ij}]$ and matrices $\mathcal{B} = [\beta_{ij}]$ are the adjacency matrix of the communication network. For simplicity, we assume $\alpha_{ij} = \beta_{ij}$. $\mathcal{N}_i$ represents the neighboring set of the module i, which contains all the modules it communicates with.

For the followers, i.e. VCMs, the output voltage is regulated by the secondary controller (3a)-(3c). The open-loop-control voltage reference for VCMs is generated using (3a) with secondary control inputs E_i and δ_i, which are computed by (3b) and (3c), respectively. From (3b) and (3c), it can be observed that the secondary controller requires the ith VCM to obtain $\overline{v_{\mathrm{ref},j}^2}$ and Q_j from all its neighbours. Then, all the modules should update and share their own $\overline{v_{\mathrm{ref}}^2}$ and Q through the communication network. The controller gains k_i and κ_i in (3b) and (3c) correspond for the secondary control convergence speed. For the leader, i.e. CCM, the regulation of its output voltage obeys the current controller rather than the secondary controller (3a)-(3c). Although not carrying out (3a)-(3c), CCM should calculate and share its information, which is needed by the secondary controller.

In steady state, the derivative on the left-hand side of (3b) and (3c) should be zero, which is satisfied when $\overline{v_{\mathrm{ref},1}^2} = \overline{v_{\mathrm{ref},2}^2} = \ldots = \overline{v_{\mathrm{ref},N}^2}$ and $Q_1 = Q_2 = \ldots = Q_N$. Since $v_{\mathrm{ref},i}$ is a sinusoidal signal, the same moving average of $v_{\mathrm{ref},i}^2$ means the same amplitude of $v_{\mathrm{ref},i}$, i.e. $\left(\frac{\hat{V}_{\mathrm{g}}}{N} + E_i\right)$ is identical for all the modules. Then, we can obtain $E_1 = E_2 = \ldots = E_N$. Due to the same current flowing through all the modules and the same reactive power output achieved by (3c), it can be further derived that $P_1 = P_2 = \ldots = P_N$. The equal power sharing is thus realized by secondary control in steady state. And the secondary control variables, E_i and δ_i, converge to the values that generate the output voltage as needed to achieve output current regulation and equal power sharing shown in Fig. 3.

In addition, if the bipolar PWM modulation is used, the fundamental component of the module i's output voltage can be expressed as (4). For CCM, the reference voltage $v_{\mathrm{ref},1}$ can be calculated using (4). For VCM, we can get its duty cycle generator (5) by combining (3a) and (4)

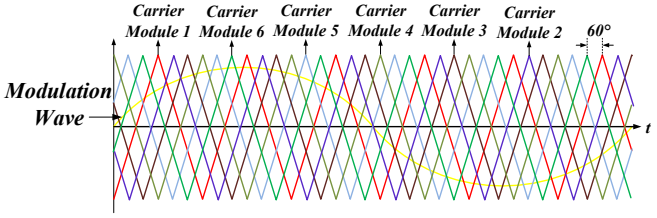


Fig. 4: The schematic diagram of CPS modulation

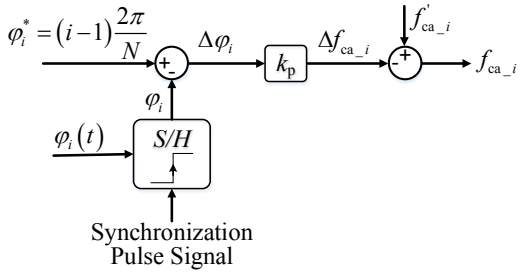


Fig. 5: The block diagram of CPS control

$$v_i = (2d_i - 1)V_{\mathrm{b}i} \tag{4}$$

$$d_i = \frac{1}{2} + \frac{1}{2V_{\mathrm{b}i}} v_{\mathrm{ref},i} = \frac{1}{2} + \frac{1}{2V_{\mathrm{b}i}}\left(\frac{\hat{V}_{\mathrm{g}}}{N} + E_i\right)\sin\left(\hat{\theta} + \delta_i\right) \tag{5}$$

where d_i is the calculated duty cycle; $V_{\mathrm{b}i}$ is the measured battery voltage. The calculated CCM reference voltage and the generated VCM duty cycle include the battery voltage, which can decouple the controller performance from battery voltage variation.

It is worth noting that the proposed secondary control does not require a fully connected communication network where each module can communicate with any other modules. Equal power sharing can be achieved with a sparse communication network where each module only communicates with its neighbor modules. This property makes it suitable for daisy-chain type communication networks such as the one used in [15].

IV. Carrier Phase Shift Control

CPS modulation has been widely used for CHB converter to achieve multilevel output voltage. Conventionally, the carrier of each module has a phase shift, $\frac{2\pi}{N}$, from its adjacent module. Fig. 4 shows the schematic diagram of CPS modulation when $N = 6$. CPS modulation is easy to implement if all the modules are controlled by a central controller. However, for distributed control, each module implements the modulation independently without a central controller and the internal clocks in different module controllers can not be accurately synchronized due to crystal frequency drift and other operation conditions difference. Then the applied carrier frequency would differ among modules and the phase shift between modules is time-varying.

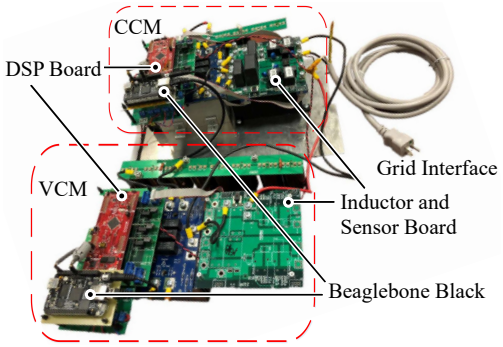


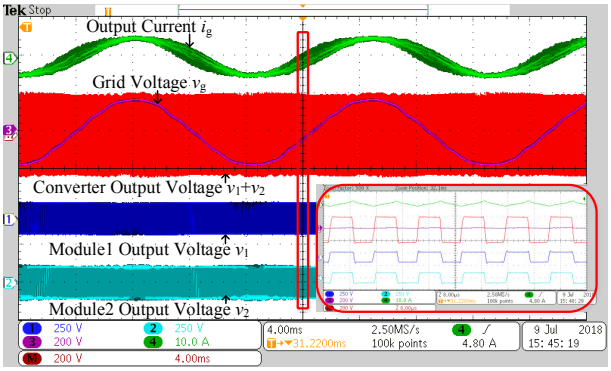
Fig. 6: Hardware with one VCM and one CCM

TABLE I: Experimental Parameters

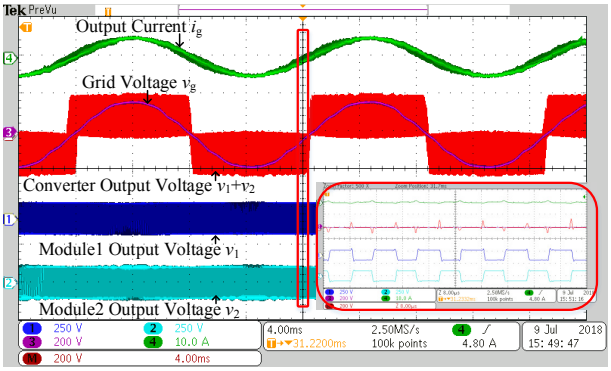
Electrical Parameters	
Grid Frequency f	60Hz
Grid Nominal Voltage V_{g}	120 $\mathrm{V_{rms}}$
Battery Nominal Voltage V_{b}	100 V
Filter Inductance L_{f}	550 μH
Switching Frequency f_{s}	75 kHz
Sync. Pulse Signal Frequency	750 Hz
Secondary Control Data Frequency	10 Hz
Controller Parameters	
Current PR controller Proportional gain	0.07
Current PR controller Resonant gain	5
Secondary Controller Coeff. k_i	0.2
Secondary Controller Coeff. κ_i	100
CPS Control Coeff. k_{p}	1×10^{-8}

To deal with the issue presented above, a corresponding CPS control method is used to achieve carrier frequency synchronization and desired CPS among modules, as shown in Fig. 5. First, we assume that there is a global synchronization pulse signal to ensure that CPS adjustment in all modules occurs simultaneously. Once receiving the synchronization pulse signal, the module controller samples and holds the carrier phase φ_i at that moment, which is then compared with the desired CPS, $\varphi_i^* = (i-1)\,\dfrac{2\pi}{N}$. The obtained error, $\Delta\varphi_i$ is multiplied by a positive coefficient k_{p}. The output, $\Delta f_{\mathrm{ca\_}i}$ is used to tune the carrier frequency and then the applied carrier frequency can be expressed as $f_{\mathrm{ca\_}i} = f_{\mathrm{ca\_}i}^{'} - \Delta f_{\mathrm{ca\_}i}$, where $f_{\mathrm{ca\_}i}^{'}$ is the unadjusted carrier frequency. In steady state, the applied carrier frequency $f_{\mathrm{ca\_}i}$ will be the same for all modules and the CPS φ_i will be controlled to the desired value. The accurate CPS is thus achieved.

Moreover, the synchronization pulse signal will have a slight time error inevitably and we assume that $(\Delta\varphi_i)_{syn\varepsilon}$ is the maximum phase error caused by the inaccuracy of the synchronization pulse signal. If the control is implemented in a digital signal processor, the carrier frequency can not be changed continuously. Assume that $(\Delta f_{\mathrm{ca\_}i})_{\min}$ is the resolution of carrier frequency change. It is necessary that the synchronization pulse signal error has no influence on the carrier frequency. That is, the coefficient k_{p} should be selected



(a) Worst case waveforms without CPS control



(b) Waveforms with CPS control

Fig. 7: Experimental results with only primary control enabled

to meet the requirement that $k_{\mathrm{p}}(\Delta\varphi_i)_{syn\varepsilon} < (\Delta f_{\mathrm{ca\_}i})_{\min}$. Besides, the CPS control should have the highest processing priority in module controllers to ensure its accuracy.

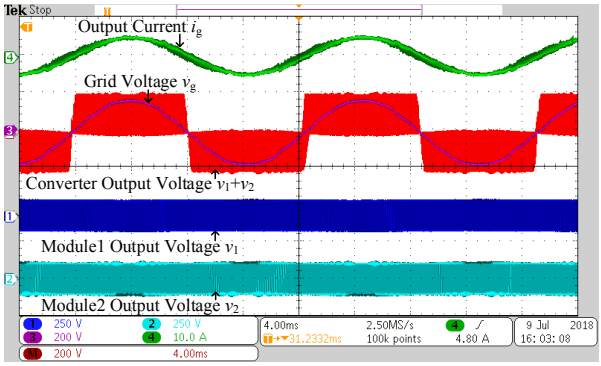
V. Experimental Verification

To verify the performance of the proposed distributed control method, a CHB converter with a CCM and a VCM is constructed, as shown in Fig. 6. The converter output is connected to the $120\mathrm{V_{rms}}$/60Hz grid via an inductor. The electrical and controller parameters are listed in Table I. The switching frequency f_{s} was set to 75 kHz. SiC MOSFET CCS050M12CM2 from Wolfspeed is used to allow high switching frequency.

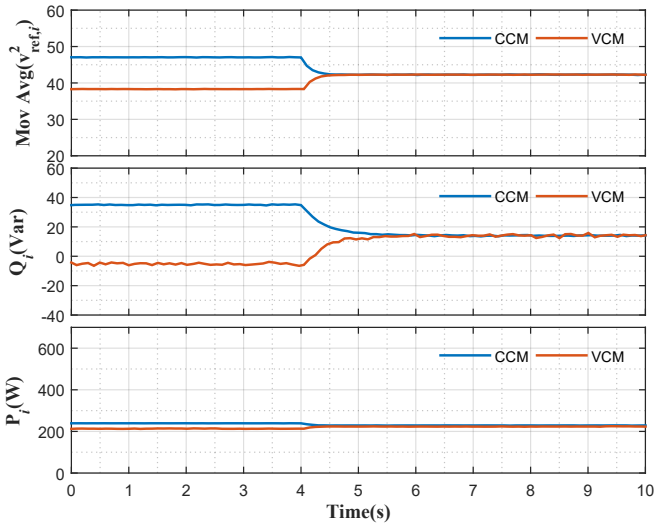
A. Implementation

The primary control is implemented in a digital signal processor (DSP) TMS320F28377S from Texas Instrument using local measurement. A PR current controller is used in CCM to achieve high bandwidth and large phase margin. The data for the secondary control was calculated in DSPs at a frequency f_{s} and transferred to the communication network at a low-frequency 10Hz.

The secondary control is implemented using the RIAPS platform. The RIAPS platform is a distributed control platform

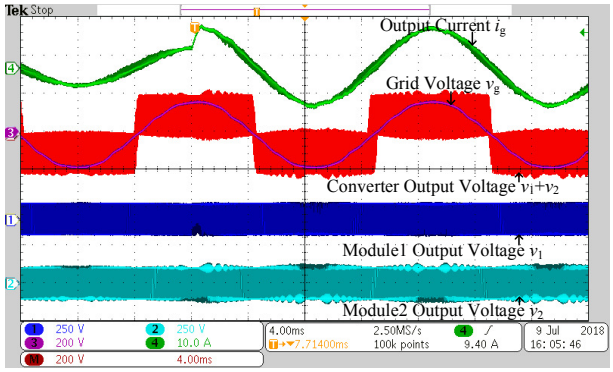


(a) Waveforms with CPS and secondary control activated

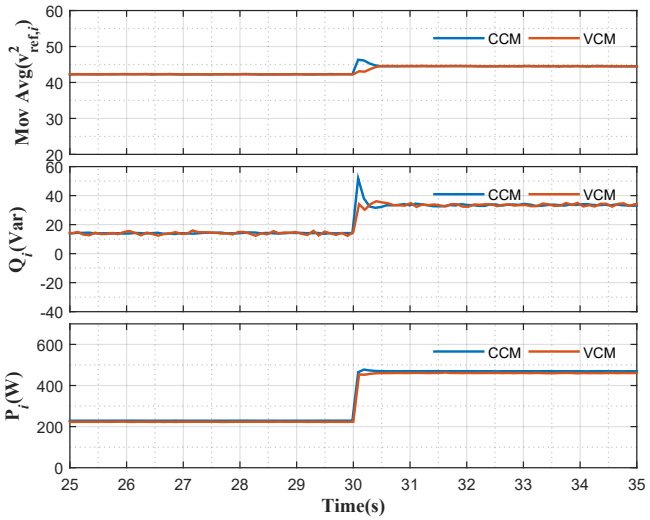


(b) $\overline{v^2_{\text{ref}}}, Q, P$ calculated by DSPs

Fig. 8: Experimental results with secondary control activated



(a) Waveforms with CPS and secondary control enabled



(b) $\overline{v^2_{\text{ref}}}, Q, P$ calculated by DSPs

Fig. 9: Experimental results when I^* steps from 5A to 10A

that allows real-time messaging and high precision synchronization. More information about the RIAPS platform and its synchronization capability can be found in [16]–[19].

The hardware for the RIAPS node is Beaglebone Black (BBB) single board computer. Each BBB can communicate with its DSP using Modbus protocol. At every time step, the BBB sends a Modbus message to pull $\overline{v^2_{\text{ref},i}}$ and Q_i calculated by the DSP. Then, based on (3b) and (3c), each BBB calculates E_i, δ_i and sends them back to the DSP to modify VCMs' reference voltage. At the same time, $\overline{v^2_{\text{ref},i}}$ and Q_i are published to the RIAPS network to be shared with other RIAPS nodes.

Besides, the RIAPS platform can generate synchronized pulses at different BBBs with a time error less than 1 μs [20]. This feature can guarantee a accurate synchronization signal used to implement the CPS control among DSPs. The synchronization pulse signal was sent from the RIAPS platform to DSPs at $f_s/100$ frequency, which is enough for DSP synchronization.

B. Experimental Results

First, only primary control is enabled to validate the current tracking performance. Module 1 and 2 are controlled as CCM and VCM, respectively. The current reference amplitude I^* is set to 5 A. In the first case, no CPS control is implemented for the converter. The phase difference between different modules becomes time-varying. The worst case happens when all the modules have the same carrier phase, as shown in Fig. 7a. In the second case, the CPS control described in Section IV is activated. Fig. 7b shows the experimental results, where the output voltage of the two modules have a fixed phase shift π. Both cases have realized the accurate output current control, which indicates that the presented primary control has a good current control performance. By comparing the experimental results from the two cases, we can conclude that the CPS control can achieve a multilevel voltage output and a lower ripple current.

Then, the secondary control is activated with the synchronized primary control enabled. The experimental results are

shown in Fig. 8a. Compared Fig. 8a with Fig. 7b, it can be found that the current tracking performance is still good after activating the secondary control. To validate the effectiveness of the secondary control, data transmitted in communication network are recorded and plotted in Fig. 8b. It can be observed that variables used in the secondary controller, $\overline{v_{\mathrm{ref}}^2}$ and Q, have accurately converged to the same value in about 2 s. For demonstration purpose, the active power output of each module is calculated in the DSP and sent out to the BBB. Fig. 8b shows that the active power mismatch between the two modules is minimized by the secondary control. However, a very small active power mismatch exists due to the current measurement difference between the two modules.

Finally, the dynamic performance of the proposed control scheme is tested and verified by stepping the current reference amplitude I^* from 5 A to 10 A. The transient responses of the output current and output voltage are shown in Fig. 9a and the secondary control responses are shown in Fig. 9b. The output current can follow the reference variation in 800 μs with little overshoot. The output power and the moving average of v_{ref}^2 have converged to the same value in about 1 s. The experimental results confirm that the proposed distributed control strategy can achieve good current tracking performance and equal power sharing among modules.

VI. Conclusion

In this paper, we propose a hierarchical distributed control architecture for CHB converter, which consisting of two levels - primary control and secondary control. The primary control is in charge of ensuring output current tracking, while the secondary control based on consensus algorithm achieves equal power sharing among modules. Moreover, a controller is designed to implement the CPS control and DSP synchronization. The proposed control strategy is proved to be effective through experiment.

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