A study of voltage feedforward under weak grid conditions

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***Abstract* — The voltage feedforward (VF) is widely used in grid-tied inverter to improve the inverter's starting performance, disturbance rejection performance and suppress the effect of grid voltage harmonics. However, under weak grid conditions, VF has negative effect on system stability and disturbance-resistant performance. In this paper, taking the L-filtered grid-tied inverter as an object, the influence mechanism of the VF on the inverter in weak grid is clarified by the equivalent transformations of the control block diagram. It is pointed out that root cause of the VF's negative effect is the control delay in VF path. Therefore, the method that incorporates a lead-lag compensator in the VF path is proposed. The proposed method improves not only the system stability but also the ability of suppressing the low order current harmonics. Simulation and experiment result verify the effectiveness of the proposed method.**

Keywords—voltage feedforward, grid-tied inverter, weak grid, control delay, lead-lag compensator

I. INTRODUCTION

The grid-connected inverter is an important interface between renewable energy system and the power grid. To improve the inverter's starting performance, disturbance rejection performance and suppress the negative effect of grid voltage harmonics, the grid voltage feedforward (VF) is widely used in grid-connected inverter [1]-[3]. However, with the increasing share of renewable energies in the power system, more and more grid-connected inverter have become attached to weak grids as they are located far from load centers[4]. And according to recent studies, VF might have negative effect on the stability of grid-tied inverter when it is connected to weak grid [5]-[9].

Some studies about the negative effects of the VF and the method of dealing with them has been carried out. Ref [6][7] reports that the VF brings in an extra positive feedback path and worsens stability in inverter connected to weak grid. Research [8][9] points out the PLL is part of the reason that the VF's negative effect and it can be overcome by decreasing the PLL bandwidth. In [10], an adaptive algorithm is proposed for the PCC voltage feedforward in the weak grid. In [11], a low-pass filter which is incorporated in the voltage feedforward path is proposed to improve the system stability. However, it will weaken the ability of suppressing the effect of grid voltage harmonics because the harmonics in the PCC voltage were filtered out by the low-pass filter. Paper [12] points out that control delay is a reason of the negative effect of the voltage feedforward control, and proposes an improved VF with band-pass filter. The effect of the error in feedforward loop caused by delays is analyzed in [13]. Ref [5] proposes a proportional voltage feedforward which improve system stability and reserve ability to improve power quality under weak grid condition.

Although many improved VF strategies for weak grid has been given, most of the research is in LCL-filtered gird-tied inverter. Some of them focus on the stability and ignore other abilities of the VF such as harmonics suppression. And the influence mechanism of the VF on the L-filtered grid-tied inverter in weak grid is not clear enough. This paper takes L-filtered grid-tied inverter as an object, analyzes the influence mechanism of the VF's effects under weak grid conditions, and proposes a method which can improve both stability and anti-disturbance performance.

The paper is organized as follows. Section II analyses the effects of the VF. Section III proposes a method which incorporates a lead-lag compensator in the grid VF path to improve the VF's performance, and analyzes the design of the compensator. To verify the effects of the proposed method, the simulation and experiment results are presented in section IV. Section V concludes all the work.

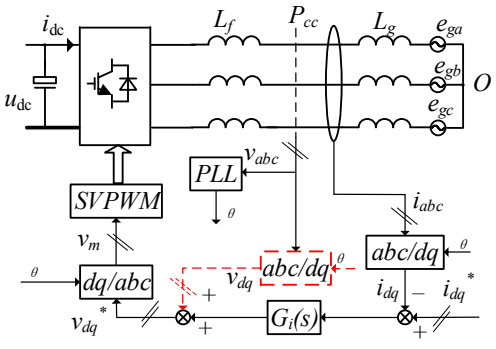


Fig.1 Structure of the three-phase L-filtered grid-tied inverter

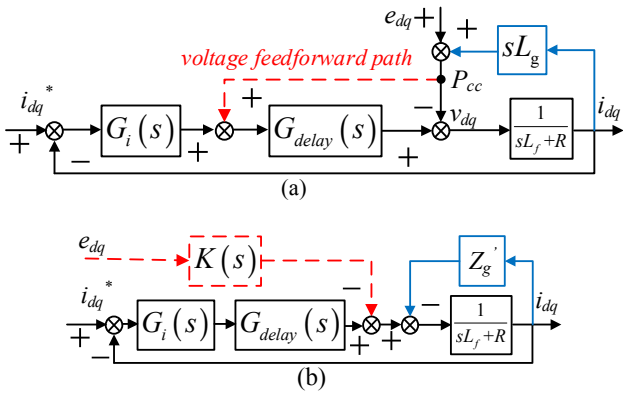


Fig.2 Control scheme of the grid-tied inverter (a) original scheme, (b) equivalent scheme

II. EFFECT OF VOLTAGE FEEDFORWARD UNDER WEAK GRID

A. Analysis of the effect of voltage feedforward under weak grid

The Fig. 1 shows the generic structure of the three-phase L-filtered grid-tied inverter with grid voltage feedforward control. The inverter is connected to the grid through an output filter L_f. The grid is equivalent to an ideal three-phase voltage sources e_{ga}, e_{gb} and e_{gc} with grid impedance L_g. u_{dc} denotes the constant dc bus voltage. Considering the effect of the delays and ignoring the influence of the PLL, the control scheme of the inverter is shown in Fig. 2(a). And it can be equivalent to Fig. 2(b).

$G_i(s)$ is the current PI regulator. $G_{delay}(s)$ represents computation delay and pulse-width modulation (PWM) delay introduced by digital control system, which is generally considered as $1.5T_s$, where T_s is the sampling period of the digital control system. The transfer functions $G_i(s)$ and $G_{delay}(s)$ can be expressed as:

$$G_i(s) = K_p + \frac{K_i}{s} \tag{1}$$

$$G_{delay}(s) = e^{-1.5sT_s} \tag{2}$$

Considering the effect of VF, the equivalent grid impedance Z_g' is:

$$Z_g' = K(s)sL_g \tag{3}$$

In consideration of the influence control delay, the effect of voltage feed-forward control can be expressed as (based on Pade approximation):

$$K(s) = (1-e^{-1.5sT_s}) \approx \frac{\frac{3}{2}sT_s}{1+\frac{3}{4}sT_s} \tag{4}$$

Unlike the LCL-filtered inverter, the L-filtered inverter is simpler in structure, so the root cause of the negative effect of VF is also much clearer. According to Fig. 2(b) and (2), if there is no control delay, which means $G_{delay}(s)$=1 and $K(s)$=0, the system stability and power quality will not be affected by grid impedance and the grid voltage. Therefore, control delay in VF path is the root cause of VF's negative effects.

However, as it is shown in Fig. 3(a) and (3), the equivalent grid impedance will exhibit negative resistance in low and middle frequency bands because of the delay in VF path. And this will result in a decrease of the system's Phase margin (PM).

In addition to stability influence, VF delay also affects the low order harmonic voltage suppression. Because of the delay in VF path, there is phase difference between the feed-forward component and the actual voltage. So the feed-forward component can't offset the effect of grid voltage and can't suppress the low order harmonic caused by grid harmonic voltage.

B. Case Study of Voltage Feedforward Effects

According to Fig. 2(b), the system stability and the harmonic suppression can be evaluated through the loop gain $L(s)$ and $F(s)$, which are given as follow:

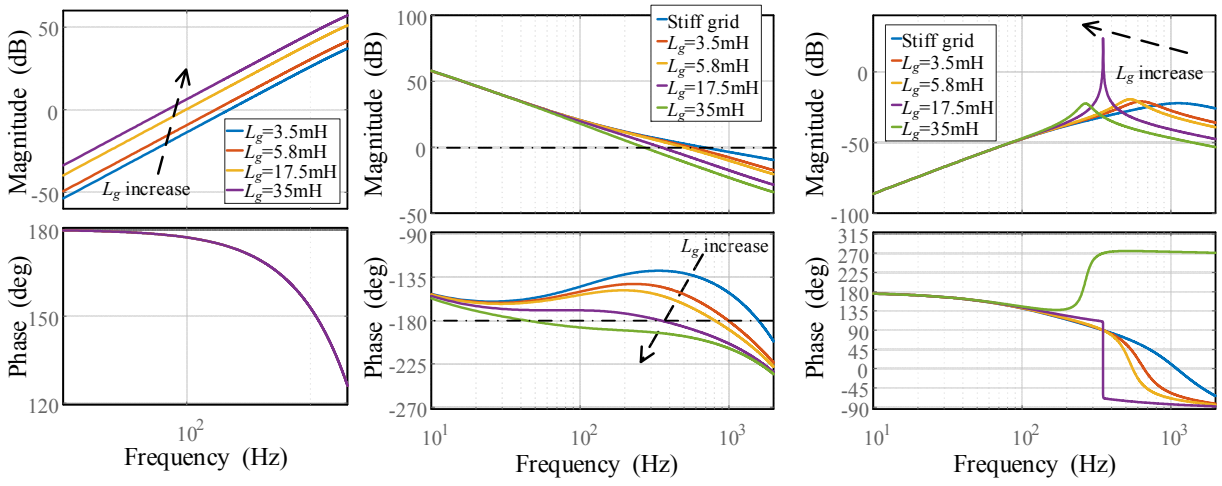
$$L(s)=G_i(s)G_{delay}(s)\frac{1}{sL_f+R+Z_g'} \tag{5}$$

$$F(s)=\frac{e_{dq}}{i_{dq}}=K(s)\frac{1}{G_i(s)G_{delay}(s)+sL_f+R+Z_g'} \tag{6}$$

The main parameters are listed in Table I.

TABLE Ⅰ. Main parameters of the grid-tied inverter

Symbol	*Value*	*Symbol*	*Value*
V_{dc}	350V	K_p	15
$V_g(rms)$	110V	K_i	12000
I	10A	f_o	50Hz
L_f	3.6mH	f_s	10000Hz
R	0.1Ω	L_g	17.5mH



(a) (b) (c)

Fig.3 Bode diagram of Z_g', $L(s)$ and $F(s)$ with different L_g (a) Z_g', (b) loop gain, (c) $F(s)$

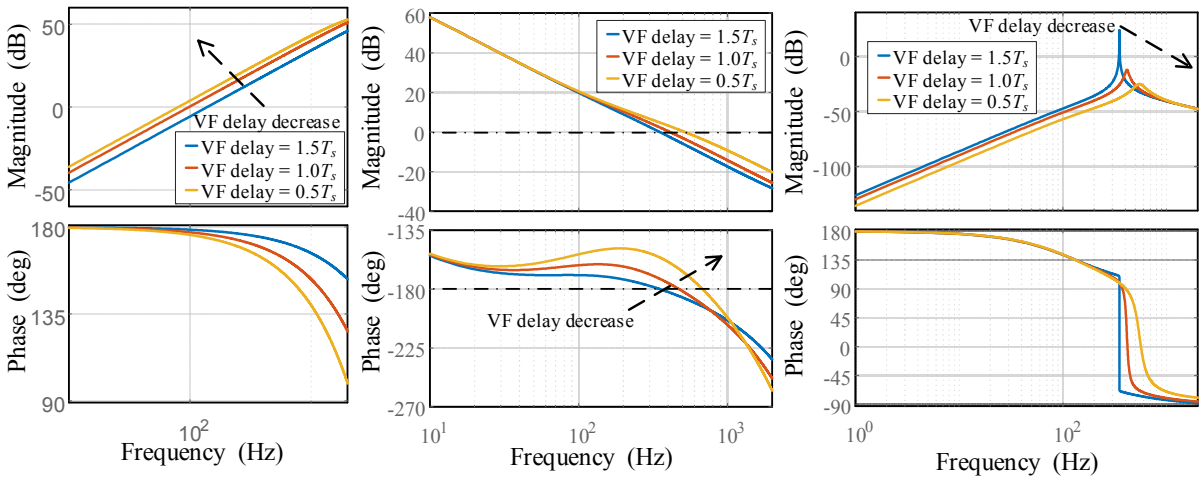


Fig.4 Bode diagram of Z_g', $L(s)$ and $F(s)$ with different VF delay (a) Z_g', (b) loop gain, (c) $F(s)$

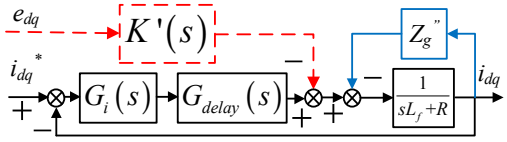


Fig.5 Equivalent control scheme of the L-filtered grid-tied inverter with compensated voltage feedforward control

Fig. 3 shows the bode diagram of Z_g', $L(s)$ and $F(s)$ with different L_g. As shown in Fig. 3(b), the PM of the system decreases when L_g increases. And according to Fig. 3(c), when L_g increases, the low order harmonics caused by grid voltage increase. And the weak grid might lead to resonance.

Fig. 4 shows the bode diagram of Z_g', $L(s)$ and $F(s)$ with different delay in VF path (delay in main path remains 1.5T_s, L_g=17.5mH). As shown in Fig. 4, the negative effects of VF on system stability and power quality would be weakened if the delay in VF path decreases.

III. Incorporate a Lead-lag Compensator in the Voltage Feedforward Path

According to the analysis and case study in section Ⅱ, the negative effects of VF could be weakened by offsetting the influence of delay in VF path. Lead compensator and lead-lag compensator are usually used to introduce phase lead to cancel the phase delay caused by control delay. But the low frequency gain and high frequency gain of lead compensator can't be unity at the same time. So there will be error in voltage feed-forward control with lead compensator in either low frequency band or high frequency band. And this might lead to other negative effects. The lead-lag compensator is expressed as:

$$G_{LL}(s)=\frac{1+T_1 s}{1+\alpha T_1 s}\frac{1+\beta T_2 s}{1+T_2 s}\ (\alpha>1,\ \beta>1) \tag{7}$$

If α = β, the compensator's low frequency gain and low frequency gain will be unity. Therefore, a method which incorporates a lead-lag compensator in the grid VF path (as shown in Fig. 2(a)) is proposed. It can improve the effect of VF by compensating the phase-lag in VF path caused by delay.

The equivalent control scheme of the three-phase L-filtered grid-tied inverter with compensated voltage feedforward control is shown in Fig. 5. Z_g'' is the equivalent grid impedance in consideration of the influence of lead-lag compensator. And it can be expressed as:

$$Z_g''=K'(s)sL_g \tag{8}$$

$$K'(s)=1-G_{delay}(s)G_{LL}(s)\approx\frac{\frac{3}{4}sT_s(k_0+k_1 s+k_2 s^2)}{(1+\frac{3}{4}sT_s)(1+\alpha T_1 s)(1+T_2 s)} \tag{9}$$

$$=K(s)\frac{2(k_0+k_1 s+k_2 s^2)}{(1+\alpha T_1 s)(1+T_2 s)}$$

where $k_0=2+\frac{4(\alpha-1)(T_1-T_2)}{3T_s}$, $k_1=(\alpha+1)(T_1+T_2)$

and $k_2=2\alpha T_1 T_2$.

A. The function of the lead-lag compensator in VF path

Fig. 6 shows the comparison on phase-frequency response of $L(s)$ and amplitude-frequency response of $F(s)$ between grid-tied inverters with traditional VF and with lead-lag VF. From Fig. 6, it can be seen that the inverter with lead-lag VF has better stability and ability of suppressing the low order harmonics.

The bode diagram of a generic lead-lag compensator is shown in Fig. 7. The compensator can introduce phase lead in VF path and compensate the phase delay caused by the control delays. If it compensate the phase delay at the frequency of the grid harmonic voltage, $K'(s)$ is close to 0 at the harmonic frequency. So, according to Fig. 5, the grid voltage harmonics won't result in current harmonics.

As discussed, the control delay will change the impedance characteristics of the equivalent grid impedance Z_g' and

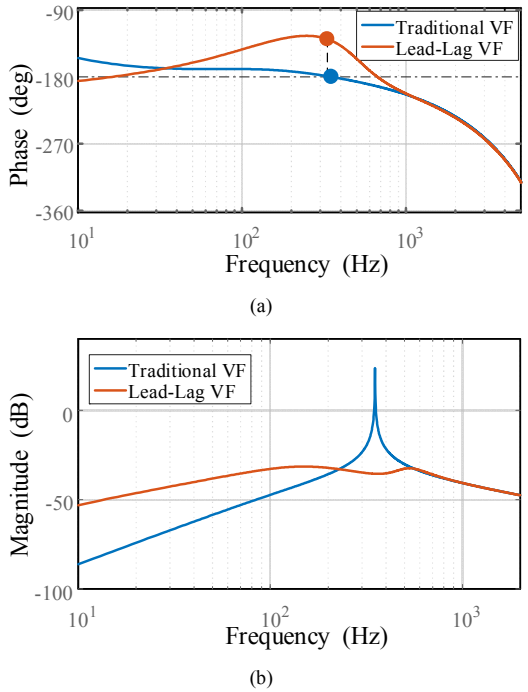


Fig.6 Comparison between traditional VF and Lead-lag VF. (a) phase response of L(s) (b) amplitude response of F(s)

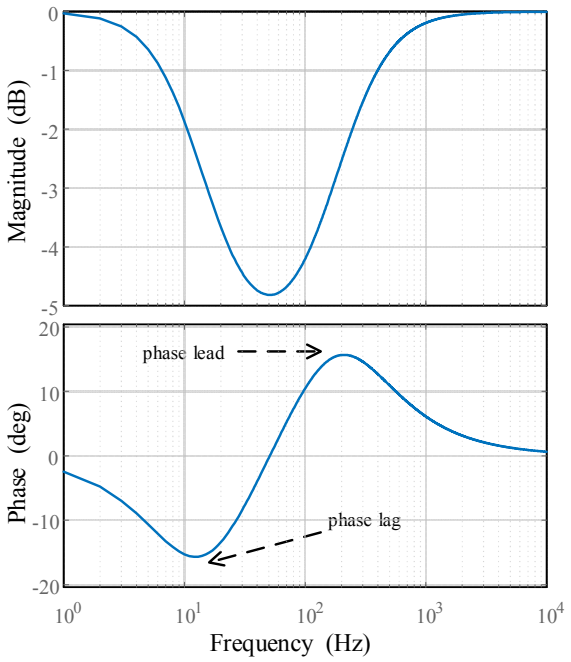


Fig.7 Bode diagram of a generic lead-lag compensator

result in decrease of the Phase margin. Fig. 8 shows the bode diagram of *K(s)* and *K'(s)* with different f_2, where $f_2 = \frac{1}{2\pi\sqrt{\alpha}T_2}$ (delay in main path remains $1.5T_s$, L_g=17.5mH). As shown in Fig. 8 and (9), the effect of the VF is changed by using the lead-lag compensator. And this reduces its negative impact on grid impedance and system stability.

B. The design of the lead-lag compensator in VF path

As shown in (7), there are four design parameters in lead-lag compensator. In this case, the high-frequency gain of the lead-lag compensator is designed to be unity, which means α must equal to β. So in fact there are only three design parameters.

Furthermore, based on the above analysis, the phase lag of the compensator will not affect the function of the compensator. So the design of the phase lag frequency f_1 has no difference with normal lead-lag compensators ($f_1 = \frac{1}{2\pi\sqrt{\alpha}T_1}$).

The design of α is related to the phase lead frequency f_2. If f_2 is decided, the parameter α is designed to make sure the introduced phase lead will compensate the phase delay caused by time delay at the selected frequency f_2. This can be expressed as (control delay is $1.5T_s$):

$$\alpha \approx \frac{2}{1-\sin(3\pi T_s f_2)} - 1 \tag{10}$$

Proper design of f_2 and α can improve the system stability and attenuate the current harmonics caused by grid voltage harmonics at the same time. The selection of f_2 need to balance the system stability improvement and grid current harmonic suppression performance.

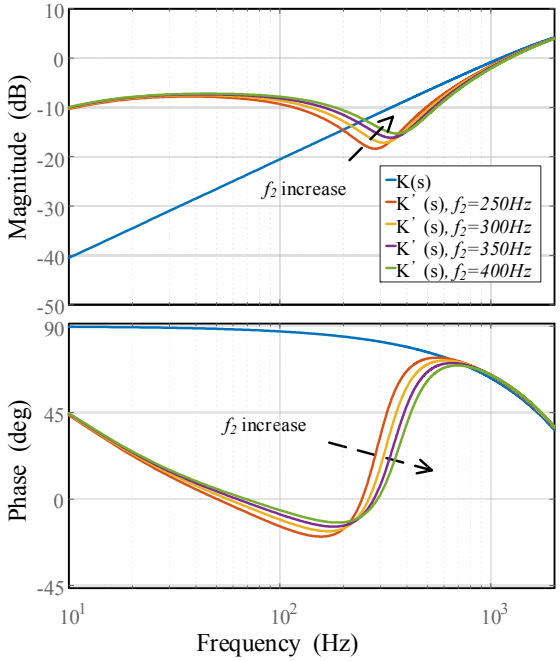


Fig.8 Bode diagram of *K(s)* and *K'(s)* with different f_2

a) System stability design

As is shown in Fig. 5 and (8)-(9), the relationship between Z_g'' and f_2 is very complicated. And this make it very difficult to establish the transfer function among PM and f_2 and get accurate design of f_2. But according to Fig. 8, the *K'(s)*'s phase lead in low and middle frequency band will

decrease if f_2 increase. In conclusion, the higher the compensator's phase lead frequency, the better the system stability.

b) Harmonics suppression design

Based on the analysis above, to improve the grid harmonics suppression, the lead-lag compensator has to offset the impact of control delay at frequency (f_r) of the grid voltage harmonic. So the phase lead frequency (f_2) has to be near to f_r. For example, if we take the suppression of 5th and 7th harmonics into consideration, the corresponding f_r is about 300Hz in *dq* coordinate. So the designed f_2 is near to 300Hz.

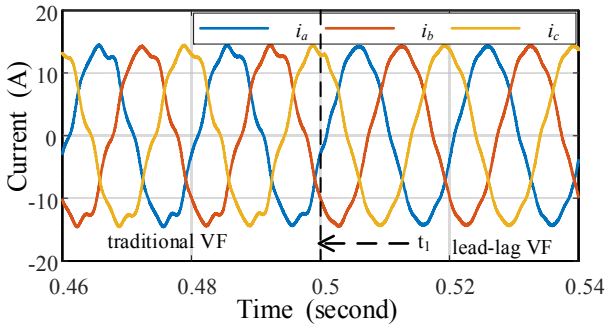
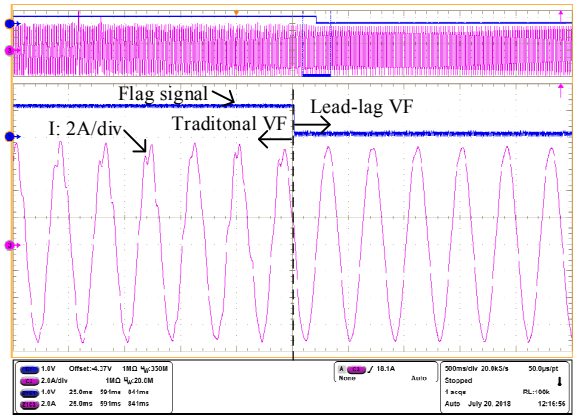
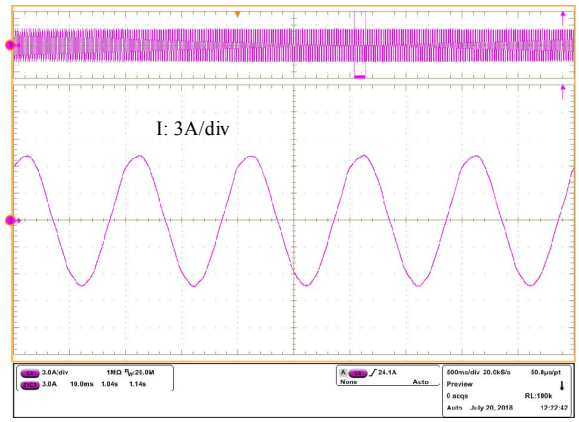


Fig.9 Lead-lag VF effect on power quality



(a)



(b)

Fig.10 Experiment results (stability) (a) VF changes from traditional VF to lead-lag VF (b) steady state of grid current

IV. SIMULATION AND EXPERIMENT RESULTS

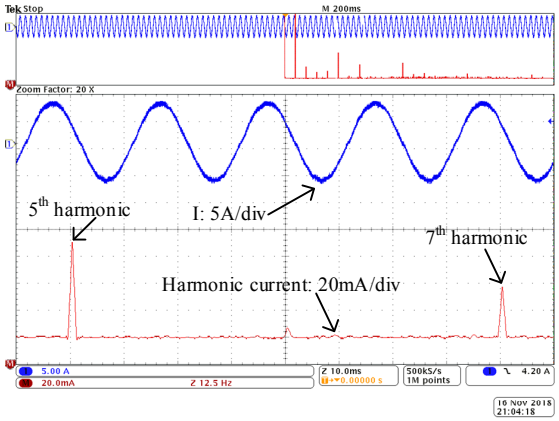
A. Simulation result

To verify the effect of lead-lag VF on suppressing the harmonics caused by grid-voltage, a model of the grid-tied inverter with lead-lag VF is set up in MATLAB/Simulink. Parameters of simulation are shown in Table I. To make sure the system is stable with traditional VF, L_g = 8mH and K_i = 9000. For the lead-lag compensator G_{LL}(s), α = β = 1.93, T_1 = 0.0159, T_2 = 0.000418.

10% 5th and 7th order voltage harmonic are injected into the grid in this simulation. The simulation result is presented in Fig. 9. Before t_1=0.5s, the inverter works with traditional VF, after t_1, it works with lead-lag VF. As is shown in Fig. 9, after t_1, the quality of the grid current is better. And Table Ⅱ is the result of FFT analysis. As can be seen from Table II, when VF changes from traditional VF to lead-lag VF, the amplitude of low order current harmonics is smaller. And this proves that the proposed method has better performance of low order current harmonics suppression.

TABLE Ⅱ. FFT analysis of simulation result

Order	*Traditional VF*	*Lead-lag VF*
fundamental	10A	10A
5^{th}	0.41A	0.21A
7^{th}	0.56A	0.24A



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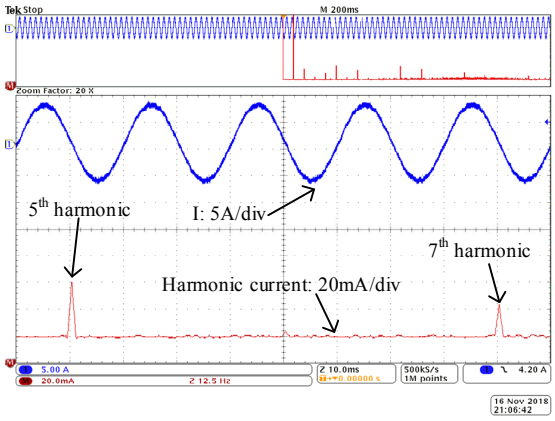

(b)

Fig.11 Grid current and FFT analysis results (a) traditional VF (b) lead-lag VF

B. Experiment results

1) Stability improvement

This part of the experiment will prove that the lead-lag VF can improve the system's stability. In this experiment, U_{dc}=100V, U_g(rms)=37V, $I_{g(rms)}$=5A, L_g =14.2mH, and the rest of the experimental parameters are the same as the simulation parameters. According to the analysis in section Ⅱ. The PM of the inverter with traditional VF is very small. And the experiment result is shown in Fig. 10. In Fig. 10(a), the blue line is the flag signal, the purple line is the current. When flag signal changes from 1 to 0, the VF changes from traditional VF to lead-lag VF, and the stability of the system increases. Fig 10(b) shows the steady state of the grid current of the inverter with lead-lag VF.

2) Low order current harmonics suppression

This part of the experiment will verify that the proposed VF method has better low order harmonics suppression. To avoid the system stability's influence on the suppression, the experiment is carried out under strong grid condition. The grid current and its FFT analysis results is shown in Fig. 11. According to Fig. 11(a), in the system with traditional VF, the 5^{th} and 7^{th} harmonics of grid currents is about 71mA and 38mA. And in Fig. 11(b), the 5^{th} and 7^{th} harmonics of the currents is about 40mA and 24mA. This proves that the proposed method could help reduce the low order current harmonics which is caused by grid voltage harmonics by almost half.

V. CONCLUSIONS

This paper analyzes the effects of VF on grid-connected inverter system stability and ability of suppressing the low order current harmonics caused by grid-voltage. The analysis shows that the traditional VF has negative effects on system stability and suppression of low order harmonics under weak grid. It also points out that the negative effect can be weakened by offsetting the influence of control delay in VF path as the control delay is the fundamental cause of the VF's negative effects. Therefore, the method that incorporates a lead-lag compensator in the grid VF path is proposed. The proposed method improves both the system stability and the ability of suppressing the low order current harmonics. Simulation and experiment results verified the effectiveness of the proposed lead-lag VF.

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