Single-Submodule Open-Circuit Fault Diagnosis for a Modular Multi-level Converter Using Artificial Intelligent-based Techniques

Ziwei Ke, Jianyu Pan, Risha Na, Karun Potty, Julia Zhang, Jin Wang, Longya Xu
School of Electrical and Computer Engineering
The Ohio State University
Columbus, OH, USA
ke.123@osu.edu

Abstract— **Modular multi-level converters (MMCs) are one of the promising topologies in recent years for medium or high voltage applications. They are considered as the next generation DC/AC converters for medium/high voltage (MV/HV) motor drive applications due to their transform-less structures, high efficiency and modularity. Reliability is one of the most important challenges in MMCs, since a large number of power switching devices are used and each of these devices can be considered as a potential failure point. It is significant to detect and locate the fault accurately and apply appropriate protections in a timely manner. This paper investigates the behavior of the failure submodules and healthy submodules and use artificial neural network (ANN) classification algorithms for single-submodule open-circuit fault diagnosis. The ANN algorithm is implemented in field programmable gate array (FPGA) and the ANN parameters training is completed offline in Matlab. Experimental results of the proposed fault diagnosis for a single-module open-circuit fault are presented in this paper.**

Keywords: Multi-level converters; artificial neural networks; artificial intelligent; modular multi-level converters; submodule open-circuit fault; fault diagnosis, FPGA.

I. INTRODUCTION

Multi-level converters are typically applied for medium voltage (MV) and high voltage (HV) high power applications. Commercial multi-level converter products have been demonstrated for high voltage DC (HVDC) transmission [1], ship propulsion and generation [2], train traction [3], high power wind energy conversion [4], and medical resonance imaging (MRI) [5], etc. The most popular circuit topologies for these multi-level converters include the neutral point clamp topology and modular multi-level converters (MMCs), etc. MMCs have identical units, called submodules, stacked on top of each other to increase the system voltage rating. The modular structure keeps the manufacturing of the converters simple and the control for each submodule is also similar. MMCs are considered as the next generation DC/AC converters for MV/HV variable speed drive applications due to their transform-less structures, high efficiency, and modularity [6-14].

Failures of switching devices can be classified into short-circuit faults and open-circuit faults. The short-circuit faults are the highest priority faults as the system needs to be shut down immediately to prevent over current. In this paper, single-submodule open-circuit faults are investigated. Over the past decade, many open-circuit fault diagnostic methods have been proposed and investigated for MMC applications using model-based, signal-based and AI-based methods. Shao proposed a submodule fault detection and localization method based on a sliding-mode observer, which compares the estimated state variables with the measured ones [15,16]. This method is able to detect the fault with high accuracy, but it has higher requirement on the controller due to the heavy computation load of the model. Li in [17] and Hu in [18] reported similar methods to detect the fault using a state observer and the characteristics of the fault behaviors of MMC. Xu in [19], Sen in [20], Yang in [21], and Ghazanfari in [22] detected and located open-circuit faults using model computation. The model computation method also has the drawbacks of heavy computational load for the microcontrollers. Several other fault diagnosis papers propose the fault detection and localization method by adding additional hardware and analyzing the frequency behavior of the output voltages [23-31]. AI-based techniques for fault diagnosis are also implemented in machine drive applications [32-36]. Khomfoi in [37, 38] proposed a fault detection method using neural network algorithm for multilevel converters. Kiranyaz in [39] proposed a real-time submodule open-circuit fault detection and identification using ANN algorithm.

Compared to model-based and signal processing-based fault diagnosis methods, AI techniques don't require any mathematical models, offer extra degree of freedom to solve a nonlinear problem, and can improve the accuracy and stability with more training data from increased number of the experiments. AI-based algorithms can be widely used in power electronics and drive systems because of advanced development of microcontroller systems and the capability of big data processing techniques.

There are several different ways to implement the ANN algorithm. Two main approaches including software-based such as Matlab, Python, and hardware-based such as digital signal processors (DSPs), graphical processing units (GPUs), and field programmable gate arrays (FPGAs). Li in [40] proposes a coordinate rotation digital computer algorithm to realize the ANN algorithm in FPGAs. A basic ANN algorithm

is also implemented in FPGAs [41]. Other FPGA implementations of ANN can be also found in [42-44]. The parallel structure of FPGAs makes themselves as good advantages to implement the ANN algorithm, which can finish the computation in a very short time. Therefore, hardware-based ANNs have more advantages than that of software-based.

The contributions of his paper are to develop a submodule open-circuit fault diagnosis including fault detection and localization methods using artificial neural network (ANN) classification algorithms, and use the experimental test to verify the proposed methods. The ANN method only take account into the single-submodule open-circuit fault scenario. Multiple submodule open-circuit faults are not considered in this paper. This paper is organized as follows: Section II reviews the circuit and basic equations of MMCs. Section III presents the characteristics of submodule open-circuit fault of MMCs. Section IV introduces the principle of submodule open-circuit fault diagnosis based on ANN algorithms. The details of implementing the ANN into FPGA and ANN parameters training are also discussed in this section. Section V presents experimental test results to verify the proposed algorithm using a three-phase load.

II. RIVEW OF MMC CIRCUIT AND MODELING

Fig.1 shows a three-phase MMC inverter connected to an RL load. This MMC circuit consists of two arms per phase leg, called the upper and lower arms. Each arm includes *N* identical submodules in series and an inductor called the arm inductor. The purpose of the arm inductor is to suppress the high-frequency components in the arm current. The commonly used submodule topologies include the half-bridge or chopper-cell, the full-bridge or bridge-cell, the unidirectional cell, the clamp-double circuit, the three-level converter circuit, and the five-level cross-connected circuit. The most popular submodule topologies are the full-bridge and half-bridge structures. The MMC in this work is based on the half-bridge topology using two switches, which results in a lower number of components and higher efficiency for the MMC compared to other topologies.

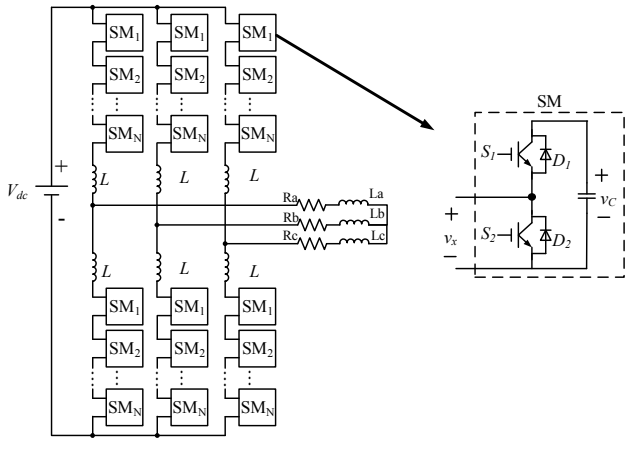

Fig. 1. A three-phase MMC with a three-phase load.

Fig. 2 shows the half-bridge submodule structure and its three operation conditions. The two switches of each submodule are a complimentary pair. The output voltage of a submodule, v_x, is either equal to its capacitor voltage v_C or zero. In state 1, the top switch is on and the bottom switch is off. In this case, the output voltage of the submodule, v_x, is equal to the capacitor voltage v_C. In state 2, the top switch is off and the bottom switch is on. In this case, the submodule is shorted, and the output voltage is zero. State 1 is called the inserted state as the submodule capacitor voltage contributes to the output of this entire phase leg. State 2 is the bypassed mode as the submodule allows current to flow through without providing any voltage to the output. The dead-time state occurs between states 1 and 2 when both switches are off and the output voltage of the submodule depends on the direction of the current. The positive direction of the submodule current is defined in Fig. 2. During dead-time, the submodule output voltage equals the capacitor voltage for positive current and zero for negative current.

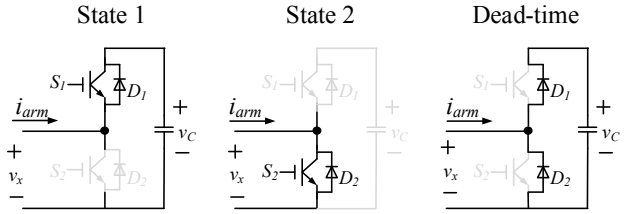

Fig 2. Three operation conditions of a submodule.

The MMC of this work is for 4.16-kV industrial drive applications. Six 1.7-kV SiC MOSFETs are used for each arm considering the voltage requirement and the commercially available SiC power electronic device products during the design phase.

In a three-phase MMC system, the upper and lower arm currents of phase *j*, where *j* = *a, b, c*, can be expressed as:

$$i_{p,j} = \frac{i_{dc}}{3} + i_{circ,j} + \frac{i_j}{2} \quad (1)$$

$$i_{n,j} = \frac{i_{dc}}{3} + i_{circ,j} - \frac{i_j}{2} \quad (2)$$

where $i_{circ,j}$ represents the circulating current within the phase *j*, i_j is the phase *j* output current, and i_{dc} is the DC link current. The circulating current, based on (11) and (12), is given by:

$$i_{circ,j} = \frac{i_{p,j}+i_{n,j}}{2} - \frac{i_{dc}}{3} \quad (3)$$

The phase output current can be calculated based on (1) and (2):

$$i_j = i_{p,j} - i_{n,j} \quad (4)$$

The output voltage v_o of any phase can be expressed by subtracting (7) from (6):

$$v_o = \frac{v_{n,j}-v_{p,j}}{2} - \frac{1}{2} L_{arm} \frac{d(i_{p,j}-i_{n,j})}{dt} = \frac{v_{n,j}-v_{p,j}}{2} - \frac{1}{2} L_{arm} \frac{di_j}{dt} \quad (5)$$

$$L_{arm} \frac{di_{circ,j}}{dt} = \frac{1}{2} V_{dc} - \frac{v_{p,j}+v_{n,j}}{2} \quad (6)$$

where $v_{cp,j}$ and $v_{cn,j}$ are the individual submodule capacitor voltages of the upper and lower arms. $n_{p,j}$ and $n_{n,j}$ are the number of inserted submodules of the upper and lower arms.

It can be seen from (5) that the output voltage is related to the voltage difference between the upper and lower arms, the arm inductance, and the output current. Eq. (6) can be also obtained by adding the two voltage equations. This equation explains the necessity of the arm inductors. Without the arm inductor, there would be huge circulating currents in the DC bus and three phase legs as the total voltage of each individual phase leg may not be equal to the bus voltage for an MMC. It is critical to control the total voltage of each phase leg to be as close to the bus voltage as possible to reduce the circulating currents.

The voltage drops across the arm inductors are much smaller than the submodule voltages if the phase leg voltages are well controlled. The upper arm voltage $v_{p,j}$ and the lower arm voltage $v_{n,j}$ can be simplified by ignoring the voltage drop across the arm inductors:

$$v_{p.j} = \frac{1}{2}V_{dc} - v_{o.j} \tag{7}$$

$$v_{n.j} = \frac{1}{2}V_{dc} + v_{o.j} \tag{8}$$

III. Single-Submodule Open-Circuit Fault Characteristics

A submodule in the MMC may experience various types of faults. There are two types of switching device faults, i.e. short-circuit and open-circuit faults, which can be considered in practical applications and hardware implementations. Since the short-circuit fault detection and protection is normally integrated into the gate driver circuit, only submodule with switching device open-circuit faults is discussed in this research proposal. Fig. 3 shows the circuit configurations of the submodule in normal operation and three open-circuit fault conditions. The three types of open-circuit faults for a submodule include upper device open-circuit fault (type I), lower device open-circuit fault (type II) and both devices open-circuit fault (type III).

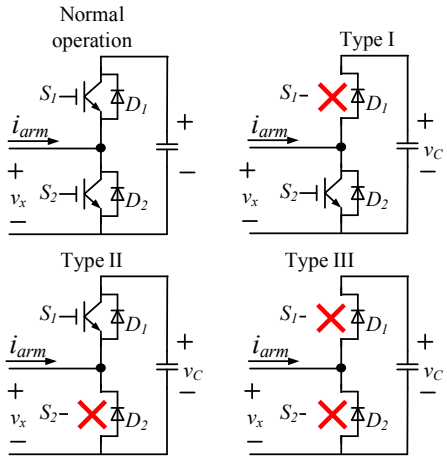

Fig. 3. Three types of submodule open-circuit fault.

In order to have a better and more clear understand of the voltage and current value when the submodule is operating at normal operation, type I fault, type II fault, and type III fault conditions, Table I-IV show the current path and output voltage of the submodule based on the Fig. 3.

Table I. Normal Operation

i_{arm}	S_1	Current flows through	v_x
>0	1	D_1 & Cap	v_c
	0	S_2	0
<0	1	S_1 & Cap	v_c
	0	D_2	0

Table II. Type I Fault

i_{arm}	S_1	Current flows through	v_x
>0	1	D_1 & Cap	v_c
	0	S_2	0
<0	1	D_2	0
	0	D_2	0

Table III. Type II fault

i_{arm}	S_1	Current flows through	v_x
>0	1	D_1 & Cap	v_c
	0	D_1 & Cap	v_c
<0	1	S_1 & Cap	v_c
	0	D_2	0

Table IV. Type III Fault

i_{arm}	S_1	Current flows through	v_x
>0	1	D_1 & Cap	v_c
	0	D_1 & Cap	v_c
<0	1	D_2	0
	0	D_2	0

In summary, the failure characteristics can be summarized into the following equations. S_1 is the switching function of the top device of the submodule, v_C is the voltage of the capacitor, and v_x is output voltage of the submodule.

During the normal operation, both devices are healthy, and the output voltage v_x of the submodule will be:

$$v_x = \begin{cases} S_1 \cdot v_C, & i_{arm} \geq 0 \\ S_1 \cdot v_C, & i_{arm} < 0 \end{cases} \tag{8}$$

In type I condition, when the arm current is greater than 0, the submodule is working normally. The current flows through the diode D_1 and the capacitor when the switching signal is 1, while it flows through the bottom switch S_2 when the switching signal is 0. When the arm current is less than 0 and the switching signal is 1, the arm current is forced to go through D_2 instead of the capacitor and S_1. Hence, the submodule voltage is equal to 0 under this condition and the submodule voltage can be described as

$$v_x = \begin{cases} S_1 \cdot v_C, & i_{arm} \geq 0 \\ 0, & i_{arm} < 0 \end{cases} \tag{9}$$

In type II bottom device fault condition, when the arm current is greater than 0 and the switching signal is 0, it is

forced to circulate through D_1 and the capacitor instead of S_2. Hence, the submodule voltage is equal to the capacitor voltage v_C. Therefore, the submodule voltage can be expressed as

$$v_x = \begin{cases} v_C, & i_{arm} \geq 0 \\ S_1 \cdot v_C, & i_{arm} < 0 \end{cases} \quad (10)$$

For type III both device fault condition, since all the switches are failure, the arm current can only be conducted through the diodes. In this case, the submodule voltage is

$$v_x = \begin{cases} v_C, & i_{arm} \geq 0 \\ 0, & i_{arm} < 0 \end{cases} \quad (11)$$

In general, from (9) to (11), the submodule with switching device open-circuit faults results in capacitor over-voltage problems. The capacitor voltages of the failure submodules are always higher than those in the healthy submodules. The open-circuit can lead to malfunction and safety of the entire MMC system. Hence, it is significant to detect and locate the fault as soon as possible so that the fault tolerant operation can be activated on time.

Fig. 4 shows the experimental submodule capacitor voltages waveform in per unit of an arm of the MMC during the normal operation and failure operation when a single submodule open-circuit fault happens. The dc bus voltage is 700 V, fundamental frequency is 800 Hz, and the modulation index is 0.5. During the normal operation, as seen from the top-left figure, all the capacitor within the same arm follow each other well and the voltage difference is minimum. Top-right figure shows the capacitor voltage waveforms when type I fault is triggered. The figures on the bottom-left and bottom-right show the type II and III fault characteristics respectively. The data are all sampled from each submodule, the sampling rated in the figure is 5 kHz.

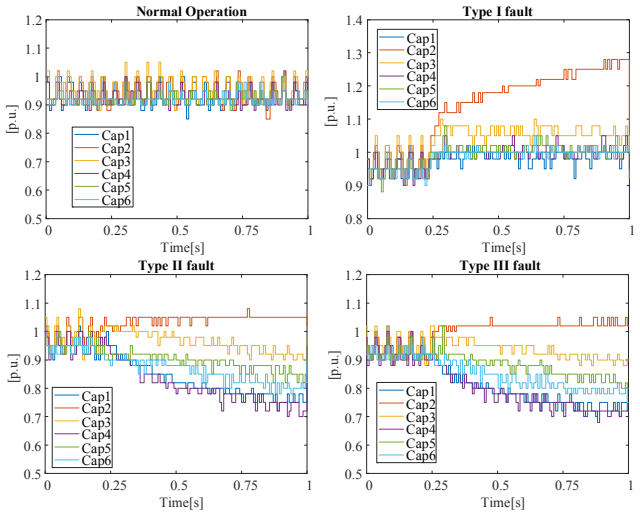

Fig. 4. Test data of arm submodule capacitor voltages of normal operation, type I fault, type II fault and type III fault.

In order to analyze the capacitor voltage waveforms by using ANN algorithm, all the failure module capacitor voltage waveforms are extracted and treated as the inputs of the ANN.

These sampled failure voltage data will be the input and the ANN algorithm can determine the fault types based on the patterns of these waveforms. The details of the proposed algorithm will be introduced in the next section.

IV. Principle of Single-Submodule Open-Circuit Fault Diagnosis Using Artificial Neural Network Algorithm

Fig. 5 shows the program flow diagram of the overall ANN-based single-submodule open-circuit fault diagnosis algorithm.

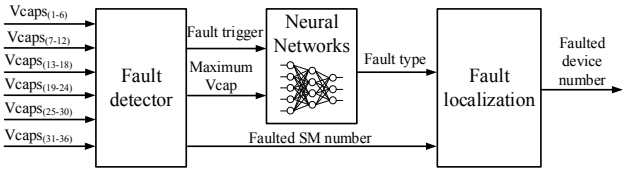

Fig. 5. Overall single-submodule open-circuit fault control diagrams.

The fault detector samples all the submodule capacitor voltages for a period of time. In this paper, 36 submodules are used in the MMC configuration with 6 submodules of each arm. The fault detector reads all the capacitor voltage data and will determine if there is a fault or not. Based on the discussion of the failure submodule capacitor voltage characteristics, the faulted submodule capacitor voltage is higher than that of the healthy submodules.

In the fault detector, the open-circuit fault will be triggered if one of the capacitor voltages keeps at highest value for a certain time. The fault detector generates the failure capacitor voltage waveforms and send them to the ANN function. The program flow diagram of the detection method is presented in Fig. 6.

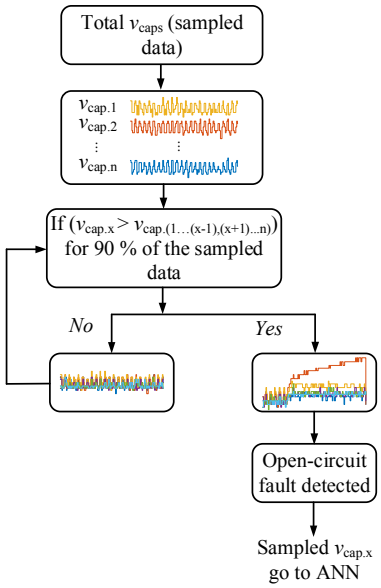

Fig. 6. Program flow diagram of fault detector.

The ANN algorithm for single-submodule open-circuit fault detection and localization is presented in Fig. 7. The whole thing is implemented in FPGA by using IEEE 754 single-precision 32-bit floating point multiplications and additions. The input sampled capacitor voltage data will be saved as a $n\times1$ vector, where n can be defined by user or system requirements. Two layers are used for the neural networks. Hence, two matrices of parameters $\boldsymbol{\Theta}_1$ and $\boldsymbol{\Theta}_2$ are used for the calculations. These two matrices are optimized by training offline through optimizing the cost function in Matlab, which is shown in Fig. 8. The failure submodule capacitor voltage data is stored and applied as the input of the data training. Back propagation algorithm is used to calculate the optimal value of the neuron weight matrices and achieve the minimum value of the cost function $J(\Theta)$. The logic sigmoid function is used to generate a normalized result between 0 and 1, where the input is the multiplication of the data matrix and the parameter matrix. The first layer of the ANN is the sigmoid function of the input data matrix $\mathbf{X}$ and neuron weight $\boldsymbol{\Theta}_1$, which generates the middle layer matrix $\boldsymbol{a}_{(m\times1)}$. The output layer $\boldsymbol{h}_{\boldsymbol{\Theta}(k\times1)}$ is generated by applying the similar function of the first layer. At the end, for the application in this paper, k is defined as 3, due to the three types of the submodule open-circuit faults. The output vector of the ANN will be a 3×1 matrix containing the probability of each fault type. The maximum value of the matrix corresponds to the estimation of the fault types. As shown in Fig. 7, P_1 represents the probability of fault type I, P_2 is the probability of fault type II, and P_3 is fault III. However, in the real-time application in the experiment, type II and III cause similar failure submodule capacitor voltage waveforms as shown in Fig. 4. The ANN training finds a difficulty to distinguish the difference between fault II and III. Only type I of the single-submodule open-circuit fault can be solved and proceed to the reconfiguration control by passing the failure submodule. Therefore, ANN combines type II and III to a same class. The output vector of the ANN will be a 2×1 matrix.

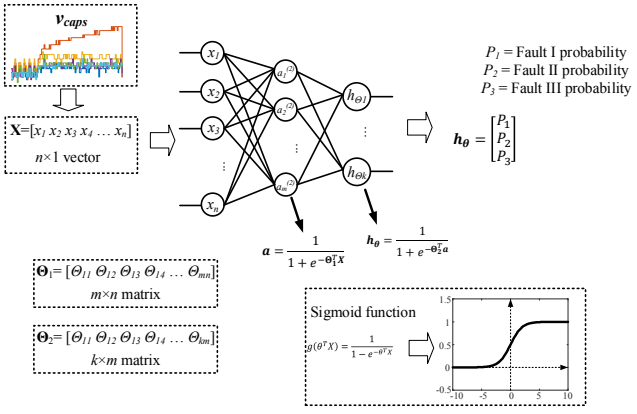

Fig. 7. Data processing of ANN in FPGA.

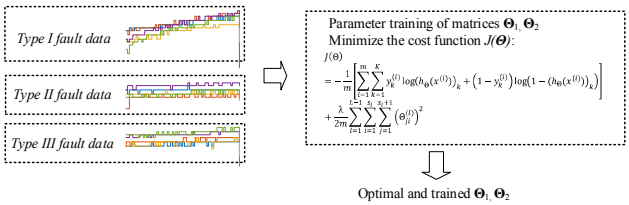

Fig. 8. Data training of ANN.

The standard way to implement the logic sigmoid function in FPGA is using a look-up-table (LUT) since the sigmoid function is a non-linear function so that it can reduce the usage of logic elements of the hardware. Another method to simplify the process of the sigmoid function is linearizing the function. Fig. 9 below shows the original sigmoid function and the linearized sigmoid function.

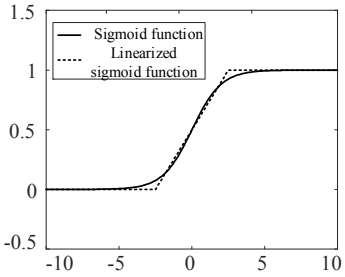

Fig. 9. Logic sigmoid function and linearized sigmoid function.

The linearized sigmoid function can be presented as

$$g(\Theta^T X)=\begin{cases}0, & \Theta^T X<-2.5\\ 0.2\times\Theta^T X+0.5, & -2.5\le\Theta^T X\le 0\\ 1 & \Theta^T X>2.5\end{cases}$$

The architecture of ANN process in FPGA is presented in Fig. 10. The parameters are the two trained matrices $\boldsymbol{\Theta}_1$ and $\boldsymbol{\Theta}_2$, and the input data vector is the sampled failure submodule capacitor voltage values. Floating point multiplier, adder and linearized sigmoid function are used to process the matrix computation.

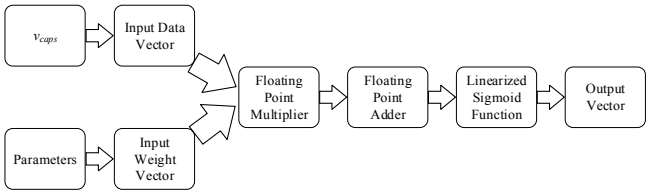

Fig. 10. ANN implementation in FPGA.

V. Experimental Verifications

Experimental tests on a three-phase MMC with a three-phase RL load have been done to verify the proposed open-circuit fault diagnosis algorithm. The experimental tests were done on a 1-MVA 7-kV 7-level three-phase MMC drive system using 1.7-kV, 250-A SiC MOSFETs. The power and voltage ratings are based on the system requirements of an on-going project in our research center. The objective of the

project is to demonstrate the MMC technology using new SiC power electronics devices. During the design stage of this MMC, only 1.7-kV SiC MOSFETs were available. Based on the power/voltage rating requirements and the commercially available SiC power semiconductors during the design stage of the MMC, the 7-level structure was selected for the prototype.

The entire MMC has 36 half-bridge submodules. The converter controller includes a DSP (Texas Instrument TMSF28377D) an FPGA (Altera Cyclone IV EP4CE115F29C7N). The MMC system level controls including the current close loop control and low frequency control were implemented in the DSP. The voltage sorting and PWM generation were implemented in the FPGA due to a large number of submodules. Fig. 11 shows the hardware system of the MMC, controller circuit, and submodule circuit.

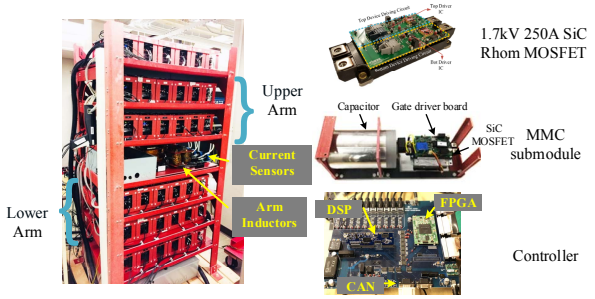

Fig. 11. 1-MVA 7-kV 7-level MMC test setup.

Table V shows the key experimental parameters for the MMC system for verifying the proposed single-submodule open-circuit fault diagnosis using ANN algorithm. The dc bus voltage is 700 V, modulation index is 0.5, and the output fundamental frequency is 800 Hz.

Table V. Key experimental parameters

Parameters	Values
Number of submodules	36
submodule capacitance	620 μF
Load Inductance	1.7 mH
Load Resistance	0.1 Ω
DC-link Voltage	700 V
Output Current Magnitude	20 A
Output Frequency	800 Hz

Experimental test using the 1-MVA MMC inverter platform were performed to verify the proposed single-submodule open-circuit fault diagnosis algorithm. Fig. 12 shows the test results by generating the type I fault for random selected two different submodules. Since the ANN parameter training needs a large number of experimental tests to get different voltage data, the three different types of fault estimation are not accurate yet and it needs more tests and training.

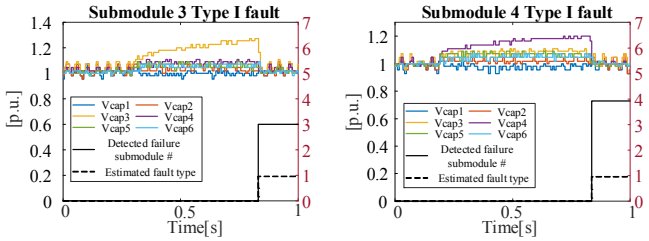

Fig. 12. Experimental results of single-submodule open-circuit fault detection and localization.

Three of the subplots show the submodule #3 open-circuit fault and the rest of the plots show the fault voltage waveform of submodule #4. In Fig. 12, six submodule capacitor voltages are in colors, solid black line represents the detected the submodule number of which has the open-circuit fault, and the dash line is the estimated fault type of the failure submodule. By the time when the fault is detected, the type of the fault is generated as well.

In the experimental test, the open-circuit fault is generated by disable the PWM signals of the corresponded switching device. In order to protect the drive system, once the fault is detected, the PWM signals of that device will be enabled again. Hence, the capacitor voltages become balanced once the fault is detected and recognized. The detection time of the submodule open-circuit is around 0.5 seconds since the sampling rate of the fault detection is 50 Hz. The purpose of the test in this paper is to verify the open-circuit fault diagnosis algorithm. For the future work, the sampling rate of the fault analysis system will be increased to reduce the detection time.

VI. Conclusion

This paper investigates a new open-circuit fault diagnosis algorithm based on the ANN classification method. Comparing to other fault diagnosis methods such as signal-processing based, and model based, ANN method provides several advantages such as mathematical model free and less development time. The detection method is based on the characteristics of the faulted submodule capacitor voltage comparing to that of other healthy submodules, and the localization method is based on the waveform pattern of the faulted submodule capacitor voltage. Experimental results verify the proposed single-submodule open-circuit fault diagnosis algorithm by using a DSP+FPGA controller. All three type of fault classification will be updated in the future publications. This paper only studies the single-submodule open-circuit fault during the steady state at 800 Hz. Further investigations will cover all three fault classifications, multiple-submodule open-circuit faults and reconfiguration controls.

References

[1] M. Davies, M. Dommaschk, J. Dorn, J. Lang, D. Retzmann, D. Soerangr, "HVDC PLUS – Basics and Principle of Operation," SIEMENS brochure, link: https://www.energy.siemens.com/br/pool/br/transmissao-de-

energia/transformadores/hvdc-plus-basics-and-principle-of-operation.pdf

[2] "ABB Drives for Marine Medium Voltage Drives for Reliable and Efficient Operations at Sea," ABB brochure, link: https://library.e.abb.com/public/2e7b508ea530471ac125785b00446c95/Marine%20brochure%20RevB_lowres.pdf

[3] U. Henning, R. Hoffmann and J. Hochleitner, "Advanced static power converter and control components for TRANSRAPID maglev system," *Proceedings of the Power Conversion Conference-Osaka 2002 (Cat. No.02TH8579)*, Osaka, Japan, 2002, pp. 1045-1049 vol.3.

[4] "PCS 6000 for large wind turbines Medium voltage, full power converters up to 9 MVA," ABB borchure, link: https://new.abb.com/docs/default-source/ewea-doc/pcs6000wind.pdf?sfvrsn=2

[5] P. Venkatesa, "System and Method for Controlling Current in Gradient Coil of Magnetic Resonance Imaging System," US patent US20110074413A1, Sept. 29, 2009.

[6] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *in IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4-17, Jan. 2015.

[7] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *in IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 37-53, Jan. 2015.

[8] S. Debnath, J. Qin and M. Saeedifard, "Control and Stability Analysis of Modular Multilevel Converter Under Low-Frequency Operation," *in IEEE Transactions on Industrial Electronics*, vol. 62, no. 9, pp. 5329-5339, Sept. 2015.

[9] M. Hagiwara, K. Nishimura, and H. Akagi, "A Medium-Voltage Motor Drive With a Modular Multilevel PWM Inverter," *in IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1786-1799, Jul. 2010.

[10] M. Hagiwara, I. Hasegawa and H. Akagi, "Start-Up and Low-Speed Operation of an Electric Motor Driven by a Modular Multilevel Cascade Inverter," *in IEEE Transactions on Industry Applications*, vol. 49, no. 4, pp. 1556-1565, July./Aug. 2013.

[11] J. Korn, M. Winkelnkemper and P. Steimer, "Low output frequency operation of the Modular Multi-Level Converter," *IEEE Energy Conversion Congress and Exposition*, Atlanta, GA, 2010, pp. 3993-3997.

[12] A. Antonopoulos, L. Ängquist, S. Norrga, K. Ilves, L. Harnefors and H. Nee, "Modular Multilevel Converter AC Motor Drives With Constant Torque From Zero to Nominal Speed," *in IEEE Transactions on Industry Applications*, vol. 50, no. 3, pp. 1982-1993, May-June 2014.

[13] S. P. Engel and R. W. De Doncker, "Control of the Modular Multi-Level Converter for minimized cell capacitance," *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, Birmingham, 2011, pp. 1-10.

[14] D. A. Guzman P., and J. C. Balda, "The Impact of High-Voltage and Fast-Switching Devices on Modular Multilevel Converters," *in IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2013, pp. 2171-2177.

[15] S. Shao, P. W. Wheeler, J. C. Clare and A. J. Watson, "Open-circuit fault detection and isolation for modular multilevel converter based on sliding mode observer," *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, 2013, pp. 1-9.

[16] S. Shao, A. J. Watson, J. C. Clare and P. W. Wheeler, "Robustness Analysis and Experimental Validation of a Fault Detection and Isolation Method for the Modular Multilevel Converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3794-3805, May 2016.

[17] B. Li, S. Shi, B. Wang, G. Wang, W. Wang and D. Xu, "Fault Diagnosis and Tolerant Control of Single IGBT Open-Circuit Failure in Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3165-3176, April 2016.

[18] X. Hu, J. Zhang, S. Xu and Y. Jiang, "Fault diagnosis of modular multilevel converters based on extended state observer," *2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, Vancouver, BC, 2016, pp. 1-6.

[19] K. Xu, S. Xie, Y. Yan, Z. Zhang, B. Zhang and Q. Qian, "A fast fault diagnosis method for submodule failures in modular multilevel converters," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1125-1130.

[20] M. Sen, M. Alaraj and J. D. Park, "Open circuit fault detection and localization in modular multilevel converter," *2016 North American Power Symposium (NAPS)*, Denver, CO, 2016, pp. 1-6.

[21] Q. Yang, J. Qin and M. Saeedifard, "Analysis, Detection, and Location of Open-Switch Submodule Failures in a Modular Multilevel Converter," in *IEEE Transactions on Power Delivery*, vol. 31, no. 1, pp. 155-164, Feb. 2016.

[22] A. Ghazanfari and Y. A. R. I. Mohamed, "A Resilient Framework for Fault-Tolerant Operation of Modular Multilevel Converters," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2669-2678, May 2016.

[23] J. Wang, H. Ma and Z. Bai, "A Submodule Fault Ride-Through Strategy for Modular Multilevel Converters With Nearest Level Modulation," in *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1597-1608, Feb. 2018.

[24] O. S. Yu, N. J. Park and D. S. Hyun, "A Novel Fault Detection Scheme for Voltage Fed PWM Inverter," *IECON 2006 - 32nd Annual Conference on IEEE Industrial Electronics*, Paris, 2006, pp. 2654-2659.

[25] W. Song and A. Q. Huang, "Fault-Tolerant Design and Control Strategy for Cascaded H-Bridge Multilevel Converter-Based STATCOM," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2700-2708, Aug. 2010.

[26] R. Picas, J. Zaragoza, J. Pou and S. Ceballos, "Reliable Modular Multilevel Converter Fault Detection With Redundant Voltage Sensor," in *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 39-51, Jan. 2017.

[27] P. Lezana, R. Aguilera and J. Rodriguez, "Fault Detection on Multicell Converter Based on Output Voltage Frequency Analysis," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2275-2283, June 2009.

[28] C. Turpin, P. Baudesson, F. Richardeau, F. Forest and T. A. Meynard, "Fault management of multicell converters," in *IEEE Transactions on Industrial Electronics*, vol. 49, no. 5, pp. 988-997, Oct 2002.

[29] S. Haghnazari, M. Shahbazi and M. R. Zolghadri, "A new fault detection method for modular multilevel converter semiconductor power switches," *IECON 2015 - 41st Annual Conference of the IEEE Industrial Electronics Society*, Yokohama, 2015, pp. 50-55.

[30] S. Yang, Y. Tang and P. Wang, "Open-circuit fault diagnosis of switching devices in a modular multilevel converter with distributed control," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 4208-4214.

[31] F. Deng, Z. Chen, M. R. Khan and R. Zhu, "Fault Detection and Localization Method for Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2721-2732, May 2015.

[32] P. Vas, *Artifiicial-intelligence-Based Electrical Machines and Drives*. New York: Oxford University Press, 1999.

[33] F. Fiippetti and P. Vas, "Recent developments of induction motor drives fault diagnosis using AI techniques," *Industrial Electronics Society, 1998. IECON '98. Proceedings of the 24th Annual Conference of the IEEE*, Aachen, 1998, pp. 1966-1973 vol.4.

[34] S. Hayashi, T. Asakura and S. Zhang, "Study of machine fault diagnosis system using neural networks," *Neural Networks, 2002. IJCNN '02. Proceedings of the 2002 International Joint Conference on*, Honolulu, HI, 2002, pp. 956-961.

[35] S. Zhang, T. Asakura, X. Xu and B. Xu, "Fault diagnosis system for rotary machines based on fuzzy neural networks," *Proceedings 2003 IEEE/ASME International Conference on Advanced Intelligent Mechatronics (AIM 2003)*, 2003, pp. 199-204 vol.1.

[36] A. Bernieri, M. D'Apuzzo, L. Sansone and M. Savastano, "A neural network approach for identification and fault diagnosis on dynamic systems," *1993 IEEE Instrumentation and Measurement Technology Conference*, Irvine, CA, 1993, pp. 564-569.

[37] S. Khomfoi and L. M. Tolbert, "Fault Diagnostic System for a Multilevel Inverter Using a Neural Network," in *IEEE Transactions on Power Electronics*, vol. 22, no. 3, pp. 1062-1069, May 2007.

[38] S. Khomfoi and L. M. Tolbert, "Fault Diagnosis and Reconfiguration for Multilevel Inverter Drive Using AI-Based Techniques," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2954-2968, Dec. 2007.

[39] S. Kiranyaz, A. Gastli, L. Ben-Brahim, N. Alemadi and M. Gabbouj, "Real-Time Fault Detection and Identification for MMC using 1D Convolutional Neural Networks," *in IEEE Transactions on Industrial Electronics*. doi: 10.1109/TIE.2018.2833045.

[40] Z. Li, Y. J. Huang and W. C. Lin, "FPGA implementation of neuron block for artificial neural network," *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hsinchu, 2017, pp. 1-2.

[41] S. Li, K. Choi and Y. Lee, "Artificial neural network implementation in FPGA: A case study," *2016 International SoC Design Conference (ISOCC)*, Jeju, 2016, pp. 297-298.

[42] S. Singh, S. Sanjeevi, A. Talashi, "FPGA Implementation of a Trained Neural Network," *in Journal of Electronics and Communication Engineering*, vol. 10, no. 3, pp. 45-54, May-Jun 2015.

[43] Z. Li, Y. J. Huang and W. C. Lin, "FPGA implementation of neuron block for artificial neural network," *2017 International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Hsinchu, 2017, pp. 1-2.

[44] S. Li, K. Choi and Y. Lee, "Artificial neural network implementation in FPGA: A case study," *2016 International SoC Design Conference (ISOCC)*, Jeju, 2016, pp. 297-298.