Switching Sequence Synthesis for Minimizing RMS Current in a Single-Inductor-Multi-Output Converter

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***Abstract*—Single-inductor-multiple-output (SIMO) DC-DC converters offer a compact power management solution in low power applications for simultaneously powering multiple DC loads. While using a time-interleaved PWM control technique, there exist multiple feasible switching sequences in a SIMO converter. The primary research focus in the recent past remains in minimizing the cross regulation and coupling effects. However, there has been a little emphasis on the design of the switching sequence for minimizing the RMS inductor current in order to minimize the conduction losses. This paper is aimed in finding a suitable switching sequence for the reduction in the RMS value of the inductor current i_L in a SIMO converter. The primary objectives are to (i) find the practically feasible switching sequences, (ii) identify the sequence with the lowest RMS value of i_L at a given operating condition, and (iii) develop an optimal algorithm for dynamically varying operating conditions. A prototype of dual-output buck converter is made. A three-output simulated and a two-output experimental case studies are considered, and analytical predictions are found to be consistent with the results.**

I. Introduction

The need for more sophisticated features within a compact size poses greater design challenges for the portable device manufacturers. In these devices, multiple modules such as liquid crystal display (LCD) monitor, light emitting diode (LED) backlight, audio and several signal processing units require different operating voltages [1]- [2]. The use of standalone converters [3]- [5] for powering each I/O device increases the component count and occupies more device area. Among all the solutions available, a single-inductor multiple-output (SIMO) converter is often preferred in which a single inductor is shared between the multiple output levels in a time-multiplexed manner [6]- [8]. However, this type of converter suffers from cross-regulation issues when there is a load change, since all the output terminals are connected to the same switch node point [9]. Various methods have been proposed in the literature to overcome the cross regulation problem in a SIMO converter, which are mainly focussed on design and control aspects [10]- [15]. The efficiency of the SIMO converter is predominantly affected by the RMS value and ripple of the inductor current, which are characterized by the switching sequence of output levels. To the best of our knowledge, none of the research methods extensively focuses on the aspects from the RMS and/or ripple current reduction for a suitable choice of the switching sequence. This is particularly important as the switching/driver losses remain more on less constant for almost all practically recommended switching sequences. Thus, the minimization of conduction losses remains a differentiating factor for improving the steady-state efficiency, which is primarily affected by the RMS value of the inductor current. This paper mainly focusses on to identify the right switching sequence of the output voltage levels in order to minimize the RMS value of the inductor current and to investigate whether this also minimizes the ripple current. Further, it is also shown that a wrong choice of the switching sequence considerably increases the RMS inductor current.

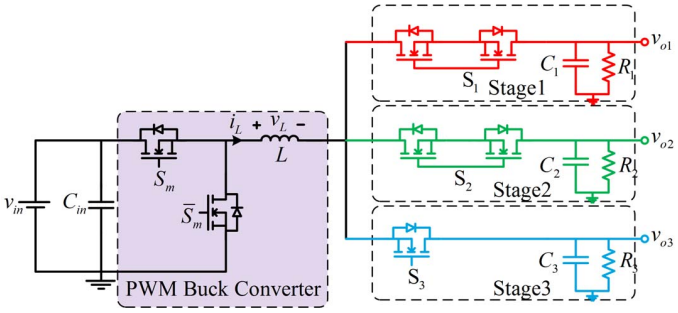

Fig. 1. Schematic of the single-inductor three output (SITO) buck converter.

II. Single-Inductor Triple-Output Buck Converter

Fig. 1 shows the schematic of a SIMO buck converter with three output voltage levels. The inductor is time-multiplexed between the output voltages v_{o1}, v_{o2}, and v_{o3} through the respective MOSFETs S_1, S_2, and S_3. Thus, at any given instant within a switching cycle, the converter can undergo six possible switching configurations, namely

- $C1 \Rightarrow S_m, S_1$
- $C2 \Rightarrow S_m, S_2$
- $C3 \Rightarrow S_m, S_3$
- $C4 \Rightarrow \bar{S}_m, S_1$
- $C5 \Rightarrow \bar{S}_m, S_2$
- $C6 \Rightarrow \bar{S}_m, S_3$

(where S_m, S_1, S_2, and S_3 indicate active high gate signals for the respective MOSFETs.)
Using a combination of the above switches, a number of

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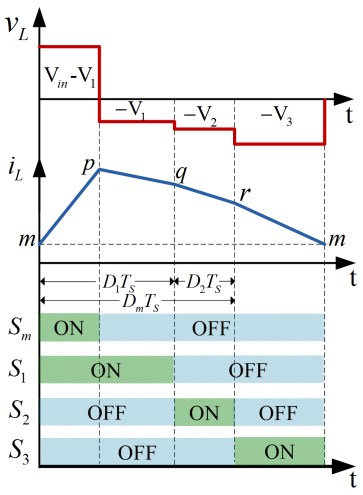

Fig. 2. Waveforms for case 1 (a) Inductor voltage (b) Inductor current i_{L} (c) Gate signals to switches

switching configurations can be generated. The objective is to identify all such configurations, then to find the set of feasible solutions among them (which are realizable with $0<d<1$) *(Step 1)*. Thereafter, these can be considered to devise an optimal solution *(Step 2)*. In order to reduce the switching and driver losses, it is practically recommended that each switch can undergo a change in its state once in a periodic switching cycle with the time period T_{s}. For low power applications, it can be shown that switching losses would be more or less the same, irrespective of the switching sequences as discussed above.

A. Possible switching Configurations and Formulating Steady State Parameters

For the single-input three output (SITO) converter as shown in Fig. 1, a combination of C1, C2, C3, C4, C5 and C6 yields eighteen different switching configurations. Fig. 2 shows the waveform for one of the configurations (denoted by case 1). However, the formulation of the steady state parameters for individual configurations is a tedious task, given the fact that a conventional state-space averaging method may not be accurate enough. This is because of ignoring the ripple information. An alternative averaging technique using the inductor current ripple can be used [16], and the parameters can be found using the inductor volt-second and capacitor-charge balance equations.

For case 1:

$$(m+p)\,D_m + (p+q)\,(D_1 - D_m) - 2\frac{v_{o1}}{R_1} = 0;$$

$$(r+q)\,D_2 - 2\frac{v_{o2}}{R_2} = 0;$$

$$(r+m)\,D_3 - 2\frac{v_{o3}}{R_3} = 0;$$

$$(v_{in} - v_{o1})D_m - v_{o1}\,(D_1 - D_m) - v_{o2}D_2 - v_{o3}D_3 = 0;$$

TABLE I
STEADY STATE PARAMETERS FOR THE POSSIBLE SWITCHING CONFIGURATIONS

Case	Combination	D_1	D_2	D_{m}	$i_{\mathrm{L,rms}}$	Δi_{L}
1	C1→C4→C5→C6	0.45	0.11	0.26	5.29	4.62
2	C1→C4→C6→C5	0.43	0.21	0.25	5.28	4.37
3	C2→C1→C4→C6	0.39	0.18	0.27	5.26	4.32
4	C2→C3→C6→C4	0.55	0.14	0.23	5.16	3.19
5	C3→C6→C4→C5	0.49	0.17	0.24	5.13	2.82

where $D_3 = 1 - D_1 - D_2$) and p, q, and r can be expressed in terms of the four basic variables m, D_1, D_2, and D_{m}; thus, their unique solutions can be obtained by solving the above four equations. Table I shows the results of a SITO converter with a parameter set: v_{in} = 8 V, v_{o1} = 1 V, v_{o2} = 1.8 V, v_{o3} = 3.3 V, R_1 = 0.4 Ω, R_2 = 2.6 Ω,R_3 = 1.75 Ω, $L = 4$ μH, and f_{s} = 100 kHz. The combinations given in Table I are five feasible switching configurations which are realizable with $o < d < 1$; thus, the *Step 1* of the analysis is now complete. The next subsection focusses on the *Step 2*, i.e., identifying the optimal solution among these feasible configurations. It is to be noted that the RMS value of the inductor current $i_{\mathrm{L,rms}}$ can be found as a function of the four basic variables. For case 1, the $i_{\mathrm{L,rms}}$ is obtained as

$$i^2_{L,rms} = \left(\tfrac{m^2+p^2+mp}{3}\right) D_m + \left(\tfrac{p^2+q^2+pq}{3}\right)(D_1 - D_m) + \left(\tfrac{q^2+r^2+rq}{3}\right) D_2 + \left(\tfrac{m^2+r^2+mr}{3}\right)(1 - D_1 - D_2) \quad (1)$$

B. Efficiency optimization

Table I shows that the minimum values of $i_{\mathrm{L,rms}}$ and the ripple current Δi_{L} are obtained for case 5, in which the conduction losses can be expected to be minimum by virtue of the RMS optimization. While case 5 remains the best case, the switching configuration in case 1 is identified to have higher $i_{\mathrm{L,rms}}$ among all the feasible one given in Table I.

Using the same output voltages, the output power levels are varied, and the optimal solution is shown in Table II. The deviation variable $\delta i_{\mathrm{L,rms}}(\%)$

$$\delta i_{L(rms)}\,(\%) = \left(\frac{i_{L(rms)}\,(worstcase)}{i_{L(rms)}\,(bestcase)} - 1\right) * 100 \quad (2)$$

is the percentage difference in $i_{\mathrm{L,rms}}$, and the same for the ripple current is $\delta\Delta i_{\mathrm{L}}$. The output power levels are taken as P_{o1},P_{o2} and P_{o3}. This can be as large as 4% and 40% respectively. Thus, an improper choice of the switching sequence will have a considerable impact on the overall converter efficiency, in which the optimal switching sequence is of particular interest. It is reasonable to synthesize the sequence based on the output switches, because the input switch S_{m} is turned on at every rising edge of the clock and S_{m} is turned off based on the net output power demand,

TABLE II
VARIATION OF i_{L} FOR DIFFERENT POWER LEVELS

Optimal turn-on sequence	P_{o1} (W)	P_{o2} (W)	P_{o3} (W)	$\delta i_{\mathrm{L,rms}}$ (%)	$\delta\Delta i_{\mathrm{L}}$ (%)
S3→S1→S2	0.63	3.13	6.25	3.90	39.8
S2→S1→S3	3.13	0.63	6.25	0.30	0.46
S2→S1→S3	6.25	3.13	0.63	0.14	4.40
S2→S3→S1	6.25	0.63	3.13	0.29	11.8
S2→S1→S3	0.83	8.33	0.83	0.28	6.20
S2→S1→S3	3.13	6.25	0.63	0.40	7.30

which is taken care by the output feedback controllers. Thus, the number of feasible switching sequence is further reduced to six from eighteen. The switching sequence is generally decided by the output voltage levels. The output $v_{\mathrm{o1}}<v_{\mathrm{o2}}<v_{\mathrm{o3}}$ implies the switching sequence to be S3→S2→S1 (if it is feasible). However, Table II shows that the above choice does not necessarily guarantee the minimum RMS inductor current.

C. Effect of change in operating conditions

Figs. 3–5 show the effect of deviation in $i_{\mathrm{L,rms}}$ between the best case and the worst case for different operating conditions. For each graph, one of the variables among switching frequency f_{s}, net power P, and input voltage v_{in} is varied while keeping the other parameter at their nominal values as given in Section II-A. It is clear from the Figs. 3–5 that the sequence optimization is more pronounced for a higher v_{in} and/or lower f_{s} and power P, in which $\delta i_{\mathrm{L,rms}}$ (%) deviation is quite prominent; thus, the efficiency would considerably differ between the best and the worst cases. Fig. 6 shows the combined effect of change in operating conditions,with P and v_{in} in the axes limits and each surface corresponding to decreasing f_{s}.

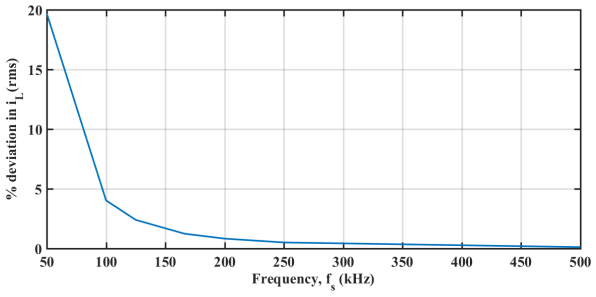

Fig. 3. Effect of change in frequency f_{s} on $\delta i_{\mathrm{L,rms}}$ (%)

Another important factor in determining the $\delta i_{\mathrm{L,rms}}$ (%) deviation is the number of output terminals of the SIMO converter. From analysis, it is found that the difference in $i_{\mathrm{L,rms}}$ between different switching configurations is

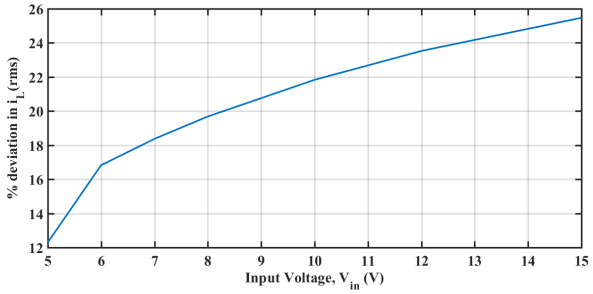

Fig. 4. Effect of change in input voltage v_{in} on $\delta i_{\mathrm{L,rms}}$ (%)

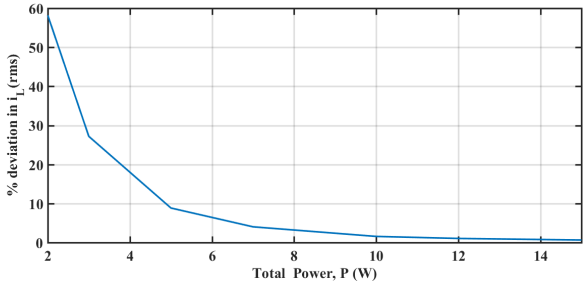

Fig. 5. Effect of change in total Power P on $\delta i_{\mathrm{L,rms}}$ (%)

significantly high for relatively less number of output levels of SIMO converter. However, for a converter with higher number of output levels (typically, above four), the difference in $i_{\mathrm{L,rms}}$ between the feasible switching configurations is relatively low; thus, the the choice of the switching sequence makes little difference in efficiency. Besides, for single-input dual output (SIDO) or SITO converters, the deviation in $\delta i_{\mathrm{L,rms}}$ is much more prominent, which makes the analysis interesting.

III. GENERIC ALGORITHM FOR OPTIMAL SEQUENCE

The case study in Section II-B indicates that the optimal switching sequence for a SIMO converter can be different from the sequence as demanded by the output voltages. This section focusses on developing a generic algorithm for deciding the optimal sequence. The same input parameters used in Table I

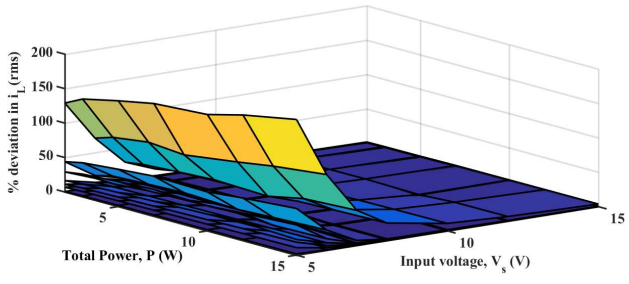

Fig. 6. Combined effect of change in operating conditions f_{s}, P and v_{in} on $\delta i_{\mathrm{L,rms}}$ (%)

TABLE III
INDIVIDUAL PRIORITY QUEUES BASED ON OUTPUT VOLTAGE AND CURRENT

Case	Turn-on sequence	Priority based on Voltage	Priority based on Current
1	S3→S2→S1	1	4
2	S3→S1→S2	2	3
3	S2→S3→S1	3	6
4	S2→S1→S3	4	5
5	S1→S3→S2	5	1
6	S1→S2→S3	6	2

are chosen to verify whether the algorithm leads to the same optimal solution (case 5 in Section II-B).

A. Identifying the output Voltage and Current level orders

The output voltages and load currents for a SITO converter are v_{o1} = 1 V, v_{o2} = 1.8 V, v_{o3} = 3.3 V, and I_{o1} = 2.5 A, I_{o2} = 0.69 A, I_{o3} = 1.88 A.
Thus, $v_{o1}<v_{o2}<v_{o3}$ and $I_{o2}<I_{o3}<I_{o1}$

B. Forming priority queue based on the order

Once the orders have been determined, a priority queue of all the possible switching sequences is to be formed. The priority queue is the set of all sequences with the sequence that follows the voltage (or current) level order and most closer sequence are placed at highest priority. For instance, if the order of voltage levels are $v_{o1}<v_{o2}<v_{o3}$, then the switching sequence S3→S2→S1 receives the highest priority. Thus, based on the output levels and currents, Table III gives the priority of different switching sequence.

C. Identification of a sequence by the combination in voltage and current priorities

Using the priority queues given in Table III, the optimal switching sequence need to be identified. For simplicity of analysis, a linear weighing function is used here (equal weightage given to both the queues) to identify the overall highest priority sequence. For some cases, however, it might involve a non-linear weighing function.

D. Selection of optimal switching sequence

Table IV gives the priority of the sequence using the technique described in Section III A. The final step is to identify the feasibility of switching sequence starting from highest priority. This involves formulating the steady-state equations for the particular sequence and checking if they yield a valid solution. The highest priority feasible sequence is the optimal solution. From Table IV, S3→S2→S1 is checked for feasibilty. However, it gives an invalid solution. Next, S3→S1→S2 is chosen which indeed gives a feasible steady-state solution. Hence, the sequence S3→S1→S2 is identified as the optimal sequence, which is the same as found in Sec.II-B. Thus, the algorithm repeats once the operating condition changes.

TABLE IV
COMBINED PRIORITY QUEUE

Case	Turn-on sequence	Priority
1	S3→S2→S1	1
2	S3→S1→S2	1
3	S1→S3→S2	3
4	S1→S2→S3	4
5	S2→S3→S1	5
6	S2→S1→S3	6

IV. OPEN-LOOP MODELLING OF THE SIMO CONVERTER

Once the optimal switching sequence is chosen for a given set of nominal parameters, a state-space model of the converter is needed for compensator design. The inductor current ripple based state-space averaging technique is used to preserve the ripple current information.
The optimal case, i.e. case 5 from Section II is chosen. It comprises of four switching configurations, namely C3, C6, C4, and C5. The variables p, q, and r can be expressed in terms of the basic variables m, $D_{\rm i}$ and $v_{\rm oi}$, where $i = 1, 2, 3$ as

$$\begin{aligned} p &= m + \frac{(v_{in} - v_{o3})\, D_m T_s}{L} \\ q &= p - \frac{v_{o3}(1 - D_1 - D_2 - D_m) T_s}{L} \\ r &= m + \frac{v_{o2}(D_2) T_s}{L} \end{aligned} \tag{3}$$

The average inductor current over a switching cycle T_s, as shown in Fig. 1 is obtained as

$$\begin{aligned} \bar{i_L} = \frac{(m+p)}{2} D_m + \frac{(p+q)}{2} (1 - D_1 - D_2 - D_m) \\ + \frac{(q+r)}{2} D_1 + \frac{(r+m)}{2} D_2 \end{aligned} \tag{4}$$

The state-space model is derived for one of the four switching configurations C4 at which $S_m = S_1 = S_3 = 0$ and $S_2 = 1$. However, in a similar ways, the state-space model for other configurations ca be derived. The $\bar{i_{\rm L}}$, v_{o1}, v_{o2}, and v_{o3} are the state-variables. Then, for C4 $(1\text{-}D_1\text{-}D_2)T_{\rm s}<t<(1\text{-}D_2)T_{\rm s}$, the state-equations are given as,

$$\frac{di_L}{dt} = -\frac{v_{o1}}{L}$$

$$\begin{aligned}\frac{dv_{o1}}{dt} &= -\frac{(r+q)}{2C_1} - \frac{v_{o1}}{R_1C_1}\\ \frac{dv_{o2}}{dt} &= -\frac{v_{o2}}{R_2C_2}\\ \frac{dv_{o3}}{dt} &= -\frac{v_{o3}}{R_3C_3}\end{aligned} \tag{5}$$

where using charge balance across the capacitor C_1,

$$\frac{(r+q)}{2} = \frac{v_{o1}}{R_1}D_1 \tag{6}$$

Thus, using (5) and (6), the state space model for configuration C4 is obtained as

$$\begin{bmatrix}\dot{i_L}\\ \dot{v_{o1}}\\ \dot{v_{o2}}\\ \dot{v_{o3}}\end{bmatrix} = \begin{bmatrix}0 & 0 & -\frac{1}{L} & 0\\ 0 & -\frac{1}{R_1C_1} & 0 & 0\\ 0 & 0 & -\frac{1}{R_2C_2}\left(1+\frac{1}{D_2}\right) & 0\\ 0 & 0 & 0 & -\frac{1}{R_3C_3}\end{bmatrix}\begin{bmatrix}i_L\\ v_{o1}\\ v_{o2}\\ v_{o3}\end{bmatrix} \tag{7}$$

Once the state-space model of all the individual configurations are identified, the overall state-space model over a switching cycle T_s can be obtained.

V. Hardware Implementation

A. Implementation of the proposed scheme

A hardware prototype is made, the setup diagram is shown in Fig. 7, and the experimental results in Figs. 8-11. Voltage mode DPWM control methods are considered for individual output feedback loops, which implemented using an FPGA device.

The nominal parameters are as $v_{\rm in} \in [5\,{\rm V}, -12\,{\rm V}]$, $v_{\rm oi} = [1\,{\rm V} - 5\,{\rm V}]$, $L = 4\ \mu$H, C_1, C_2, $C_3 = 100\ \mu$F, $P_{\rm max}$=20 W. A single-inductor-dual-output (SIDO) is implemented using a voltage DPWM control technique with $v_{\rm in}$ = 8 V, $v_{\rm o1}$ = 1 V, and $v_{\rm o2}$ =3.2 V using the switching frequency of $f_{\rm s}$ = 500 kHz. Two different sets of power levels are considered with each consisting two different switching configurations of which steady-state experimental results are shown in Figs. 8-11. The analysis of a SIDO converter is similar to SITO converter shown in Section II. While four configurations seem to be possible, for the two sets of the power levels, only two feasible configurations (denoted by case 1 and case 2) exist for each set of the power levels. case 1 is the one when $v_{\rm o1}$ is turned on first followed by $v_{\rm o2}$, and the reverse sequence is represented by case 2.

B. Discussion

The experimentally measured parameters are summarized in Table V. While the measured parameters slightly deviate from their analytical values, because of practical parasitic and voltage drops, the predictions of the best and worst cases seem to be consistent for both the cases. The Table V shows that case 2 is the optimal switching sequence with smaller $i_{\rm L,rms}$ as well as $\delta i_{\rm L}$) for both the power levels. This is consistent with the result from the algorithm. For both the

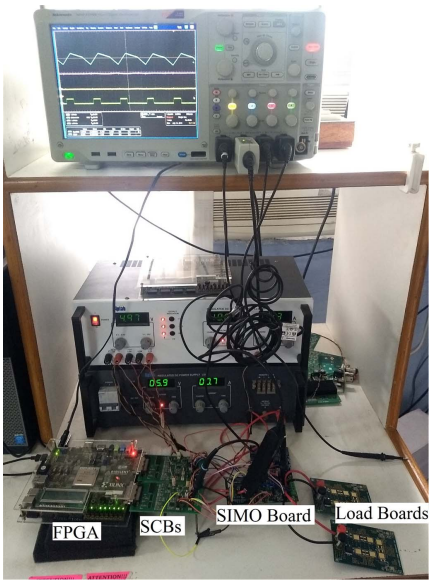

Fig. 7. Experimental setup of the system

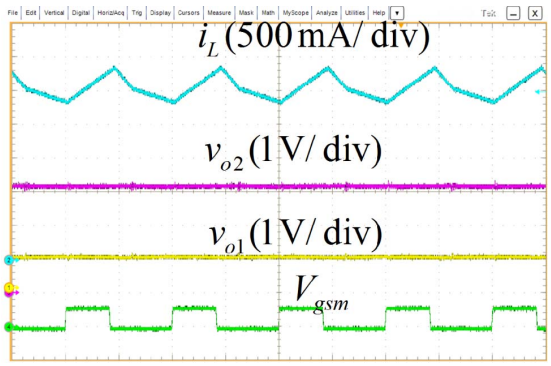

Fig. 8. Waveforms for P1 = 1 W and P2 = 4.8 W when $v_{\rm o2}$ is turned on first (case 2), time scale = 2 μs

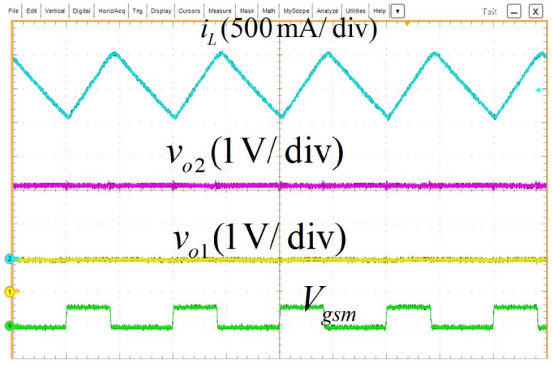

Fig. 9. Waveforms for P1 = 1 W and P2 = 4.8 W when $v_{\rm o1}$ is turned on first (case 1), time scale = 2 μs

TABLE V
EXPERIMENTAL RESULTS FOR THE SIDO CONVERTER

P1 = 1 W, P2 = 4.8 W	i_{L} Parameters	Case 1	Case 2
	Ripple	0.9 A	0.6 A
	rms value	2.50 A	2.45 A
P1 = 3.8 W, P2 = 1 W	i_{L} Parameters	Case 1	Case 2
	Ripple	0.56 A	0.42 A
	rms value	4.07 A	3.66 A

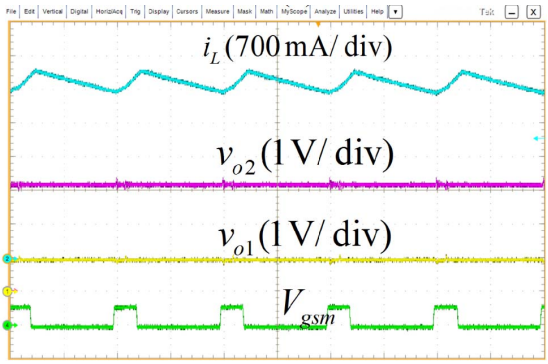

Fig. 10. Waveforms for P1 = 3.8 W and P2 = 1 W when v_{o2} is turned on first (case 2), time scale = 2 μs

cases, v_{o1}<v_{o2} with I_{o1}<I_{o2} (and vice-versa). This should have resulted in case 1 being optimal for the second set. However feasibility analysis in Step4 of the algorithm rules it out. Hence, it is found that case 2 (S2→S1) is optimal for both. It is also found that the differences in $i_{\mathrm{L,rms}}$ and δi_{L} seem to be considerably high between two cases with almost 10 % and 33 % respective deviations for $P1$ = 3.8 W and $P2$ = 1 W. Thus, an improper choice of the switching sequence may lead to higher conduction losses, which would eventually degrade the steady-state efficiency.

VI. CONCLUSIONS AND FUTURE WORK

In this paper, the method to find an optimal switching sequence (and thus, improving efficiency) was discussed for minimizing the RMS current in a SIMO converter. A more detailed mathematical (optimization) framework can be developed for a more generic SIMO converter.The Generic Algorithm discuussed in Sec. III concluded our study. The priority queue can be based on three output parameters:- (1) voltage level (2) current level (3) power level. In this paper, only first two factors were considered using a linear weighing function. The effect of the the third factor using non-linear weighing function involves rigorous mathematical analysis and can be the scope of future study.

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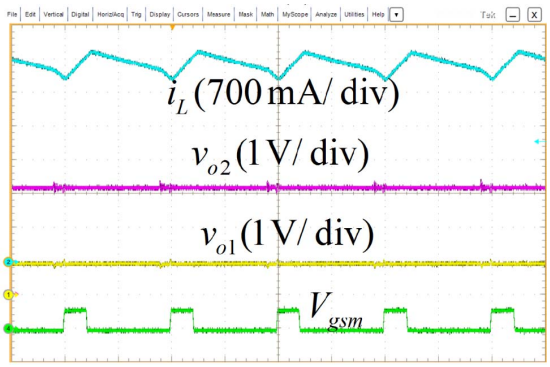

Fig. 11. Waveforms for P1 = 3.8 W and P2 = 1 W when v_{o1} is turned on first (case 1), time scale = 2 μs

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