An Integrated Regulated Resonant Switched-Capacitor DC-DC Converter For PoL Applications

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***Abstract*—This paper proposes an integrated regulated resonant switched-capacitor DC-DC converter for a 2.5 V to 1.2 V, 3 A conversion designed in a 130 nm CMOS technology. The voltage is regulated through a combined frequency/time shift on-chip controller that operates thanks to a zero-crossing detector for the tank current. By using such control technique, an output voltage greater than $V_{in}/2$ can be reached. The integrated circuit also implements a medium-load and a light-load control modes that maximize the efficiency at every load condition. The external resonant tank is composed of a 12 nH air-core inductor and a 4.7 μF capacitor in a 0805 package, achieving high power density. In this paper, the operation principle and the control techniques are discussed, demonstrating that the inductor value can be reduced by a factor of more than 8 compared to an integrated buck converter designed for the same application, without incurring in a significant efficiency degradation.**

I. INTRODUCTION

SWITCHED Capacitor Converters (SCCs) have been the subject of intense research for many years for various applications, covering a wide range of power levels, form point-of-load converters to electrical vehicle power systems [1]-[14]. Their main advantage is their lack of bulky magnetic components, in contrast with classical inductor-based topologies. In these systems, step-up/down conversions are achieved by stacking voltages during the switching cycle, instead of using high-value inductors as energy storage devices. One of the main drawbacks of the SCC topology is that the charge redistribution mechanism leads to consistent power losses, since it causes a high RMS current value inside the switched elements [15].

To overcome the charge redistribution problem, an additional inductive element can be used to achieve soft charging of the switched capacitors and/or Zero-Voltage-Switching (ZVS)/ Zero-Current-Switching (ZCS) for the switches [16]. In this way, Resonant Switched-Capacitors (ReSC) converters are obtained, which show high efficiency and power density [17]-[18]. Several control methods have been proposed in literature for such converters ([19]-[25])

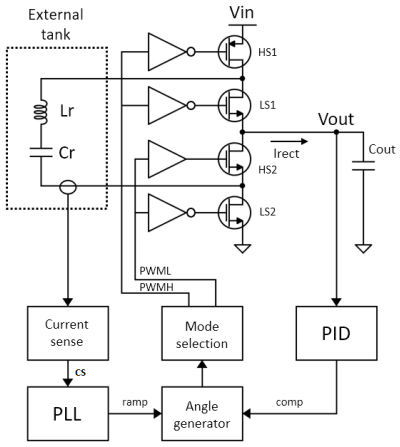

Fig. 1: ReSC architecture and and block scheme of the proposed controller.

This work proposes and demonstrates the implementation of a controller that can set different operation modes for high, medium and light loads, in order to optimize the efficiency of the ReSC converter shown in Fig. 1 (which consists of an LC impedance and four stacked power FETs) for every value of the load current. The control loop is based on the zero-crossing detection of the tank current: in particular, the phase shift of the driving signals from the zero-crossing instant is adjusted. ZVS or ZCS is obtained for all the switches. Using the proposed controller, $V_{out} > V_{in}/2$ can be obtained, extending the application range for this topology. An ASIC featuring the power switches and the proposed controller has been designed in a 130 nm CMOS technology. This converter achieves high power density by using a small air-core inductor (12 nH). The use of the air core inductor is required by the application, since the converter has to operate in the High-Luminosity Large Hadron Collider (HL-LHC) experiments, where no magnetic materials are allowed due to the presence of a magnetic field

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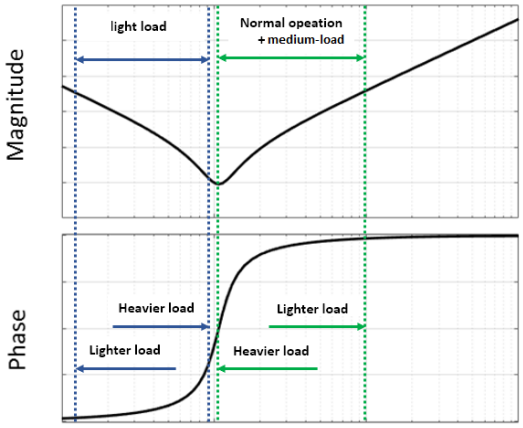


Fig. 2: Tank impedance and operating regions.

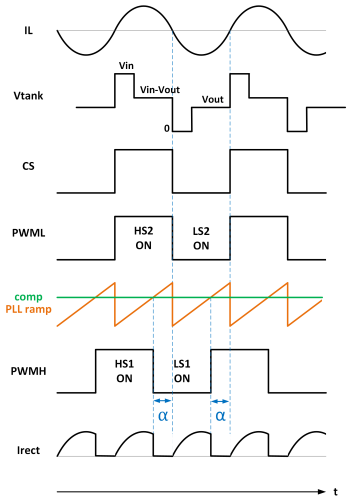


Fig. 3: Main control signals in the α operation mode. α is the phase-advance between PWMH and the current zero-crossing signal CS. It is generated by comparing the control signal *comp* to the ramp generated by the PLL (which is synchronized with CS). In this figure, the tank current waveform has been approximated by its first harmonic.

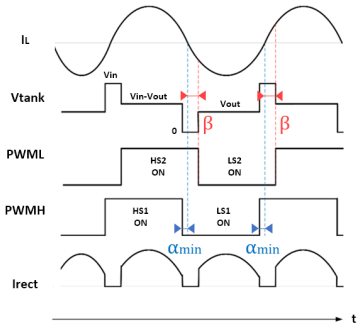


Fig. 4: Tank voltage and signals with β operation. α is saturated to α_{min} and β increases with output current. The tank current waveform has been approximated by its first harmonic.

up to 4 T. In addition, the ASIC has been designed to be radiation-hard to survive to the high radiation levels reached in the HL-LHC experiments. The ReSC converter is particularly interesting for this application because of its low mass, since any added material is detrimental for the physics performance of the experiments.

II. PRINCIPLE OF OPERATION

In the ReSC converter, the output voltage regulation is achieved through the modulation of the tank excitation voltage; this is done by tuning the phase shift of the driving signals PWML and PWMH (shown in Fig. 1) from the zero-crossing instants of the tank current, adjusting the frequency and amplitude of the excitation voltage. PWML and its negated version drive respectively the two bottom switches HS2 and LS2, while PWMH is used as the driving signal for the two top switches HS1 (which is the only PMOS switch in use) and LS1. As reported in Fig. 2, heavier loads require excitation frequencies closer to the tank resonance, as

$$Z_{tank} = \frac{1}{sC} + sL + R_{tank} \tag{1}$$

In normal operation, the converter operates above the tank resonant frequency (see Fig. 2). At sufficiently small load currents, PWML is identical to the CS signal, which is synchronized to the tank current zero crossing instants (assuming the logic value '1' when the tank current is positive, and the logic value '0' when it is negative, see Fig. 3). Regulation is achieved by tuning the PWMH phase lead angle α (see Fig. 3). In this mode, HS2/LS2 operate in ZCS and HS1/LS1 are turned on at zero voltage. A PLL is locked to the CS signal to obtain a ramp synchronized with the zero crossing instants of the tank current. Such ramp is compared to the control signal to obtain the phase lead α for PWMH (Fig. 3). This mode can be referred to as α-operation. In α-operation, the maximum output current is obtained for $\alpha \to 0$ (full tank resonance and synchronized PWMs). At full resonance, the output current is limited by the parasitic tank resistance. To overcome this limitation, β-operation is introduced (Fig. 4): in this mode, the phase lead of PWMH from CS is kept to its minimum value α_{min} and PWML lags of an angle β behind the tank current zero-crossing. Using β, the tank excitation peaks become increasingly long as the load increases, resulting in an equivalent voltage excitation boost. The α and β modes are similar to the control scheme proposed by [24], while in this case the control loop acts on actual phases and not on time delays.

As lighter loads require moving away from resonance (high operating frequency), the efficiency is heavily degraded with α and β modes; to overcome this issue, medium-load and light-load operation modes are proposed. For medium-load conditions, the converter operates with fully-synchronized driving signals with a common leading-phase angle α from the zero crossing of the tank current (Fig. 5). α is adjusted according to the required output current, resulting in a frequency-modulation operation [21]. In this mode, the voltage excitation of the tank has a reduced amplitude (as the tank voltage

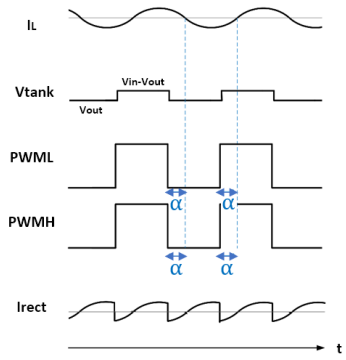


Fig. 5: Medium-load operation mode: PWMH/PWML are synchronized and shifted from CS by a phase α. The tank current waveform has been approximated by its first harmonic.

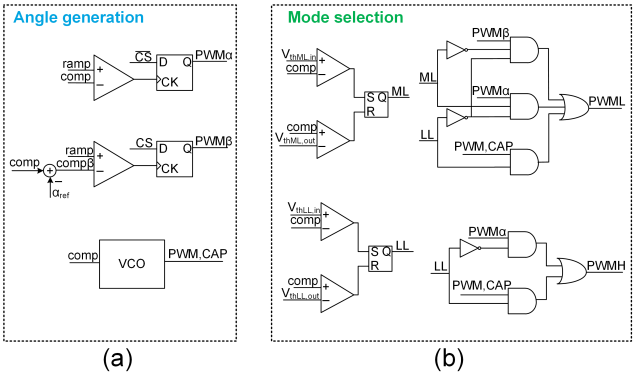


Fig. 6: a) Angle generation block and b) mode selection block. ML assumes the logic value '1' when the medium load operating mode is selected, while LL assumes the logic value '1' when the light load operating mode is selected.

can only be either $V_{in} - V_{out}$ or V_{out}). In addition, for switching frequencies that are close to resonance, the tank current is almost fully rectified: this results in a reduced RMS current for the same load compared to the α mode. The medium-load mode is functional only for $V_{out} < V_{in}/2$, otherwise the tank excitation would be counter-phased to the resonant current: in the latter case, the controller automatically excludes this mode. For lighter loads, the switching frequency moves further from resonance, and a significant part of the current provided to the output becomes negative, leading to an inefficient operation. In such conditions, a new light-load operation mode is introduced: CS is ignored, and a VCO generates a low-frequency driving signal: the output current is modulated in the capacitive region of Z_{tank}, as shown in Fig. 2 and PWML/PWMH are synchronized. In this mode, the losses due to the absence of ZVS/ZCS are negligible due to the low switching frequency.

The generation of the driving signals PWML and PWMH is detailed in Fig. 6, together with the operating mode selection. The angle generator block relies on the control signal *comp*, on CS and on the PLL output *ramp* (which is synchronized

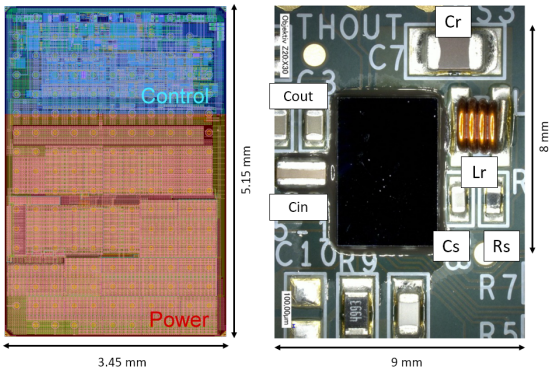


Fig. 7: ASIC layout and power area on the PCB prototype.

with CS) to generate PWM_α and PWM_β. Such signals have respectively a phase lead α and a phase lag β from CS, and in α-β mode they coincide respectively with PWMH and PWML. $comp_\beta$ is obtained as $comp - \alpha_{ref}$, where the value of α_{ref} depends on the input and output voltages. In particular, the larger is $\frac{V_{out}}{V_{in}/2}$, the lower is the load current at which $\beta > 0$ is necessary to provide the required output power. Therefore, α_{ref} decreases (and $comp_\beta$ increases) as $\frac{V_{out}}{V_{in}/2}$ increases. In the medium-load operation, PWM_α is used both as PWML and PWMH, and thus both driving signals are equally phase-shifted from CS. The control signal *comp* is also used as the input of a VCO, which generates PWM,CAP, the driving signal of the light-load operation mode.

The control signal *comp* is proportional to the output current in steady state, and the mode selection block determines whether the medium-load or the light-load operation modes must be selected by comparing *comp* to to the thresholds $V_{th,xx}$. The values of such thresholds are dependent on V_{in} and V_{out}, while $V_{thML,out} > V_{thML,in}$ and $V_{thLL,out} > V_{thLL,in}$ to prevent oscillations between the operating modes. According to the selected mode, the mode selection block routes the correspondent signals towards PWMH and PWML.

III. EXPERIMENTAL RESULTS

The prototype presented in Fig. 7 was designed in a 130 nm CMOS technology, in order to demonstrate the validity of the proposed solution. A flip-chip assembly has been adopted (182 bumps with a bump pitch of 300 μm have been used) to decrease as much as possible the parasitic inductance to the input capacitance. The PCB has been built as a rigid circuit with four layers using FR4 laminates of 30 μm thickness, cladded with copper layers of 17 μm thickness. This value has been chosen to reduce the amount of material used, as any added material is detrimental for the physics performance of the HL-LHC experiments. The selected external tank components are L_{tank} = 12 nH (Coilcraft 0908SQ-12N) and C_{tank} = 4.7 μF (Murata GRM219R61E475KA73).

Fig. 8 shows the measured waveforms for the start-up sequence and the light-load operating mode. Fig. 9a presents instead the waveforms in α mode: PWML switches as soon as the inductor current crosses zero, while PWMH has a phase lead from the current zero crossing. In Fig. 9b, it is

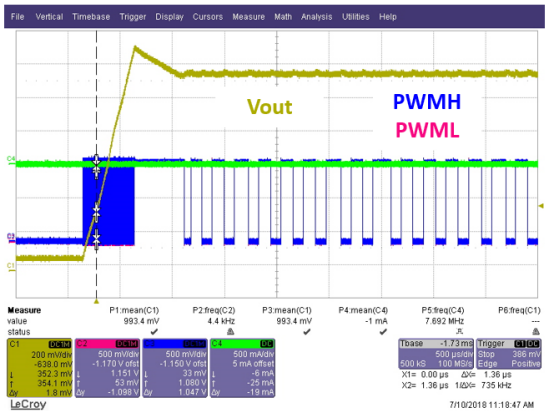
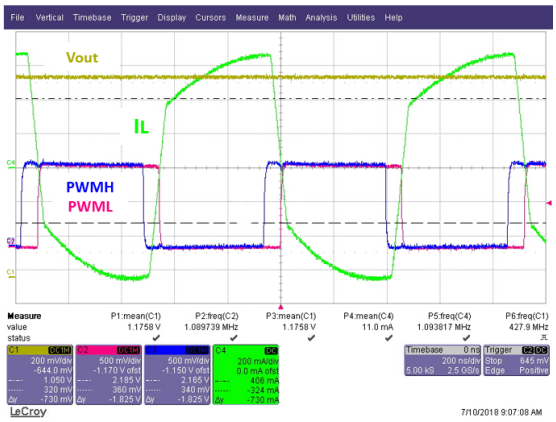


Fig. 8: Startup sequence and light-load (capacitive) mode. The output voltage overshoot is due to the fact that the final value of the ramp used as a reference for the startup is larger than the reference voltage employed once the startup phase is over. This is not critical for this specific application.

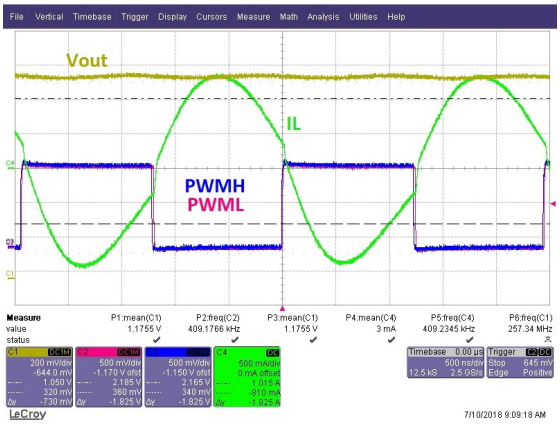
shown that the converter is working close to the tank resonant frequency, as the inductor current has a quasi-sinusoidal shape and PWMH and PWML are almost coincident. In Fig. 9c, the measured waveforms in β mode are presented, showing the phase lag of PWML from the inductor current zero crossing.

Fig. 10 shows the measured efficiency of the designed converter for V_{in}=2.5 V and I_{out} up to 3 A. For the 2.5 V $\rightarrow$ 1.2 V voltage conversion, 90% efficiency is achieved for a large load range. In Fig. 10a, the dotted lines show the efficiency degradation that would have been found when decreasing the load current if the medium-load and the light-load operating modes were not included. In addition, the strong dependence of the thresholds between the different operation modes on the V_{in}/V_{out} ratio is highlighted: such thresholds for V_{out} = 1 V and V_{out} = 1.2 V are respectively depicted in red and blue. The measured efficiency of a radiation-hard buck converter designed in the same 130 nm technology for the same application and equipped with an air-core 100 nH inductor is also shown in Fig. 10b, again for V_{in} = 2.5 V. The proposed ReSC converter allows reaching efficiencies that are comparable to those of the buck converter, while using an inductor size that is more than 8 times smaller. The efficiency of the ReSC converter is higher at medium loads for V_{out} = 1.2 V while, for the same output voltage, it drops at higher output currents due to the increase in the tank current RMS value caused by the β-operation.

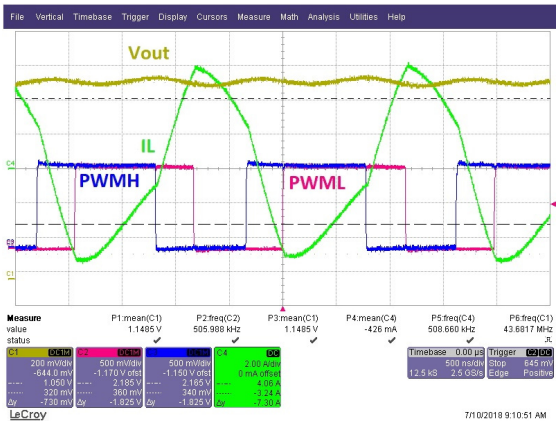
The two compared converters (i.e. ReSC and Buck) are both designed to operate with an air-core inductor: the reported efficiency must consequently be interpreted considering the high R_{ac} affecting the inductors themselves and the small thickness of the PCB copper layers. The usage of a ferrite inductor decreases copper losses caused by proximity effects and, combined with a lower operating frequency, would enable higher efficiencies for both converters. Besides, the two analyzed converters have in common a slow high-side FET turn-off, needed to minimize the voltage spikes given by the stray input inductance, and this further reduces the overall



(a)



(b)



(c)

Fig. 9: Measured converter waveforms (a) in α mode, (b) at full resonance and (c) in deep β mode (high load).

efficiency. These two power loss contributions are paramount to consider when the topologies are compared to the state-of-the art cases present in literature.

IV. CONCLUSION

In this paper, a novel integrated resonant switched capacitor converter is proposed, together with an improved

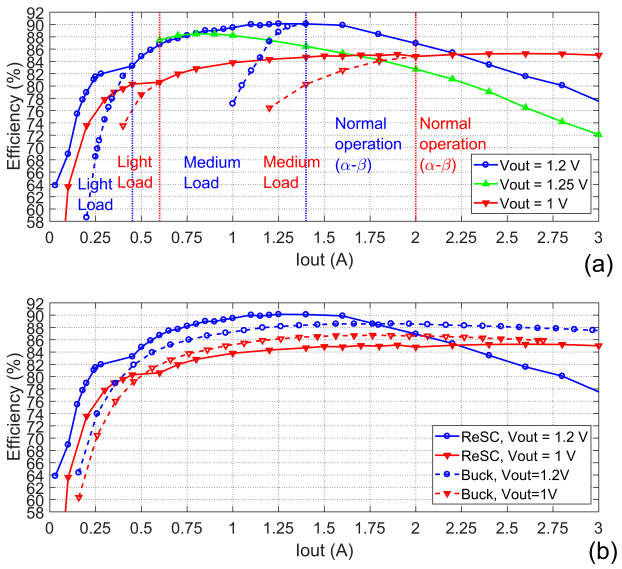


Fig. 10: Converter efficiency for V_{in} = 2.5 V and different values of V_{out}. In a), the efficiency of the ReSC converter is shown. The dotted lines show the suboptimal efficiency obtained if the medium-load and light-load modes were not included. b) Represents the comparison between the efficiency of the designed ReSC converter (solid lines) and the buck converter designed for the same application (dashed lines).

frequency/time shift control that maximizes efficiency over the whole load range through a medium-load and a light-load mode. The system is implemented in a 130 nm CMOS technology, and the targeted application are the High-Luminosity Large Hadron Collider (HL-LHC) experiments, where no magnetic components can be used and light mass is required. The converter is suitable for the 2.5 V $\rightarrow$ 1/1.2 V conversions up to I_{out} = 3 A, and it achieves high power density by using a 12 nH inductor, while showing a peak efficiency of 90%. The experimental results highlight that the proposed ReSC converter has efficiencies that are comparable to a buck converter designed for the same application, while having an improved power density. In particular, at medium load the ReSC converter features higher efficiencies, while being equipped with an 8 times smaller inductor.

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