Dynamic Interleaving of Multi-Phase Synchronous DC-DC Converters with ZVS

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***Abstract*—A decoupled control method is proposed to achieve simultaneous zero-voltage-switching (ZVS) at any load condition and interleaving with dynamic frequency in an N-phase interleaved synchronous DC-DC converter. A computationally inexpensive oscillator network generates N-phase references which retain desired interleaved state at any loading or transient condition. A model based controller calculates the required positive and negative peak phase current references to ensure ZVS. A phase compensator in each phase modulates the current reference to synchronize inductor ripple current with the respective phase reference generated by the oscillator network. The convergence of the oscillator network and the phase compensator are shown using non-linear analysis and experimental results are presented.**

I. Introduction

High switching frequency in power electronic converters offer a multitude of system level improvements such as smaller passive components, reduced ripple stress and higher power density. However, high frequency operation is accompanied by several major difficulties, namely higher switching stress on the power devices and increased switching loss [1]. Resonant and quasi-resonant topologies can reduce or eliminate such losses by enabling soft switching, i.e., ensuring turn-on and turn-off of power devices at zero voltage and zero current, respectively [2]–[4]. DC-DC converters are widely used in energy conversion systems such as in electric vehicle traction drives, PV and thermoelectric power generation systems [5]. In such converters, zero-voltage switching (ZVS) can be achieved by discharging the output capacitance (C_{oss}) of a power device before the switch turn-on event [6], [7]. ZVS can be ensured by effectively controlling the inductor current ripple beyond both a positive and a negative threshold in every switching cycle. Another widely used technology for DC-DC conversion is multi-phase interleaved topology which offers very high effective switching frequency leading to further reduction of switching ripple with smaller passive components as well as better dynamic performance [8], [9]. However, implementing both strategies simultaneously is exceedingly challenging. In general, multi-phase interleaving is done for fixed frequency operation using carrier-based modulation where carriers with required phase displacement can be generated by a standard digital controller. However, Quasi-Sqaure Wave (QSW) based ZVS scheme, to be applicable for a wide range of loading conditions, does not define a fixed switching frequency but requires switching at a dynamic frequency as a function of the load. Interleaving strategies for dynamic frequency have been reported for two phase systems using a master-slave approach [1] and a democratic approach [10], both of which suffers for systems with three or more phases. The fundamental contribution of this work is to simultaneously achieve the twofold objective of ZVS and interleaving in a system with an arbitrary N number of phases through a decoupled control method: first, an oscillator based computationally inexpensive method is developed for interleaved phase reference generation. Second, a model based controller ensures ZVS at all load conditions in each phase, while a phase compensator (PhC) synchronizes the switch turn-on and turn-off instances with the respective phase reference. A global higher level controller (HLC) generates average current references for the phases while the ZVS operation and synchronization to respective phase reference is achieved locally in each phase and the virtual oscillator network retains the desired phase displacement among the phase references dynamically.

II. Proposed Decoupled Control Method

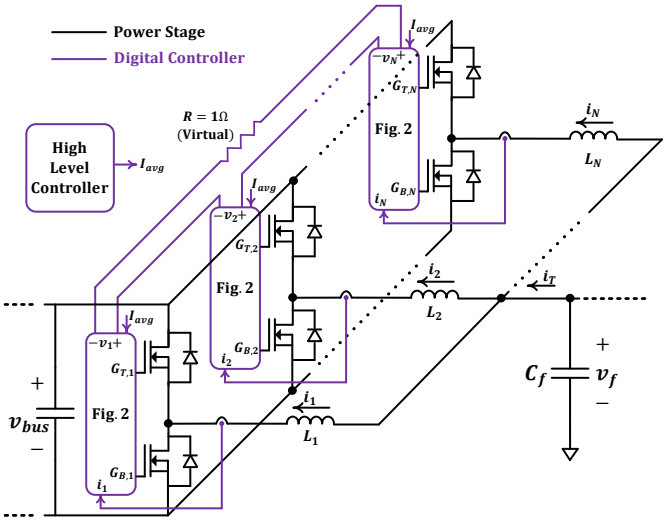

Fig. 1: An N-phase synchronous DC-DC converter.

A synchronous DC-DC converter with N interleaved phases is shown in Fig. 1. The objective of this research is to develop a general framework to achieve simultaneous interleaving and

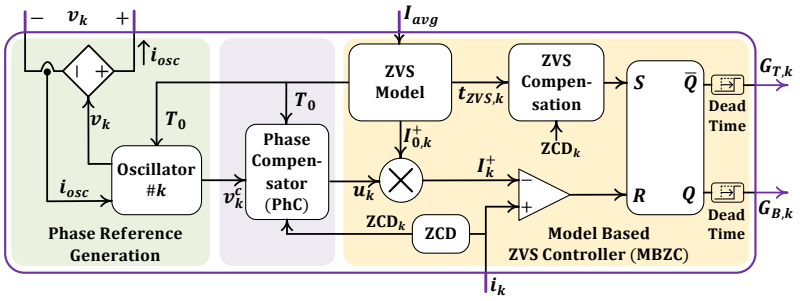

Fig. 2: Proposed control system for dynamic interleaving with $I_{avg} > 0$.

ZVS operation at any load condition. The proposed approach decouples the ZVS operation and interleaving by leveraging a model based ZVS controller (MBZC), an oscillator based interleaved phase reference generation block, and a phase compensator (PhC) that can synchronize the inductor ripple current with the respective phase reference. Fig. 2 shows the proposed control system structure for $I_{avg} > 0$. For positive average current the inductor ripple current is controlled to reach below a negative peak-reference I^- to ensure ZVS of the bottom switch by discharging its output capacitor; whereas the positive peak-reference I^+ is dynamically compensated to achieve synchronization with the phase-reference generated by the oscillator network. For a negative average current, I^+ is utilized to achieve ZVS and I^- is used as a control input for synchronization. The controller operation is similar for $I_{avg} > 0$ and $I_{avg} < 0$. To avoid repetition, the following subsections describe the operation of the control system for a positive average current.

A. High Level Controller (HLC)

The HLC block, shown in Fig. 1, is responsible for achieving a specific control objective for the entire converter. In an interleaved DC-DC converter, the HLC block may be responsible for regulating the DC bus voltage v_{bus} or the voltage across the filter capacitor v_f or average inductor current tracking may be required. Irrespective of the higher level control objective, the HLC block generates an average current reference to be tracked collectively by N phases. This average current reference is sent to the MBZC.

B. Oscillator Based Interleaved Phase Reference Generation

From Fig. 1 and Fig. 2, it is evident that the N oscillators in N phases are coupled through a virtual resistive network using controlled voltage sources and the oscillator network can be analyzed separately as shown in Fig. 3, with fundamental period T_0 as the only input from the MBZC. The output voltage of the k-th oscillator unit is taken as $v_k = \sin\{\phi_k(t)\}$. With respect to an arbitrary reference frame rotating at a frequency $\omega_0 = 2\pi/T_0$, the average phase offset $\bar{\theta}_k$ of the k-th oscillator output is defined as

$$\bar{\theta}_k = \frac{1}{T_0}\int_{t-T_0}^{t} \phi_k(\tau)d\tau \quad - \quad \omega_0 t \tag{1}$$

The desired interleaved equilibrium of the network is defined as

$$\bar{\theta}_k = \frac{2\pi k}{N}, \quad \forall k \in \underline{N} \tag{2}$$

where $\underline{N} := \{1, \cdots, N\}, N \in \mathbb{N}$. This desired equilibrium is identified as the so-called *splay-state* of the oscillators. Splay-state in oscillator networks has been extensively studied and several stabilization techniques have been proposed for different applications [11]–[13]. However, for dynamic interleaving application, a simple and computationally inexpensive method is desirable. The following subsection describes the proposed splay-state stabilization method.

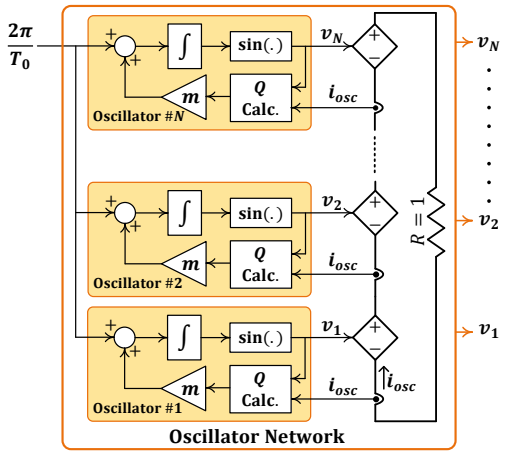

Fig. 3: Proposed oscillator network.

C. Splay-state Stabilization

To stabilize the desired splay-state equilibrium, the oscillator output is chosen as

$$\begin{aligned} \dot{\phi}_k &= \omega_0 + \sum_{n=1}^{\lfloor \frac{N}{2} \rfloor} M_n \times Q_{n,k}(t), \quad \forall k \in \underline{N}; \\ Q_{n,k}(t) &= v_k(t - \frac{T_0}{4n}) \times i_{osc}(t) - v_k(t) \times i_{osc}(t - \frac{T_0}{4n}) \end{aligned} \tag{3}$$

Here, $M_n > 0$ and $\lfloor \frac{N}{2} \rfloor$ denotes the largest integer less than or equal to $N/2$. It is worth noting that $Q_{n,k}$ can be interpreted as the reactive power flowing out of the k-th oscillator assuming a fundamental frequency of $n\omega_0$. For

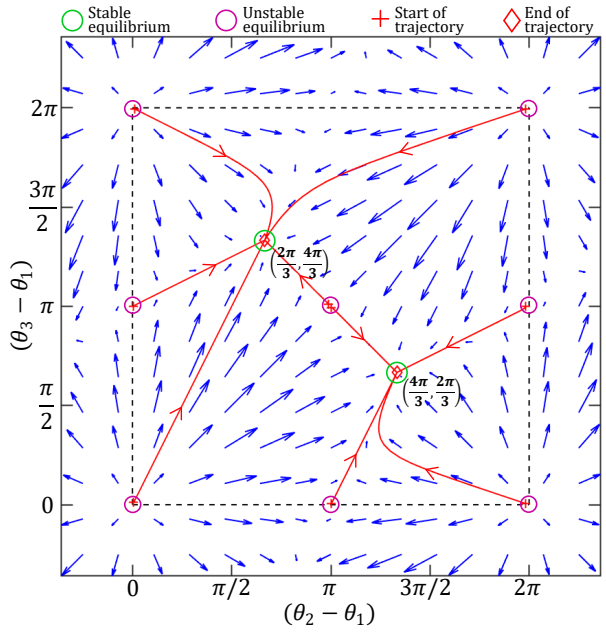

Fig. 4: Phase portrait for $N = 3$.

$N \leq 3$, the oscillators generate sinusoidal output voltage with a single frequency, i.e., ω_0, content; however, for $N > 3$, the oscillators generate periodic output which contain higher order harmonics additional to the fundamental frequency ω_0. In the following subsection, asymptotic convergence of to the splay-state equilibrium is shown for $N \leq 3$.

D. Asymptotic Convergence to Splay-state

For $N \leq 3$, the oscillator output voltages contain only fundamental frequency content and the phase offset can be obtained without averaging the instantaneous phase $\phi_k(t)$. Substituting $i_{osc} = \sum_{k=1}^{N} v_k$, the dynamics of the instantaneous phase offset θ_k can be expressed as

$$\dot{\theta}_k = m \times \sum_{l=1; l\neq k}^{N} \sin(\theta_k - \theta_l) \tag{4}$$

Here, $m = M_1$. From (4), it is worth noting that the proposed phase oscillators are repulsively coupled unlike the Kuramoto model [14]–[16]. The Kuramoto model has been widely used to analyze synchronization, i.e., reaching common frequency, in phase coupled oscillator networks. However, for generating interleaved phase references a common frequency is not enough; at equilibrium each pair of oscillators must maintain a phase displacement of $2\pi/N$.

The splay-state equilibrium set of the oscillators can be alternatively defined as $\theta_{eq} \in \mathbb{R}^N$ where $|\theta_k - \theta_l| = \frac{2\pi}{N}, \quad \forall k, l \in \underline{N}$ and $k \neq l$. For $\theta = [\theta_1 \cdots \theta_N]^T$, we choose

$$V = \frac{1}{2}\dot{\theta}^T\dot{\theta} \tag{5}$$

Taking time derivative of (5) and substituting $\dot{\theta}$ using (4), it follows

$$\dot{V} = m \times \sum_{k=1}^{N}\sum_{l=1}^{N}(\dot{\theta}_k - \dot{\theta}_l)^2 \times \cos(\theta_k - \theta_l) \tag{6}$$

1) $N = 2$: For a collection of two oscillators, solving (4), the equilibrium set is obtained as $\{(0,0),(0,\pi)\}$ where $(0,\pi)$ is the desired interleaved equilibrium. In $\mathbb{G} := \{\theta \in \mathbb{R}^2 : |\theta_1 - \theta_2| < \frac{\pi}{2}\}$, a neighborhood set of the equilibrium $(0,0)$, $V > 0$ and $\dot{V} > 0$. Arguing Chetaev's instability theory, it follows that $(0,0)$ is an unstable equilibrium. Moreover, $\frac{d}{dt}(\theta_2 - \theta_1) = 2 \times m\sin(\theta_2 - \theta_1)$ which has same sign as $(\theta_2 - \theta_1)$ in $\mathbb{G}$. Therefore, the oscillators always tend to diverge from each other and exit $\mathbb{G}$. In the remainder of $[0, 2\pi]$, the quadratic Lyapunov function $\dot{V} < 0$ except at the equilibrium $(0,\pi)$. Therefore, a system of two proposed oscillators starting from any initial point within $\mathbb{G}$ will always exit the set and subsequently converge asymptotically to the desired interleaved equilibrium point.

2) $N = 3$: Without loss of any generality θ_1 can be taken as the reference phase and with respect to θ_1 the relative states are defined as $\theta_{21} := (\theta_2 - \theta_1), \quad \theta_{31} := (\theta_3 - \theta_1)$. Using the relative phase states the oscillator dynamics can be expressed as follows

$$\dot{\theta}_{k1} = m \times \{\sin(\theta_{k1} - \theta_{l1}) + 2\sin(\theta_{k1}) + \sin(\theta_{l1})\}, \quad \forall k, l \in \{2, 3\} \tag{7}$$

Solving (7), the equilibrium set is obtained as $(\theta_{21}, \theta_{31}) \in \{(0,0),(\pi,\pi),(\frac{2\pi}{3},\frac{4\pi}{3}),(\frac{4\pi}{3},\frac{2\pi}{3})\}$. Arguing Chetaev's theorem, it can be shown that $(0,0)$ and (π,π) are both unstable equilibrium points as they lie in the set where $|\theta_{21}| < \frac{\pi}{2}$, $|\theta_{31}| < \frac{\pi}{2}$, and $|\theta_{21} - \theta_{31}| < \frac{\pi}{2}$. For $|\theta_k - \theta_l| > \frac{\pi}{2}$, the negative Lyapunov derivative $\dot{V} < 0$ establishes asymptotic convergence to either of the desired interleaved equilibrium points. Fig. 4 shows the phase-portrait of an oscillator network with $N = 3$. It is evident that except the desired interleaved points all other equilibrium points are saddle points, i.e., unstable. Infinitesimally small perturbation from these saddle points drives the network to one of the desired equilibriums which is shown by the trajectories of the network starting from initial conditions very close to the undesired equilibrium points. The sign of the oscillator output voltage is taken as the phase reference v_k^c.

$$v_k^c(t) = \text{sgn}\{v_k(t)\} \tag{8}$$

Only the HLC and the oscillator network correspond globally to all N phases but the rest of the control system is local to each phase and hence the subscript k denoting k-th phase will be dropped for further analysis.

E. Model Based ZVS Controller (MBZC)

For DC-DC converters, soft-switching is typically achieved by using Critical Mode (CRM) operation. However, for CRM operation there is a finite boundary of the input to output voltage ratio under which ZVS can be achieved. For achieving ZVS for a wide operating range, a unified control method was

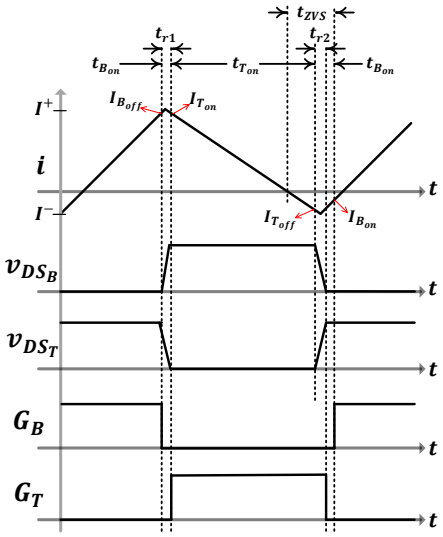

Fig. 5: Typical waveforms for Boost ZVS current control

proposed in [17] using a hybrid current control strategy for Boost PFC, which is equally applicable for a DC-DC buck or boost converter.

In essence, the ZVS controller is similar to a hysteresis controller. The positive and negative peak current references, i.e., I_0^+ and I_0^- respectively, are generated based on the I_{avg} command from the HLC. To ensure ZVS margin, i.e., sufficient positive and negative current swing to discharge the C_{oss} of both the top and bottom power switches, for $I_{avg} > 0$ the negative peak reference is modulated; The positive peak reference is dynamically compensated to synchronize with the respective phase-reference. The negative peak current control enables switching frequency limitation as well. Alternatively, I_0^+ is used for ZVS and I_0^- is utilized for phase synchronization in case of $I_{avg} < 0$. Figs. 5 and 6 summarize the ZVS control scheme, where $Z_n = \sqrt{L/2C_{oss}}$ is defined as the characteristic impedance of a half-bridge, L denotes the inductance, and C_{oss} is the output capacitance of the individual MOSFET switch.

In this section, boost mode of operation,i.e., $I_{avg} > 0$ is used to derive the analytical model and ZVS operation. However, due to the synchronous nature of the topoplogy, it is identically applicable for buck operation, albeit with a change

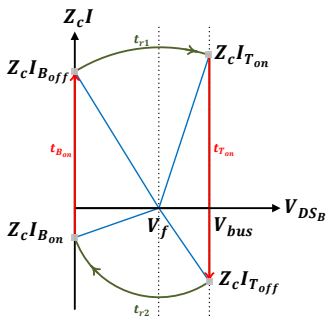

Fig. 6: State trajectory for ZVS in boost operation.

in reference current direction and definition of active switch.

From Fig. 6, an analytical model can be derived [17]. During resonance period t_{r1},

$$\begin{aligned} I_{B_{off}} &= \sqrt{I^{+2} - \left(V_f/Z_n\right)^2}, \\ I_{T_{on}} &= \sqrt{I^{+2} - \left[\left(V_{bus} - V_f\right)/Z_n\right]^2} \end{aligned} \tag{9}$$

During resonance period t_{r2},

$$\begin{aligned} I^- &= -\sqrt{\left\{\left(V_{bus} - V_f\right)/Z_n\right\}^2 + I_{T_{off}}^2}, \\ I_{B_{on}} &= -\sqrt{I^{+2} - \left(V_f/Z_n\right)^2}, \\ I^+ &= 2I_{avg} - I^- \end{aligned} \tag{10}$$

It should be noted that the resonance periods t_{r1} and t_{r2} arise from the dead-time injected between the gating pulses of the top and the bottom switches. For accomplishing both ZVS and switching frequency margin, $I_{T_{off}}$ is constrained by $I_{T_{off}} = -max\left\{0, I_\alpha, I_\beta\right\}$, where

$$\begin{aligned} I_\alpha &= \frac{V_{bus}\left(2V_f - V_{bus}\right)}{Z_n^2}, \\ I_\beta &= \left[\max\left\{\frac{V_f\left(V_{bus} - V_f\right)}{2Lf_{sw_{max}}V_{bus}} - I_{avg}, 0\right\}\right]^2 - \left(\frac{V_{bus} - V_f}{Z_n}\right)^2 \end{aligned} \tag{11}$$

The constrain on $I_{T_{off}}$ leads to the required ZVS time given as

$$t_{ZVS} = -L\frac{I_{T_{off}}}{V_{bus} - V_f} \tag{12}$$

Here t_{ZVS} is defined as the additional time that the top switch needs to be kept turned on after the inductor current reaches zero. Thus, control of t_{ZVS} ensures sufficient negative current for the inductor so that the C_{oss} of active switch, i.e., bottom switch, is completely discharged ensuring ZVS trnasition. This is also evident from Fig. 6 where the state reaches zero voltage (along the y-axis). The MBZC consists of a zero crossing detector (ZCD) which gives a rising edge on the falling slope of the inductor current and vice-versa, shown in Fig. 7. For a positive average inductor current commanded by HLC, the MBZC delays the ZCD output signal by t_{ZVS}. The delayed signal is used to set the $S-R$ latch which consequently turns on the active switch and the negative inductor current resulted by the delay ensures its ZVS turn-on.

F. Phase Compensator (PhC)

The phase compensator update is triggered by the falling zero crossing of the carrier signal v^c of the respective phase. The PhC dynamically modifies the peak current reference I_0^+ as (13) at the n-th zero crossing edge of v^c.

$$I^+[n+1] = u[n] \times I_0^+ = (1+\gamma) \times I_0^+ \tag{13}$$

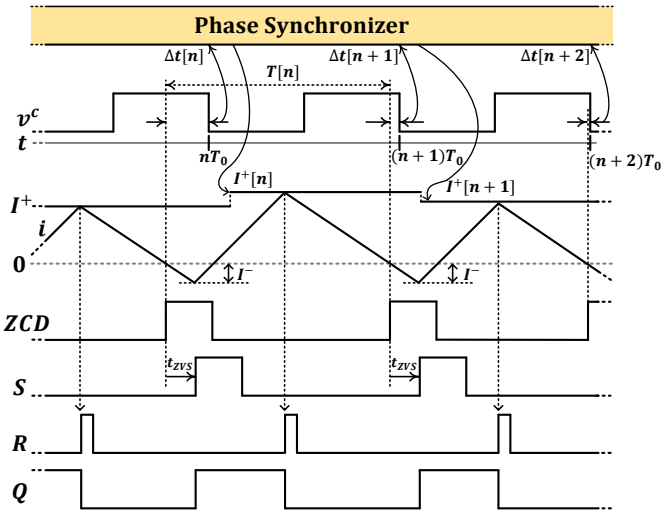

Fig. 7: Timing diagram of phase compensator (PhC).

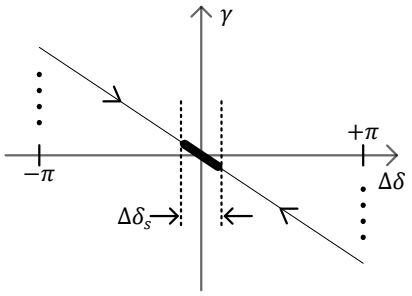

Fig. 8: Sliding surface of PhC

Here $\gamma = -K_{ps} \times \Delta\delta[n] = -K_{ps} \times 2\pi\Delta t[n]/T_0$ where $\Delta\delta$ denotes the phase error between inductor current and respective carrier. The choice of K_{PS} can be made using the dynamics of $\Delta\delta$ given by (14).

$$\Delta\delta[n+1] = \Delta\delta[n] - \xi \times K_{PS}\Delta\delta + (\xi - \hat{\xi}) \qquad (14)$$

where $\xi := \frac{2\pi L I_0^+}{T_0}\left(\frac{1}{v_f} + \frac{1}{v_{bus}-v_f}\right)$ and $\hat{\xi}$ is the estimate of ξ by the controller. From (14), it is evident that $\Delta\delta$ decays exponentially for $\xi \times K_{PS}\Delta\delta > (\xi - \hat{\xi})$. However, on the sliding surface shown in Fig. 8, due to the estimation error a chattering zone emerges whose boundary is given by

$$\max\{\Delta\delta_S\} < \frac{\max\{\xi - \hat{\xi}\}}{K_{PS}\xi} \qquad (15)$$

The estimation error may be dynamically compensated by incorporating an integral part to γ in (13).

$$\gamma(z) = -K_{PS}\left(1 + \frac{T_0/T_i}{1 - z^{-1}}\right) \times \Delta\delta(z) \qquad (16)$$

III. Simulation and Experimental Results

A. Simulation

To evaluate the the proposed controller, a 10 kW three-phase interleaved boost converter with a 400 V DC bus is simulated in PSIM. Fig. 9 shows the system response before and after a step change in the total average current reference, I_T (=$3I_{avg}$) from 44.5 A to 49.5 A. The system reaches the desired interleaved state within three switching cycles with very small transient. The high positive peak of phase currents enable ZVS of the top switches whereas the negative swing of the phase currents of ≈ -4 A ensures that the bottom switches reach ZVS.

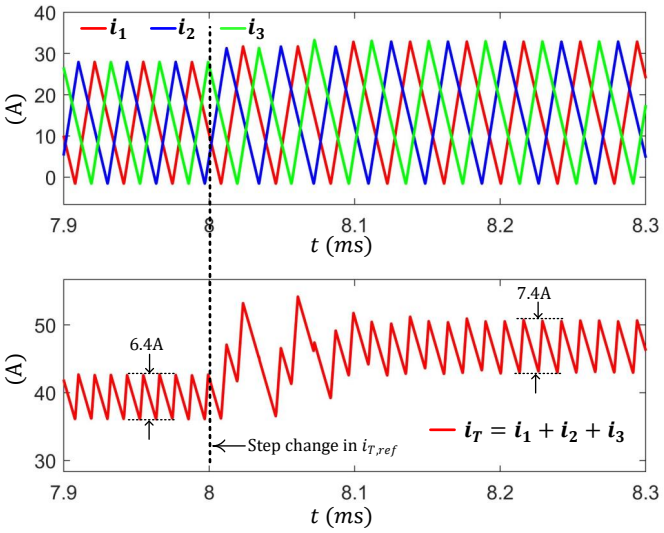

Fig. 9: Simulated response of a 3-phase converter to a step change in average I_T reference.

B. Experiment

To validate each part of the proposed control method, separate experiments are conducted. Firstly, the oscillator network is tested to verify the splay-state stabilization.

1) Splay-state Stabilization in Oscillator Network: To verify the stable splay-state equilibrium, an oscillator network with $N = 3$ is taken. The discrete implementation of the oscillator network is done with a sampling rate of 1 MHz. The three oscillators are initialized with minimal phase mismatch and a fundamental reference frequency of 25 kHz. The network quickly reached the desired splay-state equilibrium. To demonstrate the accuracy of phase displacement and synchronization speed, a step change in reference frequency to 20 kHz is introduced, shown in Fig. 10. It is worth noting that the *sign* of each oscillator output voltage is taken to obtain the phase reference and observed on the scope.

The phase displacement between each pair of phase references is extracted from the experimental test data and shown in Fig. 11, which shows that steady state is reached within one-third of a cycle.

2) ZCD and Peak Detection: Next the ZCD circuit and the peak detector circuit are tested in open-loop condition, i.e., the power switches are controlled with a fixed gate signal. Except the ZVS model block the entire MBZC is implemented using shunt current sensor, digital to analog converter (DAC) and high-speed analog comparators. The peak current reference is

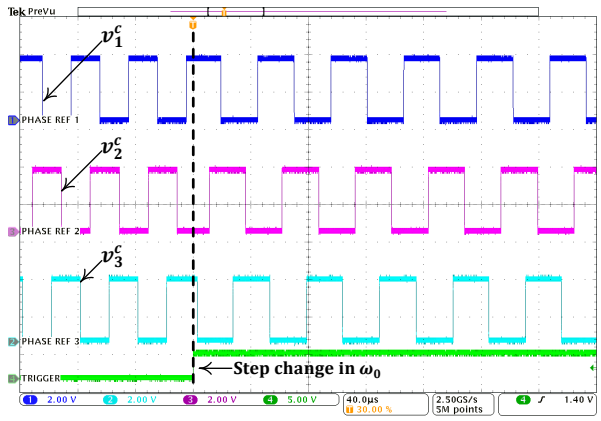

Fig. 10: Phase reference generation ($N = 3$).

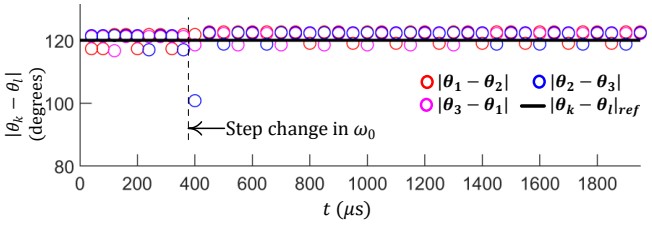

Fig. 11: Phase displacement extracted from Fig. 10.

set at $I_0^+ = 1.73$ A and the peak detection signal, shown in Fig. 12, does not exhibit any significant delay. The ZCD signal exhibits a delay t_{hys} which is caused by the hysteresis band of the ZCD comparator. However, t_{hys} is considered as a fixed offset by the MBZC while dispatching t_{ZVS} and thus can be compensated.

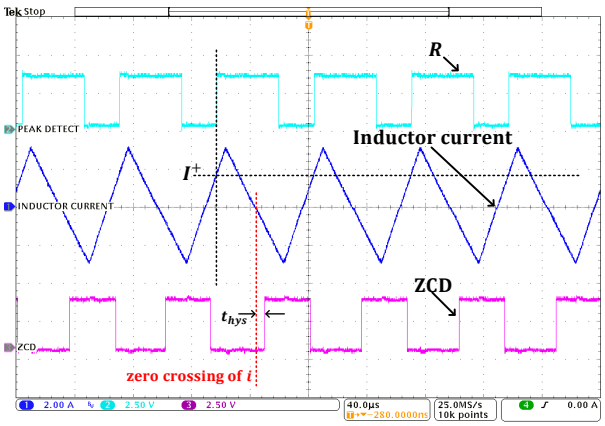

Fig. 12: Peak detection and ZCD in open loop.

3) Phase Compensator (PhC): Fig. 13 shows the operation of the PhC. Since each phase is equipped with a separate phase compensator, results are shown for a single phase. Initially the PhC is not used and therefore, the power switches are controlled based on the nominal peak current I_0^+. Without phase compensation, the inductor current zero-crossing exhibits significant phase mismatch with the phase

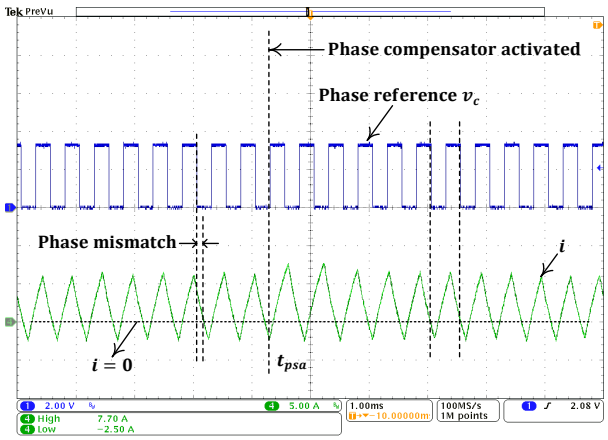

Fig. 13: Phase compensator synchronizes the inductor current with a given phase reference with minimal transient.

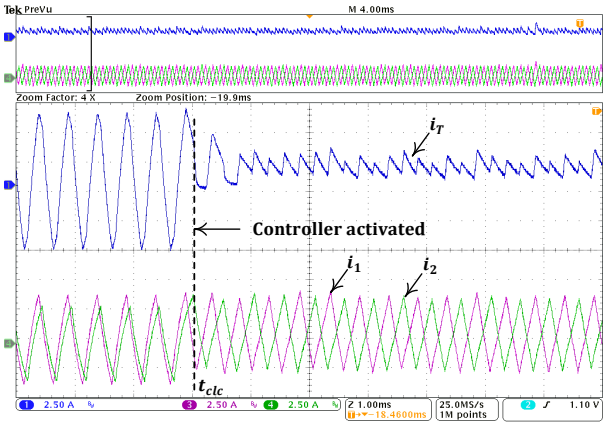

Fig. 14: Phase compensator synchronizes the inductor current with a given phase reference with minimal transient. Without integral compensation in PhC, small oscillations are observed int i_T due to model imperfection.

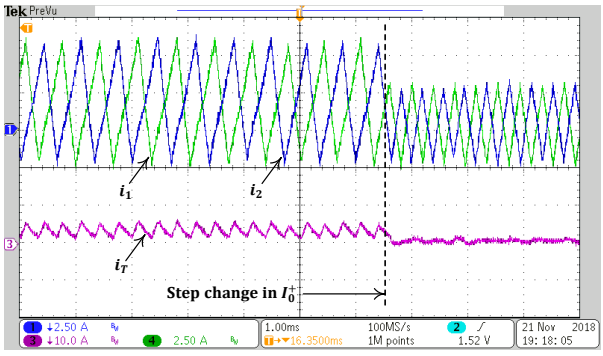

Fig. 15: System response to a step change in peak current reference I_0^+. Integral compensation completely eliminates oscillations due to model mismatch.

reference. At $t = t_{psa}$, PhC is activated with $K_{ps} = 1/4\pi$ and synchronization is immediately achieved with minimal transients in the inductor current.

4) Complete Closed-Loop Control: The proposed complete control system is tested with a two-phase system. To avoid dynamics of the HLC such as a voltage control loop, two DC voltage sources are used as V_{bus} and V_f. Initially, both phases are controlled with a fixed duty-ratio using two carriers with arbitrary phase displacement. In absence of interleaving, the inductor currents of the two phases add to give a large ripple current in the total current i_T, shown in Fig. 14. At $t = t_{clc}$, the proposed control system is activated and interleaving is achieved within one cycle. It is worth noting that to ensure ZVS, I^- is set at -2 A. The effect of interleaving is evident in i_T: the ripple at the effective switching frequency is eliminated and ripple with a period equaling half of that of the phase currents is observed.

To highlight the impact of imperfection in the model used by MBZC, initially the PhC is run without integral compensation. The total current i_T shows small irregular oscillations on top of the expected 2^{nd}-harmonic ripple. Next an integral compensation is added with $T_i/T_0 = 100$ and the oscillation is completely eliminated, shown in Fig. 15. To evaluate the dynamic performance, a step change in peak current reference I_0^+ is introduced from 5.75A to $2.6A$, i.e., a 55% decrease in positive peak-reference. The system retains interleaving with minimal transients, shown in Fig. 15.

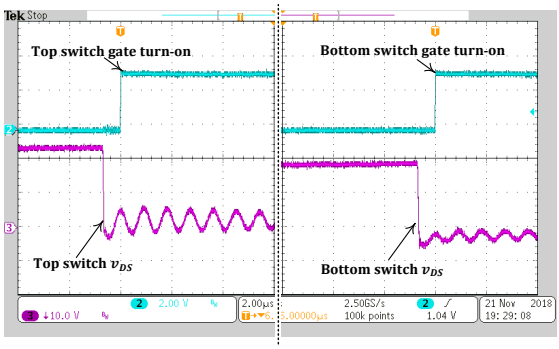

Fig. 16: Gate signals and drain-to-source voltages v_{DS} for top and bottom switches of phase 1.

To illustrate the ZVS transition of the top and bottom switches of one phase, the gate signals and the drain-to-source voltage v_{DS} are shown in Fig. 16. It is evident that for both switches, turn-on signal is sent to the gate after v_{DS} has fallen to zero; therfore, ZVS operation is achieved for both switches.

IV. Conclusion

A control scheme for a multi-phase synchronous DC-DC converter with dynamic interleaving under all loading conditions has been developed. The interleaving among phases under dynamically varying switching frequency conditions is achieved by stabilizing the splay-state equilibrium in a virtual oscillator network. The oscillator outputs are used as phase-references for the phases and the inductor current ripple in each phase is synchronized to its respective reference by a phase-compensator. A complete decoupled higher level model based controller ensures ZVS simultaneously.

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