Variable Switching Frequency Strategy based on Circulating Current Analysis in Paralleled Inverters with Interleaved PWM

Qiao Li
State Key Laboratory of Advanced Electromagnetic Engineering and Technology
Huazhong University of Science and Technology
Wuhan, China
liqiao@hust.edu.cn

Dong Jiang
State Key Laboratory of Advanced Electromagnetic Engineering and Technology
Huazhong University of Science and Technology
Wuhan, China
jiangd@hust.edu.cn

Zewei Shen
State Key Laboratory of Advanced Electromagnetic Engineering and Technology
Huazhong University of Science and Technology
Wuhan, China
shenzw@hust.edu.cn

Yechi Zhang
State Key Laboratory of Advanced Electromagnetic Engineering and Technology
Huazhong University of Science and Technology
Wuhan, China
zhangyechi@hust.edu.cn

Xuan Zhao
State Key Laboratory of Advanced Electromagnetic Engineering and Technology
Huazhong University of Science and Technology
Wuhan, China
zhaoxuan95@hust.edu.cn

Yingtao Ma
State Key Laboratory for Traction and Control System of EMU and Locomotive
Beijing, China
mayingtao@zemt.cn

***Abstract*—A time-domain model describing the circulating current of coupled inductors in paralleled inverters within a switching period is presented in this paper. Using this model, the circulating current can be predicted with interleaved PWM. To better utilize the coupled inductor's saturation limit which is determined by circulating current peak value, variable switching frequency PWM (VSFPWM) is proposed here. With the VSFPWM, both the electromagnetic interference (EMI) and switching losses of the paralleled inverters are well improved, and simultaneously the circulating current peak value is controlled within the limit. Detailed simulation and experimental results are provided to validate the proposed method.**

Keywords—circulating current, paralleled inverters, VSFPWM, interleaving

I. INTRODUCTION

The voltage source inverters (VSIs) are widely used in many power conversion applications and are often connected in parallel to achieve the higher output current, effectively increasing the power rating [1-2]. When three-phase PWM inverters are connected in parallel, a technique of interleaving can be developed to further improve the benefit of paralleled VSIs. In previous literatures, it can be found the interleaved PWM technique can lead to reduction in dc-side and ac-side current ripple, which implies that with interleaved paralleled inverters, the size of dc-link capacitor and line filter can be reduced, increasing power density [3-4]. In addition, paralleled VSIs can also increase the system reliability and has a better EMI performance [5-8].

However, with interleaved carrier signals, the circulating current is introduced due to the instantaneous voltage difference of the paralleled-legs. Circulating current is a serious concern related to the losses and stresses in both active and passive components and should be suppressed. The implementation of coupled inductors provides a high impedance path for circulating current suppression, but a low impedance path for the resultant current. The magnetic coupling between the paralleled phase-legs, by the way of coupled inductors, is a preferred solution to achieve higher power density [9-12]. If a coupled inductor has been already designed and capable of maintaining a certain effective inductance with the required bias current, the maximum value of the flux density in the core is determined by the circulating current peak value. Usually, to achieve a small size of coupled inductor, the maximum flux density is designed close to the saturation flux density of selected cores.

Recently, Variable Switching Frequency PWM (VSFPWM) has been developed for current ripple, torque ripple and dc-link voltage ripple control in two-level or three-level VSI [13-17]. VSFPWM is based on the prediction model and varies the switching frequency cycle by cycle, ensuring the control target within the requirement. Comparing the constant switching frequency PWM (CSFPWM), the VSFPWM can improve the switching losses and EMI of the VSI system. In order to make full use of the maximum flux density of coupled inductors of the paralleled VSIs system, here the VSFPWM for circulating current control of paralleled inverters will be introduced.

The rest of this paper is organized as follows: In Section II, a time-domain model describing the circulating current of coupled inductor in paralleled inverters is introduced. Using the prediction model, VSFPWM for circulating current control

has been developed, and verified through the Matlab/Simulink in Section III, The experimental results are also given for further illustrations in Section IV. Finally, the useful conclusions are summarized in Section V.

II. Circulating Current Prediction

The schematic of the two-paralleled voltage source inverters is shown in Fig. 1, where the same dc-side is shared and the ac-side can be connected to the grid, *L-R* load or an ac motor depending on the application. The circulating current is limited by three coupled inductors, and the LISN is used here to prevent external conductive noise of the dc source. Physical structure of the coupled inductors can be found in Fig. 2, with a typical case of two C-cores. The winding for two inverters are reversing connected around the flux path in the coupled inductor. The flux path for the circulating current is the main path in the coupled inductor and the leakage inductance is contributing to the load inductance. It is clear that the flux saturation is determined by the peak value of the circulating current.

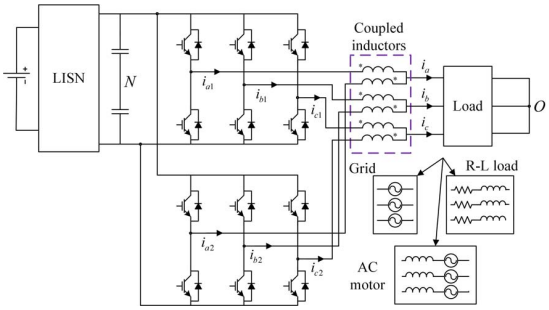

Fig. 1 Paralleled inverters with load

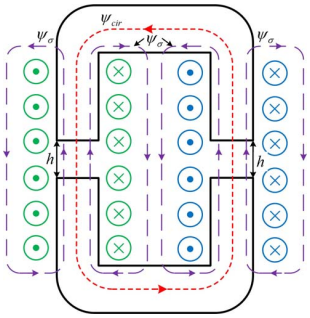

Fig. 2 Typical coupled inductors (Two C-cores)

Phase-*a* is taken as an example to analyze the circulating current shown in Fig. 3. The resultant current (i_a) is the sum of phase-*a* currents of inverter 1 and inverter 2. L_a is the line filter to limit the current ripple and e_a represents the load voltage or grid voltage. V_{cm} is the CM voltage of six-terminal voltage source here. The phase current of each inverter (i_{a1}, i_{a2}) can be decomposed into two parts given as:

$$\begin{cases} i_{a1} = i_u + i_{cir} \\ i_{a2} = i_l - i_{cir} \end{cases} \tag{1}$$

Where both i_u and i_l are the components of phase currents contributing to the resultant current, and the i_{cir} is defined as circulating current component. Ignoring the hardware asymmetry, i_u and i_l are considered equal here. Therefore, the circulating current can be written as:

$$i_{cir} = \frac{i_{a1} - i_{a2}}{2} \tag{2}$$

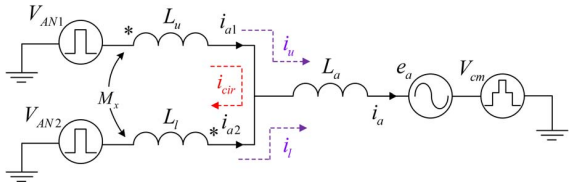

Fig. 3 Single phase equivalent circuit

The coupled inductors provide the magnetic coupling between the phase current of two paralleled inverters, the flux density in the core can be expressed as:

$$B(t) = \frac{1}{2NA}\int (V_{AN1} - V_{AN2})dt \tag{3}$$

Where V_{AN1} and V_{AN2} are the terminal voltage of phase-*a*, A is the core area and N is the number of turns. The maximum value of flux density is an important parameter for the coupled inductor design. In the other hand, according the Kirchhoff's law, the dynamic equation for circulating current design is given as:

$$V_{AN1} - V_{AN2} = (L_u + L_l + 2M_x)\frac{di_{cir}}{dt} \tag{4}$$

Where L_u and L_l represent the self-inductance, and L_u is equal to L_l here. M_x is the mutual inductance for phase-*a*.

Combining (3) and (4), the flux density is proportional to the circulating current if the core is unsaturated. When designing the coupled inductors, the size is determined by the maximum circulating current in operation.

Interleaving is a popular improving method for paralleled inverters. For phase-*a*, Fig. 4 shows a typical case of 180° interleaving for two paralleled inverters in one switching cycle, where the reference signal is compared with the carriers to generate the PWM signals. It can be seen that the two inverters share the same reference voltage, but the carrier of inverter 2 is shifted 180° with respect to the inverter 1. Since the voltage difference between two inverters is balanced in each switching cycle, the average value of circulating current is 0. The circulating current is divided into five sectors by the four edges of duty cycles, and it is symmetric about the midpoint. In each sector, the slope of circulating current can be calculated by (4), and the action time of each sector is determined by the duty cycles. Therefore, the circulating current can be predicted based on the single phase model. With the parameters shown in Table I, and the predicted peak values and the simulated results are plotted together as shown in Fig. 5. It can be observed that the predicted results match pretty well with the simulated and the circulating current is re-set in each switching cycle.

TABLE I. SYSTEM PARAMETERS

Parameter	Value
DC-link voltage (V_{dc})	200 V
Modulation index (m)	0.8
Load resistance (R)	5 Ω
Line inductance (L)	1 mH
Constant Switching frequency (f_c)	20 kHz
Coupled inductors: self-inductance (L_u=L_l), mutual inductance (M)	0.5 mH, 0.5 mH

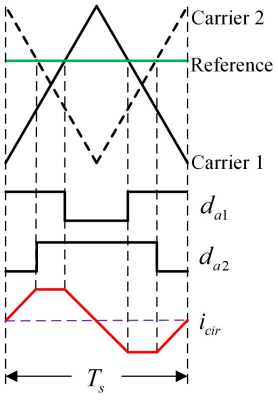

Fig. 4 Circulating current in one switching cycle

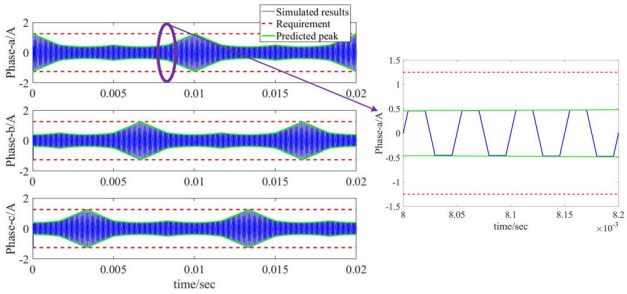

Fig. 5 Circulating current comparison

III. VARIABLE SWITCHING FREQUENCY PWM

Based on the time-domain prediction model of circulating current, variable switching frequency PWM is developed for circulating current control. Different from the traditional CSFPWM, the VSFPWM is with the circulating current prediction module and switching period updating module as shown in Fig. 6. When the circulating current prediction module receives a sampling signal, it reads three-phase duty cycles from the controller, and predicts the circulating current in real time. The maximum peak value of three-phase circulating current is developed to switching frequency updating module. To assure all coupled inductors meeting the circulating current requirement, the maximum peak value is selected and the updated switching period is obtained by (5). If a complete carrier wave is generated, the sampler produces a sampling signal and the next cycle is coming. Here, the circulating current requirement is set to 1.25 A for VSFPWM, which is defined as the maximum peak value for CSFPWM in a fundamental period.

$$T_N = T_s \frac{i_{cir\_require}}{\max(i_{cir\_peak\_a}, i_{cir\_peak\_b}, i_{cir\_peak\_c})} \quad (5)$$

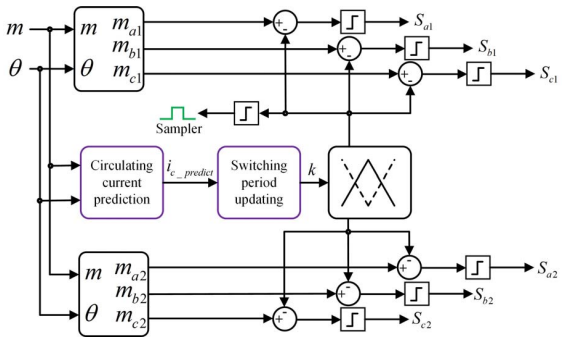

Fig. 6 VSFPWM control block diagram

As a result, the switching frequency of paralleled inverters is changing cycle by cycle to control the maximum peak value equal to the requirement. From Fig. 7, it can be seen that the switching frequency of VSFPWM is varying below 20 kHz used in CSFPWM, and a reduction of 31% in average switching frequency is achieved with VSFPWM. From Fig. 8 and Fig. 9, both the CSFPWM and the VSFPWM satisfy the requirement, which illustrates the validity of the circulating current prediction model and the availability of the proposed VSFPWM strategy.

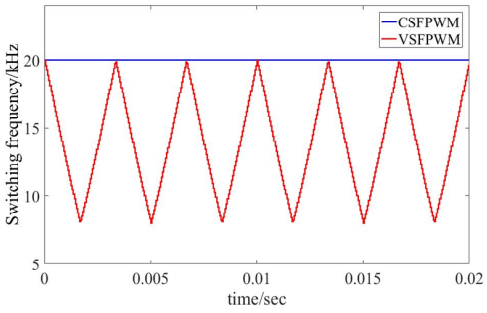

Fig. 7 Switching frequency comparison (simulation result)

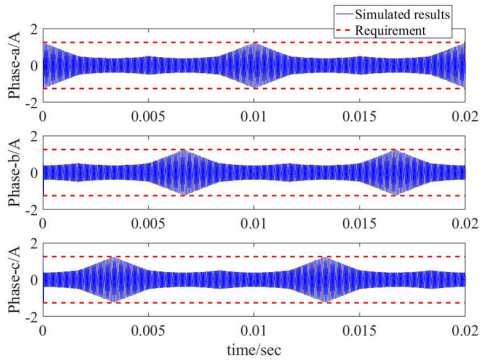

Fig. 8 Circulating current with CSFPWM (simulation result)

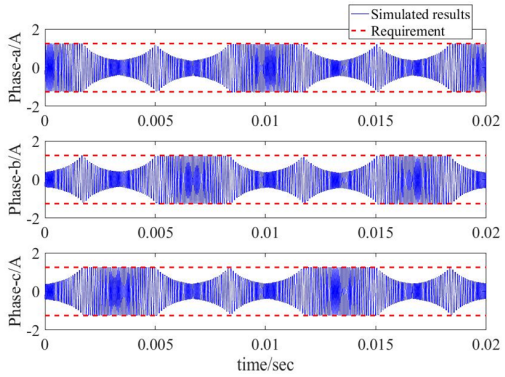

Fig. 9 Circulating current with VSFPWM (simulation result)

IV. Experimental Verification

In order to verify the variable switching frequency methods proposed in previous Sections, the experiment has been carried out in paralleled VSIs connected to the *L-R* load, with the identical parameter shown in Table I. The experimental setup is shown in Fig. 10. The R&S oscilloscope is used to record the phase current and the circulating current is derived through the "math" function. The conductive EMI is measured by R&S EMI test receiver.

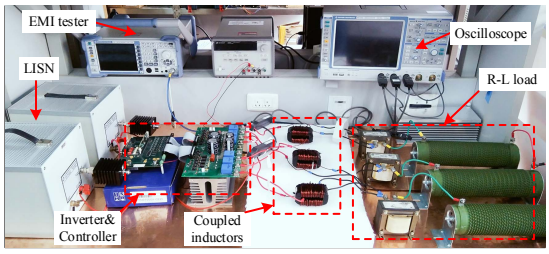

Fig. 10 Picture of experimental set-up

Fig. 11 shows the switching frequency comparison stored in DSP. It can be seen that the switching frequency of VSFPWM varies below the CSFPWM, from 8 kHz to 20 kHz. A parameter describing the switching losses is defined as (6), and then loss saving can be obtained by (7). Focusing on Table II, the VSFPWM can save up to 30.2% in switching losses for 180º interleaved PWM.

$$E_{sw} = \sum_{k=1}^{N} |\, i(t_k) \,| \tag{6}$$

$$\begin{aligned} Loss\ \text{Saving} &= (1 - \frac{E_{sw,VSFPWM}}{E_{sw,CSFPWM}}) \cdot 100\% \\ &= (1 - \frac{\sum_{k=1}^{N1} |\, i(t_k) \,|}{\sum_{k=1}^{N2} |\, i(t_k) \,|}) \cdot 100\% \end{aligned} \tag{7}$$

In the above formula, $i(t_k)$ is the instant current value in the kth commutation and N represents the number of commutations per fundamental period. Obviously the number of commutations in VSFPWM is less than the CSFPWM (N_1<N_2).

TABLE II. Comparison of Average Swiching Frequency and Switching Losses

PWM method	Peak value of circualting current	Number of commutations	E_{sw}
CSFPWM	1.25 A	200	2037.1 A
VSFPWM	1.25 A	141	1422.2 A

From Fig. 12 and Fig. 13, it can be clearly observed that the circulating current peak value of VSFPWM is same to the CSFPWM, satisfying the requirement, which verifies the validity of the proposed method. Thanks to the switching frequency variation, the VSFPWM has better EMI performance with respect to the CSFPWM, where the EMI standard of DO-160E is adopted [18]. Comparing with CSFPWM, there is an approximate reduction of 20 dB in 150-800 kHz range with VSFPWM as shown in Fig. 14.

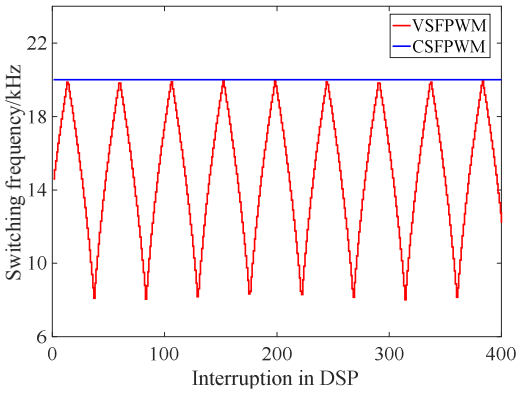

Fig. 11 Switching frequency comparison (experimental result)

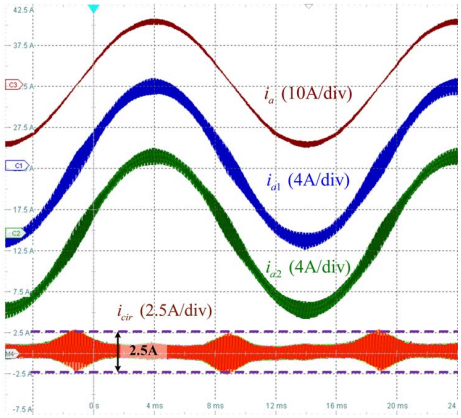

Fig. 12 Circulating current with CSFPWM (experimental result)

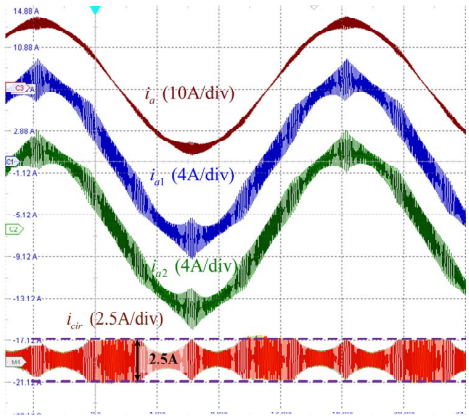

Fig. 13 Circulating current with VSFPWM (experimental result)

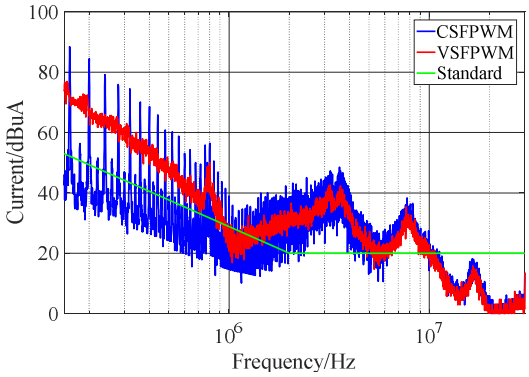

Fig. 14 EMI comparison

V. CONCLUSION

In this paper, a time-domain circulating current prediction model for paralleled inverters with coupled inductors has been proposed, based on which VSFPWM is designed and implemented to the circulating current control. The main objective is to taking the full advantage of maximum flux density of the coupled inductors in a paralleled VSIs system. The proposed algorithm can improve the system EMI performance and increase the system efficiency.

ACKNOWLEDGMENT

This paper is based on the project of State Key Laboratory for Traction and Control System of EMU and Locomotive in China (Contract No. 2017YJ176)

REFERENCES

[1] C. L. Chen, Y. Wang, J. S. Lai, Y. S. Lee, and D. Martin, "Design of parallel inverters for smooth mode transfer microgrid applications," IEEE Trans. Power Electron., vol. 25, no. 1, pp. 6–15, Jan. 2010.

[2] S. Schroder et al., "Modular high-power shunt-interleaved drive system: A realization up to 35 MW for oil and gas applications," IEEE Trans. Ind. Appl., vol. 46, no. 2, pp. 821–830, Mar./Apr. 2010.

[3] C. Casablanca and J. Sun, "Interleaving and harmonic cancellation effects in modular three-phase voltage-sourced converters," in Proc. IEEE Workshops Comput. Power Electron., Jul. 2006, pp. 275–281.

[4] Stephanie K. T. Miller, Troy Beechner, Jian Sun, "A Comprehensive Study of Harmonic Cancellation Effects in Interleaved Three-Phase VSCs", Power Electronics Specialists Conference 2007. PESC 2007. IEEE, pp. 29-35, 2007.

[5] N. Seke and H. Uchino, "Which is better at high power reactive compensation system, high PWM frequency or multiple connection," *proc. of IAS* 1994, pp. 946-953.

[6] M. Baumann and J. W. Kolar, "Parallel connection of two three-phase three-switch buck-type unity-power-factor rectifier systems with DClink current balancing," IEEE Trans. Industrial Electronics, vol. 54, no. 6, pp. 3042-3053, Dec. 2007.

[7] Z. Ye, P. Jain, P. Sen, A full-bridge resonant inverter with modified phase shift modulation for high frequency AC power distribution applications, IEEE Trans. on Industrial Electronics, Volume 54, No.5, Oct. 2007, pp 2831-2845

[8] K. Wada and T. Shimizu, "Reduction Methods of Conducted EMI Noise on Parallel Operation for AC Module Inverters," IEEE PESC 2007, pp. 3016-3021 (2007).

[9] F. Forest, T. Meynard, E. Laboure, V. Costan, E. Sarraute, A. Cuniere, and T. Martire, "Optimization of the supply voltage system in interleaved converters using intercell transformers," IEEE Trans. Power Electron., vol. 22, no. 3, pp. 934–942, May 2007.

[10] F.Forest, E.Laboure, T.Meynard, and V.Smet,"Design and comparison of inductors and intercell transformers for filtering of PWM inverter output," IEEE Trans. Power Electron., vol. 24, no. 3, pp. 812–821, Mar. 2009.

[11] J. Salmon, J. Ewanchuk, and A. Knight, "PWM inverters using split wound coupled inductors," IEEE Trans. Ind. Appl., vol. 45, no. 6, pp. 2001–2009, Nov./Dec. 2009.

[12] R. Hausmann and I. Barbi, "Three-phase dc-ac converter using four state switching cell," IEEE Trans. Power Electron., vol. 26, no. 7, pp. 1857–1867, Jul. 2011.

[13] D. Jiang and F. Wang, "Variable switching frequency PWM for three phase converters based on current ripple prediction," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4951–4961, Nov. 2013

[14] Dong Jiang, Qiao Li, Xun Han, Ronghai Qu, "Variable switching frequency PWM for torque ripple control of AC motors," ICEMS 2016, Chiba, Japan

[15] Fei Yang, Allan Ray Taylor, Hua Bai, Bing Cheng, and Ahmad Khan, "Using d-q Transformation to Vary the switching Frequency for Interior Permanent Magnet Synchronous Motor Drive Systems," IEEE TRANSACTIONS ON TRANSPORTATION ELECTRIFICATION, VOL. 1, NO. 3, OCTOBER 2015.

[16] Qiao Li, Dong Jiang, "Variable Switching Frequency PWM Strategy of Two-Level Rectifier for DC-Link Voltage Ripple Control," IEEE Trans. Power Electron., vol. 33, no. 8, pp. 7193–7202, Aug. 2018.

[17] Subhadeep Bhattacharya, Sourabh Kumar Sharma, Diego Mascarella, Géza Joós, "Sub-fundamental Cycle Switching Frequency Variation Based on Output Current Ripple Analysis of a Three-Level Inverter" IEEE Journal of Emerging and Selected Topics in Power Electronics, Volume: 5, Dec. 2017.

[18] The Boeing company, " Electromagnetic Interference Control Requirements for Composite Airplanes" , 2004.8