Effect of Current Measurement Timing and Antialiasing Filter in a Single-Phase Inverter

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***Abstract*—Synchronous current measurement is a standard method for digital inverter control. Conventionally the measurement is sampled at pulse-width modulation carrier peaks to provide an average value of the current over the modulation cycle. With increased switching frequencies of inverters, the accuracy of the current measurement may suffer, especially during short output voltage pulses at high duty cycles. This paper focuses on the effect of sampling instant timing of the current measurement of a single-phase H-bridge inverter. Experimental tests show that proper analog to digital conversion timing and antialiasing filter design will significantly improve the current measurement accuracy.**

***Index Terms*—Single-phase inverter, Current measurement, Antialiasing filter**

I. Introduction

Synchronous current measurement has been a standard method for digital inverter control for decades [1]. The inverter current control performance is limited by several delays from the measurement to eventually pulse-width modulated (PWM) output voltage waveform. In the literature, the primary delay sources have been reported to be the antialiasing filter, analog to digital conversion (ADC), computation delay, gate driver, and switching delays [2], [3].

In general, the current control is limited by the output filter, the switching frequency f_{sw} of the inverter, and system delays. Half of the switching frequency determines the Nyquist frequency of the control system. The current measurement and the computed PWM voltage reference value are zero-order hold (ZOH) by nature for digital PWM [4].

Current measurement errors impair the converter control. For example, in single-phase inverters the current measurement scaling and offset errors have been compensated with a proportional resonant controller [5]. For three-phase inverters scaling and offset error compensation methods, such as periodic disturbance observer and proportional integral plus two resonant controllers have been proposed [2], [3], [6], [7]. These compensation methods are primarily executed in the dq-frame.

The switching frequencies of modern inverters have been consistently increasing, especially as a result of advances in switch semiconductor technologies [8], [9]. For grid-connected inverters, the increased switching frequencies allow the grid filter inductive components to be dimensioned smaller [10], [11]. Even with relatively high switching frequencies (above tens of kilohertz), the current measurement accuracy is very dependent on the correct timing of the measurement.

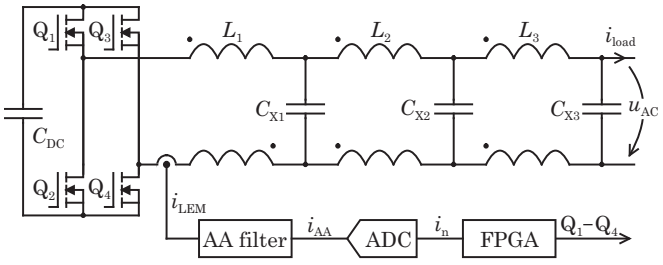

Fig. 1. Single-phase grid-forming inverter with an EMI filter. The current measurement i_{LEM} is filtered with an antialiasing filter, then converted from analog to digital format, and finally fed to the controller. i_{n} is the sampled current measurement.

In this paper, the effects of the antialiasing filter and current sample timing on the current measurement accuracy are studied. The sample timing compensation procedure is described with and without an antialiasing filter. A fixed delay compensation was used in this study, and one of the primary research questions of this paper is to find out whether a fixed delay is sufficient for current control at relatively high switching frequencies (tens of kilohertz). The study is performed with an experimental test set-up for a single-phase grid forming inverter, shown in Fig. 1. The inverter control unit is able to communicate the measured samples to a PC for post processing and analysis.

II. Current measurement of a single-phase inverter

The current measurement sample should give the average value of the load current over the PWM cycle. Conventionally the inverter output current is measured at the mid-point of the PWM cycle, or at the beginning and the mid-point of the PWM cycle. These two points are the PWM carrier triangle waveform peaks. In an ideal system, these two points give the average current over the PWM cycle, and are free of switching noise. In an actual system, during high reference duty cycles, the PWM produces very short pulses. Sampling the current during a short pulse will potentially lead to a sample with induced high frequency noise, or sampling an erroneous value

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during a current slope with very high di/dt. This problem was addressed with a single sampling current measurement method, which alternates the sampling peak of the carrier based on the duty cycle [12]. However, this method does not address the measurement error produced by the measurement loop delays.

A. Measurement error sources

The current measurement is subject to delays and phase-shift caused by the antialiasing filter, ADC, and digital signal processing. In addition, the actual voltage pulse generated by the inverter is not precisely in phase with the carrier, due to gate driver and switching delays, and an offset generated by dead time [3]. The delays also drift during operation. For example, the switching delays are a function of switched current. Also, dead time originated shift may have a discontinuity when the load current changes polarity. Other sources for measurement drift are temperature and component aging [13]. Also, the output of the antialiasing filter will not be a pure sinusoidal signal, as the duty cycle will have an effect on the waveform.

In a single-phase converter, the current measurement error must be minimized, because it may be the only measurement alongside the DC link voltage measurement. When considering the case that there is no antialiasing filter and the measurement is only limited by the sensor and the ADC, current measurement is problematic at high switching frequency with short PWM pulses. The problem arises when modulation duty cycle is high, which results in output voltage pulses in the range of hundreds of nanoseconds. During the short pulse, the current will change with an amplitude of the current peak-to-peak ripple. This will result in high di/dt. This presents an issue on the timing of the current measurement, as multiple delays in the system can cause the triggering instant to differ significantly from the center of the sampled waveform.

The measurement error that is originated by the delays has a different effect depending if the current is sampled once or twice per PWM period. Obviously, if the delays are not properly compensated, the value of each sample will be erroneous in both cases. For the single sampling method, the error will produce a DC offset on the current measurement signal. Compensation of such an error in a single-phase inverter may be hazardous, since the error may be originated by the measurement loop, or it may actually be a DC offset in the current. In the case of two samples per period, the measurement signal will have a ripple at sampling frequency. This is because the samples will be from a triangular ripple current produced by the inverter. Therefore, one of the samples will have a value that is smaller than the average current value over the PWM cycle, and the other sample value will be larger than the average current value. With this approach, the mean value of the last two samples can be used to calculate the load current average over the PWM cycle. The drawback of the additional mean value calculation is the additional delay in the current control, which limits the bandwidth [4].

The antialiasing filter dimensioning, namely the RC cut-off frequency, affects the phase-shift between the switching current ripple and the filter output signal that is sampled by the ADC. If the RC circuit is dimensioned for a lower cutoff frequency than f_{sw}, the current ripple will be attenuated, but the phase-shift of the filter will cause significant delay to the measurement. On the other hand, if the RC circuit is dimensioned for a higher cutoff frequency than f_{sw}, the phase-shift will be less than 45°, and the bandwidth limitation of the current loop will not as be significant, because the effective control bandwidth is limited by the Nyquist frequency of PWM ($f_{\mathrm{Ny}} = f_{\mathrm{sw}}/2$). In this case, the timing of the measurement will play a much bigger role in order to limit the measurement error.

B. Delay compensation tuning

The objective of the current measurement is to provide an accurate sample of the average current and to have high bandwidth for control loop. Therefore, two current samples are measured per PWM cycle. In order to minimize the phase lag, and consequently maximizing the measurement bandwidth, the antialiasing filter cutoff frequency is tuned above the switching frequency.

In [14] an antialiasing filter was used, but the triggering of the current measurement was still done at PWM carrier peaks. If the phase-shift caused by the antialiasing filter is not compensated, it will cause a measurement error. In this paper, the compensation is referred to as the required delay on the ADC trigger signal that will provide an accurate sample of the average current.

The approach used in this paper is to use an antialiasing filter with a higher cutoff frequency than f_{sw}, and compensate the delay generated by the filter in the timing of the current measurement. In order to minimize the delays of the current control loop, the voltage reference for PWM is updated as soon as the computation is executed [15].

When the sampling instant is delayed from the carrier peaks, it will cause for the sampling to be during a switching operation of the inverter. Here the trade-off will be done between the high di/dt originated error and using an antialiasing filter and introducing a delay, which has to be compensated. The antialiasing filter will reduce the switching noise seen by ADC, which is shown in Section III.

The following delays in the measurement can be considered almost constant during operation: analog to digital conversion, computation, and gate driver delays. The switching delays vary as a function of current, and antialiasing filter output as a function of duty cycle. A few approaches can be taken in the compensation of the switching delays and loading condition. A fixed delay compensation value is the simplest solution, and it was selected for this study. The effectiveness of this approach is demonstrated in Section III.

The delay compensation value was first calculated as the sum of the described delays and the final value was fine tuned experimentally to achieve the best result. The primary delay was introduced by the antialiasing filter. When the cutoff

TABLE I
EXPERIMENTAL SETUP.

f_{out}	output frequency	50 Hz
f_{sw}	switching frequency	50 kHz
f_{ctrl}	control frequency	100 kHz
f_{s}	current sampling frequency	100 kHz
f_{AA}	AA cutoff frequency	70 kHz
t_{DT}	dead time	250 ns
t_{ADC}	AD conversion time	438 ns
u_{AC}	output voltage	230 V
u_{DC}	DC link voltage	365 V
L_1	Primary inductance	410 µH
L_2	1st EMI filter inductance	2.4 µH
L_3	2nd EMI filter inductance	2.4 µH
C_{X1}	1st X-capacitance	9.1 µF
C_{X2}	2nd X-capacitance	2.2 µF
C_{X3}	3rd X-capacitance	9.3 µF
	current sensor	LTSR 15-NP LEM
	gate driver	Si8271DB-IS
	ADC	MAX11115
	FPGA	10CL010YU256I7G

frequency of the antialiasing filter was 70 kHz, the phase lag at the switching frequency of $f_{\mathrm{sw}} = 50$ kHz is 37°, which represents a delay of 2.1 µs for the switching frequency component. Rest of the delay sources are presented in Table I and the final compensation value was found at 3.5 µs.

Another approach for the delay compensation would take into account the varying delays caused by the switching delays and the effect of varying duty cycle on the phase lag of the antialiasing filter. A grid forming inverter must be able to feed various loads, including non-linear and capacitive loads. As a result, this compensation method would require an extensive look-up table for each condition. Therefore, this method is left for future research.

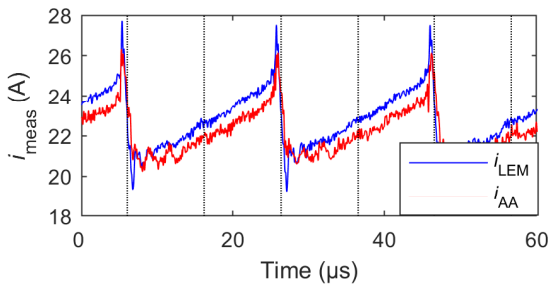
III. EXPERIMENTAL RESULTS

The effect of current measurement timing and antialiasing filter were experimentally tested with a single-phase H-bridge converter. Bipolar modulation was used and the switching frequency was $f_{\mathrm{sw}} = 50$ kHz. The measurement setup information is given in Table I. The system was tested with several loading conditions:

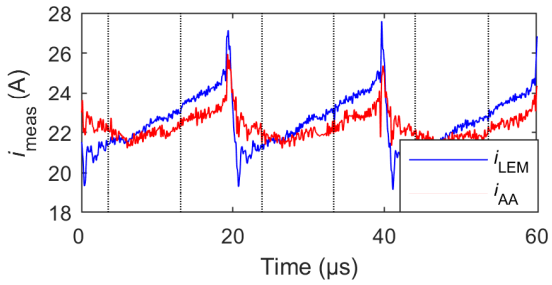
- no-load
- 26.6 Ω
- 15.3 Ω
- 86 µF
- 86 µF and 186 Ω in parallel

During the no-load condition, the inverter feeds the grid filter. The total capacitive loading imposed by the EMI filter is 20.6 µF.

The first set of measurements were performed by measuring the current sensor output signal (i_{LEM}) and the antialiasing filter output (i_{AA}) from the converter. The measured waveforms without and with the antialiasing filter capacitor are shown in Fig. 2. The sampling time of the current measurement was manually tuned to minimize the difference between the two consecutive measurement ADC samples (Δi_{n}). Without



(a) No AA filter capacitance



(b) With AA filter

Fig. 2. Current measurements from the current sensor output (i_{LEM}) and antialiasing filter output (i_{AA}). Measured current measurement sampling trigger signal is indicated with a dashed line. Both measurements are with compensated sample timing to minimize the measurement error.

the antialiasing filter the timing error was compensated by delaying the trigger signal by 500 ns from the carrier peaks and with the antialiasing filter by 3.5 µs. It can be seen from Fig. 2(a) that due to high di/dt even a small change in timing of the current sample at the falling current edge will significantly affect the sampled value.

Next, the sampled measurements from the FPGA control were logged with four different current measurement cases:

- without antialiasing filter capacitor and sampled at carrier peaks
- without antialiasing filter capacitor and sampled at compensated instants (500 ns delay)
- with antialiasing filter and sampled at carrier peaks
- antialiasing filter and sampled at compensated instants (3.5 µs delay)

These measurements were logged at no-load condition and with a 15.3 Ω resistive load. The results can be seen in Fig. 3. The effect of compensating the timing without the antialiasing filter capacitor has a very small impact on the sampled current measurement. The same applies to adding the antialiasing filter and sampling the current at carrier peaks. Once the antialiasing filter is used and proper compensation is applied, the difference between the consecutive current measurements is significantly reduced. The mean value of the absolute value of the difference between the two consecutive current samples (mean$|\Delta i_{\mathrm{n}}|$) is shown for each measurement in Fig. 3. It can be seen that the loading condition does not have a very big impact on the difference between the two consecutive samples, regardless of

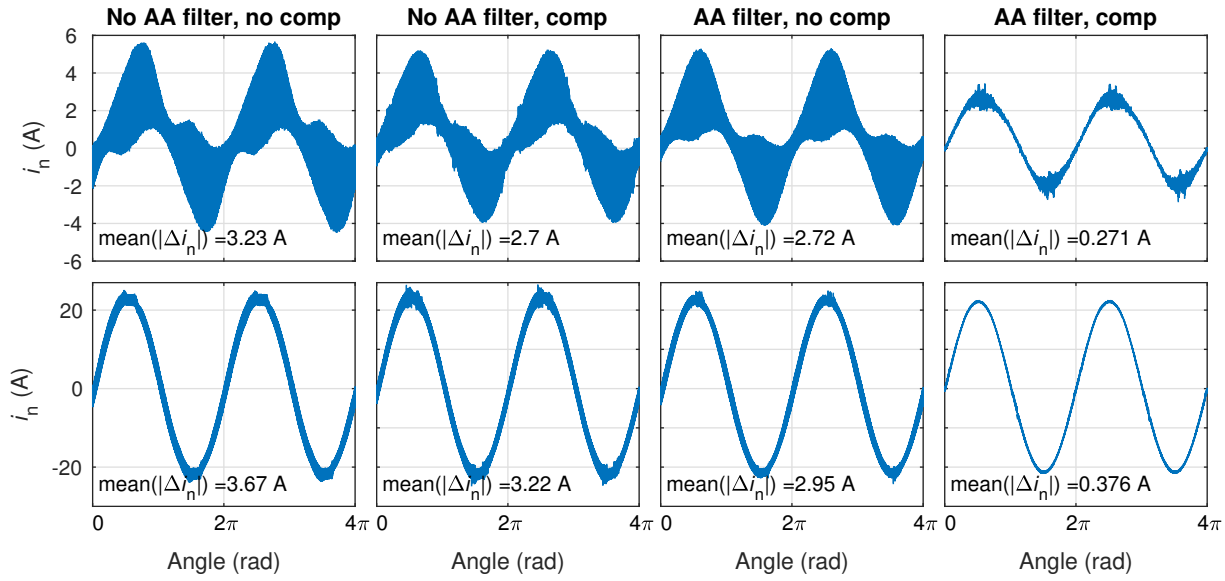


Fig. 3. Current measurements from the converter control. No load conditions on top graphs and resistive load of 15.4 A on bottom graphs. Δi_n is the difference between the two consecutive current samples.

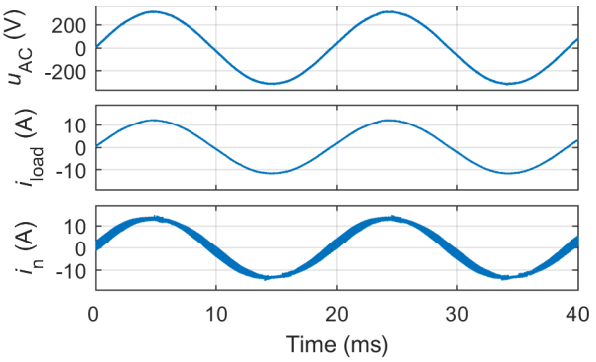


Fig. 4. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $R = 26.6\,\Omega$, and the current was sampled at carrier peaks.

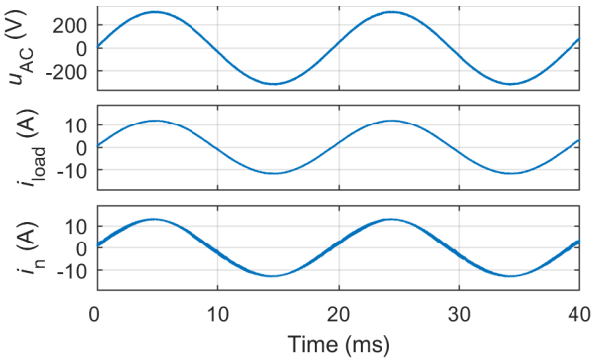


Fig. 5. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $R = 26.6\,\Omega$, and the current sample was compensated with a 3.5 µs delay.

the timing of the samples within the PWM cycle.

Next, the effect of loading condition and the delay compensation on the control are studied. For the following measurements, the antialiasing filter was used ($f_\mathrm{AA} = 70\,\mathrm{kHz}$). Now the loading conditions under study are $R = 26.6\,\Omega$, $C = 86\,\mu\mathrm{F}$, and parallel connected $C = 86\,\mu\mathrm{F}$ and $R = 186\,\Omega$. With the parallel connected RC load case, only current controller was used. The oscilloscope for the measurements was Agilent DSO 6104A, the output voltage u_AC was measured with Tektronix PS5210 differential voltage probe, and the load current i_load with Rohde & Schwarz RT-ZC20 30A current probe. The current samples from the FPGA (i_n) are illustrated with the measurements. It should be noted, that the samples from the FPGA and the measured values from the oscilloscope are manually aligned. The total harmonic distortion for the 50 first harmonics for the measured grid voltages and currents are shown in Table II.

The measurements for resistive loading condition and when the current was sampled at carrier peaks is shown in Fig. 4, and when the current sample was delay compensated in Fig. 5. The grid voltage and current show very little change, regardless of the sampling instant. Only the sampled current and the THD values in Table II have a noticeable difference.

The measurements for capacitive load of $C = 86\,\mu\mathrm{F}$ are shown in Figs. 6–7. In this loading condition, the load current has some disturbance at low current amplitudes when the measurement instant is not compensated. Also, the sampled current has a more distorted waveform compared to the compensated measurement. The current THD is improved by 0.89 % when the sampling is compensated.

The last loading condition was parallel connection of $C = 86\,\mu\mathrm{F}$ and $R = 186\,\Omega$. The measurements are shown in

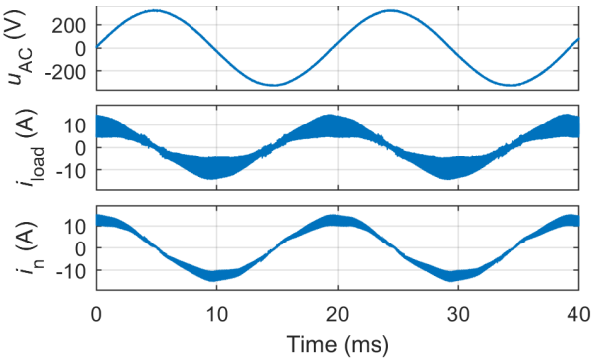


Fig. 6. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $C = 86\,\mu\text{F}$, and the current was sampled at carrier peaks.

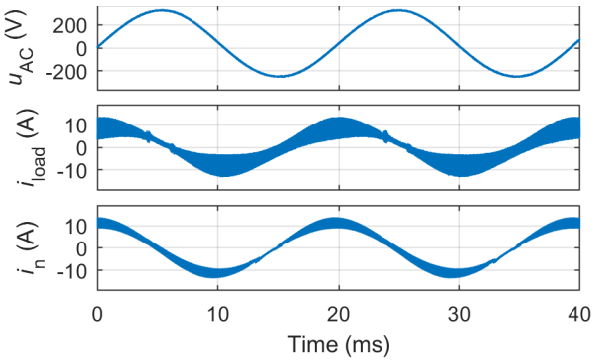


Fig. 8. Grid voltage (top), load current (middle), sampled current (bottom), when the load was parallel connected $C = 86\,\mu\text{F}$ and $R = 186\,\Omega$, and the current was sampled at carrier peaks.

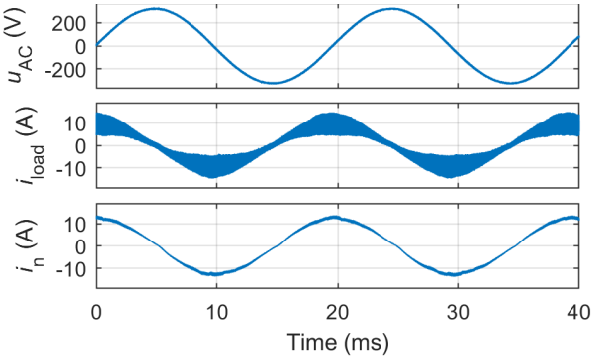


Fig. 7. Grid voltage (top), load current (middle), sampled current (bottom), when the load was $C = 86\,\mu\text{F}$, and the current sample was compensated with a 3.5 µs delay.

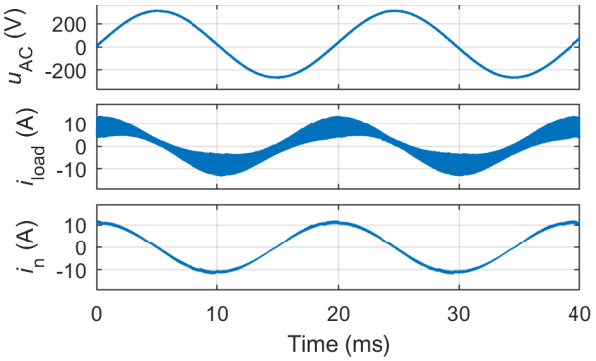


Fig. 9. Grid voltage (top), load current (middle), sampled current (bottom), when the load was parallel connected $C = 86\,\mu\text{F}$ and $R = 186\,\Omega$, and the current sample was compensated with a 3.5 µs delay.

Figs. 8–9. Again, a slight disturbance can be seen in the load current when the current is sampled at the carrier peaks. Now the load current THD is improved 0.82 % when the sampling is compensated.

When the Figs. 4–9 are studied, the effect of duty cycle and loading condition on Δi_n can be determined. The difference between the two consecutive current samples is more dependent on the duty cycle than the loading condition. This can be seen as Δi_n has the smallest value at load voltage peaks, during which the duty cycle is high. Similarly Δi_n is proportionally higher when the load voltage and the duty cycle are near zero. This trend applies to all measured cases. Even though Δi_n varies primarily as a function of the duty cycle, the absolute values change depending on loading condition. Therefore, in order to fix the residual measurement error, an extensive manual tuning would have to be performed.

Overall, when Table II is considered, it can be seen that the proper measurement timing compensation improves the THD in every loading condition. However, it can also be noticed that the THD of the formed grid voltage is below 1 % even when the current sampling is at the carrier peaks. So, it can be concluded that performance-wise the improvements were proportionally significant, when the sampling was compensated,

TABLE II
TOTAL HARMONIC DISTORTION OF THE LINE VOLTAGE AND CURRENT.

Loading condition	Sample instant	THD u_AC	THD i_load
26.6 Ω	Carrier peaks	0.59 %	0.60 %
26.6 Ω	3.5 µs delay	0.39 %	0.42 %
86 µF	Carrier peaks	0.53 %	2.76 %
86 µF	3.5 µs delay	0.46 %	1.87 %
86 µF ‖ 186 Ω	Carrier peaks	0.90 %	1.98 %
86 µF ‖ 186 Ω	3.5 µs delay	0.37 %	1.16 %

even though the absolute values of the improvements were relatively smaller.

To illustrate the effect of the sampling in the frequency spectrum, the FFT of the sampled current in the capacitive loading condition (i_n from Figs. 6–7) is shown in Fig. 10. The 5th and 7th harmonics have clearly lower magnitude with the compensation and proper sample timing. Above 6 kHz the non-compensated sampled current has a noticeably larger magnitude which is most significant around the 25 kHz Nyquist frequency of the PWM. The proper timing of the sampling instant significantly lowers the switching noise from the measured current. Obviously, the lower noise allows higher

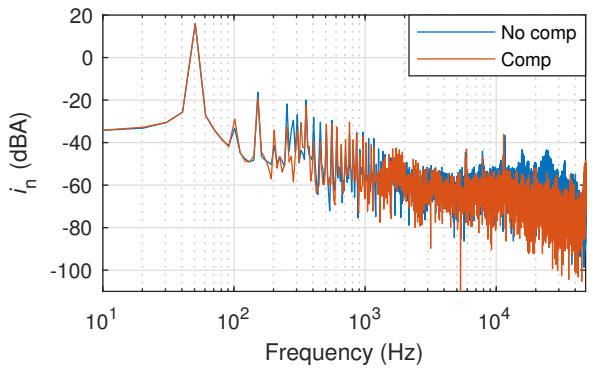


Fig. 10. Sampled current FFT, when the load was $C = 86\,\mu$F. With 'No comp' the current is sampled at carrier peaks, and with 'Comp' with a 3.5 µs delay.

gains to be used for the current control.

IV. Conclusions

In this paper, the effect of proper current measurement sample timing for a single-phase inverter was demonstrated. The conventional current measurement method of sampling at PWM carrier peaks was found to produce a significant measurement deviation for the consecutive samples. The same applied, even when the sampling and switching delays were compensated. With the use of antialiasing filter that has a cut-off frequency that is higher than the PWM Nyquist frequency, the current measurement samples showed reduced deviation. The experimental results showed that a fixed sampling compensation can provide sufficient current sampling regardless of the duty cycle and loading condition. The downside of the method was that even though the compensation delay can be estimated, manual tuning is required to achieve the best result.

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