An Integrated and Galvanically Isolated DC-to-15.3 MHz Hybrid Current Sensor

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***Abstract*—A wide-bandwidth galvanically isolated current sensor in a 180 nm CMOS technology is presented. It combines two sensing principles for the contactless and lossless current measurement in power electronic applications. A dedicated vertical Hall sensor (low frequencies) and an integrated helix-shaped Rogowski coil (high frequencies) enable to measure currents in any power line under the chip from DC up to 15.3 MHz, which exceeds prior art by 5x. Both sensing concepts are fully integrated on one microchip without the need for any kind of magnetics or post-processing. The wide bandwidth results in fast transient properties, verified by an IGBT double pulse measurement of current pulses with an amplitude of 60 A and slew rates up to 1 kA/µs. A sensitivity of 3.1 mV/A is achieved.**

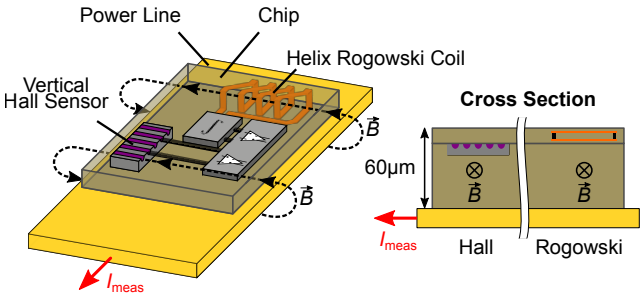


Fig. 2. Proposed integrated current sensor for off-chip current sensing.

I. Introduction

More and more power electronics applications, such as motor control or automotive electronics, renewable energy require contactless and wide-bandwidth current measurement to control the flow of energy. For fast-switching converters with modern generation power-devices like GaN, SiC and IGBT in latest trench-/fieldstop technologies, it is important to measure steep current transients in the order of kA/µs, to guarantee safe operation or to initiate an emergency stop after an error recognition [1]. To obtain an acceptable power dissipation, a shunt-based measurement needs a precise sense resistor with low impedance in addition to low parasitic inductance [2]. Shunt sensing has limited bandwidth and inherently no galvanic isolation. Current sensors like Hall [3], fluxgate [4] and AMR [5] detect the current by means of its magnetic field $\vec{B}$. They provide galvanic isolation, required for many power applications, but have limited bandwidth to frequencies far below 1 MHz, Fig. 1, and often require extensive post processing. To expand the bandwidth limitation of a CMOS Hall sensor, [6] has added an integrated pick-up coil to expand the bandwidth to 3 MHz. A discrete Rogowski coil based current sensor provides galvanic isolation and high bandwidth [7], but can only measure AC signals and is more expensive due to the realization on a large PCB. An AMR can expand the bandwidth of a discrete Rogowski coil towards DC [8], but requires additional space and adds cost. [9] has implemented an integrated current sensing circuit with a combination of a Hall sensor for DC signals and an on-chip Rogowski coil, that achieves a total bandwidth of 75 MHz. However, [9] has a focus on IC-level current sensing with limited galvanic isolation.

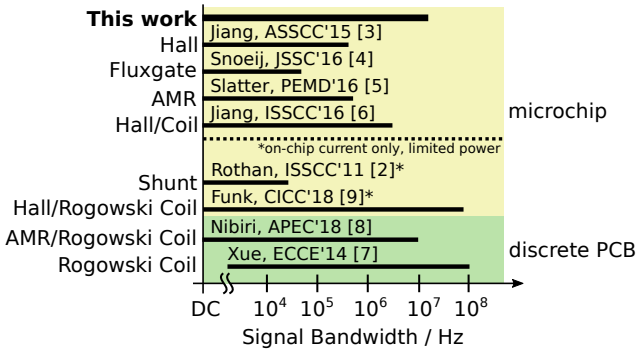
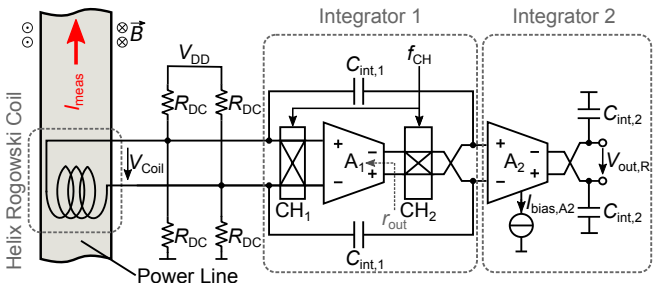


Fig. 1. Bandwidth comparison of different current sensing concepts.

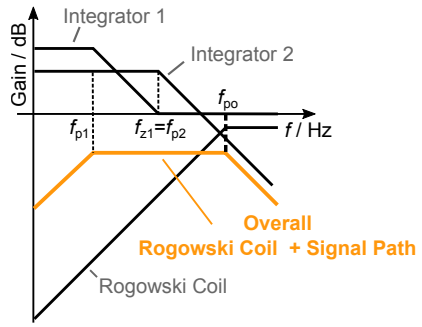
This paper proposes a cost-efficient Hall and Rogowski coil based current sensing circuit, all fully integrated on one microchip, for off-chip current sensing, Fig. 2. The combination of a vertical Hall sensor and a helix-shaped Rogowski coil results in contactless and lossless sensing of DC currents and fast transients. The large signal transfer behavior of the proposed current sensor is measured over seven decades. For the step response, a double pulse test setup employing a modern IGBT power stage in trench-/fieldstop technology is utilized. Furthermore, a gate driver comprising closed-loop regulation of the current slew rate through the device ($\mathrm{d}I_{\mathrm{meas}}/\mathrm{d}t$), following the concept in [10], is used to evaluate the sensor at a specific switching speed.

II. Current Sensor

The microchip, including the integrated helix coil, the vertical Hall sensor and the analog front-end is intended to be placed on top of the power line on a Printed Circuit Board (PCB) or on a power module. This allows a galvanically isolated and lossless current sensing. The helix-shaped coil



(a)



(b)

Fig. 3. Rogowski path including (a) block diagram and (b) transfer behavior.

and the vertical Hall sensor can measure the magnetic field $\vec{B}$, which appears in parallel to the chip surface, as indicated in Fig. 2. The Hall path measures DC signals and frequencies up to 43 kHz, while the Rogowski path covers the high frequency components up to 15.3 MHz. To achieve an acceptable sensitivity, the distance between the sensors and the power line must be minimal, since the magnetic field $\vec{B}$ is inversely proportional to that distance. Therefore, the proposed chip was back-grinded to a total thickness of 60 µm, which results in a four times higher sensitivity, compared to the regular IC-thickness.

The on-chip Rogowski coil covers an area of 0.75 mm x 1 mm. Its helix-shaped structure consists of multiple windings of both the bottom and the top metal layer, provided in the used semiconductor technology, as shown in Fig. 2. A Rogowski coil measures the change of magnetic field $\vec{B}$, based on Amperes law. The induced voltage in the coil is proportional to the derivation of the current to be measured and increases by 20 dB/decade in the frequency domain, Fig. 3b. For a constant overall transfer behavior, the output of the coil has to be integrated by the sensor front-end to compensate the differentiating transfer behavior of the coil, while the maximum bandwidth is limited by the Rogowski coil itself. Figure 3a shows the integrated sensor front-end of the helix Rogowski coil with a combination of two integrator stages. The chopped Integrator 1 compensates the low frequency components and Integrator 2 the high frequency components. For a constant gain of the overall transfer behavior of the Rogowski path, the dominant pole f_{p2} of Integrator 2 needs to match the zero of Integrator 1, i.e. $f_{p2} = f_{z1} = 1.5\,\text{MHz}$, as shown in Fig. 3b. The zero f_{z1} of A_1 is determined by the output resistance r_{out} of A_1 and the feedback integration capacitances $C_{int,1} = 462\,\text{pF}$. The pole f_{p2} is set by $C_{int,2}$, while it can be trimmed by

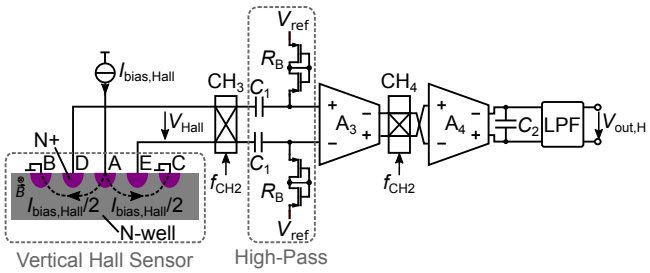


Fig. 4. Block diagram Hall path.

the bias current $I_{bias,A2}$ of A_2. Since the corner frequency between flicker noise and the flat high-frequency noise of the implemented amplifier A_1 is in the MHz region, chopping is required. Due to the combination of two integrator stages, the chopper frequency f_{CH} can be selected below signal bandwidth [9]. Additionally, with chopping the impact of the offset voltage of A_1 can be suppressed and the output of the sensor front-end will not clip to the supply rails.

The vertical Hall sensor consists of N+ terminals A-E, as shown in Figures 2 and 4. These terminals are located in an N-well and placed in parallel to the magnetic field $\vec{B}$ to be measured. The Hall sensor is biased by a current $I_{bias,Hall}$ at terminal A, which distributes in the N-well to terminal B and C. In presence of any magnetic field $\vec{B}$, the current in the N-well flows asymmetrically, which results in a Hall voltage $V_{Hall} \neq 0\,\text{V}$ between terminals D and E. V_{Hall} is proportional to the field $\vec{B}$ and to $I_{bias,Hall}$. The latter can be used to adjust the sensitivity of the Hall path to the sensitivity of the Rogowski path. A modulation of the Hall voltage V_{Hall} (chopping) to higher frequencies along with the high-pass filter (Fig. 4) reduces the offset of the Hall sensor and the noise of A_3 [3], [6], [9]. After the demodulation by CH_4, the signal is amplified with A_4 and filtered by a low-pass filter with a 500 kHz cutoff frequency to obtain an offset-compensated, low-noise current signal.

III. Experimental Verification

The proposed current sensor is implemented in a 180 nm CMOS technology with an area of 2.74 mm^2. The bare-die chip with a total thickness of 60 µm is mounted directly on a PCB for contactless measurement of the current through

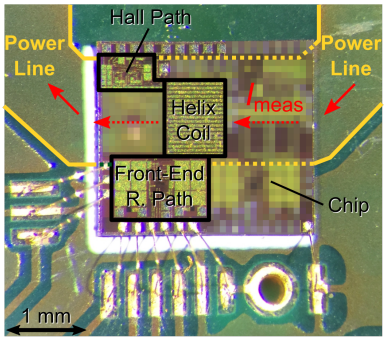


Fig. 5. Photo of the proposed current sensor.

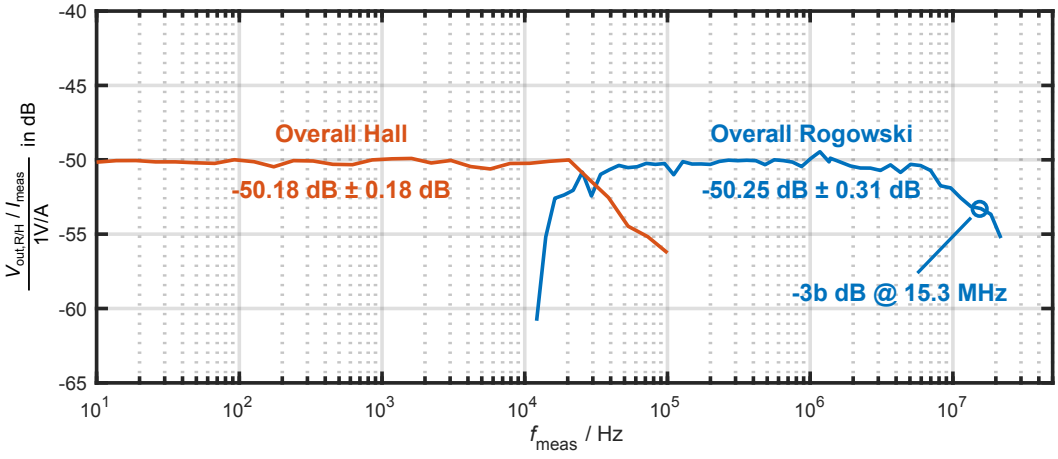


Fig. 6. Measured transfer behavior of Hall path and Rogowski path with an amplitude of the signal current I_{meas} of 1.4 A.

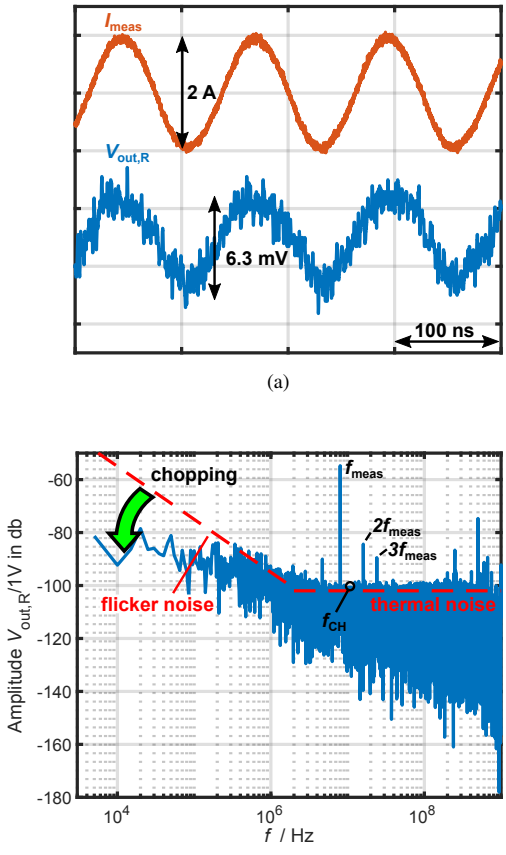


Fig. 7. Measured transient signals (a) and amplitude spectrum (b) of Rogowski path for with $I_{\mathrm{meas}} = 1\,\mathrm{A}$ and $f_{\mathrm{meas}} = 8\,\mathrm{MHz}$.

the underlying power line, as shown in Fig. 5. Bond wires from the PCB connect all external signals and supplies to the sensor chip. To achieve a flat transfer behavior, the sensitivity of the Hall path is adjusted to the resulting sensitivity of the Rogowski path by setting $I_{\mathrm{bias,Hall}} = 20\,\mathrm{mA}$.

Figure 6 shows the measured signal transfer behavior over seven decades. Sinusoidal currents I_{meas} with an amplitude of 1.4 A are generated by a 4-quadrant voltage amplifier (DC $-$ 100 kHz) and an RF broadband power amplifier (100 kHz $-$ 20 MHz). The signal transfer behavior represents the sensitivity and bandwidth of both sensor principles. The Hall path covers currents between DC and 43 kHz with a sensitivity of −50.18 dB related to I_{meas}, which corresponds to 3.1 mV/A. The variation is $< 2\,\%$. Higher frequency components, up to 15.3 MHz, are measured by the Rogowski path with a sensitivity of −50.25 dB with a variation of $< 3.5\,\%$ (3.1 mV/A $\pm 0.1\,\mathrm{mV/A}$).

Figure 7a shows the transient measurement for a 8 MHz sinusoidal current I_{meas} with a peak-to-peak current of 2 A. The sensing output $V_{\mathrm{out,R}}$ has a peak-to-peak voltage of 6.3 mV. The resulting spectrum of the $V_{\mathrm{out,R}}$ over several periods ($>$ 16k) is shown in Fig. 7b. It shows that the expected increase at low frequencies ($f < 2\,\mathrm{MHz}$) caused by flicker noise is suppressed by chopping. By means of the introduced two-stage integrator, the chopping frequency $f_{\mathrm{CH}} = 10\,\mathrm{MHz}$ disappears in thermal noise and only the signal frequency f_{meas} of the signal current I_{meas} and its harmonics are dominant.

The schematic of the 650 V, 75 A IGBT half-bridge power stage is shown in Fig. 8. The IGBT is designed in the latest trench-/fieldstop technology in order to achieve very high switching speeds. In order to test the sensor at a specific slew rate, the low-side IGBT is controlled by a gate driver with adjustable and regulated $\mathrm{d}I_{\mathrm{meas}}/\mathrm{d}t$. The hybrid current sensor is placed close to the emitter of the low-side IGBT to avoid parasitic coupling from the high-voltage nodes that may destroy it. Double-pulse measurements have been performed in order to generate the load current pulses of 60 A at a DC link voltage of 300 V. Figure 9 shows the measured step response for a current pulse I_{meas} from 0 A to 60 A, which was generated by the IGBT double pulse setup with a regulated slew rate of $1\,\mathrm{kA/\mu s}$. The output swing of 125 mV of the Rogowski path is slightly lower than expected from the measured sensitivity from Fig. 6. This can be addressed by

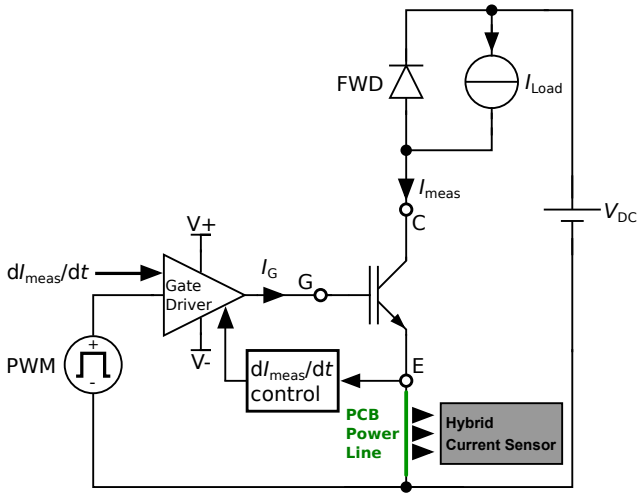


Fig. 8. Test setup with 650V, 75A trench-/fieldstop IGBT power stage comprising closed-loop dI/dt control and the proposed hybrid current sensor.

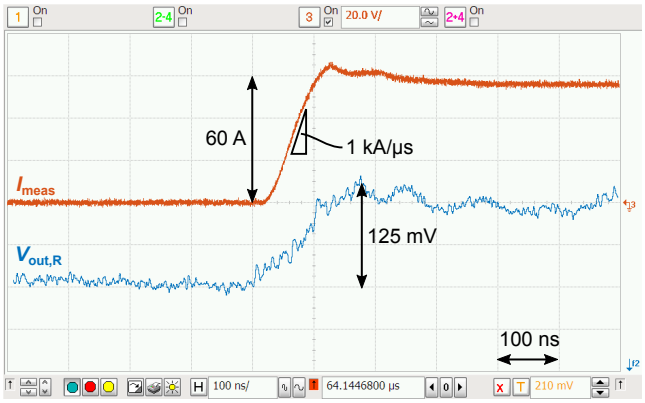


Fig. 9. Measured transient response of a 60 A current pulse with 1 kA/µs rise time.

further optimization of the test setup. The proposed current sensor precisely resolves the full current transition, including non-idealities such as the reverse recovery peak.

IV. Conclusion

An integrated cost-efficient hybrid current sensor, implemented in a 180 nm CMOS technology, for galvanically isolated and lossless measurement is presented. The current sensor combines two different sensing principles, a vertical Hall sensor for the DC and low frequency measurement (<43 kHz) and a Rogowski coil for higher frequencies up to 15.3 MHz. This exceeds state-of-the-art [6] of off-chip current sensing by a factor of 5, as outlined in Table I. The current sensor accurately resolves fast current slew rates as fast as 1 kA/µs, and is thus well-suitable for use in state-of-the-art power electronics applications such as motor drives.

TABLE I. Comparison of integrated current sensing with prior art.

	[3] A-SSCC'15	[4] JSSC'16	[6] ISSCC'16	[9] CICC'18	**This work**
Sensor Type	Hall	Fluxgate	Hall + Coil	Rogowski Coil + Hall	**Rogowski Coil + Hall**
Principle	off-chip	off-chip	off-chip	on-chip	**off-chip**
Process Node	0.18 µm	0.35 µm	0.18 µm	0.18 µm	**0.18 µm**
Area	8.75 mm^2	n.r.[a]	8.75 mm^2	3.17 mm^2	**2.74 mm^2**
BW	400 kHz	47 kHz	3 MHz	75 MHz	**15.3 MHz**
Input Range	n.r.[a]	100 µA – 80 A	±18 A	±4.1 A	**±60 A**
P_{diss}	40 mW[b]	23/17 mW	38.5 mW[b]	33.7 mW	**63.8 mW**
Output	Analog	Digital	Analog	Analog	**Analog**
Sensitivity	80 mV/A	n.r.[a]	n.r.[a]	43.5 mV/A	**3.1 mV/A**
Output Noise	n.r.[a]	n.r.[a]	0.48 Arms	0.15 Arms	**0.71 Arms**

[a]not reportet, [b]calculated

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