Determination of Cable Characteristics and Adjustment of PWM Pulse Pattern to Minimize AC Motor Terminal Over-voltage

Nandini Ganesan, Rangarajan Tallam
Rockwell Automation, 6400 W. Enterprise Drive, Mequon WI 53092
Ph: 262-512-4645, Email: nganesan@ra.rockwell.com

***Abstract*— In this paper, a method to detect characteristic impedance and oscillation frequency of a cable in an AC drive system is developed. Results are provided for different cable constructions and lengths. The application of the measured oscillation frequency to adjust the PWM pulse pattern for reflected wave motor over-voltage reduction, with reduced distortion in the output voltages, is demonstrated. Experimental results are provided to show the applicability of the reflected wave compensation at higher switching frequencies. In addition to estimating the cable characteristic impedance, the cable peak charging currents can also be estimated, which can be used to accurately determine power module losses and predict the junction temperature.**

Keywords— PWM, AC Drives, Reflected wave, Cable characteristics

I. INTRODUCTION

Long motor leads in a PWM voltage source inverter (VSI) can generate high motor line to line transient peak voltage due to the reflected wave phenomenon [1]. These high transient voltages can cause insulation breakdown in motors and cables leading to premature failures.

Prior art methods implement safeguards in their PWM algorithm through duty cycle limits, and enforcement of minimum dwell time and polarity reversal time [2, 3]. Oscillation frequency of the voltage at the motor terminals and the inverter output currents is strongly determined by cable characteristics. The dwell time, which is selected to allow cable ringing to damp between successive PWM pulses and is dependent on maximum cable length, can be about 14-16us for 600ft of standard 4-conductor shielded motor cable. As PWM frequencies increase with the use of wide band gap devices, the dwell time may become a significant portion of the PWM period, making distortion a significant problem with long cables.

The effects of long motor cables on motor terminal over-voltage, cable charging current and on power device protection based on de-saturation detection are well known [1, 2]. However, the effect on power device losses and a method to include the losses in thermal calculations to accurately predict power device junction temperature are relatively less understood.

On small AC drives (<10HP), the peak cable charging currents can be equal to or greater than the nominal full load current. At higher PWM frequencies, the increase in switching losses due to long motor cables can be significant. If the effect of these additional losses are not accounted for in thermal calculations, it could lead to inverter failure from excessive junction temperature.

In this paper, the phenomenon of increase in switching losses with long cables is studied in detail. A method to measure cable characteristic impedance and ring frequency is developed. Experimental results are provided to demonstrate how the extracted cable parameters can be used to adjust the PWM pulse pattern to reduce motor over-voltage due to reflected waves. In addition, the peak cable charging current can be measured, which can be used to estimate cable length for standard construction, and to also estimate power module losses and predict junction temperature. Experimental test results are provided to show the effect of cable length on power device junction temperature increase. An analytical method to conservatively estimate and include the effect of long cables on switching losses is also provided.

II. LONG CABLE CHARACTERISTICS IMPEDANCE AND OSCILLATION FREQUENCY MEASUREMENT

A. Double pulse test set-up with long cables

The schematic of the double-pulse test to measure cable characteristic impedance and oscillation frequency with long motor cables is shown in Fig. 1. This setup, which is a modification to the standard energy loss measurement set up without cables [4], has the advantage that the losses due to line-line as well as line-ground cable capacitance are included in the measurement. Capacitors C_1 and C_2 are generally used on AC drives for compliance to EMC regulatory requirements and must be included in the switching energy measurement tests. The effect of long cables on inverter thermals will be explained in section IV.

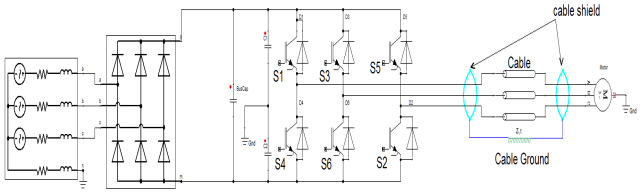


Fig.1: Schematic of double-pulse setup to measure cable characteristics

B. Estimation of cable characteristic frequency

With reference to Fig. 1, consider a switching transition from lower device to upper device in one phase (U) with the lower devices in the other two phases (V, W) turned on. This results in an increase in common-mode voltage (CMV) of

Cable Type	Cable length(m)	Peak I_{DM} (A)	Est. DM ring frequency (kHz)	Peak I_{CM} (A)	Est. CM ring frequency (kHz)	Estimated ZDM (ohm)	Measured ZDM (ohm)	Estimated ZCM (ohm)	Measured ZCM (ohm)
Standard	50	6.76	938	3.68	1250	99	99	30	36
	90	6.61	484	2.75	600	101	99	40	37
High Capacitance	50	21.50	682	16.85	556	31	34	7	11

Table 1 : Calculated and measured CM and DM impedances with different cable lengths and types

V_{DC}/3 and an increase in differential-mode voltage (DMV) of V_{DC}. Thus, there is a current spike at turn-on, with magnitude given by:

$$I_{cable} = \frac{V_{DC}}{Z_{DM}} + \frac{1}{3}\frac{V_{DC}/3}{Z_{CM}} \qquad (1)$$

Similarly, when the upper device in one phase (U) turns off with the other two phases clamped to the lower DC rail, there is a decrease in CMV and DMV, resulting in a negative spike of current with magnitude according to eqn. (1). During the transition, currents are measured on the three inverter outputs (Iu, Iv and Iw). The current in any one phase is the sum of its differential and common mode components, both of which can be extracted from the current measurement using eqn. (2) and (3).

$$I_{CM} = \frac{Iu + Iv + Iw}{3} \qquad (2)$$

$$I_{DM} = Iu - I_{CM} \qquad (3)$$

For a 480V, 2HP drive that uses a 1200V, 10A IGBT module, output current measurements were taken with a standard 4-conductor shielded motor cable and a high capacitance 4-conductor shielded motor cable. Output current measurements are shown in Fig. 2, and the rectified value of DM and CM currents are shown in Fig. 3. The average value of the separation between the peaks provides an estimate of oscillation period. The characteristic DM and CM impedance of the cable can be determined from the measured DC bus voltage and the first current peak magnitudes in the DM and CM waveforms.

Since the oscillation frequencies for typical cables are in the hundreds of kHz range, the current signal need to be sampled at least with 10MSPS resolution to obtain the cable ringing signature properly.

The calculated CM and DM mode impedances along with measurements made using an impedance analyzer [5] at 100 kHz are provided in Table 1 for different cable constructions. It can be seen from the table that the calculated impedance values closely match the measured values.

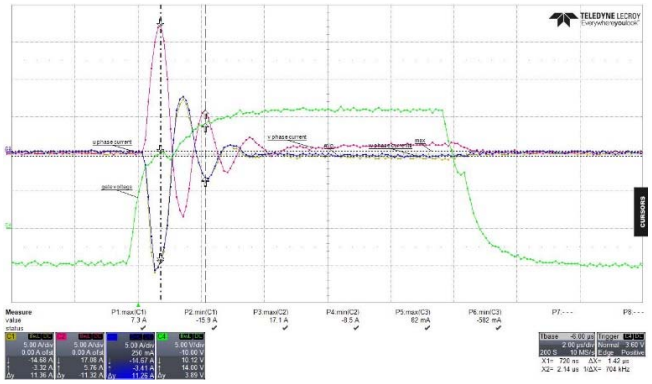


Fig 2: Output current measurement from double pulse test with high capacitance cable

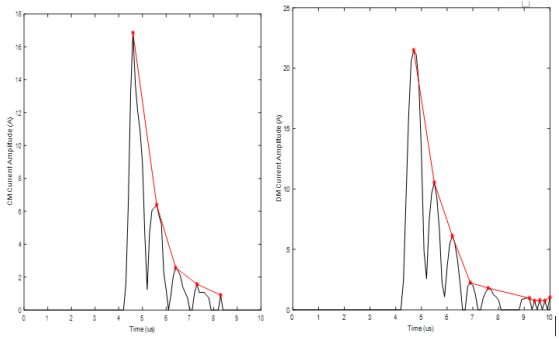


Fig. 3: Extracted CM and DM currents from output current measurements

III. PWM Pulse Pattern Adjustment To Minimize Motor Over-Voltage

With long motor leads, the waveforms of drive output and motor terminal line-line voltage are shown in Fig. 4. To prevent motor terminal voltage from exceeding twice inverter DC bus voltage, the PWM pulse pattern can be modified to enforce a minimum dwell time by clamping the modulation index [2]; with minimum dwell time enforced, oscillations in the voltage attenuate before the next switching event occurs. The dwell time is chosen to limit motor over-voltage up to a certain maximum cable length – 14-16 µs is required for shielded cable lengths up to 600 feet. At higher switching frequencies, the dwell time becomes a significant portion of the PWM cycle making output voltage distortion a problem for applications with long cables.

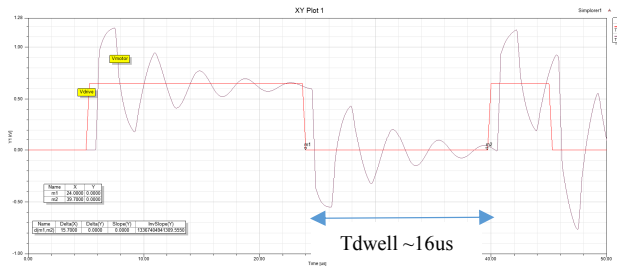


Fig 4: Drive and motor line-line voltage with long motor leads [1].

The proposed method to reduce peak motor voltage with a smaller value of minimum dwell time than the method based on modulation index clamping [2] can be explained with reference to Figs. 5-7, where the line-line voltage waveform transitions (blue waveform) from DC bus voltage to 0 in the first switching event and from 0 to DC bus voltage in the second switching event. The waveforms were obtained with a 480V, 15HP AC drive running a 460V, 7.5HP, 60Hz, 1170RPM induction motor, with 600 feet of 4-conductor 12AWG shielded cable. In Fig. 5, the second switching event coincides with the motor voltage (yellow waveform) at a negative peak following the first switching event, resulting in high over-voltage following the second switching event. In Fig. 6, the second switching event occurs at a positive peak following the first switching event; thus, the motor over-voltage is significantly reduced. In Fig. 7, the second switching event occurs in between a negative and positive peak in the voltage following the first switching event; thus, the subsequent peak motor voltage is in between those of Fig. 5 and Fig. 6.

The methodology explained in Section II can be used to estimate the positive and negative peaks for any cable. With the known cable oscillation frequency, the second switching event can be enforced to occur at an instant that the motor voltage is at a positive peak following the first switching event. Thus, the minimum dwell time and the distortion in output voltage can be significantly reduced.

For line-line voltage transitions from negative DC bus voltage to 0 and back to negative DC bus voltage, the second switching event must occur at a negative peak of the motor voltage following the first switching event.

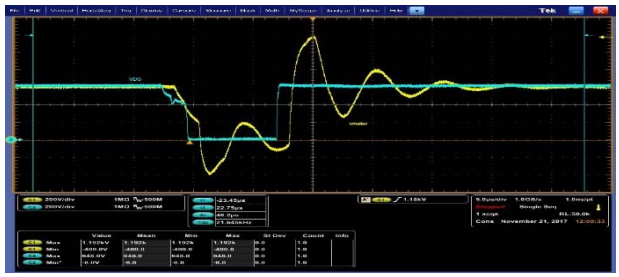


Fig. 5: Drive and motor voltage with 2nd switching instant aligned to negative peak of motor voltage waveform
(DC bus voltage = 610VDC, peak motor voltage = 1192V, ratio = 1.95)

Fig. 6: Drive and motor voltage with 2nd switching instant aligned to positive peak of motor voltage waveform
(DC bus voltage = 610VDC, peak motor voltage = 984V, ratio = 1.61)

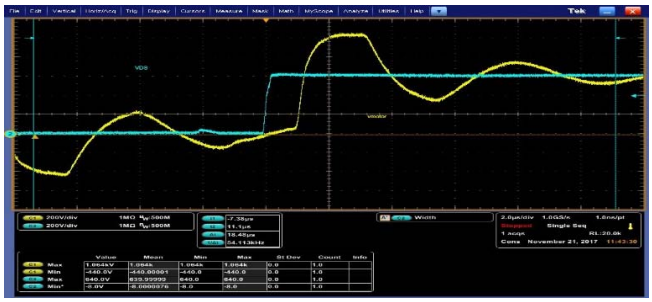


Fig. 7: Drive and motor voltage with 2nd switching instant aligned to zero crossing of motor voltage waveform
(DC bus voltage = 610VDC, peak motor voltage = 1064V, ratio = 1.74)

This can be explained with reference to Figs. 8-10 where a line-line voltage transitions (blue waveform) from DC bus voltage to 0 in the first switching event and from 0 to -DC bus voltage in the second switching event. These waveforms were obtained through a simulation model. In Fig 8, the second switching instant is close to a positive peak in the motor voltage waveform resulting in over-voltages.

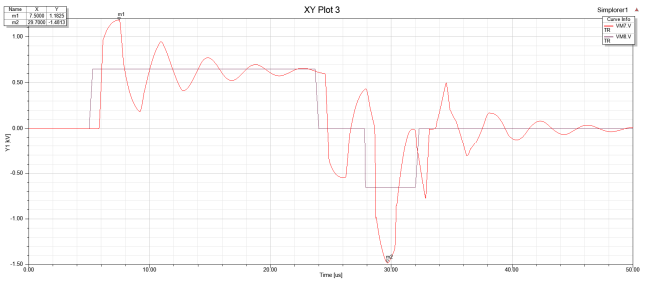


Fig 8: Drive and motor voltage with 2nd switching instant aligned to positive peak of motor voltage waveform
(DC bus voltage = 650VDC, peak motor voltage = 1481V, ratio = 2.27)

In Fig 9, the second switching instant is close to a negative peak in the motor voltage waveform. Thus, the motor

over-voltage is significantly reduced. In Fig. 10, the second switching event occurs in between a negative and positive peak in the voltage following the first switching event, with the subsequent peak value of motor voltage in between those of Fig. 8 and Fig. 9.

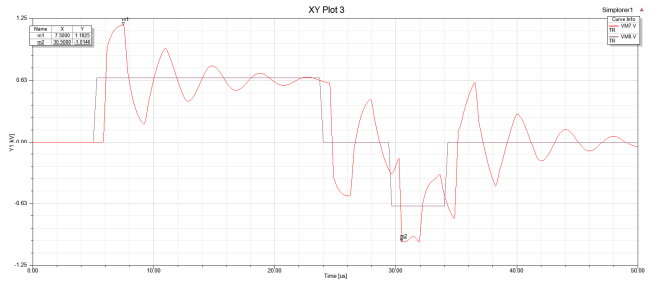


Fig. 9: Drive and motor voltage with 2nd switching instant aligned to negative peak of motor voltage waveform
(DC bus voltage = 650VDC, peak motor voltage = 1014V, ratio = 1.56)

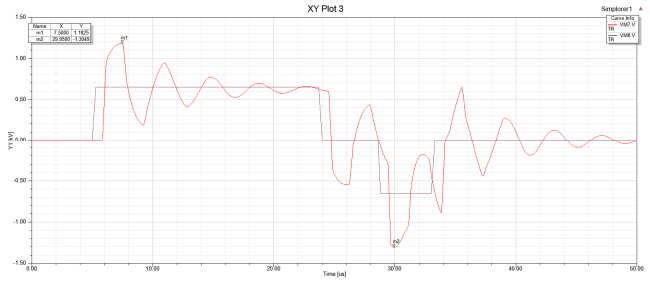
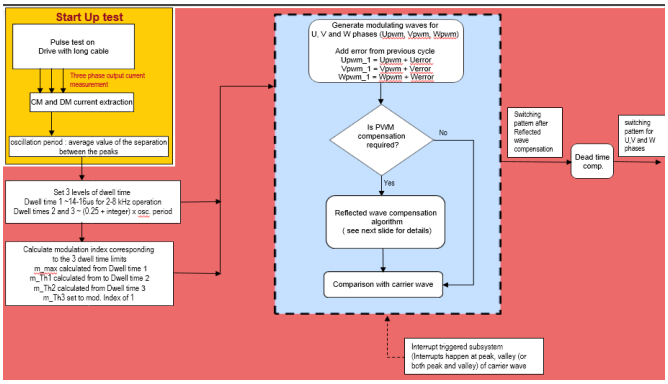


Fig. 10: Drive and motor voltage with 2nd switching instant aligned to zero crossing of motor voltage waveform
(DC bus voltage = 650VDC, peak motor voltage = 1304V, ratio = 2)

Fig. 11: Flowchart of reflected wave compensation scheme



The flowchart for the modified PWM algorithm is shown in Fig. 11, where the concepts explained in Figs. 6-11 are implemented as multiple discrete modulation index limits (or dwell times). The dwell times are set to be multiples of the time period of the oscillation. Transmission delay time through the cable, which is approximately one-fourth of an oscillation period, is also taken into account. One of the dwell times is set to a large value (*e.g.* 14-16 μs) and corresponds to the time it takes for the oscillations to attenuate with a shielded cable of about 600 feet length. The detailed reflected compensation methodology for one of the inverter phases, for all switching transitions, is shown in Fig. 12.

The compensation scheme clamps the commanded PWM duty to one of the chosen modulation index limits to limit overvoltage to about 2 p.u. This modulation index adjustment for reflected wave compensation (*i.e.* clamping to modulation index lower or higher than commanded) causes volt-second imbalance in the output voltage, which can cause distortion and DC offset. Volt-second balance is achieved by accumulating the error and compensating for it by modulation index adjustment in subsequent PWM cycles. The PWM patterns thus generated then undergo dead time compensation before being applied to generate the gating commands for the inverter power devices.

Dead time in typical IGBT inverters is about 1-2 μs and could be set lower for SiC MOSFET inverters. Dead-time compensation could be done on a pulse-by-pulse basis and requires current polarity to be known. Around the zero crossings of the current waveform, where polarity of the current may not be correctly detected by the drive, dead-time compensation could be inaccurate and adversely affect the RWC method proposed in this invention by either extending or shortening the pulse. This could result in > 2 p.u. voltage at the motor terminals. If the current is high such that polarity can be accurately determined, then the proposed reflected wave compensation method is used. When the current has low amplitude in a band around zero and reflected wave compensation is required, the dwell time is set to the maximum value of the conventional prior art compensation method (*e.g.* 14-16 μs).

The reflected wave compensation method shown in Figs 11-12 was simulated for a 480V, 15HP drive. The cable model used in the simulation was for a 100m, 4-conductor shielded cable [7]. A simulation implementing the double-pulse test described in Section II with the FEA cable model yields the DM and CM current waveforms as shown in Figs. 13 and 14 respectively, with oscillation time period of about 2.25 μs.

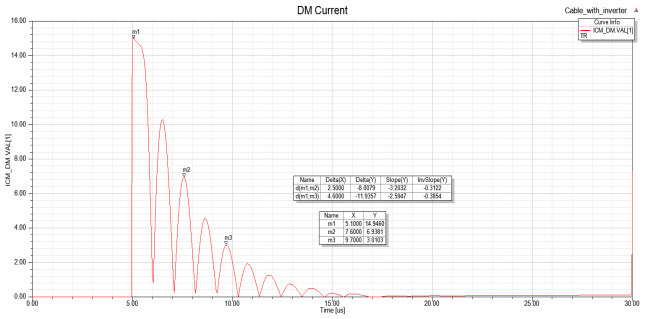


Fig. 13: Simulation results of rectified DM current for 100m cable

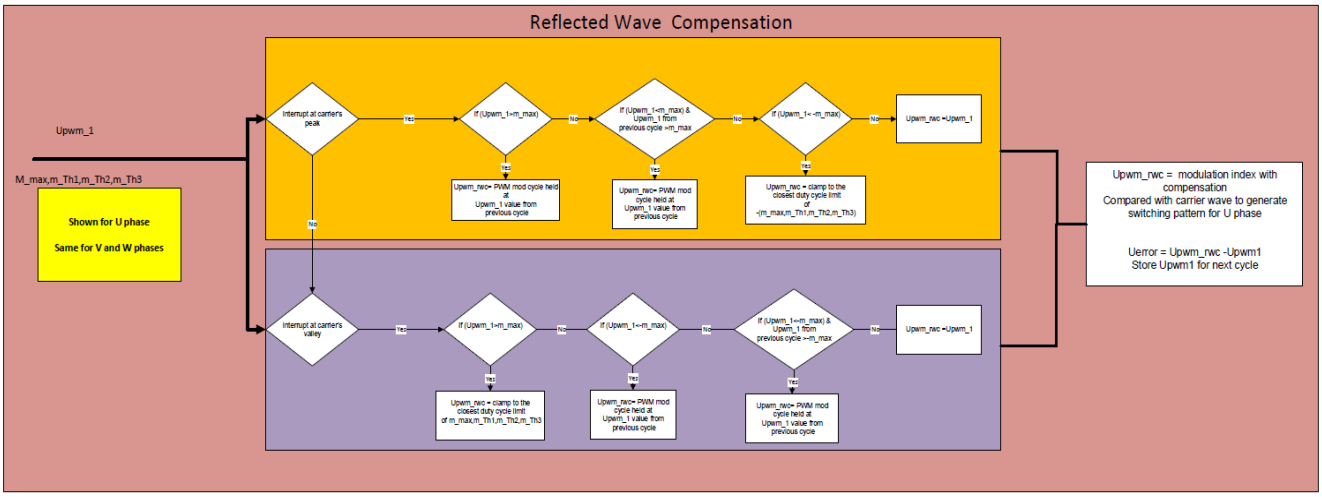


Fig. 12: Algorithm for reflected wave compensation at all switching transitions

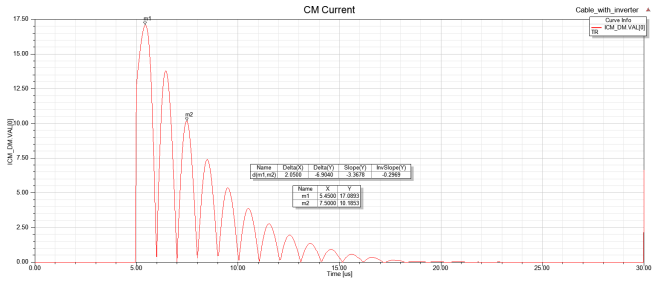


Fig. 14: Simulation results of rectified CM current for 100m cable

With the oscillation period determined from the measured DM current, the dwell times for the simulations were set at 2.25 µs, 4.5 µs, 6.75 µs, 9 µs, 11.25 µs and 14 µs. The switching frequency was set to 16 kHz. The motor line-line voltage waveform is shown in Fig. 15 for 60 Hz output frequency. Clearly, the motor terminal voltage is limited to 2 p.u even at the high PWM frequency.

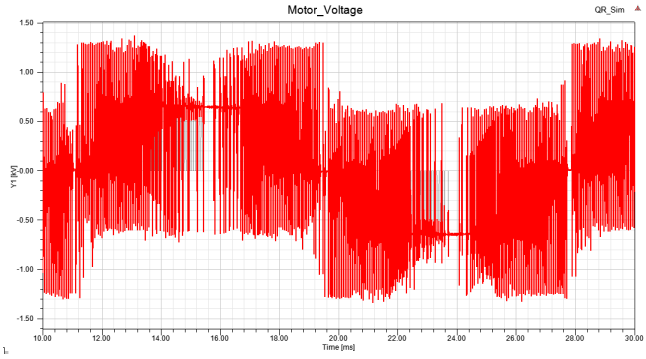


Fig. 15: Simulated motor terminal line-line voltage waveform (DC bus voltage = 680VDC, peak motor voltage = 1370V, ratio = 2)

The modulating waveforms with reflected wave compensation applied are shown in Fig. 16.

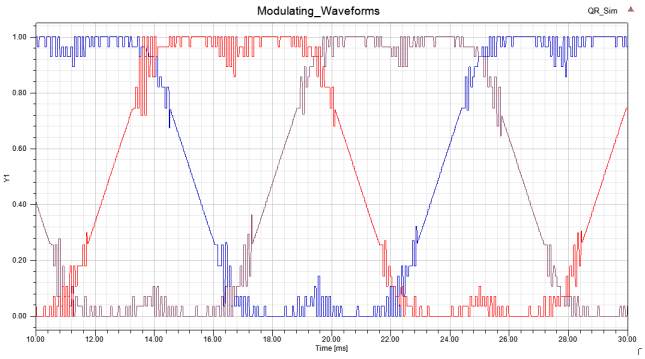


Fig. 16: Simulation results for modulating waveforms with reflected wave compensation

As the modulating waveforms approach 0 or 1, the discretization of the values to generate a specific value of dwell time that minimizes peak motor voltage is evident. The effect of clamping the dwell time to one of the discrete values on the motor line-line voltage waveform is shown in Fig. 17.

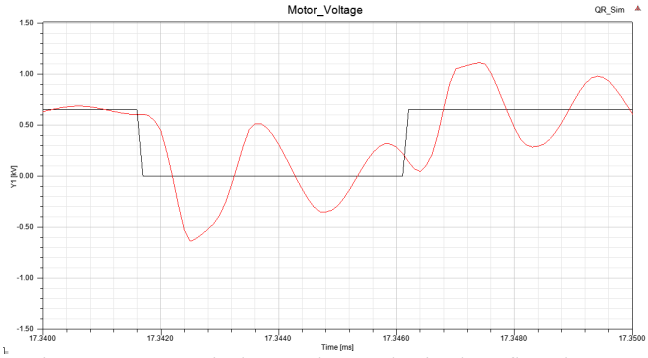


Fig. 17: Motor terminal overvoltage reduction by reflected wave compensation (dwell time = 4.5 µs)

The amplitude *vs*. frequency of the inverter output voltage are shown in Fig. 18 for the cases of no reflected wave compensation applied (16 kHz PWM), conventional

compensation method (4 kHz PWM) and the proposed compensation method (16 kHz PWM), at 60Hz output frequency. It can be seen that there is no noticeable difference in distortion introduced by the proposed method.

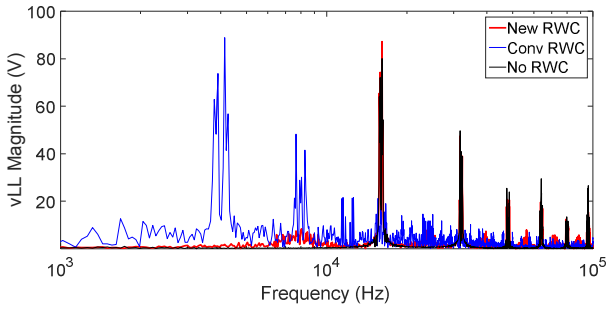


Fig. 18. Amplitude *vs*. frequency plots for the inverter output voltage (Red – New method, Blue – Conv. method, **Black** – No comp)

IV. Effect Of Long Motor Cables On Inverter Power Loss

The double pulse setup described in Section I is used to assess the effect of long cables on inverter losses. For a 480V, 2HP drive that uses a 1200V, 10A IGBT module, the turn-on and turn-off switching energy per pulse at different cable lengths, with standard 4-conductor shielded motor cable, are shown in Table II.

The reduction in turn-off switching energy with increasing cable length can be explained with reference to Fig. 19. As the upper IGBT turns off, the voltage across it increases to DC bus voltage before the current commutates to the lower diode. This causes a negative *dv*/*dt* at the output terminal, which results in a negative current pulse due to cable capacitance. Thus, the collector current of the IGBT is reduced, resulting in a reduction in turn-off energy.

On the other hand, during the turn on of the upper IGBT, current commutates from the lower diode to the upper IGBT followed by a positive *dv*/*dt* at the output terminal. Therefore, the collector current of the IGBT is increased, resulting in an increase in turn-on energy, as shown in Fig. 20.

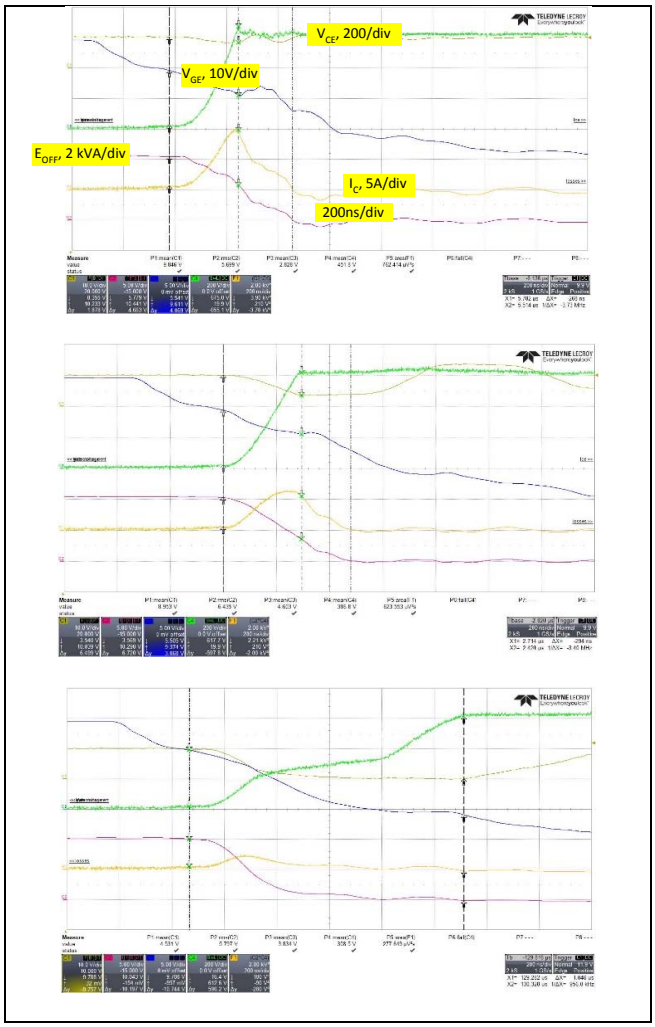


Fig.19: Turn-off switching waveforms for 3m standard cable (top), 50m standard cable (middle) and 50m high capacitance cable (bottom) at 600VDC, 10A load current.

A. Effect of gate drive on change in voltage fall time and increase in turn-on switching power loss

The parasitic capacitances in an IGBT gate drive are C_{GE}, which is the effective gate-emitter capacitance (including any externally added capacitance) and C_{GC}, which is the reverse transfer capacitance.

In reality, the effective gate-collector capacitance will be increased due to circuit layout on a PCB, primarily from transformer inter-winding capacitance (gate drive power supply) and parasitic PCB capacitance.

The plateau in the gate-emitter voltage (v_{GE_iC}) is the minimum voltage required to support the collector current and depends on the IGBT's output characteristic [8]. During the plateau region, the gate current flows through the effective gate-collector capacitance and discharges it, reducing the collector-emitter voltage.

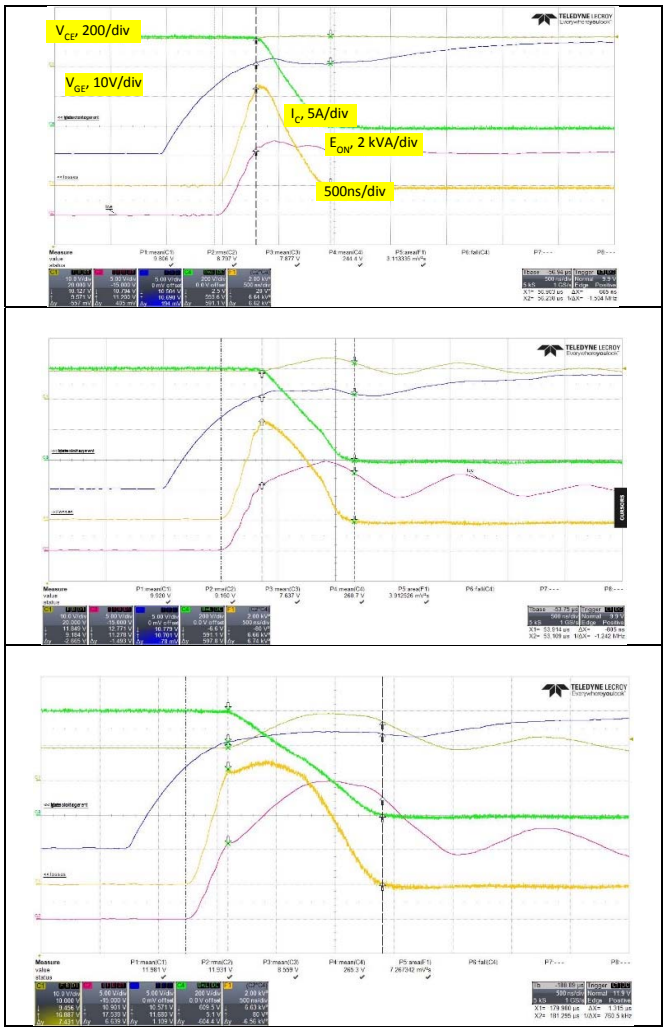


Fig.20: Turn-on switching waveforms for 3m standard cable (top), 50m standard cable (middle) and 50m high capacitance cable (bottom) at 600VDC, 10A load current

Since, the collector current has a spike at turn-on when the collector-emitter voltage falls, the plateau voltage v_{GE_iC} increases. Thus, the gate current that discharges the effective gate-collector capacitance ($i_{gate\_GC\_ON}$) is reduced, as shown below, resulting in a longer fall time for the collector-emitter voltage. The fall time increases with higher turn-on resistance and lower turn-on voltage (V_{GE+}).

$$i_{gate\_GC\_ON} = \frac{V_{GE+} - v_{GE\_iC}}{R_G} = C_{GC}\frac{dv_{CE}}{dt} \qquad (4)$$

The collector current during turn-on is the sum of the load current and the spike due to the cable characteristic impedance. The portion of the power loss due to the initial collector current rise from zero to the load current is unaffected by the cable type or length; subsequently, an increase in voltage fall time due to the cable charging current results in higher turn-on switching power loss due to the combined effect of the load current and the cable charging current.

The measured value of average gate current during the plateau in the gate-emitter voltage time was 50mA for 50m of standard cable and 35mA for the 50m high capacitance cable at a gate resistor value of 80.6Ω. From these gate current measurements and fall time values from Table 2, the effective value of gate-collector capacitance was determined to be 65 pF approximately; this value is higher than the IGBT's reverse-transfer capacitance of 24 pF and is due to the parasitic capacitance introduced by the gate drive power supply transformer and the PCB layout. These results also clearly validate the explanation provided for the increase in switching power loss.

The plateau voltage will be lower with long cable as the collector current is reduced by the negative spike of cable charging current due to the rise in collector-emitter voltage. The gate current that charges up the effective gate-collector capacitance is as follows, where V_{GE-} is the turn-off voltage:

$$i_{gate\_GC\_OFF} = \frac{v_{GE\_iC} - V_{GE-}}{R_G} = C_{GC}\frac{dv_{CE}}{dt} \qquad (5)$$

Since a negative bias voltage of about 5V is typically used, the effect of cable charging current on change in collector-emitter voltage rise time is not very significant.

B. Inverter Thermal Tests to Determine IGBT Junction Temperature with Long Cables

Thermal tests were conducted on the 480V, 2HP drive with 1200V, 10A IGBT module, with varying lengths of two

	Cable length (m)	Standard Cable				High Capacitance Cable			
		E_{ON} (mJ)	Eoff (mJ)	V_{CE} fall time (ns)	Vce rise time(ns)	E_{ON} (mJ)	Eoff(mJ)	V_{CE} fall time (ns)	Vce rise time(ns)
22.6	3	1.5	0.60	302	221				
	50	1.7	0.57	416	270	3.7	0.29	795	933
	90	1.7	0.54	441	314				
80.6	3	3.1	0.76	665	268				
	50	3.9	0.62	705	294	7.3	0.27	1165	1046
	90	3.8	0.57	742	307				

Table 2 : Measured turn-on losses and V_{CE} fall time for the 1200V, 10A module with different gate resistors

different types of cable. The module has an internal NTC temperature sensor as shown in Fig. 21 [9].

The IGBT junction temperature is estimated in the drive from the measured NTC sensor output and a thermal model based on power losses estimated from measured output current and known switching losses (obtained from double pulse characterization tests) [10]. Since, the cable length and its effect on switching losses are unknown, the objective of this experiment was to determine the change in IGBT junction temperature due to cable length using infrared imaging on an open module (IGBT and diode dies are exposed, with a thin layer of silicone gel applied for voltage isolation). The error between the measured IGBT temperature using infrared imaging and the temperature estimated by the thermal model was also determined.

The temperature results are shown in Table 3. There was a significant increase in IGBT temperature due to the high capacitance cable, as expected. However, with the standard 4-conductor shielded cable, the increase in IGBT temperature was not significant. It was also observed that the internal NTC sensor nearly tracked the IGBT temperature due to its close proximity to the IGBT dies [10]. Therefore, the error between the infrared imaging results and the thermal model calculations was small. In modules where the NTC sensor is not located close to the IGBT dies, it is possible that the measured (actual) junction temperature will be higher than the estimated value, if the additional losses due to cable charging current are not taken into account.

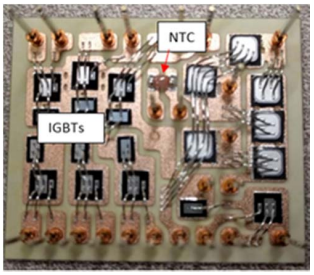


Fig. 21. Location of NTC thermistor within the power module

Cable Type	Cable length (m)	NTC resistor temp. (ºC)	IGBT junction temp. from thermal model (ºC)	Infrared measured IGBT temperature (ºC)
Standard	50	55	63	55
High Capacitance	50	85	93	88

Table 3: Thermal test results for the 1200V, 10A module with different cable types

C. Modifications to Thermal model for accurate junction temperature prediction

The increased switching losses because of long cables can be accounted for in the drive thermal model through two methods. Method 1 assumes that for a particular drive, the cable type and length requirement are known. Switching losses (Eon + Eoff) for different (standard) lengths of the standard cable construction can be measured and impedance values for cables can be characterized and implemented as look up tables in the drive. Switching losses and impendence for cable lengths different than of standard length extracted by curve fitting the data in the look up table. Auto-tuning with the proposed algorithm gives an estimate of impedance values. Losses can be adjusted through the look up table. This ensures that the effect of gate drive circuit of the drive is considered in the characterization but the method is test intensive.

Method 2 involves initial characterization with short cable length. Auto tuning with the proposed algorithm in Section I gives an estimate of peak current due to the long cable. The switching losses can be scaled as a fraction of increase in the current (ratio of the sum of load current and measured peak cable charging current over load current). This method is conservative and may over predict the losses. In Table 4, it is shown that the losses predicted through Method 2 are 50% more than the actual losses measured for the drive at 10A.

	Cable Type	Method I Measured Losses (mJ)	Method II Estimated Losses (mJ)
Rg = 22.6 Ω	3m std.	1.96	1.96
	50m std.	2.08	2.99
	90m std.	1.99	2.98
	50m High cap	3.51	5.02

Table 4 : Switching loss adjustment for long cables with different methods

V. CONCLUSIONS

A method to measure cable characteristic impedance, peak cable charging current and oscillation frequency for an AC drive with long motor leads has been developed. The application of the measured oscillation frequency to adjust the PWM pulse pattern and reduce peak motor voltage has been demonstrated through experimental results. This method reduces output voltage distortion compared to conventional reflected wave compensation schemes that clamp maximum modulation index to ensure a long dwell time and reduce peak motor voltage, and can be applied to inverters switching at high frequencies. Details of the PWM pulse pattern adjustment method, including the effects of dead time and volt-second imbalance were discussed.

A method to measure the power losses is described and a detailed explanation of the influence of cable parameters, power device characteristics and gate drive are provided. Experimental results are provided to validate the theory for the increase in power losses, and the influence of motor cable and gate drive parameters. Thermal test results, including infrared imaging, are provided to demonstrate the severity of the issue for small drives. An analytical method to estimate the increase in power losses to account for long cable effects, and

conservatively estimate IGBT junction temperature has also been provided.

VI. REFERENCES

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