75 MHz discrete GaN based multi-level buck converter for envelope tracking applications

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***Abstract*— The operation, design and implementation are described of a multi-level buck converter for switching frequencies approaching 100MHz together with an isolated high-side driver. The analysis of the converter identifies the trade-offs amongst the number of levels, switching frequency, efficiency, and filter bandwidth, which are key considerations for Envelope Tracking (ET) applications. The results show that this topology is particularly suitable to limit power losses caused by semiconductor output capacitances and common-mode parasitic capacitances as well as to increase the output filter tracking bandwidth. The power loss results are validated through simulation and experimentally using a 30V, 14W two-level prototype and a 30V, 14W five-level prototype operating at 75MHz and built using discrete GaN devices.**

Keywords—DC-DC converter, buck, multi-level, Envelope Tracking (ET), dynamic power supply, Gallium nitride (GaN).

I. Introduction

Envelope Tracking (ET) DC-DC converters can improve the efficiency of Radio Frequency Power Amplifiers (RFPAs) by modulating the supply voltage to the RFPA in accordance with the RF signal envelope, however this requires a very high dynamic performance from the DC-DC converter, Fig. 1. Gallium Nitride High Electron Mobility Transistors (GaN HEMTs) are well suited to this application not only because their switching speeds can bring improvements in efficiency, but also because the tracking speed and the accuracy of the converter output voltage increases with the switching frequency [1].

The buck converter and its multi-phase and multi-level variations have been investigated for ET supply modulators owing to their high efficiency and conversion-ratio linearity. Implementations of these converters have been reported in recent years using both GaN based Application Specific Integrated Circuits (ASICs) [2]–[5] as well as commercial and custom-made discrete GaN HEMTs [5]–[10]. ASICs are pushing the boundaries of the achievable operating frequency beyond 200MHz [3], and up to 800MHz [2], and are mainly constrained by thermal management, which limits their power rating and maximum voltage. On the other hand, implementations of these converters using discrete GaN devices have been reported to achieve up to 25MHz switching frequency with maximum power and input voltage ratings up to 68W and 42V respectively, mainly limited by the additional switching losses introduced by PCB layout parasitic components and the HEMETs output capacitance. For example, synchronous buck converters operating at 10MHz have been reported in [6] and [7] providing 40W from 20V and 10W from 20V respectively. A four-phase buck converter is reported in [8] achieving 25 MHz per phase from a 30V supply and power as high as 68W. Finally, MOSFET-based, three-level and four-level buck converters are reported in [9], [10], delivering 35W from 15V and 24W from 12V respectively at 4MHz switching frequency.

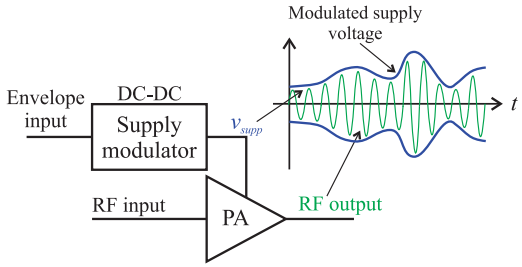

Fig. 1. Envelope tracking system.

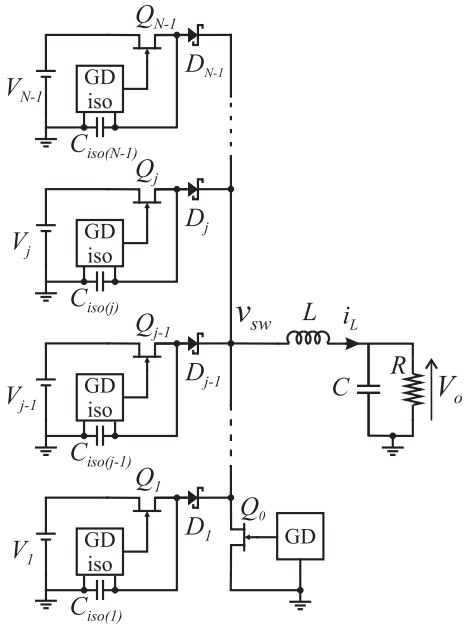

Fig. 2. N-level buck converter.

This paper reports on the operation, filter design, power loss analysis, and implementation of the multi-level buck

This work was supported by the U.K. Engineering and Physical Sciences Research Council, project reference [EP/N016610/1].

circuit, Fig. 2, up to 75MHz. Compared with previous research, a new switching pattern is proposed and the trade-offs amongst switching frequency, number of levels, efficiency and output filter bandwidth (maximum tracking frequency) are identified. The contribution of the semiconductor output capacitance and the common-mode capacitance charge/discharge mechanisms are included in the power loss modelling. Finally, the output filter design of the converter is compared against that of a single, two-level buck converter. Furthermore, to implement the converter, a floating high-side driver is demonstrated. (The fastest half-bridge driver in the market is the Texas Instruments LMG1210 achieving 50MHz).

The converter operation is discussed in Section II. The power loss modelling for an N-level converter and its filter design are presented Section III and IV respectively. The prototype implementation of a five-level buck and two-level/synchronous buck are discussed in Section V. The power loss model is validated experimentally and the efficiency and tracking performance of the prototypes is compared in Section VI. Finally, Section VII provides the conclusion and research contributions.

II. Multi-level Converter Operation

Fig. 2 shows the circuit diagram of the multi-level buck converter. The circuit comprises $N–1$ branches connected in parallel to an LC output filter and to a synchronous rectifier, Q_0. Each branch consists of an input voltage source, V_j, a transistor, Q_j, and a diode, D_j, where $j = 1, 2, \ldots, N–1$. The transistor control signals are level-shifted using an isolated gate-driver, which is represented by the block *"GD iso"* and a corresponding equivalent isolation capacitance, $C_{iso(j)}$. The value of the input voltage sources per branch is $V_1 < V_2 < \ldots < V_{N-1}$, where the values are chosen to meet the application minimum and maximum output voltage requirements respectively. The diodes in the circuit prevent current flowing from a higher voltage source to a lower one.

Two adjacent branches are operated at any time whilst the remaining ones are inactive. As depicted in Fig. 2, the active upper branch is identified with the subscript j and the lower, active branch with $(j–1)$. The time that branch j remains active is defined as $(d_{j,\,j-1})T$, where $d_{j,\,j-1}$ is the duty ratio between branches j and $(j–1)$, and T is the switching period. Conversely, $(1–d_{j,\,j-1})T$ is the interval when branch $(j–1)$ is conducting.

The waveforms shown in Fig. 3 illustrate the operation of a five-level converter assuming ideal components and continuous conduction of the inductor current. The first waveform depicts v_{sw} whilst the waveforms below show the magnification of six switching cycles. The first magnified waveform shows v_{sw}; the second, third and fourth waveforms are the control signals of transistors Q_4 to Q_2, V_{g4} to V_{g2} respectively; the bottom waveform is the inductor current, i_L.

During the first three switching cycles of the magnified waveforms in Fig. 3, the converter is commutating between V_3 and V_4. Q_4 follows a PWM pattern whilst Q_3 remains on. When Q_4 is conducting, interval $(d_{4,\,3}T)$, diode D_3 is reverse-biased and $v_{sw} = V_4$. Conversely, when Q_4 is deactivated, $(1–d_{4,\,3})T$, D_3 is forward biased and $v_{sw} = V_3$. The diodes of the lower branches are reverse biased during this interval. Finally, for the remaining three switching cycles of Fig. 3, v_{sw} is commutating between V_3 and V_2.

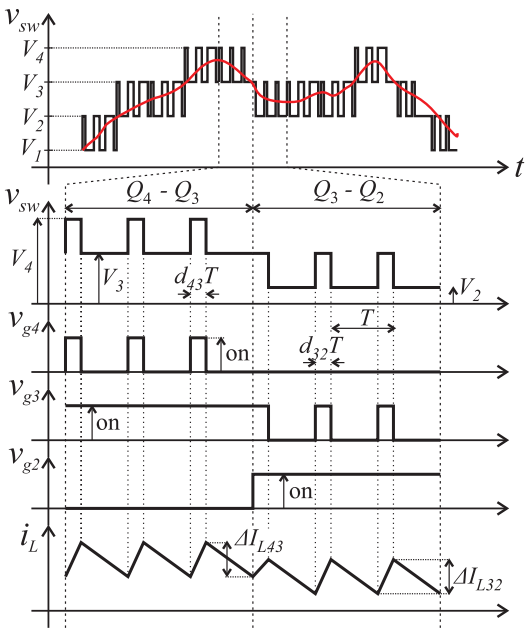

Fig. 3. Five-level buck converter waveforms.

The local average converter output voltage can be derived via the inductor volt-second balance, yielding:

$$V_o = d_{j,j-1}V_j + (1-d_{j,j-1})V_{j-1} \tag{1}$$

The inductor current ripple amplitude can be expressed as:

$$\Delta I_L = \frac{\left(V_j - V_{j-1}\right) d_{j,j-1}\left(1-d_{j,j-1}\right)}{2 f_{sw} L} \tag{2}$$

Finally, using the capacitor charge balance together with (1) and (2), the output voltage ripple is:

$$\Delta V_o = \frac{\left(V_j - V_{j-1}\right) d_{j,j-1}\left(1-d_{j,j-1}\right)}{8 f_{sw}^{\,2} LC} \tag{3}$$

III. Power Loss Analysis

The first part of this section details the power loss modelling for an N-level buck converter. The second part uses the model to predict the loss behavior and to identify the trade-offs amongst switching frequency and number of levels.

A. Power loss modelling

The analysis includes the power-stage conduction losses, turn-on switching losses, turn-off switching losses, and inductor losses. It is assumed that the semiconductor components in the converter branches are identical and the inductor operates with continuous current. The inductor power losses were obtained from the manufacturer's tool available on their website [11].

1) Conduction losses

Fig. 4 (a) and 4(b) show equivalent circuits of the converter operating in multi-level mode the total conduction losses are:

$$P_{cond} = \left(I_L^2 + \frac{\Delta I_L^2}{12} \right) r_{ds(on)} + I_L V_{fwd} \tag{4}$$

where I_L is the average inductor current, $r_{ds(on)}$ is the transistor on-resistance and V_{fwd} the forward voltage of the diodes. When the lowest branch of the converter is operated, the losses are:

$$P_{cond} = \left(I_L^2 + \frac{\Delta I_L^2}{12} \right) r_{ds(on)} + I_L V_{fwd} d_{j,j-1} \tag{5}$$

2) Turn-Off switching losses

The turn-off losses of Q_j are neglected since the active and inactive branch capacitances act as snubber capacitor connected to v_{sw}, allowing the transistor current to fall before its drain-to-source voltage rises significantly.

3) Turn-On switching losses

The turn-on loss is calculated from the current rise/voltage fall transition in the transistor Q_j (hard-switching) and by the charging/discharging of the switching-node capacitance introduced by the active and the inactive branches of the converter. The hard-switching loss during the turn-on transition of Q_j is:

$$P_{sw} = \left[\frac{\left(V_j - V_{j-1} \right) I_{Lmin}}{2} \left(t_{i\_rise} + t_{v\_fall} \right) \right] f_{sw} \tag{6}$$

where $I_{Lmin} = I_L - \Delta I_L/2$, and t_{i_rise} and t_{v_fall} are the rise time of the transistor drain current and the fall time of the transistor drain-to-source voltage respectively.

The power loss introduced by the charging/discharging of the semiconductor and isolation capacitances of the active branch is:

$$P_{C\_active} = \left\{ \frac{1}{2} C_{oss\_eq} \left(V_j - V_{j-1} \right)^2 + \frac{1}{2} C_{D\_eq} \left(V_j - V_{j-1} \right)^2 + \ldots \right.$$
$$\left. \ldots + \frac{1}{2} C_{iso} \left[(V_j)^2 - (V_{j-1})^2 \right] \right\} f_{sw} \tag{7}$$

C_{oss_eq} is the energy-related equivalent output capacitance of Q_j, C_{D_eq} is the energy-related equivalent capacitance of D_{j-1}, and C_{iso} is the common mode capacitance of the driver in channel j.

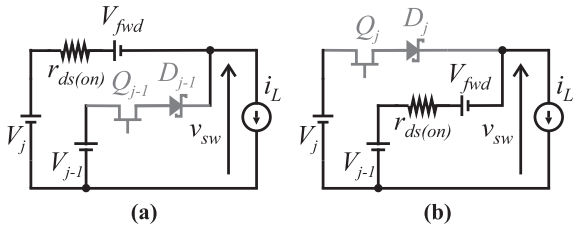

Fig. 4. Equivalent circuits for conduction loss modelling.(a) Interval $(d_{j,j-1})T$ and (b) Interval $(1-d_{j,j-1})T$.

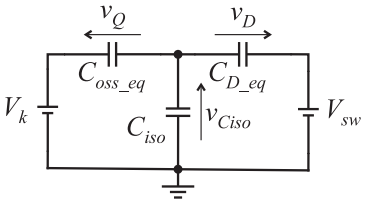

Fig. 5. Equivalent capacitive circuit of the inactive branches.

The power loss due to the charging/discharging of the parasitic capacitances of the inactive branches is:

$$P_{C\_inactive} = P_Q + P_D + P_{Ciso} + \frac{1}{2} C_{oss\_eq} \left(V_j^2 - V_{j-1}^2 \right) \tag{8}$$

where P_Q, P_D and P_{Ciso} are (9), (10) and (11) respectively (bottom of the page). The functions $V_Q(V_k,V_{sw})$, $V_D(V_k,V_{sw})$ and $V_{Ciso}(V_k,V_{sw})$ in (9) to (11) give the voltage across the transistor, diode and isolation capacitance in the k^{th} inactive branch and are determined from the equivalent circuit of Fig. 5:

$$V_Q(V_k, V_{sw}) = \frac{V_l C_{iso} + \left(V_k - V_{sw} \right) C_{D\_eq}}{C_{iso} + C_{oss\_eq} + C_{D\_eq}} \tag{12}$$

$$V_D(V_k, V_{sw}) = \frac{V_l C_{iso} - \left(V_k - V_{sw} \right) C_{oss\_eq}}{C_{iso} + C_{oss\_eq} + C_{D\_eq}} \tag{13}$$

$$V_{Ciso}\left(V_k - V_{sw} \right) = \frac{V_k C_{oss\_eq} + V_{sw} C_{D\_eq}}{C_{iso} + C_{oss\_eq} + C_{D\_eq}} \tag{14}$$

where V_k is the branch input voltage.

B. Power loss model predictions

The power loss model was implemented in a MATLAB script to evaluate the sensitivity of the power losses to the number of levels and switching frequency. The parameters are listed in Table I and correspond to the prototypes used in Section V. The input voltages of the converters were equally

$$P_Q = \frac{1}{2} C_{oss\_eq} \left\{ \sum_{k=1}^{j-2} \left[V_Q^2(V_k, V_{j-1}) - V_Q^2(V_k, V_j) \right] + \sum_{k=j+1}^{N-1} \left[V_Q^2\left(V_k, V_{j-1}\right) - V_Q^2\left(V_k, V_j\right) \right] \right\} f_{sw} \tag{9}$$

$$P_D = \frac{1}{2} C_{D\_eq} \left\{ \sum_{k=1}^{j-2} \left[V_D^2(V_k, V_j) - V_D^2(V_k, V_{j-1}) \right] + \sum_{k=j+1}^{j-2} \left[V_D^2\left(V_k, V_j\right) - V_D^2\left(V_k, V_{j-1}\right) \right] \right\} f_{sw} \tag{10}$$

$$P_{Ciso} = \frac{1}{2} C_{iso} \left\{ \sum_{k=1}^{j-2} \left[V_{Ciso}^2(V_k, V_{j-1}) - V_{Ciso}^2(V_k, V_j) \right] + \sum_{k=j+1}^{j-2} \left[V_{Ciso}^2\left(V_k, V_{j-1}\right) - V_{Ciso}^2\left(V_k, V_j\right) \right] \right\} f_{sw} \tag{11}$$

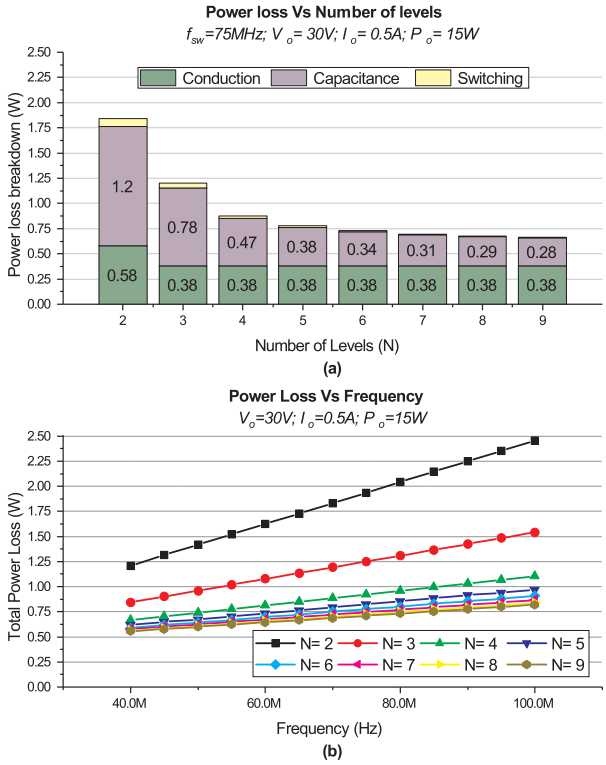

Fig. 6. (a) Power loss break down as the number of levels is varied. (b) Total power loss as the number of levels and frequency are varied.

TABLE I. MODEL INPUT PARAMETERS

Transistor: GaN EPC8002				Diode: PMEG4005		Other	
$R_{ds(on)@125°C}$	C_{oss_eq}	C_{gs_eq}	V_{sd}	$V_{fwd@0.5A}$	C_{D_eq}	C_{iso}	L
608mΩ	8.9pF	26.6pF	2.3V	590mV	10.2pF	9.26pF	1μH

distributed between the minimum output voltage (11V) and the maximum output voltage (28V).

Fig. 6(a) shows the predicted power loss breakdown for converters with two up to nine levels. The assumed operating point was f_{sw}= *75MHz,* V_o= *30V,* I_o= *0.5A* (maximum power). The conduction losses do not change significantly with the number of levels except for the two level converter where additional loss is generated during the dead-time periods when the synchronous rectifier "body-diode" conducts the free-wheeling current. The switching-node capacitance loss is the dominant switching-related loss but reduces as the number of levels is increased since the parasitic capacitances are charged/discharged to a smaller fraction of the maximum input voltage.

The plots in Fig. 6(b), show the losses as a function of the switching frequency and the number of levels. The operating point was assumed to be I_o= 0.5A, V_o= 30V, maximum power. As expected, the power losses decrease significantly as the number levels increase from two up to four, enabling higher switching frequencies to be reached; however, the power losses do not decrease significantly for levels higher than four.

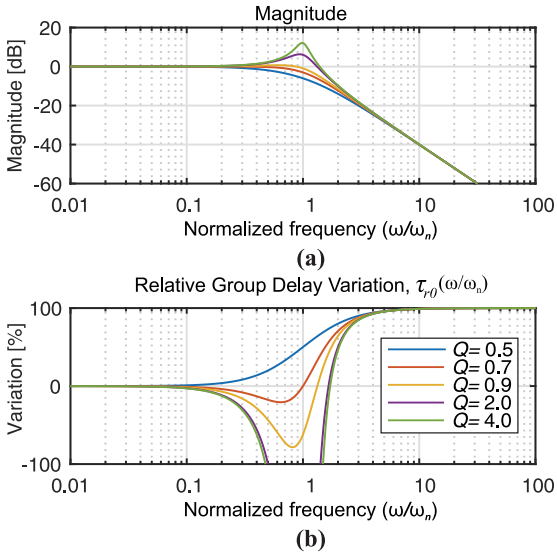

Fig. 7. Second order filter frequency response. (a) Magnitude, (b) Group delay variation with respect to its low frequency value.

IV. FILTER DESIGN FOR BAND-LIMITED ENVELOPE SIGNALS

The filter design is a compromise between providing sufficient attenuation of the switching frequency ripple of the converter output, whilst ensuring faithful reproduction of the envelope waveform. The converter output filter, Fig. 2, is a standard second order circuit with natural frequency ω_n and quality factor Q where:

$$\omega_n = 1/\sqrt{LC} \tag{15}$$

$$Q = R\sqrt{C/L} \tag{16}$$

For an N-level converter, the output-voltage ripple, can be found using (3) and (15):

$$\Delta V_o = \frac{\pi^2 \left(V_j - V_{j-1}\right) d_{j,j-1} \left(1 - d_{j,j-1}\right)}{2} \left(\frac{f_n}{f_{sw}}\right)^2 \tag{17}$$

To achieve distortion less reproduction of the envelope waveform, the magnitude of the filter input-output voltage transfer function must be flat over the frequency range of the envelope waveform, up to f_{env_max}. Furthermore the group delay of the input-output transfer function must remain constant for frequencies up to f_{env_max}. The group delay, τ, is an indication of the phase distortion introduced to a signal by a filter over a band of frequencies and it is defined as the derivative of the filter phase response with respect to the angular frequency, ω:

$$\tau\left(\omega/\omega_n\right) = \tau_0 \left[\frac{1 + \left(\omega^2/\omega_n^2\right)}{1 + \left(\left(1/Q^2\right) - 2\right)\left(\omega^2/\omega_n^2\right) + \left(\omega^4/\omega_n^4\right)}\right] \tag{18}$$

TABLE II. FILTER CHARACTERISTICS AND COMPONENT VALUES

(A): f_{sw}= 75MHz, ΔV_o= 0.25V

Levels	*2*	*3*	*4*	*5*	*6*
f_n *[MHz]*	6.2	8.7	10.7	12.3	13.8
f_{e_max}@τ_{r0}=2% *[MHz]*	0.88	1.3	1.5	1.8	2
L [µH]	2.0	1.4	1.2	1.0	0.91
C [pF]	326.0	230.0	188.0	163.0	146.0

(B): f_n= 12.3MHz, ΔV_o= 0.25V

f_{sw} *[MHz]*	151.2	106.9	87.3	75.0	67.6

(C): f_{sw}= 75MHz, f_n= 12.3MHz

ΔV_o *[V]*	1.0	0.50	0.34	0.25	0.20

where τ_0 is the group delay at low frequency, $\tau_0 = 1/(Q\omega_n)$. Since the group-delay changes with Q, the variation of the group delay with respect to τ_0 can be used to quantify its maximum variation:

$$\tau_{r0}\left(\omega/\omega_n\right) = \left(100/\tau_0\right)\left[\tau_0 - \tau\left(\omega/\omega_n\right)\right][\%] \qquad (19)$$

Fig. 7(a) shows the magnitude of the filter input-output voltage transfer function for a range of Q values. The frequency axis is normalized to ω_n. Fig. 7(b) shows the relative group delay variation. To prevent any peaking in the magnitude response in the region of ω_n, the maximum Q is limited to 0.7, whilst to ensure the relative group delay varitaion is less than 2%, ω_n must be seven times ω_{env_max}.

A. Converter number of levels and filter characteristics

Table II summarizes the filter design for an increasing number of levels. Table II(A) assumes f_{sw}= 75MHz, ΔV_o= 0.25, Q= 0.7 and a maximum permitted group delay variation of 2%, and shows that the filter natural frequency, ω_n, and the maximum tracking frequency, f_{env_max}, increase with the number of levels due to the inherently lower output ripple in the multi-level circuits. A tracking frequency of 1.8MHz is achieved for a five-level circuit. Table II(B) shows the switching frequency that is needed to achieve the output voltage ripple target of 0.25V using the filter values for the five-level circuit. The switching frequency with the two-level topology would need to be doubled to 150MHz to match the performance of the five-level circuit, which would severely reduce the system efficiency. In contrast, Table II(C) shows how the output voltage ripple varies with the number of levels for a fixed switching frequency of 75MHz and using the filter values for the five-level circuit. The output voltage ripple with only a two-level circuit is increased by a factor of four compared with the five-level topology.

V. CONVERTER PROTOTYPES

A two-level and a five-level prototype were fabricated to validate the power loss predictions and the voltage tracking capacity. The prototype parameters, Table III, assume an RF amplifier with maximum drain voltage of 28V and a maximum power of 14W. Both prototypes, used EPC8002 GaN

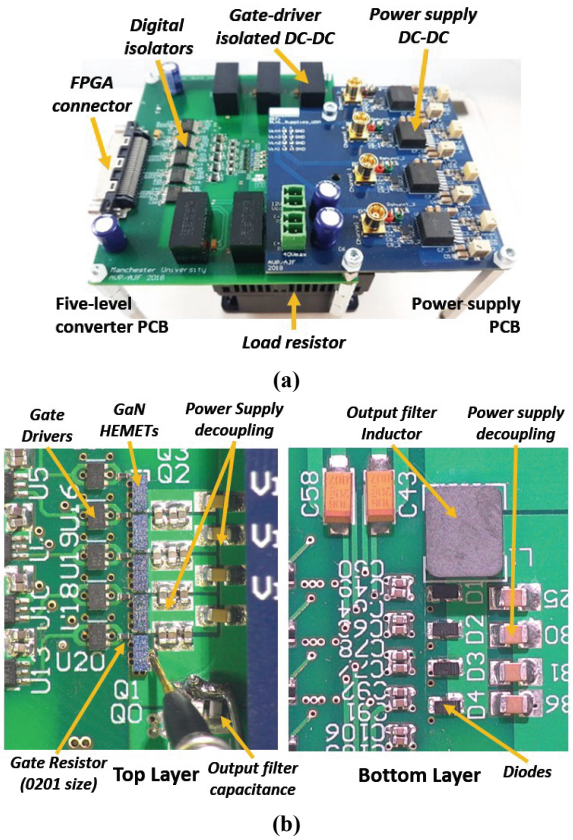

Fig. 8. Five-level converter prototype. (a) Full system including isolated gate-drivers, power stage transistors, power supply PCB and load. (b) Close up of the power stage.

TABLE III. CONVERTER DESIGN PARAMETERS

$V_{in(max)}$	$V_{o(min)}$	$V_{o(max)}$	$I_{o(max)}$	$I_{o(min)}$
30V	11V	28V	0.5A	0.1A

HEMETs (65V, 2A) due to their low output capacitance. For the five-level converter, Nexperia PMEG4005EPK Schottky diodes were used (40V, 0.7A). The output filter inductors were the Coil Craft 1812PS series with a resonant frequency above 350MHz. Four-layer PCBs were used to optimize the layout and minimize circuit parasitics. Four Texas Instruments, LMZ14201HTZ step-down converters were used to provide the input voltages for the five-level converter. Fig. 8(a) shows the five-level converter including the power supply PCB, whilst Fig. 8(b) and 8(c) show a close up of the power stage transistors, gate-drivers diodes and filter components.

A. Isolated gate-driver

To reach 75MHz operation an isolated gate driver was implemented. Fig. 9 shows a block diagram with the main stages of the gate-driver circuitry. The first stage is the Analogue Devices, ADN4650 digital isolator to level-shift the incoming control signals from the FPGA. These digital isolators operate with low-voltage differential signaling (LVDS) which is capable of operation up to 600Mbps. The second stage level-translation circuitry amplifies the LVDS signals to 5V. Finally, two UHS logic buffers (NC7WZ16)

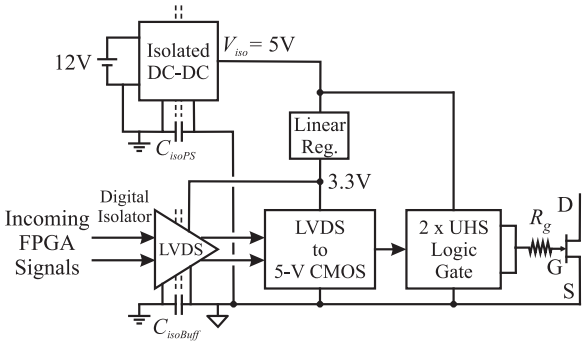

Fig. 9. Isolated gate-driver.

connected in parallel are used to drive the transistor gates. The gate-driver circuitry was powered using a RECOM R12P05S/R8 isolated DC-DC regulator from a 12V DC supply. The total measured current consumption of the gate-driver was 40mA under static conditions and 48mA at 75MHz operation.

B. *Converter control and PWM signal generation*

A Marvin Test Solutions GX3700e development card was used to control the converter prototypes. This card features an Stratrix III FPGA where a hybrid Digital Pulse-Width-Modulator, DPWM, with a base-clock of 600MHz and approximately 30ps resolution was implemented to generate the transistor control signals [12]. Additional VHDL scripts were developed to generate the complimentary signals with dead-time of the two-level converter and to operate the five-level converter channels.

VI. Experimental Results

A. *Model validation and efficiency*

Figs 10(a) and 10(b) show a comparison of the static power-stage efficiency predicted for the five-level converter against that measured from the prototype at 50MHz and 75MHz respectively. Similarly, Fig. 10(c) compares the measured and predicted static efficiency for the power-stage of the two-level converter at 75MHz. The five-level converter power supply losses are excluded. To obtain these results, the output voltage was varied from 11V to 30V with fixed values of output current: I_o= 100mA (red plots) and I_o= 500mA (blue plots). The solid lines show the predicted efficiency and the squares the experimental data.

A good agreement between the predictions and the experimental results was obtained. An over-estimation of the losses is observed for the five-level converter. This is attributed to the non-linear capacitances of the semiconductors which were approximated with their energy-related equivalents. The major discrepancies are at points of operation with low current/voltage and attributed to the accuracy of the measurement system as well as second order effects such as parameter variation with temperature, and additional PCB circuit parasitics. The maximum absolute error between the measured and predicted efficiency of the five-level converter at 75MHz, 100mA was approximately five percentage points and the maximum average error over the range of operation for these conditions was 2.6%.

The plots in Figs. 11(a),11(b) and 11(c) compare the measured total efficiency of the two-level and the five-level

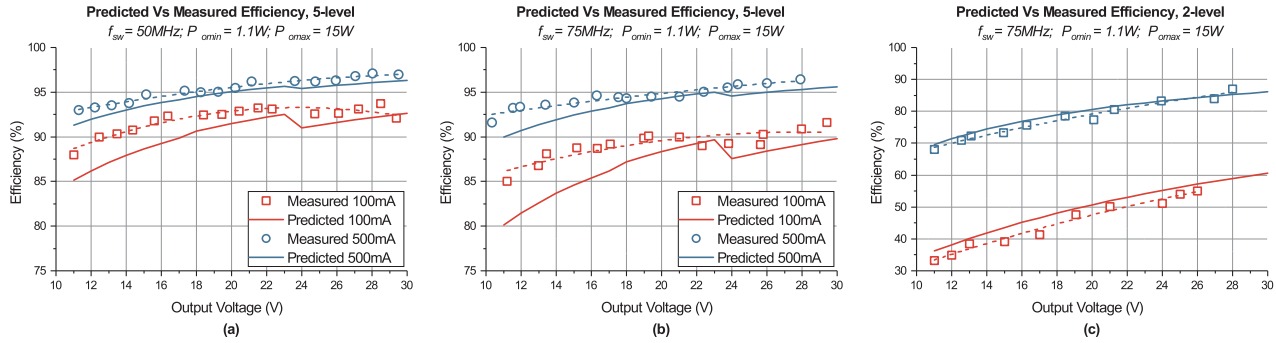

Fig. 10. Comparison between predicted efficiency and measured efficiency. (a) Five-level converter at 50MHz; (b) Five-level converter at 75MHz; (c) Two-level converter at 75MHz.

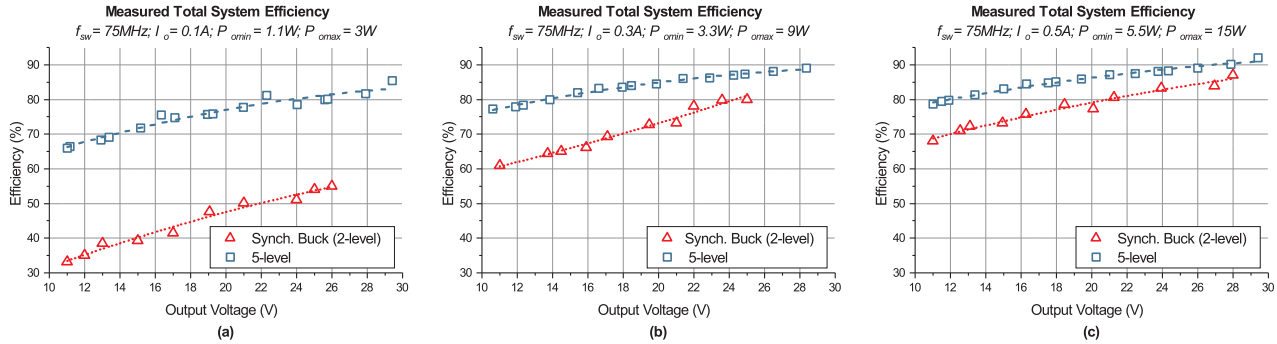

Fig. 11. Comparison of the total system efficiency for the five-level converter and the two-level converter. The five-level converter system plots include the efficiency of the power-supplies used to generate all the converter input voltages.

converter prototypes at I_o= 100mA, 300mA and 500mA. This measurements include the losses in the five-level converter input power supplies. The measurements were performed at 75MHz switching frequency with V_o going from 11V to 30V. The triangles are data measured from the two-level converter and the squares are the data from the five-level converter.

The average efficiency for the five-level converter over the range of operation shown is 76.6%, 83.6% and 85.2% for 100mA, 300mA and 500mA respectively, whilst for the two-level converter it is 44.5%, 70.9% and 77.3% respectively. The superiority of the five-level converter stands out especially at low-power levels with 32.1 percentage points of difference. The five-level converter efficiency peaks at 92% and the two-level at 87% at 500mA output current.

B. Converter operation and output voltage tracking

For the experiments shown in this section, the component values of the converter output filters were set to L= 1µH and C= 164pF, corresponding to the design case (C) of Table II where f_{sw}= 75MHz, and ΔV_o= 1V for the two-level converter and ΔV_o= 0.25V for the five-level converter.

Fig. 12(a) shows the gate-to-source voltages of the high-side and low-side transistors, v_{gs_Q1} (yellow) and v_{gs_Q0} (pink) respectively, and v_{sw} (green) for the two-level converter confirming the correct operation of the gate-driver. The dead-time between the transistor gate signals was set to 1 ns. Fig. 12(b) shows the two-level converter tracking a 750kHz ramp waveform with duty-ratio going from 36% (11V) to 90% (27V). (The maximum duty-ratio is limited by the maximum pulse-width capacity of the hybrid DPWM, which is determined by the time taken to reload its tapped-delay line [12]). Fig. 12(c) shows results of the two-level converter output voltage tracking a 1MHz sine waveform with duty-ratio going from 36% (11V) to 90% (27V) with a total efficiency of 62%.

Fig. 13(a) shows v_{gs_Q4} (yellow), v_{gs_Q2} (pink) and v_{sw} (green) of the five-level converter prototype at 75MHz and with input voltages 11V, 17V, 23V and 30V. An 80% over-shoot is observed during the transistor turn-on transitions (v_{sw} rising) caused by the parasitic inductances of the PCB. Fig. 13(b) shows results of the five-level converter output voltage tracking a 750kHz ramp going from 11V to 28V. The sudden variations observed in the slope of the ramp occur when the converter is transitioning from a pair of active branches to the next. At these boundaries, the current pair of active branches reach $d_{j,j-1}$= 90% (limited by the DPWM) and transition to the next pair of active branches where $d_{j+1,j}$= 0%. The 10% gap in these transitions generate the distortion. Finally, Fig. 13(c) shows the output voltage tracking a sinusoidal waveform of 1MHz with a measured efficiency of 85.3%. The distortion observed is also caused by the DPWM pulse-width limitation.

VII. Conclusions

This work presents the operation, filter design, power loss modeling, and implementation of a multi-level buck circuit suitable for switching frequencies approaching 100MHz. This circuit was found to be effective in reducing the parasitic capacitance losses at transistor turn-on due to the reduced switching voltage across the capacitors. It was shown that

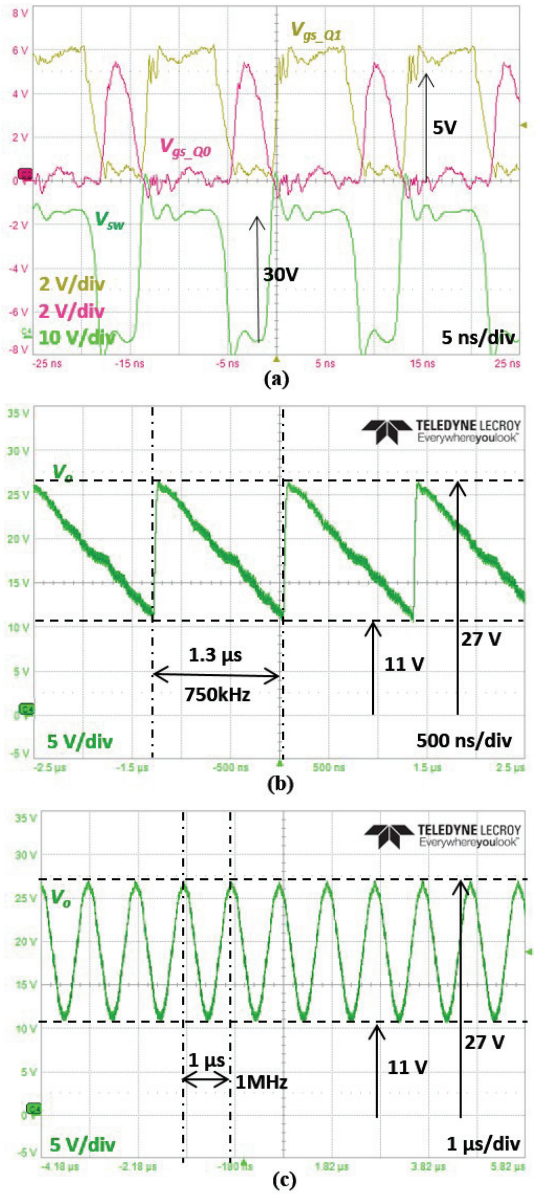

Fig. 12. Experimental results of the two-level converter at f_{sw}= *75MHz,* and input voltage of *30V*. (a) Switching waveforms measured at V_o=*19.2V* and I_o= *0.5A*; (b) Output voltage tracking a 750kHz ramp waveform, R_{load}=*56 Ω*; (c) Output voltage tracking a 1MHz sinusoidal waveform, R_{load}= *56 Ω*.

increasing the number of levels beyond five for an EPC8002 based converter does not bring significant benefits to the efficiency at 14W power level. Also, the results suggest that it is possible to extend the frequency of operation of a five-level converter up to 100MHz. In terms of filter design, increasing the number of levels whilst keeping the same filter natural frequency results in significant switching frequency and/or output-voltage ripple amplitude reductions.

A five-level and a two-level converter were demonstrated operating at up to 14W, 75MHz together with an isolated high-side driver developed to operate at frequencies beyond 50MHz and without minimum pulse-width restrictions. The total gate

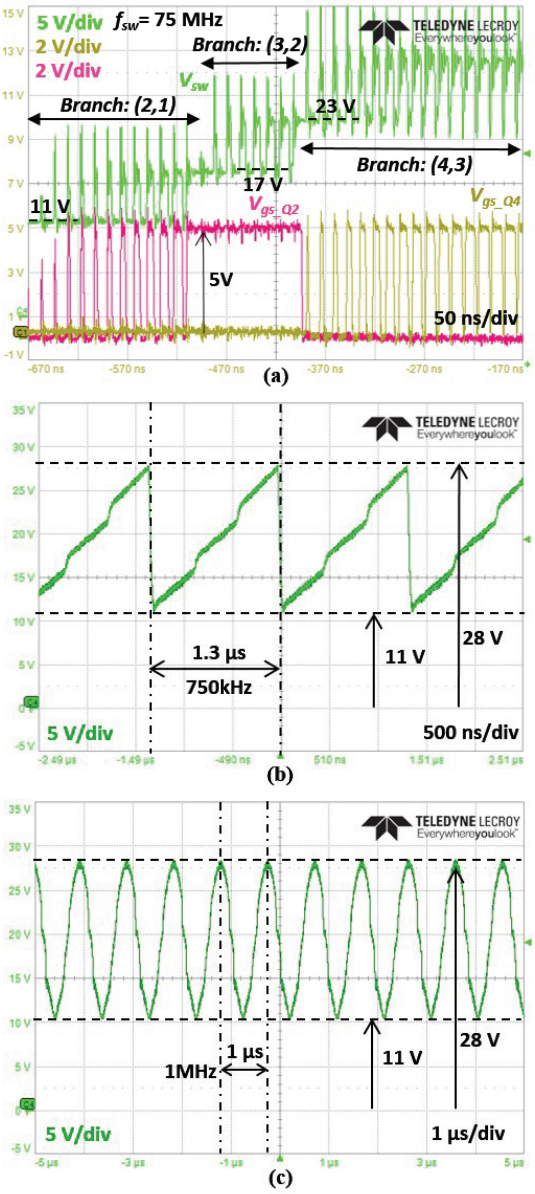

Fig. 13. Experimental results of the five-level converter at f_{sw}= *75MHz,* and input voltages of *11V, 17V, 23V* and *30V*. (a) Switching-node waveforms measured with the output voltage tracking a sinusoidal waveform and R_{load}=*56 Ω*; (b) Output voltage tracking a 750kHz ramp waveform, R_{load}=*56 Ω*; (c) Output voltage tracking a 1MHz sinusoidal waveform, R_{load}= *56 Ω*.

driver current consumption was measured to be 48mA from a 12V power supply and has not been included in the experimental and/or predicted power losses as the driver circuit was not optimized for efficiency performance. The prototypes were used to validate the efficiency predictions of the power-stage showing a maximum absolute error between measurements and predictions of 5 percentage points and a maximum average error of 2.6%. The experimental results confirm the predicted superior efficiency of the five-level converter, which was 32 percentage points more efficient than the two-level one at *Io*= 100mA and 8 percentage points more efficient at *Io*= 500mA. Importantly, these results include the additional losses in the DC-DC converters that provided the multi-level input voltage rails from the DC supply.

Finally, the tracking performance of both converters was assessed using 750kHz ramp and 1MHz sinusoidal waveforms. The maximum voltage achieved by the two-level converter was limited due to the maximum pulse-width of the FPGA-based PWM generator. This also created some minor distortion in the operation of the five-level converter as the system transitioned from one pair of levels to the next pair.

Overall, the results highlight the promise of multi-level converters for very high frequency envelope tracking applications. Ongoing research is investigating the best combinations of transistors and number of levels to optimize the efficiency over typical envelope tracking operating profiles, more sophisticated switching strategies to overcome the cross-over distortion effect between pairs of active levels and the development of an efficiency optimized gate-driver.

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