A KY Buck-Boost Converter with Extended Ramp Control Achieving 1500% Output Variation Reduction for Smooth Mode Transition

Yu-Ting Hung
Graduate Institute of Electronics Engineering
National Taiwan University
Taipei, Taiwan
d09943004@ntu.edu.tw

Chieh-Ju Tsai
Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan
f04943123@ntu.edu.tw

Ching-Jan Chen
Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan
chenjim@ntu.edu.tw

Chun-Yu Hsieh
NovaTek Corporation
Taipei, Taiwan
azure_hsieh@novatek.com.tw

***Abstract*—In this paper, a KY buck-boost converter with extended ramp control for the Li-ion battery in the mobile applications is presented. Conventional non-inverting buck-boost converter suffers from several issues, including high conduction loss due to the excessive average inductor current and right-half-plane (RHP) zero existence which degrades the system stability and the transient performance. A KY buck-boost converter is a good candidate to relieve these problems. Unlike the conventional triple mode control utilized in the buck-boost converters, the proposed extended ramp control can achieve smaller output voltage fluctuation when the input voltage is close to the output voltage. The chip prototype is designed using a TSMC 0.18um BCD process. Simulation results show that compared with triple mode non-inverting buck-boost converter, 1500% output voltage fluctuation reduction (less than 10mV) during mode transition is achieved in the proposed control. The peak efficiency of this work can achieve 95.1%.**

Keywords—Buck-Boost converter, KY Buck-Boost converter, Li-ion battery management, Smooth mode transition

I. INTRODUCTION

In the recent years, the Li-ion battery has been widely used for mobile devices [1]. As time goes by, the voltage of Li-ion battery will gradually decrease from 4.2V to 2.7V. However, most functional blocks in the mobile devices require a stable 3.4V supply voltage. The common method is implemented by a non-inverting step up/down converter [2] – [4]. The structure and operation of the conventional non-inverting buck-boost converter is shown in Fig. 1(a). A large conversion range can be achieved to meet the requirement for the Li-ion battery in the mobile devices. Nevertheless, as depicted in Fig. 1(b), the RHP zero attributed to the discontinuous power delivery to output not only degrades the system stability but also slows down the load transient response of the converter. Besides, large average inductor current leads to significant conduction loss and thus deteriorates the power efficiency at heavy load which is also demonstrated in Fig. 1(b).

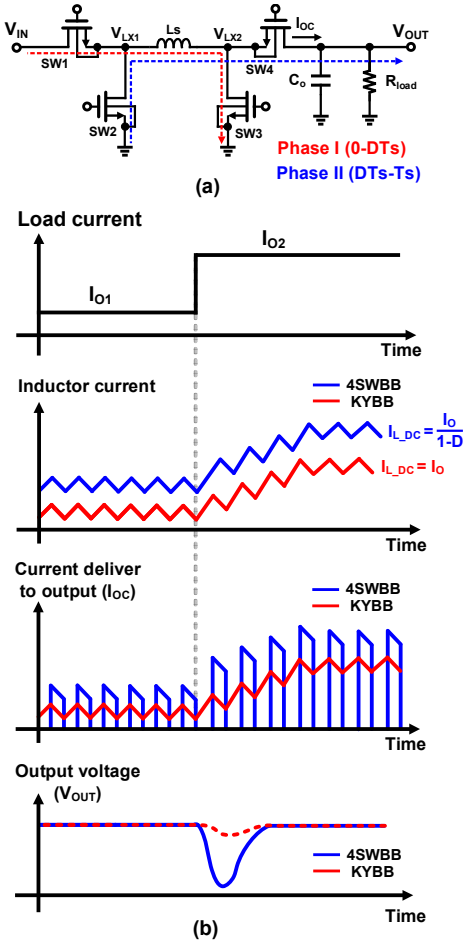

Fig. 1. (a) Structure & operation of conventional non-inverting buck-boost converter. (b) Load transient waveform comparisons of two buck-boost converter.

A hybrid topology named as KY buck-boost converter [5] has the potential to relieve the issues which are mentioned above. Fig. 2 shows the structure and operation of the KY buck-boost converter. The buck mode is identical to the conventional buck converter which is composed of phase I and phase II. For the boost mode operation that is the same as the KY boost converter [6], during phase III, V_{LX} is pumped to $2V_{IN}$ causing the inductor L_s to be magnetized and the flying capacitor C_{fly} to be discharged. On the other hand, during phase IV, C_{fly} is charged by the input voltage. The ideal conversion ratio of the boost mode can be derived as 1+D which D represents the duty cycle of the switch control signal. Since the inductor is placed at the output as the buck converter, the KY buck-boost converter delivers a continuous output current and a faster load transient response is achieved compared to the conventional non-inverting buck-boost converter. Furthermore, the average inductor current is independent to the duty cycle of the switch control signal, thereby causing a smaller conduction loss when the input voltage is close to the output voltage.

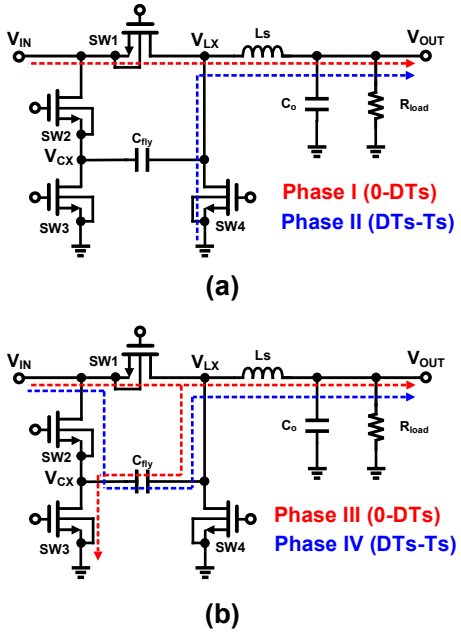

Fig. 2. Structure & operation of KY buck-boost converter : (a) buck mode (b) boost mode.

To improve the power efficiency of the converter, triple mode buck-boost converter has been proposed in [7] – [8]. The operation of the triple mode buck-boost converter is depicted in Fig. 3(a). Buck mode and boost mode are added. The original operation mode is equal to the buck-boost mode. As shown in Fig. 3(b), the average inductor current (I_L) is reduced in both buck mode and boost mode. However, there is still no reduction in the buck-boost mode. Furthermore, some challenges including large output fluctuation during mode transition as demonstrated in Fig. 3(c) and RHP zero existence in the boost and buck-boost mode occur in the triple mode buck-boost converter. Although some prior works [9] – [11] insert a buffer region to replace the buck-boost mode to achieve smooth mode transition, circuit design complexity is also increased. Therefore, an extended ramp control without additional mode control is proposed in this paper not only to achieve smooth mode transition but also to reduce the design complexity.

The paper is organized as follows. System architecture and the introduction of the proposed extended ramp control are presented in section II. The chip simulation results of the proposed KY buck-boost converter are demonstrated in section III. Finally, a conclusion will be given in section IV.

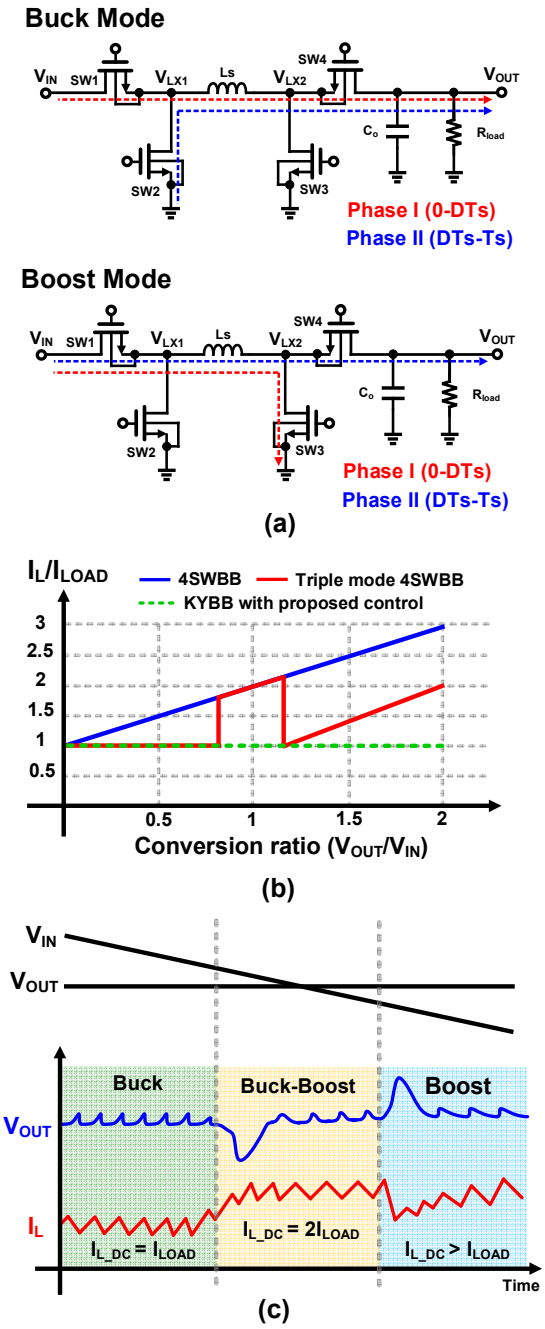

Fig. 3. (a) Operation of the triple mode buck-boost converter. (b) Ratio of inductor current versus load current among three converters. (c) Mode transient waveforms of the triple mode buck-boost converter.

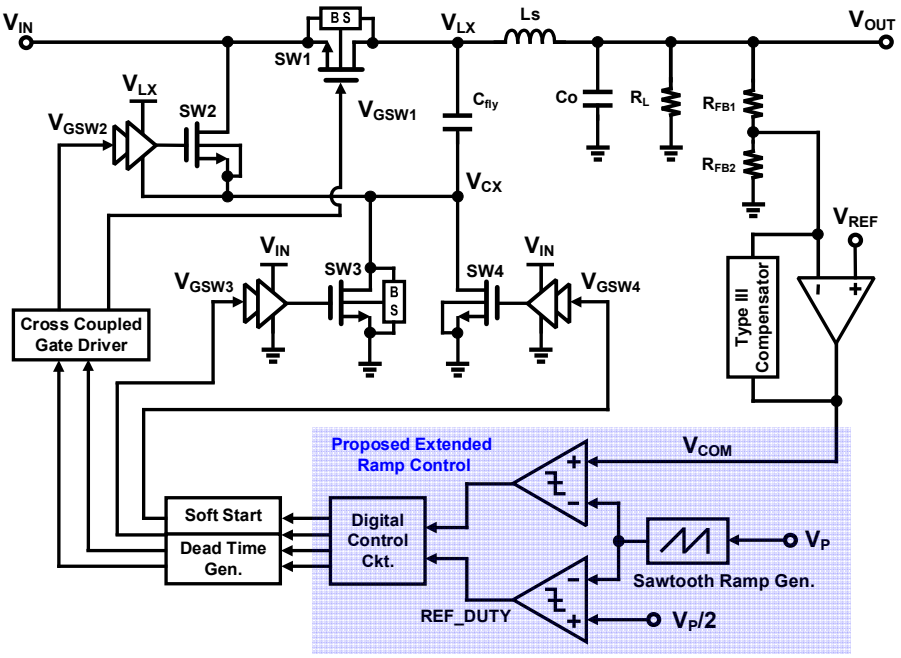

Fig. 4. Architecture of the proposed KY buck-boost converter with the extended ramp control.

II. The Proposed KY Buck-Boost Converter With Extended Ramp Control

A. The proposed system architecture

Fig. 4 demonstrates the architecture of the proposed KY buck-boost converter with the extended ramp control. The converter is mainly composed of a KY buck-boost power stage, a sawtooth waveform generator and digital control circuits including pulse-width modulation (PWM) control circuits. The switch control signal (V_{GSW1} ~ V_{GSW4}) is generated through the digital control circuits and the cross coupled gate driver. A proportional integral derivative (PID) compensator is applied in this work to stabilize the converter. Besides, this converter employs all NMOS power switches (SW1 ~ SW4) for the power stage and the body switching technique [12] is used for SW1 and SW3. Smaller chip size and high efficiency of the proposed converter can be achieved simultaneously. In order to drive the NMOS power switch properly, we usually utilize a bootstrap circuit to generate the driving signal. However, it will increase the chip size due to a large bootstrap capacitor. In this work, the gate driver of SW2 reuses the flying capacitor C_{fly} as bootstrap capacitor which significantly reduces the chip area [13].

B. The proposed extended ramp control

The architecture and operation of the proposed extended ramp control are shown in Fig. 4 and Fig. 5, respectively. The controller consists of two comparators, one sawtooth ramp generator and digital control circuits. The reference signal REF_DUTY is generated to help determine the operation mode. The error amplifier output signal V_{COM} is compared with a sawtooth ramp signal. As depicted in Fig. 5(a), the sawtooth ramp signal is divided into two parts by a DC signal V_{mid} which is half of the amplitude of the sawtooth ramp generator. When V_{COM} is larger than V_{mid}, the converter enters the boost mode. On the contrary, when V_{COM} is smaller than V_{mid}, the converter will enter the buck mode. The complete switching diagram at two operation modes are shown in Fig. 5(b) and Fig. 5(c), respectively.

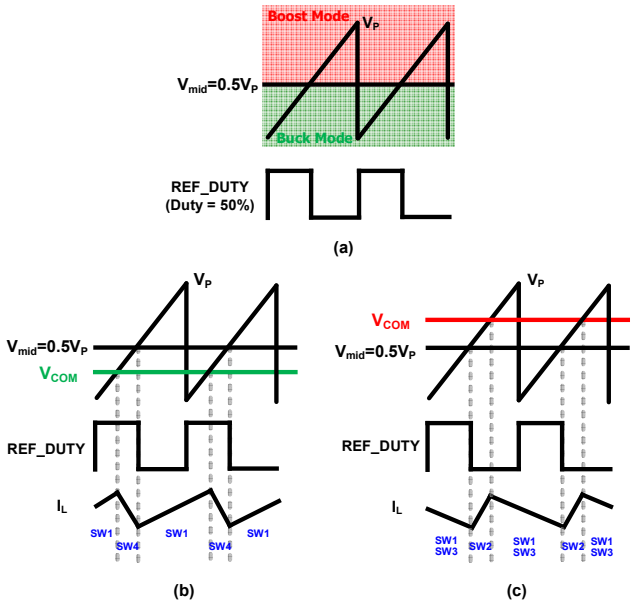

Fig. 5. Proposed extended ramp control : (a) Conceptual diagram (b) Buck mode operation (c) Boost mode opration.

For the conventional control utilized in the conventional non-inverting buck-boost converter, PWM nonlinearity [14] issue usually occurs at the interface of the buck mode and

boost mode. As demonstrated in Fig. 6, when the input and output voltages are similar and the V_{COM} is approaching zero or one, PWM discontinuity will cause pulse-skipping and then result in significant fluctuation at the output voltage. Previous works have proposed various methods to avoid this problem. [9] – [11] add a buffer region and [15] – [17] implement other controls to make the improvements for smooth mode transition. In the proposed extended ramp control, when the input voltage is close to the output voltage, V_{COM} is roughly located at the middle of the sawtooth ramp. The PWM nonlinearity issue is naturally resolved without inserting extra buffer region and the smooth mode transition can be attained at the same time. The line transient waveform of the proposed control is depicted in Fig. 7. Fig. 8 shows the SIMPLIS simulated output voltage waveforms of two buck-boost converters with their corresponding controllers during line transition. It can be observed that 1500% output deviation reduction during mode transition is achieved when the proposed extended ramp control is applied.

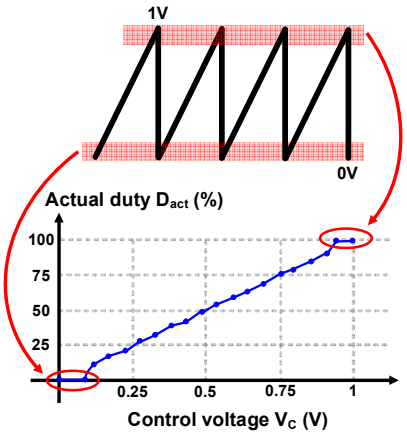

Fig. 6. Issue of PWM nonlinearity.

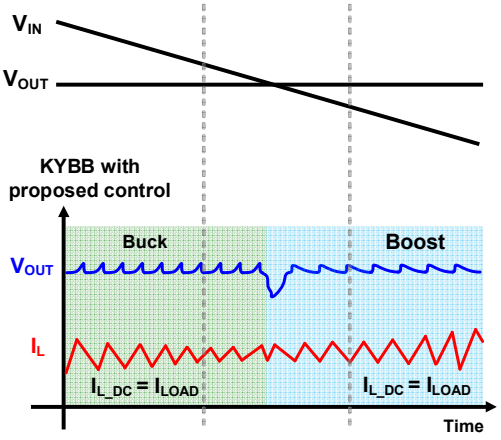

Fig. 7. Line transient waveform of the proposed KY buck-boost converter.

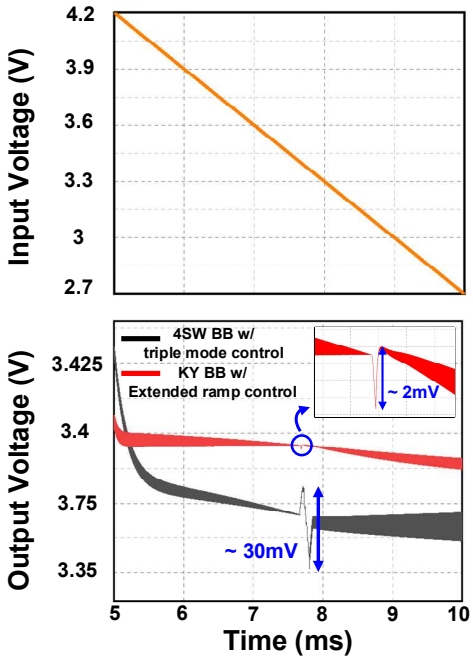

Fig. 8. Simulated line transient waveform of two buck-boost converters with their corresponding controllers.

III. Chip Simulation Result

The proposed KY buck-boost converter with extended ramp control has been implemented in TSMC 0.18um BCD process to verify the proposed design. Fig. 9 depicts the overall chip layout. The total chip area is about 1.4 mm x 1.5 mm including pads. This converter operates with an input voltage ranging from 2.7V to 4.2V and the nominal output voltage is 3.4V. The switching frequency in this work is designed as 1.5 MHz at continuous conduction mode (CCM). Besides, for the off-chip components, this work includes a 2.2 µH inductor, a 4.7 µF flying capacitor and a 4.7 µF output capacitor.

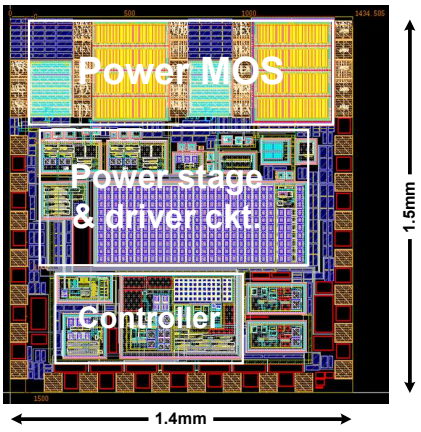

Fig. 9. Chip layout of the proposed KY buck-boost converter.

Fig. 10(a) and (b) demonstrate the simulated steady-state results of the proposed KY buck-boost converter when the input voltage is 2.7V and 4.2V, respectively. The proposed

converter can operate properly at both buck mode and boost mode. Fig. 11 depicts the line transient response when the load current is 100mA. The input voltage varies from 4.2V to 2.7V within 500us. It is shown that when the proposed extended ramp control is applied, the output voltage fluctuation during mode transition can be reduced less than 10mV. The simulated power efficiency of the proposed converter is shown in Fig. 12. The peak efficiency of this work is 95.1% at 200mA load current.

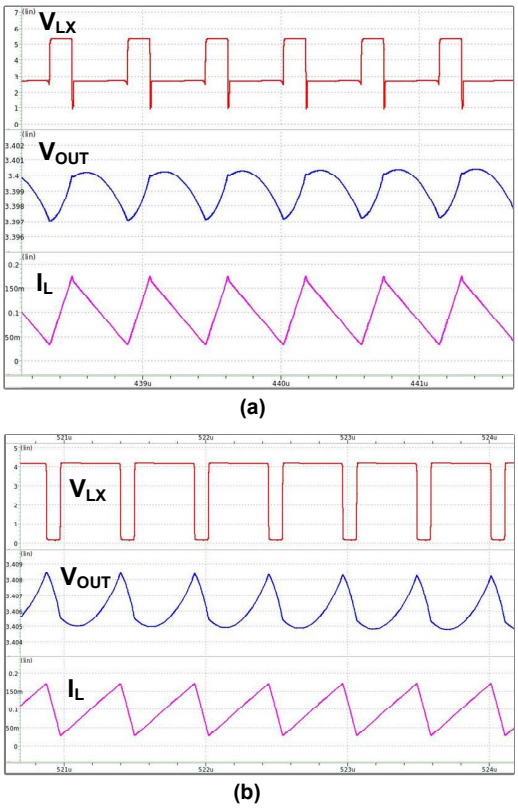

Fig. 10. Simulated steady-state waveform when V_{IN} is (a) 2.7V (b) 4.2V.

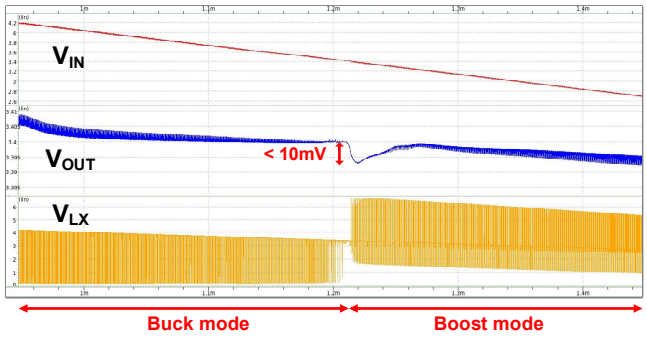

Fig. 11. Simulated line transient response when V_{IN} decreases from 4.2V to 2.7V.

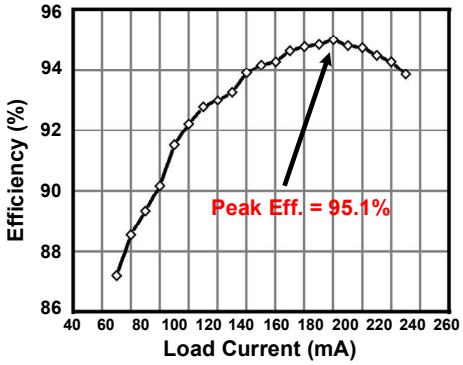

Fig. 12. Simulated power efficiency versus load current.

IV. Conclusion

The paper presents a KY buck-boost converter with extended ramp control. The proposed converter achieves a seamless mode transition without applying extra buffer region. When the proposed extended ramp control is applied, the output voltage fluctuation is less than 10mV. 1500% output variation reduction during mode transition and 95.1% peak efficiency is realized in the proposed converter. The chip fabrication and measurement are in-progress.

Acknowledgment

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