Online Dead-Time Control for Half Bridges Without Preliminary Training Based on Switching Transient Steepness

1st Lukas Knappstein
Chair of Energy Conversion
TU Dortmund University
Dortmund, Germany
lukas.knappstein@tu-dortmund.de

2nd Niklas Falkenberg
Chair of Energy Conversion
TU Dortmund University
Dortmund, Germany
niklas.falkenberg@tu-dortmund.de

3rd Martin Pfost
Chair of Energy Conversion
TU Dortmund University
Dortmund, Germany
martin.pfost@tu-dortmund.de

***Abstract*— Half bridges operating at high switching frequencies allow power electronics to achieve higher energy densities. However, they also suffer from proportionally high switching losses. Soft-switching techniques can mitigate these losses, but achieving optimal switching dead times is crucial, as shorter or longer dead times lead to increased switching losses. This study proposes an online dead-time controller that utilizes in-situ measurements. To achieve this, the controller evaluates the steepness of the switch node voltage, leveraging the fact that the maximum steepness increases during hard switching. The proposed algorithm utilizes this dependency independently of system characteristics, thereby eliminating the need for preliminary training.**

***Index Terms*—Dead-Time Control, Switching Slope Derivative, Switching Losses, Peak Detection**

I. Introduction

Modern power electronic applications utilize higher switching frequencies, thus allowing for higher energy densities. However, operating at high frequencies can lead to significant switching losses. These losses can be mitigated through soft switching, which typically necessitates longer dead times to avoid hard switching. Conversely, excessively long dead times can cause substantial reverse-conduction losses [1][2]. Therefore, the dead time should be optimized to be as close as possible to the threshold that ensures soft switching.

Recent studies have introduced dead-time controllers that utilize look-up tables, demonstrating a significant impact on switching efficiency [3]. However, these controllers are strictly limited to a specific set of operational points and require extensive training procedures. More advanced dead-time controllers use analytical transistor models, which perform online calculations of the switching dead time instead of relying on look-up tables [4][5]. Despite these advancements, such controllers lack adaptability to changes of system parameters.

This limitation poses practical challenges, as modifications in system design necessitate retraining. Furthermore, these studies rely on DC current and voltage measurements taken outside the converters. These measurements are influenced not only by the transistors but also by passive system components, which can change over time due to factors like aging and temperature. As a result, they can significantly impact the controller performance.

To address these issues, a gate driver based on the switching slope is being developed in [6]. The design process reveals that a circuit that consists of 18 transistors is required, which necessitates a very sensitive calibration. Moreover, a tightly constrained calibration could lead to critical detection errors in practical applications.

In [7], a dead-time controller is introduced that also relies on measuring the switching slope. The key difference is that it utilizes the simple relationship between hard and soft switching. This controller can operate without a preliminary training process and has been tested in real-time on a running synchronous converter. However, to evaluate the full switching slope, the approach requires an expensive FPGA and a separate ADC to implement the metric, making it less attractive for industrial applications.

This study introduces a dead-time controller that automatically adapts on the switch-node voltage steepness by using a simple analog measurement. This approach eliminates the need for static reference values by leveraging the strong correlation between steepness and dead time during hard switching. This dependency remains valid across various systems, allowing the controller to function effectively without extensive calibration or reliance on specific transistor models. The proposed method does not have special requirements and works even with a cost-effective microcontroller with an integrated ADC.

II. Methodology for Dead-Time Control

The proposed method is used in a synchronous converter utilizing a half bridge operating GaN Systems GS66516B at $V_{\text{in}} = 400\,\text{V}$. During a switching event, the output capacitances C_{OSS} of the transistors have to be recharged. In a hard switching case, this is done by the opposite transistor during its turn on, resulting in an excessive switching loss. In a DC-to-DC conversion, a half bridge is connected to an inductor. The

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inductor current i_q can be assumed constant during a switching event. For soft switching, C_{OSS} is recharged by i_q. This asks for a dead time t_D after a transistor gets turned off before the opposite transistor will be turned on. A too short t_D will result in partial hard switching, while a too long t_D results in reverse conduction mode and increased losses. This study proposes a dead-time controller which yields an optimal t_D preventing hard switching, but also large reverse conduction losses.

For this, the strong dependency of the switch-node voltage steepness dv_{sw}/dt on t_D during hard switching is being used. During the brief duration of hard switching, the current that these transistors will handle is significantly higher than i_q. This results in a consistently higher dv_{sw}/dt during hard switching compared to soft-switching operation. During soft switching where i_q fully discharges C_{OSS}, dv_{sw}/dt remains unaffected by t_D even when considering excessively long values of t_D. The dead-time controller utilizes the dependency that if t_D is increased during hard switching, dv_{sw}/dt will continuously decrease until soft switching is achieved. To determine this, the peak value of dv_{sw}/dt during a switching event is captured.

This study uses a a first-order high-pass filter to obtain dv_{sw}/dt. For a better understanding of the method, the circuit diagram of an LTSpice simulation is shown in Fig. 1. Note that the operation of the controller is exemplified for negative switching transients resulting from the transition from the high-side transistor (HS) to the low-side transistor (LS).

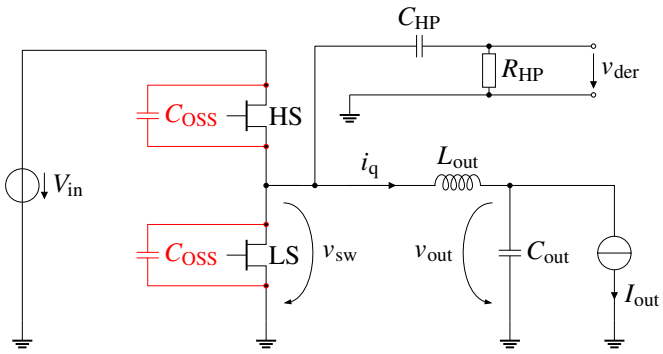

Fig. 1. Overview of the simulation setup with a half bridge in a synchronous converter.

Using this simulation, the impact of t_D on the switching performance is investigated with an outflowing inductor current of $i_q = 2\,A$ during a negative switching event, i.e. transferring i_q from the HS to the LS. The simulation results in Fig. 2 show the switch node voltage and the high-pass filter output voltage v_{der} for different values of t_D. These simulation results show how the output of the high-pass filter, v_{der}, can clearly represent the derivative dv_{sw}/dt. Furthermore, it becomes evident that the dependency of the minimum v_{der} value, $v_{der,min}$, strongly depends on t_D during partial hard switching, which is the basic requirement for the dead-time controller algorithm.

Dependencies between $v_{der,min}$ and t_D are shown in Fig. 3 for output currents from $i_q = 2\,A$ to $i_q = 10\,A$. This shows a decreasing behavior of $v_{der,min}$ with respect to t_D during partial hard switching, as the portion of v_{sw} where hard switching occurs diminishes. Once soft switching is reached, $v_{der,min}$ remains constant.

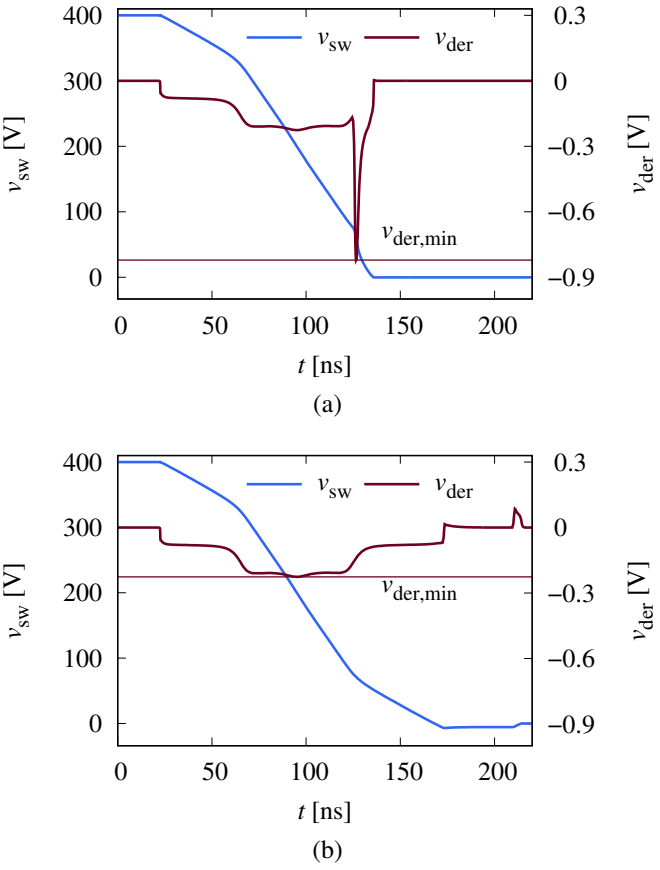

Fig. 2. Simulated switch node voltage v_{sw} and its derivative v_{der} with (a) a too short dead time and (b) a too long dead time for a positive current $i_q = 2\,A$.

The dead-time controller algorithm is shown in Fig. 4. It adjusts t_D by monitoring and utilizing changes in $v_{der,min}$. If an increase in t_D results in a lower dv_{sw}/dt and therefore a lower value of $v_{der,min}$, this indicates a hard-switching operation, which suggests a further increase of t_D. To avoid an excessive t_D, which leads to reverse conduction losses, it should be decreased to identify the precise t_D where $v_{der,min}$ stabilizes. Similarly, when t_D is decreased, a negative change in $v_{der,min}$ indicates a hard switching, while a steady or positive change in $v_{der,min}$ a soft-switching operation, cf. Fig. 3.

III. Test Bench

To demonstrate the functionality of the dead-time controller, it is run online in a test bench while its resulting dead times are recorded as $t_{D,ctrl}$. This test bench consists of a synchronous converter utilizing GaN Systems GS66516B in a half bridge configuration operating at a switching frequency of $f_s = 500\,kHz$. The converter is powered by a power source (PS) that is set to a constant input voltage of $V_{in} = 400\,V$. Additionally, a computer runs an operating-point controller

that manages an electrical load (EL) using measurements of v_{sw} and i_q. This allows for the benchmarking of the dead-time controller with various inductor currents i_q. On this computer, the dead-time controller operates by using only the measurement of the maximum switch-node voltage steepness $v_{der,rect}$, which is a rectified version of v_{der} and thus corresponds to $v_{der,min}$.

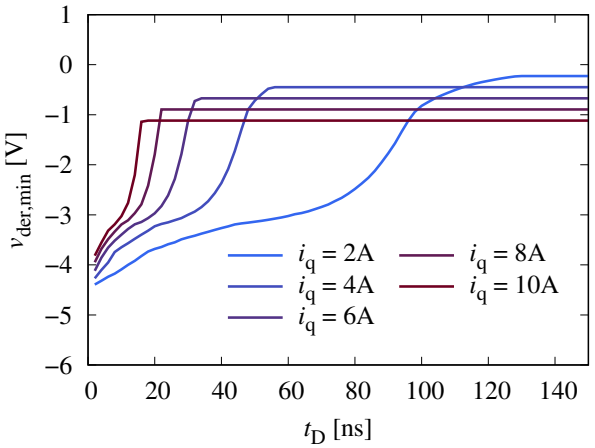

Fig. 3. Dependency of $v_{der,min}$ on t_D with i_q from 2 A to 10 A during a switching event.

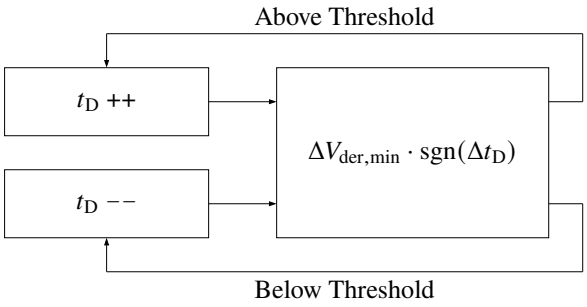

Fig. 4. Dead-time controller using the dependency of $v_{der,min}$ on t_D.

An overview of the test bench is provided by Fig. 5. Additionally, Fig. 6 presents a photograph of the synchronous converter. A more detailed description of the converter circuit is shown in Fig. 7. It also includes the measurement functionality for gathering $v_{der,rect}$, which is explained in the following section.

Centerpiece of the proposed method is the measurement of the maximum switch node voltage steepness: This involves a derivative measurement circuit utilizing first-order high-pass filter, which outputs v_{der}. This high-pass filter consists of a capacitor C_{HP} = 1 pF, which is loaded by a resistor R_{HP} = 50 Ω. The capacitor C_{HP} is implemented directly on the PCB using two copper planes with an area of 4 mm^2, positioned in the first two PCB layers with a separation of 140 µm. To compensate for the high impedance of the high-pass filter, it is followed by an operational amplifier, which is configured as a non-inverting amplifier circuit with a gain of G = 3 to achieve maximum output swing during hard switching events.

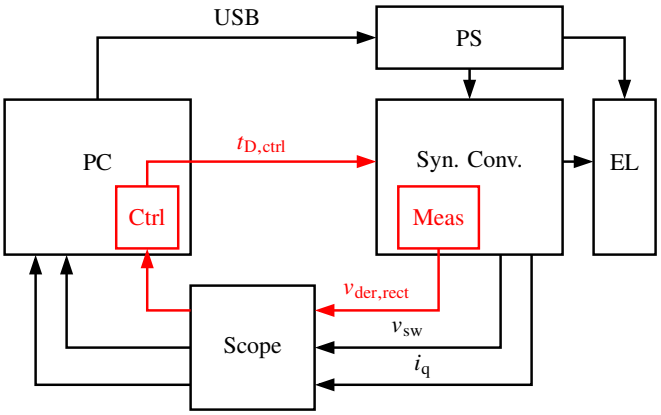

Fig. 5. Overview of the test bench, in which the dead-time controller was tested. All signals used by the dead-time controller are marked red, other signals are used for setting the operational points.

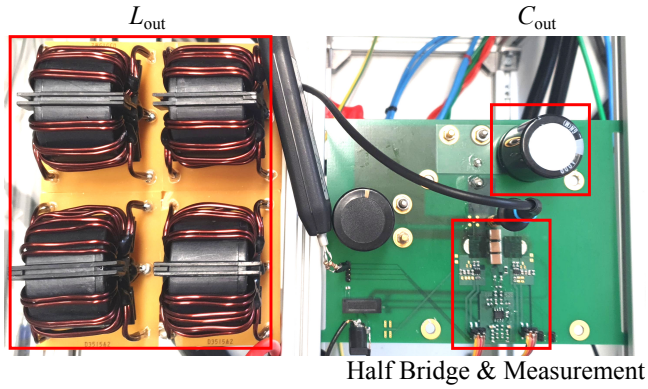

Fig. 6. Photograph of the synchronous converter.

In this example where negative switching transients are considered, hard switching is defined by the negative peak values of v_{der}, seen in $v_{der,min}$. To facilitate continuous measurement of $v_{der,min}$, a peak detection of v_{der} is implemented by a rectifier. That rectifier is composed of a diode D_{rect} and a capacitor C_{rect} = 1 µF, cf. Fig. 7, and outputs $v_{der,rect}$. Given that changes of $v_{der,rect}$ are expected within a few switching cycles while the controller adjusts t_D, the capacitor C_{rect} must be continuously discharged. Here, a discharge resistor R_{rect} = 100 kΩ is connected to the positive supply voltage of the operational amplifier, V_{CC} = 12 V. A photograph of the half-bridge along with the associated measurement setup is shown in Fig. 8.

This configuration ensures proper rectification of all negative peak values of v_{der} below 0 V, accounting for the forward voltage drop across the diode. Due to this voltage drop, $v_{der,rect}$ will not accurately represent the peak value of v_{der}. However, this voltage shift does not impact the functionality of the dead-time controller, as it primarily responds to relative changes of $v_{der,rect}$.

To evaluate the performance of the proposed dead-time controller on the test bench, it is essential that i_q can be set

to a specific level precisely at the moment of a switching event. This cannot be guaranteed by directly setting I_{out} on the EL, as i_q is also influenced by the output filter ripple current. Therefore, i_q is measured using a current probe directly before a switching event, denoted as $i_{q,sw}$ in Fig. 9. This allows the operating-point controller to regulate $i_{q,sw}$ to a desired value by successively adjusting the electrical load. Any measurements of i_q and v_{sw} are only used for testing the dead-time controller and are not required for the operation of the dead-time controller itself.

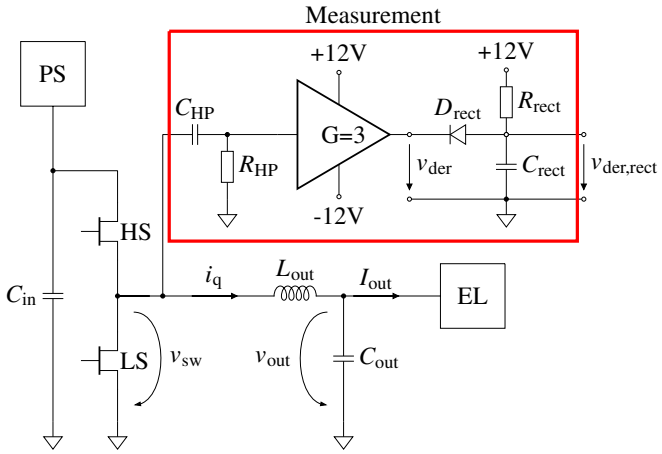

Fig. 7. Circuit of the test bench consisting of a synchronous converter and the derivative measurement circuit. $v_{der,rect}$ is the negative rectification v_{der} and therefore represents $v_{der,min}$ for the dead-time controller.

IV. Online Dead-Time Control on the Test Bench

Before the dead-time controller can be operated, it is essential to verify that the derivative measurement v_{der} yields the expected results. This specifically means that v_{der} shows a distinct negative swing during a hard switching event and that $v_{der,rect}$ shows a significant reaction to that swing. Tests were conducted for an outflowing current of $i_{q,sw} = 2\,A$, using both a too-short and a too-long dead time. The results are presented in Fig. 10.

These measurements demonstrate the expected dependence of $v_{der,rect}$ on the hard switching of v_{sw}. However, they also reveal that $v_{der,rect}$ does not completely reach the minimum of v_{der} due to the forward voltage drop of the rectification diode D_{rect}. Therefore, it is necessary to further investigate whether the dependency of $v_{der,rect}$ on t_D is sufficient for the algorithm to operate effectively. For this, the dependency of $v_{der,rect}$ requires a constant increase during the hard-switching range until the optimal level of t_D is reached, where they remain independent of t_D. Consequently, $v_{der,rect}$ was measured with $i_{q,sw}$ ranging from 2 A to 10 A, each with t_D varying from 0 ns to 150 ns, cf. Fig. 11. The measurements confirm that this requirement is fulfilled.

After those measurements have shown the sufficient behavior of $v_{der,rect}$, the dead-time controller was operated online. To evaluate its performance, it was enabled on the running converter for 200 switching cycles. For improved visibility of

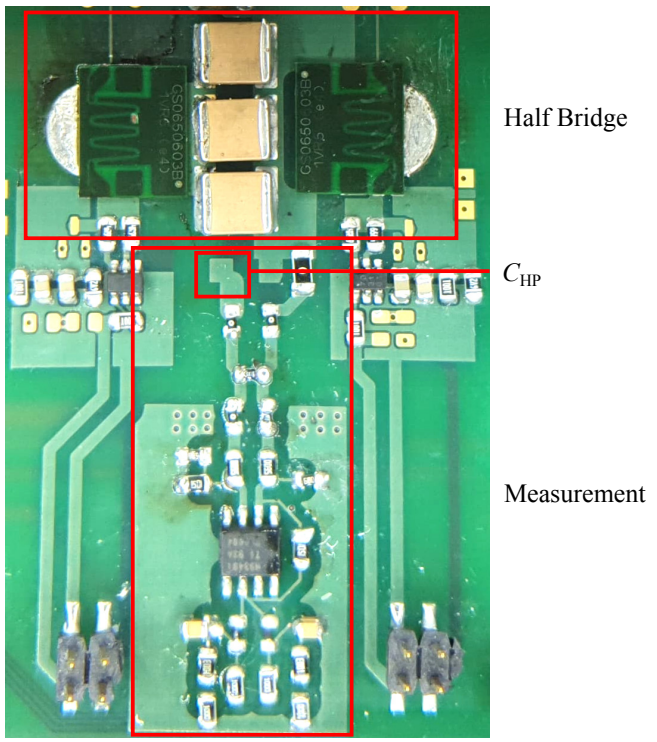

Fig. 8. Detailed photograph of the half bridge and the measurement. Note that C_{HP} is implemented in PCB instead of using a discrete component.

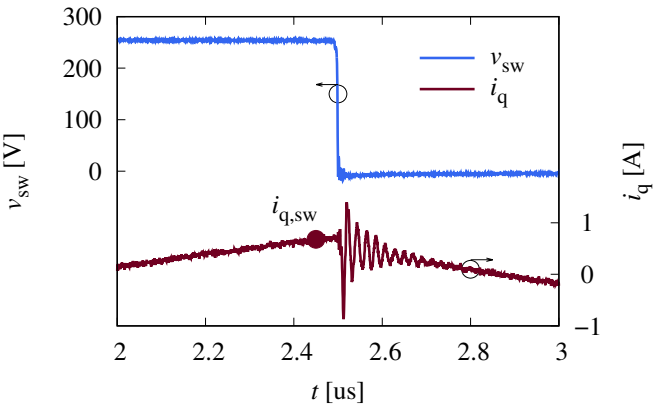

Fig. 9. During operation the measurement of i_q shows a large current ripple. Therefore i_q will be captured directly before the switching event as basis for dead-time control.

the dead-time controller behavior, a distribution of the last 100 cycles, after the dead-time controller had settled, is presented in Fig. 12. The values for $t_{D,ctrl}$ over the 200 switching cycles are shown in Fig. 13.

To evaluate the performance of the dead-time controller, it is necessary to measure the switching losses of the low-side transistor (LS) separately. An investigation of the efficiency of the test bench would encompass the entire synchronous converter, including the output filters and the high-side (HS) transistor. Since only the switching losses of LS are relevant

for assessing the dead-time controller, temperature differences between LS and the heat sink, denoted as ΔT_{LS}, are measured as a metric for its losses, see Fig. 14. The minimum of each temperature curve is referenced as $t_{\mathrm{D,opt}}$.

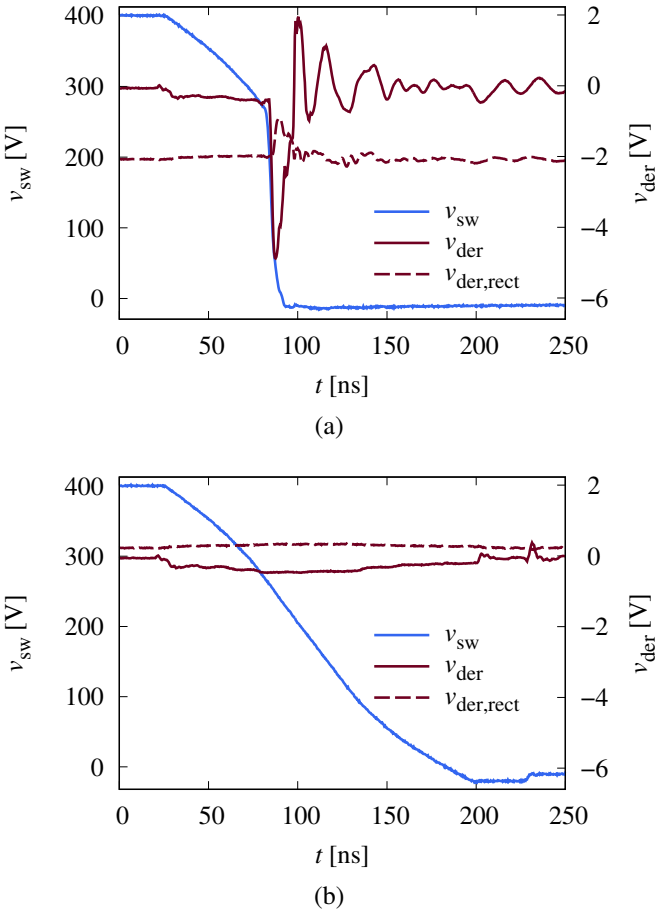

Fig. 10. Measurement results showing v_{sw}, v_{der}, and the rectified $v_{\mathrm{der,rect}}$ for an outflowing current of $i_{\mathrm{q,sw}} = 2\,\mathrm{A}$ during a switching event. (a) regards a switching dead time of $t_{\mathrm{D}} = 50\,\mathrm{ns}$ (too short), (b) of $t_{\mathrm{D}} = 200\,\mathrm{ns}$ (too long).

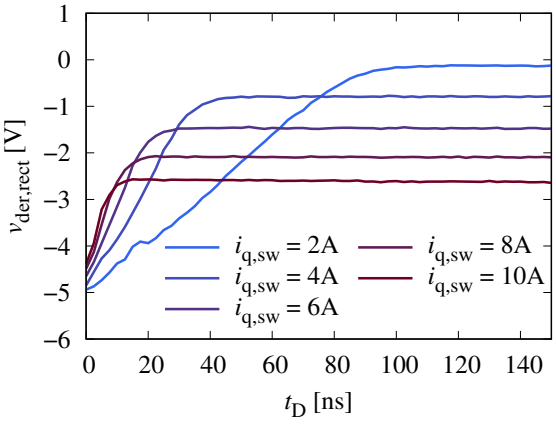

Fig. 11. Measured $v_{\mathrm{der,rect}}$ while running the converter in static conditions with $i_{\mathrm{q,sw}}$ from 2 A to 10 A and t_{D} from 0 ns to 250 ns.

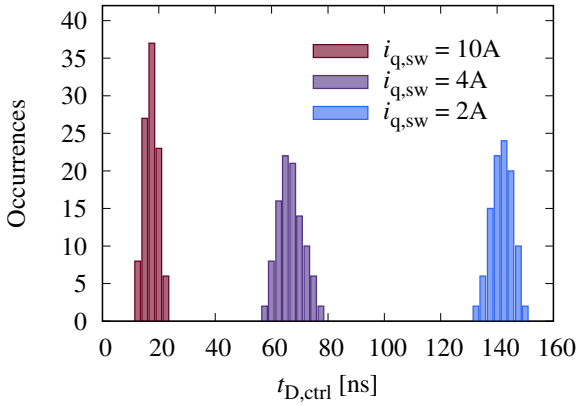

Fig. 12. Distribution of $t_{\mathrm{D,ctrl}}$ during a 200 switch cycle testrun regarding the last 100 switching cycles, where $t_{\mathrm{D,ctrl}}$ has settled.

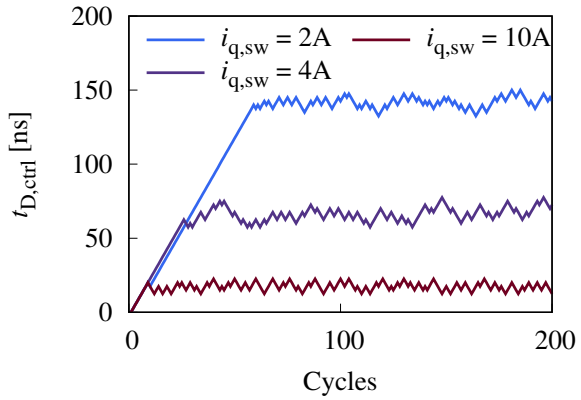

Fig. 13. Values of $t_{\mathrm{D,ctrl}}$ during an online run of the dead-time controller for 200 switching cycles.

A comparison of the resulting controller dead times $t_{\mathrm{D,ctrl}}$ to the empirically determined $t_{\mathrm{D,opt}}$ is presented in Fig. 15 for currents ranging from $i_{\mathrm{q,sw}} = 2\,\mathrm{A}$ to $i_{\mathrm{q,sw}} = 10\,\mathrm{A}$ in increments of 2 A. To enhance the visibility of the controller results, only the values between the first and third quartiles of the distributions for $t_{\mathrm{D,ctrl}}$ are displayed.

These values show that the dead-time controller, on average, matches the $t_{\mathrm{D,opt}}$ values, but maintains a small variation in t_{D}, fluctuating around them. It is important to investigate how significant these fluctuations are. The losses of LS, represented by ΔT_{LS}, are therefore tested for three examples of static t_{D} values and compared to the operation of the dead-time controller in Fig. 16. It can be observed that a short static t_{D} causes ΔT_{LS} to rise to a high level due to hard switching behavior. Conversely, a high t_{D} results in significant reverse conduction losses, particularly at larger currents. Additionally, a comparison of the losses between $t_{\mathrm{D,opt}}$ and $t_{\mathrm{D,ctrl}}$ is illustrated in Fig. 17. An operation with the dead time controller results in a ΔT_{LS}, which is only 2 °C higher than with $t_{\mathrm{D,opt}}$. These tests demonstrate that the effects of the small varying deviation of $t_{\mathrm{D,ctrl}}$ against $t_{\mathrm{D,opt}}$ on the losses remain within a reasonable range.

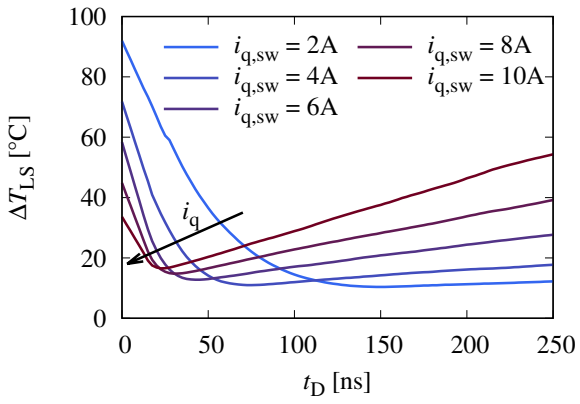

Fig. 14. Losses of LS, represented by ΔT_{LS} for $i_{q,sw}$ from 2 A to 10 A and t_D from 0 ns to 250 ns.

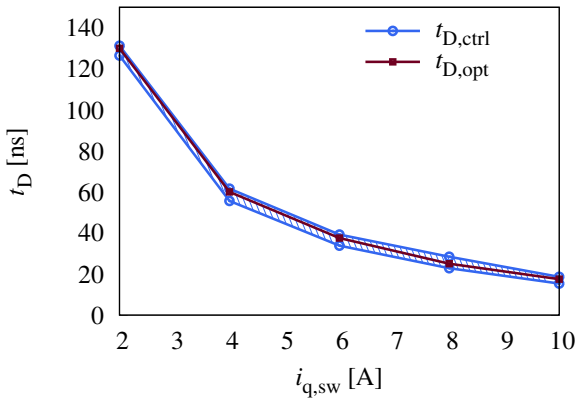

Fig. 15. Resulting $t_{D,ctrl}$ of the dead-time controller compared to $t_{D,opt}$. The dead-time controller, on average, matches the ideal dead times, but remains within a varying deviation.

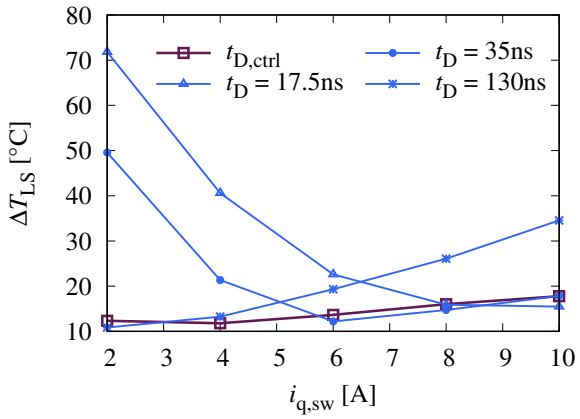

Fig. 16. Losses represented by ΔT_{LS} when operating with three static values for t_D and $t_{D,ctrl}$. The dead-time controller shows reasonably low losses compared to the static dead times.

V. Conclusion

This study proposes an active dead-time controller designed to significantly reduce switching losses by dynamically adjusting the dead times to an optimal level during the operation of power electronic applications. The controller leverages the relationship between switching transient steepness and hard switching behavior.

It can be implemented on a cost-effective microcontroller with an integrated ADC, eliminating the need for high sample rates. The advantages of this approach include simplicity, cost efficiency, and adaptability. Unlike other methods that rely on pre-trained system models, this approach leverages the intrinsic relationship between switch-node voltage steepness and hard switching behavior, which is common for many systems.

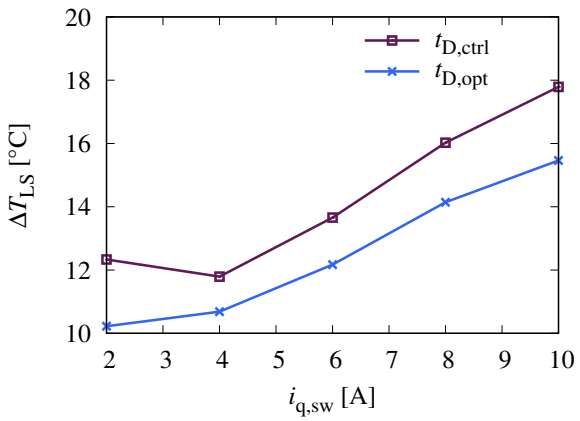

Fig. 17. Losses represented by ΔT_{LS} when operating with the dead-time controller agains operating with $t_{D,opt}$.

VI. Acknowledgment

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