Decentralized Interleaving of Series-Stacked DC-DC Converters via Extremum-Seeking Control

Ivan Petrić[a], Vignesh Iyer[b], Shoudong Hu[b], Chirayu Rajpurohit[b], Bailey Sauter[b], Milan Ilić[a], Luca Corradini[b], and Dragan Maksimović[b]

[a]Future Energy Technology Center, Hanwha Qcells Technologies, Santa Clara, CA 95054, USA
[b]Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, CO 80309, USA

***Abstract*—This paper introduces a fully decentralized solution for achieving optimal interleaving of series-stacked power converters based on distributed, module-level extremum-seeking controllers. This approach ensures switching-cycle-level synchronization, effectively minimizing switching ripple and significantly reducing the size of passive filters. The proposed control system is model-free, straightforward to design and implement, and offers continuous synchronization to mitigate clock drifts while also supporting asymmetric module operation. To guide system design, dynamic modeling is presented for a series-stacked architecture with two modules. The proposed approach is validated through simulations involving up to seven modules and by experiments with up to three modules.**

***Index Terms*—Decentralized interleaving, Ripple minimization, Series-stacked dc-dc converters**

I. Introduction

SERIES-stacked (cascaded) converter modules allow multi-port power conversion with reduced voltage-rated semiconductors in applications such as photovoltaic (PV) dc optimizers [1], [2], as illustrated in Fig. 1. With a proper switching-cycle-level synchronization (interleaving), the cascaded architecture offers additional system-level improvements, in terms of significantly faster dynamic performance and reduction of passive filters, due to harmonic cancellation effects [3].

While interleaving is widely implemented across the field, it is most often set fixed using the symmetric phase-shifted pulsewidth modulation (PS-PWM), which is optimal for the balanced module operation [3]. For applications where mismatches between the modules are significant, asymmetric interleaving should be imposed instead [4]. However, calculating the optimal asymmetric interleaving angles represents a difficult optimization problem that brings a high computational complexity, unsuitable for real-time implementation [5]. Additionally, in many applications, fully decentralized control of the modules within a multi-cell architecture is preferred [6], [7], as it avoids non-standard wiring, reduces cost, and increases reliability. There, module interleaving becomes very challenging due to the lack of a synchronizing signal and the appearance of clock drifts due to crystal oscillator tolerances. All this has resulted in an expanded research interest in adaptive and decentralized interleaving, without any fast inter-module communication [5], [8]–[12].

In [8], the output ripple of paralleled converters is minimized using digital nonlinear oscillators, which requires a very fast FPGA implementation and is limited to symmetric paralleled units. In [9], it is assumed that all units operate with equal duty cycles, and the method depends on a single sample taken at the switching instants, which inherently increases sensitivity to noise. The works [5], [11] offer two decentralized methods based on gradient descent. However, both approaches necessitate an iterative, sequential optimization of individual modules, rather than enabling continuous and simultaneous corrective actions across all modules. This limitation may be problematic in the presence of clock drifts. Furthermore, both methods are computationally intensive and rely on model-based approaches, making them susceptible to unmodeled dynamics and parameter tolerances. The methods from [10], [12] feature several approximative assumptions and are also based on the gradient descent, where the gradient estimation relies on precisely setting the single-sampling instant within a switching cycle, depending on the system parameters, including the sensor bandwidth. All the above-mentioned methods are strictly model-based and have several disadvantages in terms of implementation robustness and complexity.

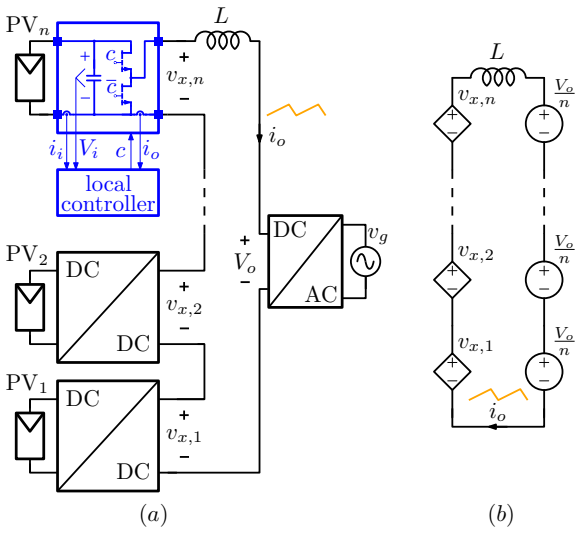


Fig. 1: (a) A series-stacked dc converter architecture employed in a PV system based on dc optimizers, and (b) an equivalent circuit for calculating the current ripple.

To overcome these limitations, this paper proposes a model-

free, adaptive algorithm for decentralized interleaving, based on extremum seeking control (ESC) [13]. The algorithm has a simple design procedure and is capable of minimizing the current ripple robustly, regardless of asymmetries between the modules, while rejecting the impact of clock drifts. It is computationally efficient, suitable for implementation in standard digital signal processors (DSPs), and compatible with oversampling techniques that are often implemented in state-of-the-art feedback control loops [14]. As the first investigation of the ESC capabilities for decentralized interleaving of power converter modules, this paper focuses its analyses and demonstrations on minimizing the output current ripple of series-stacked dc architectures, such as the system shown in Fig. 1. For system design guidelines and convergence analysis, dynamic modeling is presented and validated in simulations for two series-stacked modules. Results showing decentralized interleaving are provided for up to seven modules in simulations and up to three modules experimentally.

The paper is organized as follows. A series-stacked dc architecture is introduced and the principles of harmonic cancellation by interleaving are briefly summarized in Section II. In Section III, the proposed ESC approach is analyzed and a small-signal dynamic model is derived for a system with two modules. Verifications of the algorithm operation and the proposed model are presented in Section IV. Finally, conclusions are presented in Section V.

II. Series-stacked dc-dc architecture

Fig. 1(a) shows a series-stacked dc-dc converter architecture that can be found in, for example, residential PV systems based on dc optimizers [1], [2]. It consists of n low-voltage (LV) dc-dc converter modules that are connected in series to interface to the high-voltage (HV) dc link via a single inductive filter L. The grid connection is then established using a string inverter, which regulates the dc bus voltage V_o. Aside from enabling improved energy capture via module-level maximum power point tracking, the main motivation for the series-stacked architecture comes from being able to interface to the HV dc link without isolation and relying only on LV components. This enables ultra-high efficiency and power density while using cost-effective, high figure-of-merit low-voltage Si or GaN semiconductors. An important target feature is the fully decentralized control of LV modules, which obviates the need for fast inter-module communication. This brings plug-and-play operability and, hence, increases reliability, simplifies installation and wiring, and reduces the overall cost.

In this paper, each LV module's output stage utilizes a simple half-bridge buck-type switching cell; however, the method can be readily applied to other topologies. The plug-and-play LV modules feature only local controllers [2] that generate the switching signals $c(t)$, using PWM with the nominal frequency f_{sw}. The instantaneous switched node voltages are equal to $v_x(t) = c(t)V_i$ and their average values are equal to $V_x = DV_i$, where V_i is the module's input voltage and D is the duty cycle of c. The output voltage of the series-stacked architecture is equal to $V_o = \sum_{k=1}^{n} D_k V_{i,k}$, which, for

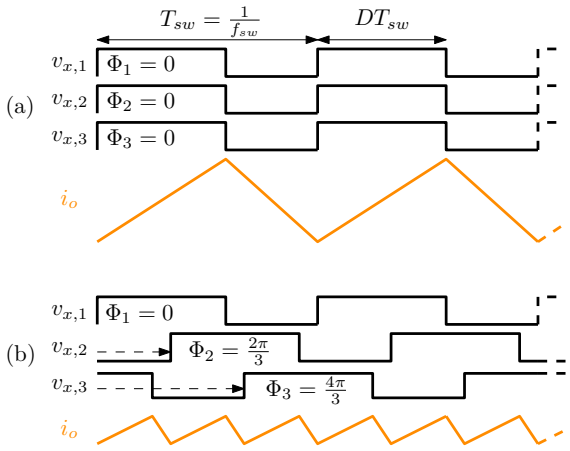


Fig. 2: Illustration of the worst case in-phase operation and the optimal symmetric PS-PWM for $n = 3$ balanced LV modules.

balanced LV modules ($\forall k \in \{1, ..., n\}\ D_k = D$ and $V_{i,k} = V_i$) results in $V_o = nDV_i$.

The output current spectrum, which depends on the sum of all LV modules' switched node voltages, can be calculated by applying the superposition principle to each pair of $v_{x,k}$ and V_o/n, as shown in Fig. 1(b). For the considered half-bridge topology, k^{th} module's contribution to the current ripple, represented by phasors at multiples of the switching frequency, can be found as

$$\underline{I}_{o,k}(jl\omega_{sw}) = \frac{V_{i,k}}{\pi\omega_{sw}L}\frac{1}{l^2}\left[e^{-j2\pi lD_k} - 1\right]e^{-jl\Phi_k}, \quad (1)$$

where $\omega_{sw} = 2\pi f_{sw}$, l is the switching harmonic order, j is the imaginary coefficient, and Φ_k is the phase angle (in radians) of the switched-node voltage $v_{x,k}$. The total current ripple phasors are found as a sum of (1) for all $k \in \{1, ..., n\}$, and are a function of modules' input voltages, duty cycles, and switched nodes' phase angles. A simplification is obtained for balanced LV modules, for which the output current harmonics are equal to

$$\underline{I}_o(jl\omega_{sw}) = \frac{V_i}{\pi\omega_{sw}L}\frac{1}{l^2}\left[e^{-j2\pi lD} - 1\right]\left[1 + \sum_{k=2}^{n} e^{-jl\Delta\Phi_k}\right]. \quad (2)$$

Note that the first LV module is taken as a reference for other modules' phase shifts, *i.e.*, $\Phi_1 = 0$ and $\Delta\Phi_k = \Phi_k$. As illustrated in Fig. 2, for a balanced series-stacked architecture, current harmonics are maximized with the in-phase operation (zero phase shifts) and minimized with the symmetric PS-PWM, for which the switched node voltages are phase-shifted $2\pi/n$ apart. Besides reducing the magnitude of the voltage pulse applied to the filter inductor, with balanced modules the symmetric PS-PWM results in the first $n-1$ current ripple harmonics being equal to 0, thus pushing its spectral content to higher frequencies. This enables a drastic reduction of the output inductance and RMS ratings of the HV dc capacitors without having to increase the switching frequency of the individual modules, hence, reducing losses and electromagnetic interference.

In balanced series-stacked systems with centralized (or distributed) control, imposing symmetric PS-PWM to minimize (2) is straightforward and widely implemented. Complexity is significantly increased for unbalanced systems, where the minimal current ripple may no longer correspond to the symmetric PS-PWM. There, finding the optimal phase shift distribution represents a non-convex optimization problem. Calculating a solution in real time is impractical, especially for a large number of modules [4], [5]. Finally, achieving optimal interleaving for decentralized LV modules is highly challenging due to the absence of a synchronization signal and the fact that each local controller generates its own PWM clock. This leads to clock drifts between units, stemming from the tolerances of the crystal oscillators. As a result, a continuously-applied synchronizing action is necessary, rather than relying on synchronization at specific moments, such as during start-up. To address these challenges, this work proposes a new method for optimal decentralized interleaving, based on distributed adaptive extremum-seeking controllers.

III. Ripple minimization via extremum seeking control

The goal of the method proposed in this paper is to bring the series-stacked system from Fig. 1 to its optimal point in terms of minimizing the output current ripple, using decentralized interleaving. To achieve this, a decentralized multi-variable ESC algorithm illustrated in Fig. 3 is introduced in Section III-A, followed by a dynamic model development in Section III-B.

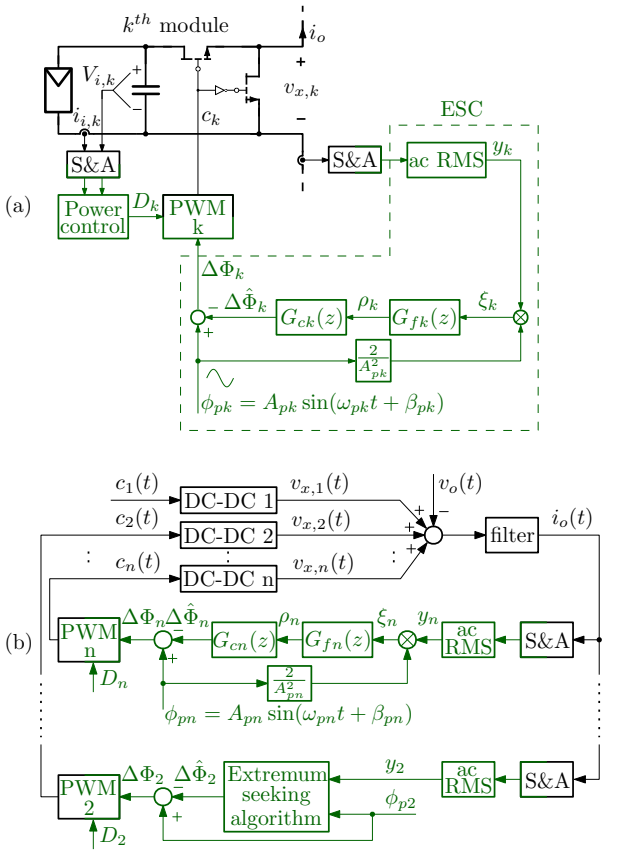


Fig. 3: (a) The proposed module-level ESC system for decentralized interleaving. (b) Block diagram of the series-stacked system forming the multi-variable ESC.

A. System overview

A block diagram of the ESC system for the k^{th} module is shown in Fig. 3(a). The ESC determines a trajectory of the optimization variables by perturbing them to measure the local gradient of the chosen cost function. In the considered multiple-input single-output system, the optimization variables are the LV modules' phase shift angles $\Delta\Phi_k$ and the cost function y_k quantifies the output current ripple. Due to the series connection, the output current i_o is shared, meaning that all LV modules have access to the same cost function. The output current acts as a system link, creating a multi-variable ESC system from the distributed controllers, as shown in the equivalent system block diagram in Fig. 3(b). For n modules there are $n-1$ phase shifts. Hence, one module can be employed without running the ESC algorithm (e.g. the module 1 sets a fixed $\Phi_1 = 0$ and serves as a reference for other phase shifts).

First, it is necessary to perform the sensing and acquisition (S&A) of the output current. In the digital implementation considered in this paper, the current is oversampled $N_s = 32$ times over the switching period and the cost function is calculated using the standard deviation (AC *root mean square* (RMS)) of the obtained samples. Other measures can be used as well, for example, the variance, the peak-to-peak ripple value, and similar. Once every switching period, after N_s samples are stored in the memory (e.g. using a *direct memory access* (DMA) module), the standard control interrupt is used for the ESC algorithm. Referring to the k^{th} module, a sinusoidal phase-shift perturbation signal ϕ_{pk}, with the frequency $f_{pk} = \omega_{pk}/2\pi$ and the magnitude A_{pk}, is calculated. A sinusoidal signal is chosen, although other waveforms can be used as well [13]. To allow independent perturbations, all $n-1$ modules have different perturbation frequencies, which can be set during the system start-up.

The cost function y_k is demodulated to allow the k^{th} module to independently react to its perturbation. A scaling factor $2/A_{pk}^2$ used for the demodulation allows the convergence dynamics to be invariant to the perturbation magnitude, as explained in the following subsection. The demodulated signal ξ_k contains a dc component, indicative of the local partial derivative of the cost function, and higher-order components at frequencies that are, at least, linear combinations of all the perturbation frequencies. Those components do not contribute to the convergence and are, therefore, attenuated using a digital filter $G_{fk}(z)$, where z is the variable of the Z-transform. The obtained signal ρ_k is processed by a compensator $G_{ck}(z)$ (in this work selected as an integrator with the gain k_i), which ensures the system's convergence. The compensator output $\Delta\hat{\Phi}_k$ determines the slowly-varying phase shift value, which is subtracted from the perturbation to calculate the total phase shift of the k^{th} PWM module. Due to the decentralized nature of the system, it is not possible to directly apply phase shifts

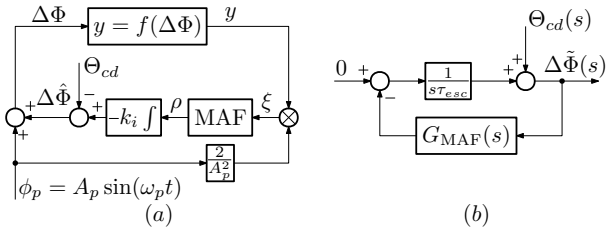


Fig. 4: Block diagrams of (a) the single-input, single-output ESC loop for a system with two modules where the clock drift is analyzed using a phase disturbance signal Θ_{cd} and (b) a small-signal system model for operation around the optimal phase shift $\Delta\Phi^* = \pi$, which can be used to analyze clock-drift disturbance rejection.

between the modules. Rather, the module PWM frequency is adjusted to achieve the target phase increment between the two consecutive ESC executions. Besides the phase shift command, the PWM receives a duty cycle command D_k from the power flow controller and outputs the switching signal $c_k(t)$.

An important design step concerns selecting the perturbation frequencies and magnitudes. Considerations on the necessary time-scale separation between the ESC dynamics, perturbation frequencies, and the optimization plant dynamics can be found in [13]. In particular, a simplification is obtained for applications where the cost function can be considered to be a static map. In the considered application, this imposes the need to limit the ESC dynamics to frequencies well below the switching harmonics. Therefore, perturbation frequencies are set well below the switching frequency, and the compensator gain is set significantly lower than the perturbation angular frequency, i.e., $k_{ik} \ll \omega_{pk} \ll \omega_{sw}$. As for distributing the perturbation frequencies among the LV modules, the demodulation process causes frequency components at their linear combinations to appear in the system. In [13], to ensure convergence without additional filters, it is recommended that the multi-variable ESC is implemented such that $\omega_{pp} + \omega_{pq} \neq \omega_{pr}$, for any triplet of the used perturbation frequencies. This approach is adopted here. Moreover, having very low differences between the perturbation frequencies will result in low-frequency components that must be rejected by the loop filters, thus limiting the achievable dynamics. Hence, the desired system dynamics must be considered when choosing the minimal difference between any two perturbation frequencies.

B. Convergence analysis and small-signal modeling for $n = 2$

Besides ensuring the system's convergence, dynamics of the ESC loop employed for decentralized interleaving must be fast enough to compensate the clock drifts between the LV modules. Following the approach from [13], a simple small-signal model is derived here to gain an insight into the system dynamics and, consequently, parameter design guidelines. As a starting point, this paper analyzes the simplest case of two LV modules, which results in a single-input single-output (SISO) ESC.

Consider the system from Fig. 4(a), which shows the ESC loop and introduces a signal Θ_{cd}, which models the phase disturbance caused by the clock drift between the modules. For $n = 2$, the cost function y has one optimization parameter, which is the phase shift $\Delta\Phi = \Delta\Phi_2$ between the two modules. The optimal value of the phase shift is denoted as $\Delta\Phi^*$. The cost function is nonlinear, which is why the convergence analysis is performed using a Taylor expansion around the optimal point determined by $\Delta\Phi^*$ and y^*,

$$y = f(\Delta\Phi) = y^* + \frac{y''}{2}\left(\Delta\Phi - \Delta\Phi^*\right)^2. \tag{3}$$

The ESC error $\Delta\tilde{\Phi}$ is defined as

$$\Delta\tilde{\Phi} = \Delta\Phi^* - \Delta\hat{\Phi}. \tag{4}$$

Based on the block diagram in Fig. 4(a), the cost function can be expanded as

$$\begin{aligned} y &= y^* + \frac{y''}{2}\left(\Delta\hat{\Phi} + \phi_p - \Delta\Phi^*\right)^2 = y^* + \frac{y''}{2}\left(\phi_p - \Delta\tilde{\Phi}\right)^2 \\ &= y^* + \frac{y''}{2}\left(A_p\sin(\omega_p t) - \Delta\tilde{\Phi}\right)^2. \end{aligned} \tag{5}$$

The cost function is then demodulated, which results in the signal ξ,

$$\begin{aligned} \xi = &-\Delta\tilde{\Phi}y'' + \Delta\tilde{\Phi}y''\cos(2\omega_p t) \\ &+ \left(\frac{2}{A_p}y^* + \frac{1}{A_p}y''\Delta\tilde{\Phi}^2\right)\sin(\omega_p t) + A_p y''\sin^3(\omega_p t). \end{aligned} \tag{6}$$

The demodulation factor $2/A_p^2$ is chosen to make the dc component of ξ independent from the perturbation magnitude. Observing the spectral content of ξ in (6), the filter $G_f(z)$ is selected as a moving average filter (MAF) across the perturbation period window. Such filtering completely removes all non-dc frequency components from (6). Note that, for $n > 2$, such filtering does not ensure cancellation of all non-dc components, due to perturbations coming from the other LV modules. However, as subsequently demonstrated, the low-pass response of the ESC loop helps suppress the remaining impact.

The output of the MAF is the signal ρ, which measures the local gradient of the cost function

$$\rho = \mathrm{MAF}\{-\Delta\tilde{\Phi}y''\} = -y''\mathrm{MAF}\{\Delta\tilde{\Phi}\}, \tag{7}$$

where $\mathrm{MAF}\{\}$ represents the filtering action, which does not impact the static term y''. Although the system is implemented digitally, the remaining analysis is performed in the s-domain, which is adequate considering that dynamics of interest are well below the algorithm execution rate. The output of the extremum-seeking algorithm is obtained by integrating the signal ρ and adding the disturbance signal Θ_{cd},

$$\begin{aligned} \Delta\hat{\Phi}(s) &= -\frac{k_i}{s}\rho(s) - \Theta_{cd}(s) \\ s\Delta\hat{\Phi}(s) &= k_i y'' G_{\mathrm{MAF}}(s)\Delta\tilde{\Phi}(s) - s\Theta_{cd}(s), \end{aligned} \tag{8}$$

where $G_{\mathrm{MAF}}(s)$ is the s-domain transfer function of the averaging filter. From (4), it follows that

$$s\Delta\hat{\Phi} = -s\Delta\tilde{\Phi} \tag{9}$$

which yields

$$
\begin{aligned}
-s\Delta\tilde{\Phi}(s) &= k_i y'' G_{\mathrm{MAF}}(s)\Delta\tilde{\Phi}(s) - s\Theta_{cd}(s) \\
&= \frac{1}{\tau_{esc}} G_{\mathrm{MAF}}(s)\Delta\tilde{\Phi}(s) - s\Theta_{cd}(s),
\end{aligned} \tag{10}
$$

where $\tau_{esc} = 1/k_i y''$ is the time constant of the ESC system, which describes the first-order dynamics around the optimal point. The resulting small-signal closed-loop system is shown in Fig. 4(b), and the disturbance-rejection transfer function is found as

$$
\frac{\Delta\tilde{\Phi}(s)}{\Theta_{cd}(s)} = \frac{s}{s + G_{\mathrm{MAF}}(s)\frac{1}{\tau_{esc}}}. \tag{11}
$$

The ESC small-signal stability is limited by the perturbation frequency due to the phase lag introduced by the MAF.

As expected, the transfer function (11) has a high-pass property and fully rejects constant disturbances (e.g. a step change of the phase shift), whereas the suppression of ac disturbances (such as the one imposed by clock drifts) depends on the loop bandwidth, $\omega_{esc} = 1/\tau_{esc}$. For analyzing the clock drift rejection, the phase disturbance can be represented as $\Theta_{cd}(s) = \omega_{cd}/s^2$, where the ramp slope is determined by the clock drift angular frequency ω_{cd}. Since the ESC loop has a first-order structure, it results in a non-zero steady-state response to the ramp waveform $\Theta_{cd}(s)$,

$$
\Delta\tilde{\Phi}(t \to \infty) = \omega_{cd}\tau_{esc}. \tag{12}
$$

A design criterion can be to limit this steady-state error to, for example, 1%. As an example, for a clock drift equal to $5\,\mu\mathrm{s/s}$ and $f_{sw} = 20\,\mathrm{kHz}$, $\omega_{cd} = 2\pi/10\,\mathrm{rad/s}$ and $\tau_{esc} < 0.1\,\mathrm{s}$.

From (11), it is clear that the system dynamics are determined by the integrator gain, k_i, and the second derivative at the optimal point, y'', which depends on all system parameters. This means that the information on y'' is necessary for determining dynamics. For a preliminary gain selection, or to narrow-down the search-space, it is possible to find off-line the worst-case (lowest) value of y'', such that a satisfactory clock drift rejection is achieved.

As an example, the cost function y is numerically calculated, based on (2), and is shown in Fig. 5, for the balanced case of two LV modules with $V_i = 60\,\mathrm{V}$, $D = 0.4$, $f_{sw} = 20\,\mathrm{kHz}$, and $L = 200\,\mu\mathrm{H}$. The traces show the impact of using different number of harmonics in (2), highlighting the minor contribution of the ones above the n^{th}. The second derivative at the optimal point, y'', as a function of D, is calculated for the first 1000 harmonics and plotted in Fig. 6. It is noteworthy that the AC RMS cost function is not smooth at $D = 0.5$; however, it was verified that this did not pose issues in the implemented ESC scheme.

Some additional remarks concerning the proposed modeling approach are provided here. First, the derivations are only valid around the optimal point y''. Considering operation far from the optimal interleaving, e.g., to analyze convergence speed starting from the worst-case in-phase operation, the first-order Taylor-expansion term (i.e. the cost-function gradient) of y can be added to the model. Regarding extensions to $n > 2$, the convergence and small-signal analyses become dependent on the multi-variable cost function matrix partial derivatives

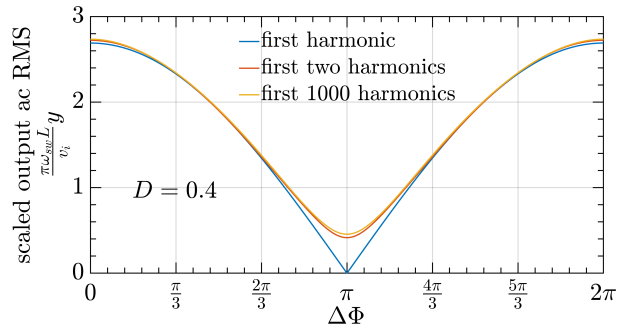


Fig. 5: Normalized cost function y for $n = 2$ balanced modules with $V_i = 60\,\mathrm{V}$, $D = 0.4$, $f_{sw} = 20\,\mathrm{kHz}$, and $L = 200\,\mu\mathrm{H}$, using (2) with different number of considered harmonics.

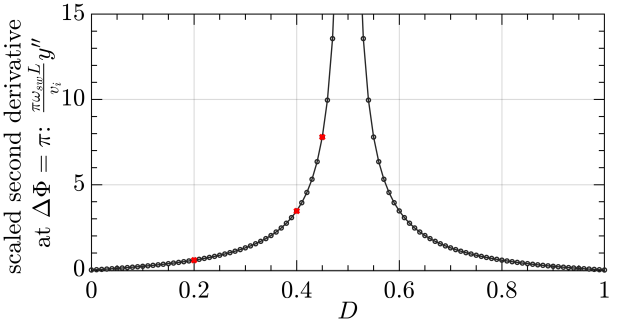


Fig. 6: Normalized second derivative y'' at the optimal point $\Delta\Phi = \pi$ as a function of duty cycle D. Operation at points marked with red are subsequently validated by simulations shown in Fig. 8.

(elements of the gradient and the *Hessian*). For a larger number of modules and, moreover, considering their possible unbalanced operation, the optimization space becomes very large. These topics are left for future work.

IV. Verifications

This section presents simulations and experimental results that validate the derived model and demonstrate the proposed approach's ability to achieve optimal interleaving in the presence of clock drifts and asymmetries among the LV modules. For all results, the switching frequency is $f_{sw} = 20\,\mathrm{kHz}$ and the ESC algorithm runs at the same rate. The PWM is implemented using trailing-edge carriers and all results are obtained for open-loop dc modulation.

A. Simulation results

The simulation model, implemented in MATLAB/Simulink, features a series-stacked system from Fig. 1(a). The load for the series-stacked system is formed using a passive parallel RC network, with $C = 33\,\mu\mathrm{F}$ and R determined based on target output power for different values of n and D. Simulation results are shown for balanced LV modules with input voltages equal to $V_i = 60\,\mathrm{V}$ and the total output filter inductance $L = 200\,\mu\mathrm{H}$. Sampling, modulation, and the ESC algorithm faithfully emulate the implementation in the DSPs used for the experimental results. The current measurements are simulated using 200 kHz bandwidth sensors with the ADC resolution that results in $LSB = 10.5\,\mathrm{mA}$.

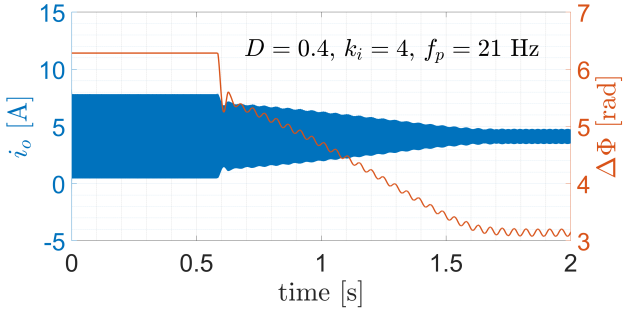


Fig. 7: Simulated ESC convergence from the worst case in-phase condition for $n = 2$ LV modules. The blue trace represents the output current and the red trace represents the phase shift.

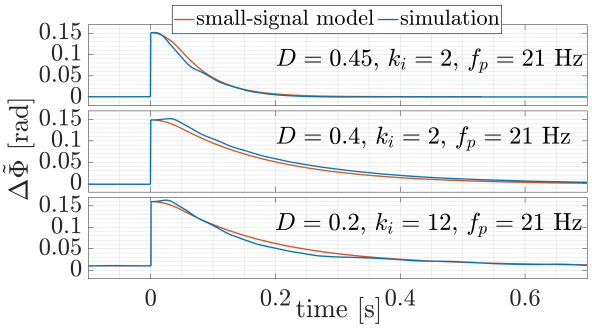


Fig. 8: Simulated validation of the disturbance rejection dynamics for $n = 2$ modules with different values of k_i and D corresponding to the red markers in Fig. 6. A step phase disturbance of $0.15\,rad$ is imposed at $t = 0$. The simulated traces closely align with the small-signal model (11).

The first set of results is given for $n = 2$ balanced LV modules and the total output power of 200 W. The perturbation frequency and magnitude are set to $f_p = 21$ Hz and $A_p = 2\pi/100$, and several values of k_i are tested to affirm the dynamic modeling. For these results, the clock drift is not included in the simulation. In Fig. 7, the convergence of the ESC is shown for $D = 0.4$ and $k_i = 4$. The system starts from the in-phase condition, which corresponds to the worst-case i_o ripple magnitude. After the ESC algorithm is enabled, the phase shift angle $\Delta\Phi$ converges to the optimal value, π, which minimizes the current ripple. Note that the small-signal modeling of Section III-B is not sufficient to estimate the total convergence time starting from the in-phase condition, as the starting point is far away from the optimum. to address this issue, the model can be extended based on the first-order term in the Taylor expansion of y.

To verify the first-order dynamics, a step phase disturbance $\Theta_{cd} = 0.15\ rad$ is imposed to the LV module operating with the optimal interleaving angle. The results, comparing the simulated response of $\Delta\hat{\Phi} - \pi$ with $\Delta\tilde{\Phi}$ modeled by (11), are given in Fig. 8 for the three values of D marked in Fig. 6. First, the top subplot is given for $D = 0.45$ and $k_i = 2$, which results in $\tau_{esc} = 84.4$ ms. For the middle subplot, the duty cycle is reduced to $D = 0.4$ and the gain is kept equal to $k_i = 2$. This increases the time constant to $\tau_{esc} = 144.3$ ms, which is predicted well by the model. Finally, the third subplot shows the case of $D = 0.2$ and the gain $k_i = 12$, which is chosen to result in the same time constant $\tau_{esc} = 144.3$ ms. As shown in the figure, the small-signal model accurately predicts the first-order dynamics. The presence of some unmodeled dynamics is anticipated due to the nonlinear characteristics of the ESC. Small steady-state errors can be seen, with values always bounded below the peak-to-peak value of the perturbation signal ($2A_p = \pi/100$). Similar verifications were repeated for various other operating conditions and, qualitatively, results did not change in terms of the dominant first-order response. However, it was noticed that the response does feature some dependency on the time at which the transient is imposed, which may be caused by different starting angles of the perturbation signal or the PWM carrier.

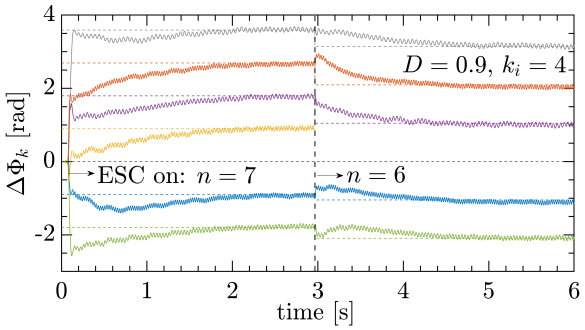


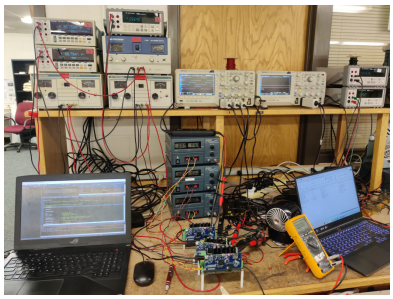
Fig. 9: ESC convergence for $n = 7$ LV modules, followed by a shut-down of one of them and the convergence to the optimal interleaving for $n = 6$.

Subsequently, the ESC is tested for 6 and 7 balanced LV modules. The output load resistance is set to obtain 3.8 kW with $V_o = 380$ V and the duty cycles are fixed to $D = 0.9$. The perturbation frequencies are set as $\{21, 24, 28, 32, 36, 40\}$ Hz, while the magnitude $A_p = 2\pi/100$ and the compensator gain $k_i = 4$ are set for all the modules. The clock drifts are simulated by injecting ramp signals to the PWM phases of all LV modules employing the ESC algorithm. The drift values are set equal to $\{2.44, -2.38, 2.27, -2.22, 2.78, -2.63\}$ μs/s, which corresponds to an arbitrary distribution around the maximal value measured between the microcontrollers used in the experimental setup.

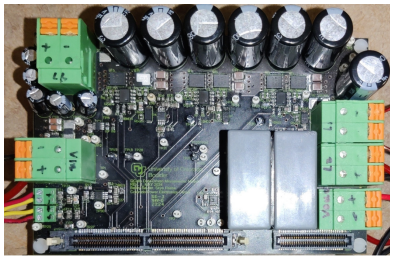
The results shown in Fig. 9 first demonstrate the convergence of a system with 7 balanced LV modules, starting from the in-phase operation. The full-line traces show simulated values of phase shifts $\Delta\Phi_k$ and the dashed traces show their optimal values corresponding to the symmetric PS-PWM. Following the initial ESC convergence, around $t = 3$ s, one of the modules is shut down, to which the system adapts and converges to the new optimal point, determined by $n = 6$, without modifying anything in the ESC loops. This is an important result, as it demonstrates a true plug-and-play nature of the ESC-based decentralized interleaving.

B. Experimental results

A photo of the experimental set-up is shown in Fig. 10(a), while the developed LV module prototype is shown in Fig. 10(b). Intended to serve as dc optimizers or as dc-ac units, the LV modules feature a soft-switched boost front-

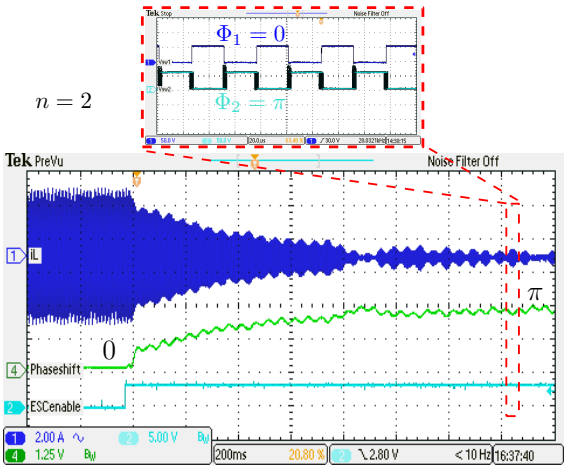


(a)

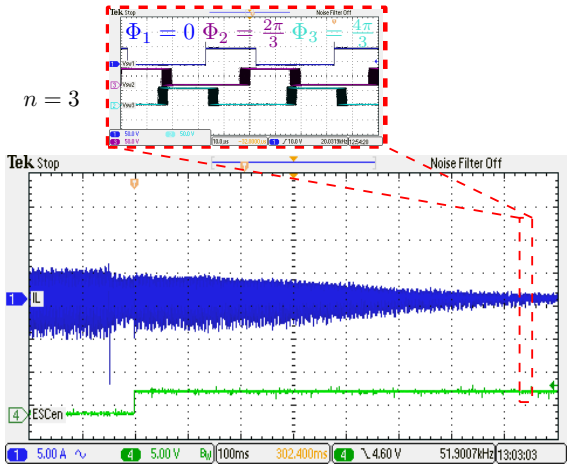


(b)

Fig. 10: (a) Photo of the experimental set-up with 3 LV modules; (b) photo of the LV module hardware prototype.



(a)



(b)

Fig. 11: (a) ESC convergence for: (a) $n = 2$ LV modules with $V_{i,1} = V_{i,2} = 58\,\text{V}$, $D_1 = D_2 = 0.5$, $f_p = 20\,\text{Hz}$, $A_p = 2\pi/100$, and $k_i = 4$; (b) $n = 3$ LV modules with $V_{i,1} = V_{i,2} = 56\,\text{V}$, $D_1 = D_2 = 0.4$, $f_{p1} = 109\,\text{Hz}$, $f_{p1} = 117\,\text{Hz}$, $A_p = 2\pi/160$, and $k_i = 0.2$. The ESC enable signal is triggered when the third module algorithm starts.

end that regulates the module dc-link voltage, and a full-bridge output that is, in this paper, configured to operate as a half-bridge stage. Each LV module is rated for 450 W and is controlled using its own controller based on the Texas Instruments F28379D. The load resistor is $R = 22\ \Omega$, the output capacitor is $C = 33\ \mu\text{F}$ and the filter inductor is $L = 180\ \mu\text{F}$.

Fig. 11(a) shows operation of $n = 2$ balanced LV modules with $V_{i,1} = V_{i,2} = 58\,\text{V}$, $D_1 = D_2 = 0.5$, $f_p = 20\,\text{Hz}$, $A_p = 2\pi/100$, and $k_i = 4$, including an illustration of the convergence to ideal interleaving after the ESC algorithm is enabled, as well as steady-state switched-node waveforms showing ideal π interleaving of the two balanced stacked modules. The phase shift is measured by outputting the ESC result using the digital-to-analog converter (DAC). One may also observe continuous small perturbations in the switched-node waveform of the second module. The second result, shown in Fig. 11(b), is given for $n = 3$ balanced LV modules, with $V_{i,1} = V_{i,2} = 56\,\text{V}$, $D_1 = D_2 = 0.4$, $f_{p1} = 109\,\text{Hz}$, $f_{p1} = 117\,\text{Hz}$, $A_p = 2\pi/160$, and $k_i = 0.2$. It can again be seen that the ESC algorithm results in the optimal interleaving. For both results, the modules are initially synchronized using an external signal, to allow starting from the in-phase condition.

Finally, the capability of ESC to synchronize unbalanced LV modules was validated for $n = 2$, by lowering the input voltage of the second module. Steady-state waveforms comparing the operation of symmetric and asymmetric interleaving are shown in Fig. 12. The ESC parameters are $f_p = 30\,\text{Hz}$ and $A_p = 2\pi/100$. The asymmetry is achieved by setting $V_{i,1} = 58\,\text{V}$ and $V_{i,2} = 40\,\text{V}$, while the duty cycles are kept equal, $D_1 = D_2 = 0.8$. It is verified analytically that the optimal phase shift for equal duty cycles and mismatched input voltages remains equal to π, which is achieved experimentally. The corresponding theoretical AC RMS value is equal to $0.52\,\text{A}$, which is close to the experimentally measured value of $0.55\,\text{A}$.

It is important to note that the presented results primarily focus on verifying the ESC's ability to compensate for clock drifts among the module microcontrollers in the prototype hardware setup. Faster dynamic performance of the ESC may be necessary to mitigate increased component stresses during start-up transients, which is an area for future work.

V. Conclusions

This paper presents a decentralized solution for achieving optimal interleaving of series-stacked dc-dc converters using a module-level extremum-seeking control (ESC) approach. The developed method is capable of minimizing the current ripple without any communication between the stacked modules, while compensating for the impact of clock drifts among module microcontrollers. Compared to existing methods, advantages include the model-free nature of the ESC, plug-and-play

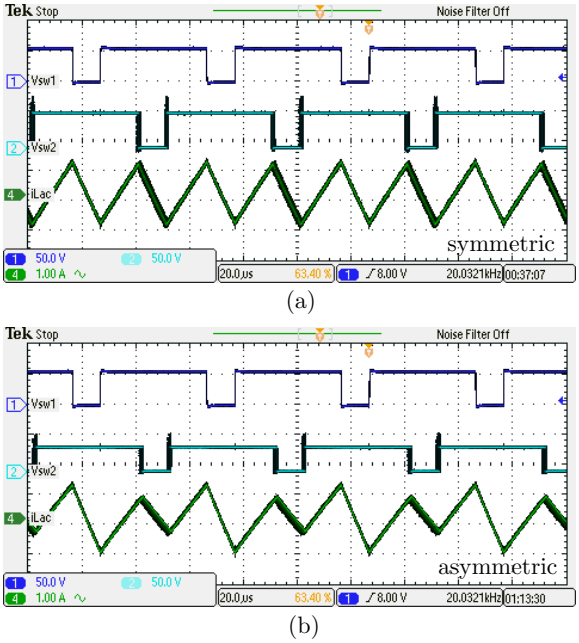


Fig. 12: Steady-state waveforms showing interleaving of $n = 2$: (a) balanced LV modules with $V_{i,1} = V_{i,2} = 58\,\text{V}$, $D_1 = D_2 = 0.8$ and (b) unbalanced LV modules with $V_{i,1} = 58\,\text{V}$, $V_{i,2} = 40\,\text{V}$, $D_1 = D_2 = 0.8$.

operability with asymmetric modules, and simple design and digital implementation without relying on sophisticated sampling schemes. To facilitate a preliminary analysis of system dynamics and clock drift disturbance rejection, a small-signal dynamic model is proposed and validated for the case when the system consists of two modules. Decentralized interleaving is validated by simulations for up to seven series-connected modules, also showing the capability to ride-through a module shut-down. Experimental results are provided for a system comprising up to three modules, including unbalanced module operation.

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