Digital Control of a 600-V to 28-V 20-kW Two-Stage DC-DC Converter

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***Abstract*—A trend of increasing powertrain voltages is seen in electric vehicles and more electric aircraft. However, the systems close to humans have stayed at 12 to 48 V for safety reasons. A combination of control and converter architecture is needed to efficiently meet the required gain over all line and load conditions. This work briefly introduces a converter architecture and, in detail, demonstrates a digital control technique for a 600 V to 28 V 20 kW two-stage DC-DC converter. A modular input-parallel output-parallel (IPOP) configuration with two identical 10 kW modules is used. Each module consists of a buck stage for regulation followed by a series-resonant DC transformer (SR-DCX) for isolation and a fixed gain. A current sharing compensator is designed to ensure equal current sharing between IPOP modules. The control technique considers constraints due to signal-chain processing and minimizes digitization delays. The scheme experimentally demonstrates robust control over the required line and load variations for the 10 kW module. The devised control technique demonstrates equal current-sharing amongst the paralleled modules using a PLECS simulation.**

***Index Terms*—Aerospace, average current mode control, buck converter, current sharing, dc-dc converter, digital control, series-resonant dc transformer (SR-DCX), timing diagrams.**

I. Introduction

The powertrain bus levels of aircraft and electric vehicles are rising to reduce cabling weight and losses. However, the systems near humans have stayed around 12-48 V for safety reasons. Recent trends show that for an aircraft's Electrical Power Distribution System (EPDS), the main DC bus voltages may range from ±270 V to 3 kV [1]. The current generation of the electrical power system (EPS) EPS-A4 in aircraft uses a ±270 V DC bus on the high-voltage (HV) side, and 28 V DC bus on the low-voltage (LV) end [1]. Similar EPS have also found their way to military ground vehicular applications [2]. The typical bus voltages for EPS-A4 are governed by MIL-STD-704F [3] for both HV and LV buses and by MIL-PRF-GCS600A [4] on the HV bus for military ground vehicles. Given the gain, typical power level, and reliability requirements, this poses an exciting challenge for an interlinking converter between the two buses. The present state-of-the-art presents a topological analysis and improvements for similar converters in [5]–[7]. In [8], the authors describe efficiency improvement through improvements in modulation techniques. There have been contributions for controlling 270 V to 28 V converters in [9], [10]. However, the literature is limited to topological improvements, focusing only on module-level improvements. Furthermore, average efficiencies over the total input voltage span are unknown, given design optimizations and demonstration at nominal operating voltages. Similarly, a gap in the demonstration of control techniques exists for such converters. The practical challenges arising in sensing signal chains due to the converter size are also not discussed.

Thus, this work addresses the gaps in the literature using a two-stage converter topology and demonstrates a digital control approach for a high-gain converter tailored to such applications. Given the power rating of the converter, an input-parallel output-parallel (IPOP) two-stage DC-DC converter architecture is used in this work. The buck converter is regulated by regulating the average inductor current, which is set by an outer voltage regulation loop. However, the paralleled modules bring another layer of control challenge of ensuring equal current sharing (CS) amongst both modules. The review in [11] highlights various approaches for controlling paralleled converters. The work in [12] is used as a starting point and expanded on to design a compensator for ensuring equal power sharing by both modules.

The article is split into five Sections: Section II details the converter structure, key components, operational requirements, and basic operating principles. The control problem is defined in Section III. Herein, the overall control law is derived, the analysis for regulating the first stage, and solutions for ensuring equal CS between paralleled modules are explored. Furthermore, signal chain constraints and discretization penalties are also added to the control problem, and a compensator design is derived. In Section IV, based on the established control law, the timing sequencing arranged for easy and improved microcontroller implementation is discussed. Finally, simulation results for the 20 kW converter and experimental results for a 10 kW module over the entire line and load conditions are demonstrated in Section V.

II. Converter Topology, Design, and Operation

The converter schematic, topology, and the values of critical components can be seen in Fig. 1. The converter is constructed using two identical modules of 10 kW each, connected in an IPOP configuration. Each module comprises a single 10 kW HV power processing end. The LV end, however, is split into

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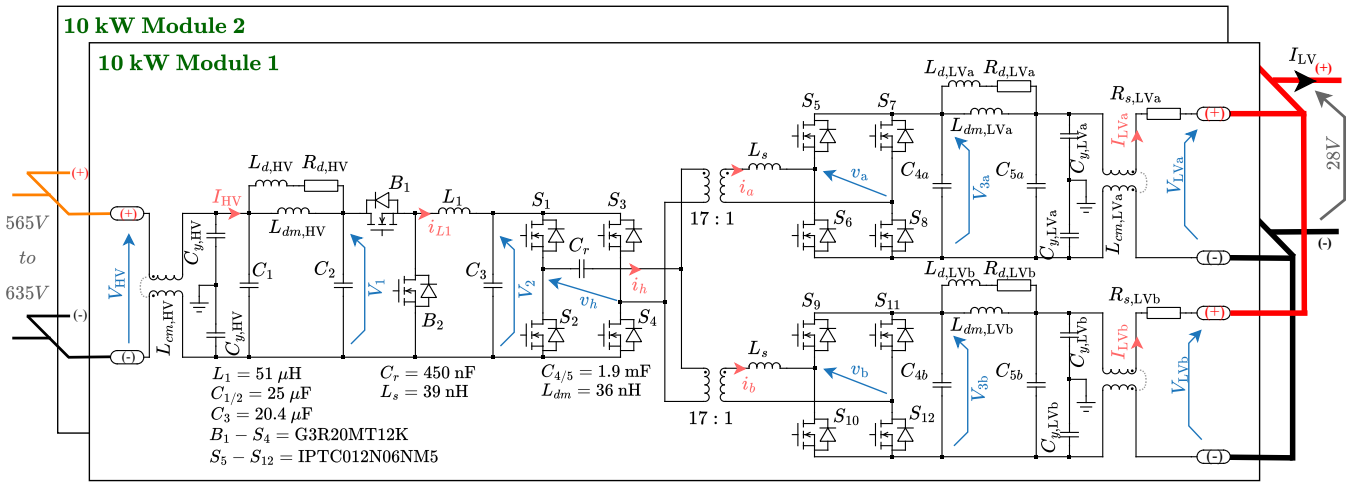


Fig. 1: Schematic of the 600-V to 28-V 20-kW two-stage DC-DC converter.

two 5 kW sub-modules. The HV end uses Silicon-Carbide (SiC) switches without paralleling on all nodes. The LV end is constructed using silicon switches and uses three devices in parallel to meet the necessary current ratings. Each of the 10 kW modules consists of a two-stage converter. The first stage is a synchronous-buck converter, and the second is a series-resonant DC transformer (SR-DCX). The buck stage is responsible for meeting the converter's full line and load regulation requirements. The buck converter's design and operating range ensure a continuous-current mode operation at all operating conditions except at very light loads. In contrast, the SR-DCX operates near its resonant frequency in an unregulated mode. The operation near resonance results in the SR-DCX stage exhibiting an almost fixed gain, irrespective of load variations. However, a small but linear reduction in the gain occurs with increasing power delivered by the converter [13], which is compensated by the buck converter.

Given the current levels on the LV end, the key reason for selecting an SR-DCX topology is to operate close to zero-current switching at the LV side of the converter. This approach relaxes thermal constraints on the LV side and has the added benefit of inherently lower EMI impact [14]. The SR-DCX on the LV side enables two key design improvements: Firstly, the sub-module's rated current decreases, reducing the number of devices needed in parallel and the challenges associated with device paralleling. Secondly, the split allows for magnetics design with standard cores for handling the required currents and PCB design to meet package constraints. The partial paralleling structure also allows the using two independent 5 kW low-voltage modules to be fed from a single 10 kW HV end [15]. The partial paralleling approach also allows optimal utilization of space and rating of high-voltage components. The SR-DCX also enables near-symmetric current-sharing between the two LV modules [16]. The partial paralleling is achieved by having a common feed capacitor while using the inherently high system leakage inductance. The leakage inductance is high given the high turns ratio of the transformer at $N = 17$, thus amplifying the effect of transformer and PCB leakage inductance by a factor of N^2. This leakage inductance is also relatively unaffected by piece-to-piece variations due to PCBs' tight geometric manufacturing capabilities, further aiding symmetric CS. It should be noted that symmetric current-sharing is achieved in the SR-DCX stage without having any control degree of freedom between the two LV modules. The buck converter and SR-DCX are synchronously operated at the same switching frequency f_s of around 100 kHz. It should be noted that the switching frequency is similar but different in the two paralleled 10 kW modules due to the variations in the SR-DCX's tank components.

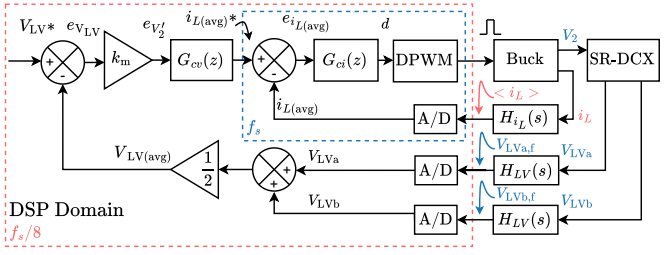


Fig. 2: Control scheme for a two-stage 10-kW module.

III. Control Strategy, Modeling and Analysis

The converter structure selected for its various benefits imposes a layered control challenge. Firstly, the IPOP connection introduces a static and dynamic CS challenge between the two modules. Secondly, the two-stage nature of the module introduces modeling peculiarities. In order to address these, the following control strategy and model simplifications are done to analyze the control performance of the converter.

A. 10-kW Module Control

The module-level control strategy can be seen in Fig. 2. The buck stage is regulated using a fixed frequency variable duty cycle control approach. The employed control technique

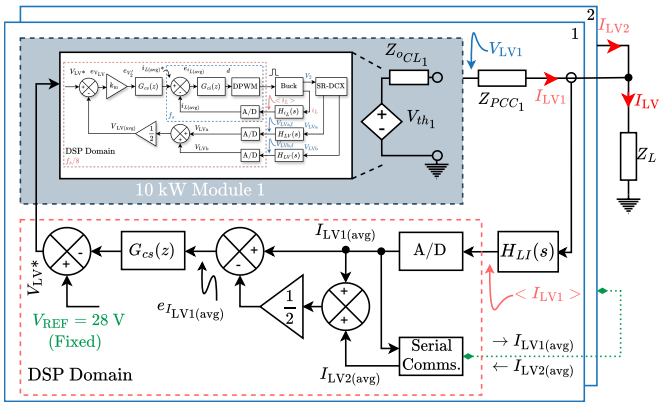


Fig. 3: Control scheme for the 600-V to 28-V 20-kW DC-DC converter.

is the dual-loop average current mode control approach [17]. The buck stage is controlled to directly regulate the average voltage seen on $V_{LVa/b}$ nodes. The SR-DCX's unregulated operation at a constant switching frequency near resonance is tuned offline for optimal full-load efficiency. Given the SR-DCX's operation near resonance, this stage exhibits an almost constant gain and only minor phase penalties. This constant gain effectively acts as a proportional controller k_m for the SR-DCX stage embedded within the first stage's control mechanism.

$$G_{id}(s) = \left(\frac{V_2}{dR_{eq}}\right) \frac{1 + sR_{eq}C_3}{s^2L_1C_3 + s\frac{L_1}{R_{eq}} + 1} \tag{1}$$

$$G_{vd}(s) = \left(\frac{V_2}{d}\right) \frac{1}{s^2L_1C_3 + s\frac{L_1}{R_{eq}} + 1} \tag{2}$$

where, d is the operating point duty ratio, R_{eq} is reflected load resistance by the SR-DCX on the buck converter, C_3, L_1, and V_2 are as referenced in Fig. 1.

$$G_{cv}(z) = \frac{0.1073z - 0.1046}{z - 1} \tag{3}$$

In order to use the small-signal approximation for modeling the buck-converter, the modeling involves making two key approximations. Firstly, the EMI filter feeding the buck stage of the converter is designed to satisfy the Middlebrook stability criteria [18]. Thus, it is assumed that this circuital element does not impact the closed-loop analysis. Secondly, given that the second stage operates close to resonance, the first-harmonic approximation accurately refers the load resistance to the primary side [16]. Thus, as seen by the buck stage, the load is purely resistive. The stability analysis of the buck stage of the module is now carried out over the entire line and load regulation range.

$$G_{vc}(s) = \left(\frac{1}{H_{i_L}}\right)\left(\frac{G_{vd}}{G_{id}}\right)\frac{T_i}{1 + T_i} \tag{4}$$

where, H_{i_L} is the averaging filter with a bandwidth of 12 kHz, T_i is the current loop gain, a product of G_{ci}, G_{id}, H_{i_L}, and discretization delay e^{-st_d} assuming the gain of the DPWM block is unity.

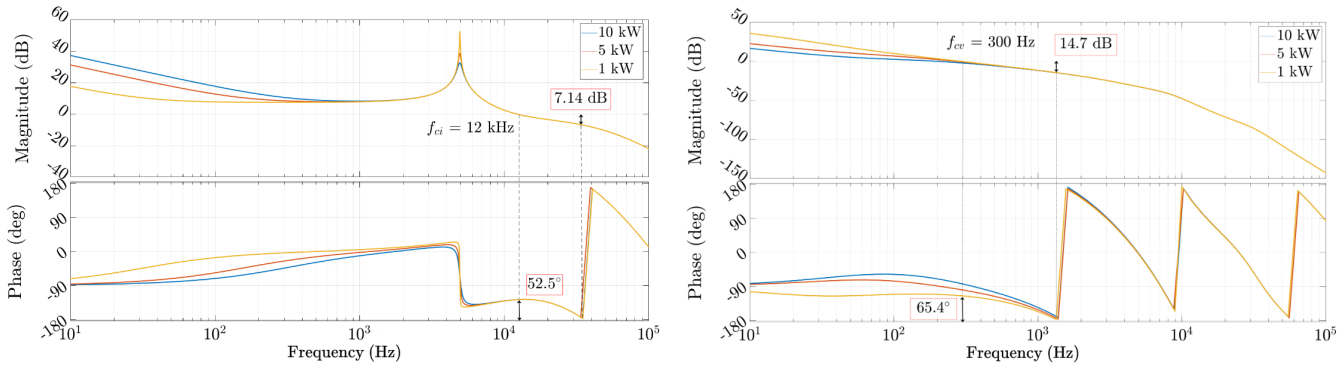
The average inductor current of the buck converter is tightly regulated with the help of a Type-3 compensator. The control-to-inductor current transfer function $G_{id}(s)$ of the plant is described by (1). The current controller is designed to have a bandwidth of 12.5 kHz around $\frac{1}{8}^{th}$ of the switching frequency. The current measurement is done with the help of a high-bandwidth hall-effect current transducer, and a third-order analog filter averages the signal to a bandwidth of 12 kHz. The Type-3 compensator $G_{ci}(z)$ accounts for the averaging filter (5). The compensator is designed for operation at the 650 V V_{HV} 10 kW operating point and discretized at the converter switching frequency using the Tustin approximation.

$$G_{ci}(z) = \frac{0.03055z^3 - 0.05192z^2 + 0.03131z - 0.006769}{z^3 - 0.4193z^2 - 0.4999z - 0.08083} \tag{5}$$

After the inner current loop is closed, the plant $G_{vc}(s)$, as observed by the outer voltage loop, is described by (4). Herein, the control-to-output voltage behavior $G_{vd}(s)$ of the plant is represented by (2). The outer voltage regulation loop uses a PI compensator $G_{cv}(z)$ with anti-windup capability and is band-limited at 300 Hz (3). The voltage loop runs at $\frac{1}{8}^{th}$ the switching frequency of 12.5 kHz and is discretized at this rate again using Tustin approximation. Both the compensators are also evaluated to ensure that the input voltage fluctuations are not dominant in governing the converter output. Given the digital control approach, discretization delays due to loop execution and analog-to-digital conversion (ADC) are considered in these loop gain plots using second-order Pade approximation of e^{-st_d}. The resulting continuous time margin plots for a 600 V V_{HV} operating point with different power levels can be seen in Fig. 4(a) and Fig. 4(b).

B. Paralleled Module Control

The 20 kW control block diagram is shown in Fig. 3. The paralleling of power modules using bus-bars to a point-of-common-coupling (PCC) introduces a connecting impedance Z_{PCCx} where $x \in \{1, 2\}$. In order to ensure equal CS between the paralleled modules, the Thevenin voltage V_{thx} must be regulated such that it overcomes both Z_{oCL} and Z_{PCCx} instantaneously to deliver the necessary current. Thus, the voltage reference at the input of Fig. 3 V^*_{LV} is used to overcome various system impedances using a CS compensator $G_{cs}(z)$. The compensator $G_{cs}(z)$ generates an error voltage added to the fixed reference to regulate the converter output voltage. The compensator is fed by the difference of: Firstly, the sum of the sensed output current from both the 5 kW sub-modules and, secondly, the average current flow out of both the 10 kW modules. This difference effectively corrects any current-sharing imbalances between the two modules. The current measured by each module I_{LV1} and I_{LV2} are communicated over a full-duplex RS-485 serial bus dedicated for control purposes.



(a) (b)

Fig. 4: Bode plot showing (a) current loop gain (T_i) and (b) voltage loop gain with inner loop closed (T_v).

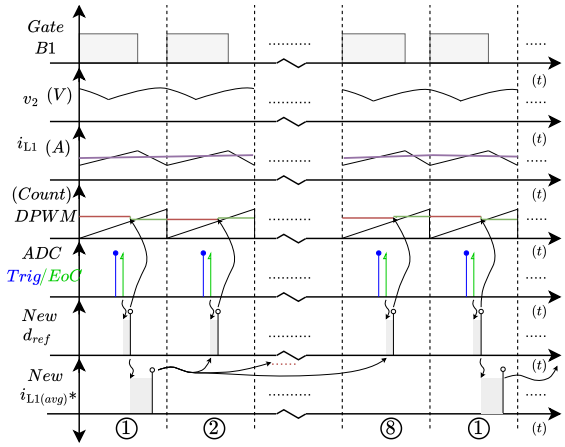


Fig. 5: Control logic timing diagram for a 10-kW module.

In order to ensure equal current-sharing between the two 10 kW modules, firstly, the impact on the converter's output impedance with a closed current loop is analyzed and is given by Z_{oCL} [17]. Then, the module level transfer function is achieved by block reduction of both the current and the voltage loops, representing the module's Thevenin voltage V_{thx}. This information is used to construct a Thevenin equivalent circuit. In order to overcome the impedances, the compensator $G_{cs}(z)$ must be analyzed to ensure that the changes to the voltage reference it makes do not make either of the modules unstable. The transfer functions from the reference voltage to the module output current for the same module is given by (6) and for the other module is given by (7) [12]. The transfer functions depend on the Thevenin parameters F and, crucially, the gain of the CS compensator $G_{cs}(z)$. Thus, designing $G_{cs}(z)$ such that G is stable while tuning it to a desired bandwidth and margins [12] enables a stable CS operation. In this work, pole-zero placement is done to achieve a desired loop response from G. The compensator $G_{cs}(z)$ is also discretized using Tustin approximation and is executed at the same rate as the voltage compensator loop T_v.

$$\frac{I_{lv_j}}{V_{\mathrm{REF}j}} = \frac{F\left(1+H+\frac{G}{2}\right)}{(1+G)(1+2H)} \tag{6}$$

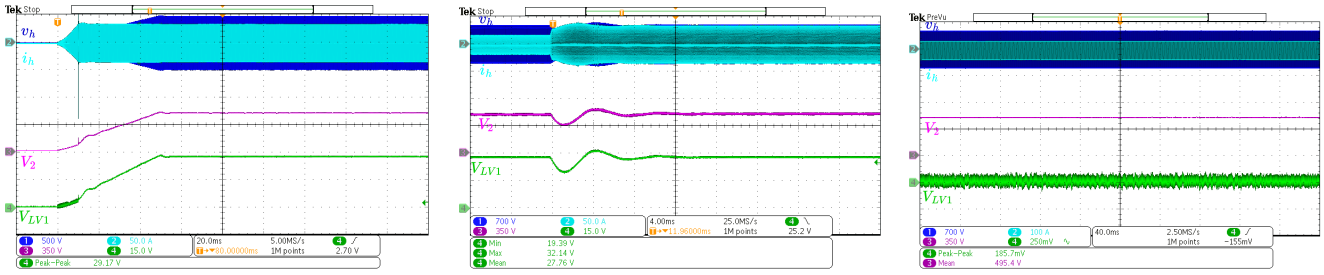
$$\frac{I_{lv_k}}{V_{\mathrm{REF}j}} = \frac{F\left(\frac{G}{2}-1\right)}{(1+G)(1+2H)} \tag{7}$$

$$\text{where, } F = \frac{1}{H_{lv}}\frac{T_v}{(1+T_v)Z}\ ,\ Z = Z_{PCC_x} + \frac{Z_{\mathrm{OL}}}{1+T_i}$$

$$G = FG_{cs}, \text{ and } H = \frac{Z_L}{Z}$$

IV. Discrete Implementation

As designed in Section III-A, the compensator difference equations are executed on a custom control board based on TMS320F28377D. Figure 5 shows the control sequence and how various digital signal processor (DSP) resources emulate a close-to-analog behavior. Firstly, all the control elements are linked to a base PWM module, which generates the gating signals for the buck converter stage. The analog-to-digital converter (ADC) conversion for sampling the average inductor current is triggered at a fixed 50% duty based on a compare-capture event on the base PWM module. The sampling point is selected to represent a noise-immune approximation of the average inductor current for the nominal operating points. Two samples with an acquisition window of 0.6 μs are picked and averaged to minimize operating point sensitivity. It should be noted that the position of sampling is selected based on the nominal operating duty range. Given that the duty range under regular operation ranges between 72 to 90%, there is approximately a 1 μs window for computing new duty value. The end-of-conversion notification from the ADC triggers the current compensator difference equation computation. Finally, the new duty value is immediately loaded for comparison, resulting in a worst-case discretization delay of approximately 0.4 cycles or e^{-st_d}, where $t_d = \frac{0.4}{f_s}$. Since most of the above actions are enabled by hardware configurations, very little CPU overhead is added while maintaining a symmetric cycle-by-cycle operation. Thus, the implementation enables a minimal phase margin penalty despite the discrete operation.



(a) (b) (c)

Fig. 6: Experimental results of a 10-kW module at V_{HV} = 650-V : (a) Soft-start at 10-kW, (b) Step load addition 5-kW → 10-kW, (c) Steady-state AC coupled response at 10-kW.

Similarly, the voltage compensator loop is executed by a separate PWM module linked to the base PWM module for synchronous operation. Here, the clock feed is prescaled by a clock divider of $\frac{1}{8}^{th}$, thereby resulting in an execution rate that is 8 times slower than the current compensator loop. Given all the PWM modules are linked, the prescaled clock feed to the voltage loop ensures a synchronized operation between current and voltage loops. The ADC conversion is triggered at a fixed 10% duty of the voltage loop timer to provide a new $i^*_{L(avg)}$ reference between two consecutive current loop executions. Furthermore, the same voltage loop PWM module samples the other analog signals used for over-current and over-voltage protection mechanisms. The SR-DCX stage's gating commands are also generated in alignment with the buck converter's base PWM module. This enables a synchronous operation between the two converters. It should be noted that the resonant frequency is tuned offline at full power, and start-up calibration of the resonant frequency is not considered in this work.

V. Results

The experimental setup for the 600 V to 28 V 20 kW two-stage DC-DC converter is seen in Fig. 7. The discussed digital control technique is demonstrated experimentally on a 10 kW module. The CS demonstration for the full 20 kW converter control scheme is done using PLECS simulations. The experimental results using the above-designed compensator and control scheme can be seen in Fig. 6 for an input voltage V_{HV} of 650V. The soft-start operation for the converter is done by linearly increasing the reference voltage command from 0 to 28 V, as shown in Fig. 6(a) with the load set to 10 kW when performing the soft-start sequence. This result empirically confirms the control approach's large-signal stability. In order to evaluate the dynamic performance of the control scheme, a step load addition test is carried out. In this test, the load is increased from 5 kW to 10 kW with a current slew rate of $1\frac{A}{\mu s}$. Results can be seen in Fig. 6(b) shows a voltage sag of about 30%, within MIL-STD-704F limit [3]. The results in Fig. 6(c) show the steady-state AC coupled results with a peak-to-peak ripple of about 0.6%. The steady-state ripple results are shown with the load configured to 10 kW. The scheme is experimentally verified similarly for the entire input range of 550 to 650 V at the V_{HV} node as highlighted in Table I.

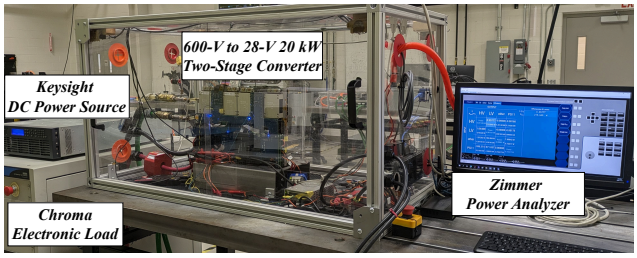


Fig. 7: Experimental setup of the two-stage 20-kW DC-DC converter.

The control approach for paralleling two modules, described in Section III-B, is evaluated using a discrete step solver in PLECS with a fixed step execution rate of 100 ns based on Tustin approximation. The CS compensator, voltage- and current-control loops are simulated to match the DSP behavior as in Fig. 5. Also, a noise component is injected on all sense lines to simulate a more realistic system. The noise content is modeled by a line frequency sinusoidal component, a triangular wave-based impulse content for switching instances, and a random noise content. The noise component is kept at 5% of the signal swing range, as seen by the ADC. The operating point of the converter is set at 650 V at the V_{HV} node and a load of 14 kW at start-up. The results are shown in Fig. 8. The left half of the results show converter behavior

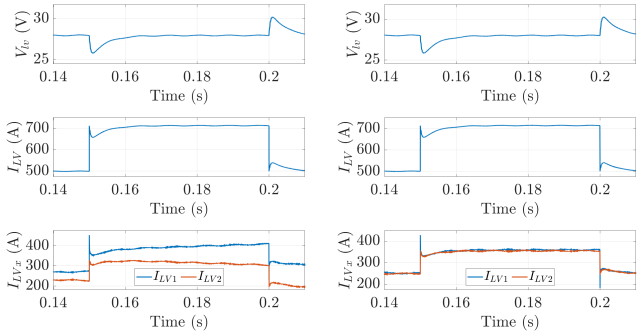


Fig. 8: PLECS simulation results of 20-kW closed-loop operation. Left: Without current sharing scheme and Right: With current sharing scheme.

TABLE I: Experimental results for a 10-kW module under digital closed-loop control.

Input (V)	Steady State AC ripple (mV_{pp})			$5 \rightarrow 10$ kW	$10 \rightarrow 5$ kW
V_{HV}	1 kW	5 kW	10 kW	Sag (V)	Swell (V)
550	172	288	198	8.6	6.8
600	165	197	1200	8.6	9.1
650	180	176	185	8.3	10

under no CS control, and the right half shows the behavior with the CS control enabled. The test sequence involves stepping the load from 14 kW to 20 kW at 150 ms and removing the load at 200 ms. The static CS is significantly off by a factor of 25% when the CS controller is not enabled. The CS controller ensures the current is balanced within $\pm$ 10A of the current demanded by the load.

VI. Conclusion

The paper discussed a digital control approach to regulate a 600 V to 28 V 20 kW two-stage converter. A brief introduction to the converter structure was provided. The control approach and analysis were discussed. A simple modeling approach for regulating the two-stage module is taken and experimentally verified for line and load operating conditions. Efficient DSP implementation for minimizing digitization delays is highlighted. The control analysis is experimentally verified on a 600 V to 28 V 10 kW module with a steady state AC ripple of 0.6%. A current sharing compensator is designed by modeling the closed-loop behavior of the modules and using the interconnecting impedances. A PLECS study is carried out to check and verify the effect of the current sharing loop, which ensures static current sharing stays within $\pm$ 10A of either module. The next revision to this work will experimentally demonstrate symmetric current sharing under dynamic and static loading scenarios. It will also discuss the mathematical framework for dynamic current sharing challenges and delays resulting from the digital communication link. Furthermore, improvements in the dynamic performance of the 10 kW module will be explored by phase compensation for the SR-DCX stage.

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