Frequency Stop-Band Management System for DC-DC Converters

Alessandro Bertolini, Alberto Cattani, Claudio Luise and Alessandro Gasparini
STMicroelectronics, APMS R&D, Milan
Email: alessandro.bertolini@st.com

***Abstract*—Ever complex electronic systems have pushed the requirements on power management to new limits, with applications needing to satisfy stringent operating frequency constraints while maintaining high efficiency. This article addresses the requirement to avoid any operation of a DC-DC converter in specific frequency bands when regulating light loads in discontinuous-conduction-mode (DCM) and operating in pulse-skip-mode (PSM). The presented stop-band-management-system (SBMS) is a versatile mixed-signal solution that has been designed for an inverting buck-boost (IBB) converter, which generates a programmable output voltage in the range of -1V to -9V from a Li-Ion battery. Targeting consumer Active-Matrix-Organic-Light-Emitting-Diode (AMOLED) display applications, a power-management-integrated-circuit (PMIC) has been fabricated in a 180nm bipolar-CMOS-DMOS (BCD) process, and the effectiveness of the proposed solution is shown with experimental results.**

***Index Terms*—power management, PMIC, inverting buck-boost, DC-DC, switching regulator, BCD, power converter, DCM, stop-band, PSM, current-mode, EMI, PFM, AMOLED, SMPS.**

I. Introduction

In many applications, the need for high-quality, ultra-low-noise power rails poses new challenges in providing such regulated rails. High-end Active-Matrix-Organic-Light-Emitting-Diode (AMOLED) panels are among these applications, requiring a clean and stable power supply to avoid flickering-on-screen (FOS) and not impact the user experience [1]. Any noise on such rails affects the voltages of each single pixel's thin-film transistor, manifesting as noise in the luminescence of the display [2], [3], [4], eventually causing eye fatigue. In addition, in densely packed consumer devices noise interference with other sub-systems is a concern, and thus both conducted and radiated electromagnetic interference (EMI) emissions in specific frequency bands must be avoided. De facto, in AMOLED display FOS can be also induced by any frequency beating with the panel operating frequencies. Concurrently, efficiency cannot be traded-off in providing these power rails, especially in battery-powered applications. For these reasons and considering the efficiency penalty posed by low-dropout (LDO) linear regulators (especially at high load), the design community has been recently pushed to investigate on switching-mode-power-supplies (SMPS) capable of generating high-quality regulated rails [5], [6]. Furthermore, to the best of the authors' knowledge, the request to seamlessly avoid any operation of clocked DC-DC converters in specific frequency bands has never been disclosed. Generally, the involved DC-DC converters exploit the widely used peak-current-mode control (PCM) [7], [8], due to the inherent current limitation and simpler compensation compared to voltage-mode-control (VMC) [9]. At high load (e.g., up to 1 A), when the power converters are operated in continuous-conduction-mode (CCM), they typically operate with a switching frequency ($F_S = 1/T_S$) well above any stop-band SB (e.g., $F_S = 1.5\,\mathrm{MHz}$). On the contrary, the focus is on light load conditions, where the converter is regulating in discontinuous-conduction-mode (DCM) and its switching activity is reduced (e.g., [10], [11], [12]). In fact, the aforementioned requirement is intended both in terms of i) switching frequency in CCM and/or DCM, and ii) pulse-skip-mode (PSM [13]) frequency or pulse-frequency-modulation (PFM [14]) activity. Typically, to allow a proper measurement a sampling-window SW up to a maximum of 1 ms is provided. The power converter is thus required to: 1) auto-detect its activity when steadily lying within an undesired band, and 2) "move" its operation outside forbidden bands without compromising the regulation performance. For the latter, in "moving" the converter operation outside forbidden bands the controller is required to minimize any output variation, guaranteeing a seamless correction, meaning ideally not visible on V_{OUT}. In this process, the output voltage ripple and the efficiency should not be degraded, making the forced-CCM operation a non-viable option. In Table I are reported some exemplary stop-band specifications, typically programmed from kHz up to hundreds of kHz and dynamically selected on-the-fly.

TABLE I
Stop-Band Specifications

Stop-Band	F_{SB}^{MIN}	F_{SB}^{MAX}
SB1	15 kHz	35 kHz
SB2	40 kHz	60 kHz
SB3	90 kHz	110 kHz
SB4	135 kHz	155 kHz

The remainder of this article is organized as follows. The proposed solution and system architecture are described in Section II, with detailed implementation of the digital controller in Section II-B, circuit design insights are given in Section II-C, and an exemplary simulation showing the system behavior is presented in Section II-D. Experimental results are presented in Section III, while the conclusions are drawn in Section IV.

979-8-3315-1611-6/25/$31.00 ©2025 IEEE

II. Proposed Solution & Implementation

A. System Architecture

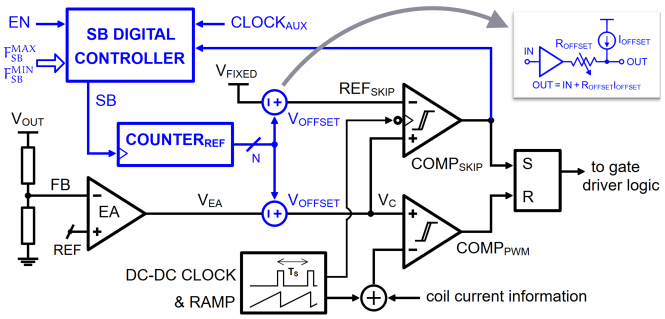

Fig. 1. Simplified schematic of the proposed solution (drawn in blue) applied to a generic peak-current-mode-controlled DC-DC converter (depicted in black) featuring PSM for light load operation.

Figure 1 shows the simplified schematic of the proposed solution (drawn in blue) applied to a generic DC-DC converter with peak-current-mode-control[1] (depicted in black) and is now briefly introduced. As a simple convention, the beginning of each switching cycle is defined by the DC-DC converter clock falling edge. In this precise moment, the skip comparator $COMP_{SKIP}$ is checked. By monitoring the control voltage V_C with respect to a fixed voltage REF_{SKIP}, this comparator decides whether to perform a new switching cycle (e.g., in CCM) or to halt the switching activity. As a normal PWM-based operation, the PWM comparator sets the converter duty-cycle for proper V_{OUT} regulation. At light load, when V_C goes below REF_{SKIP} (i.e., $COMP_{SKIP}$ does not trigger high), the converter activity is reduced to enhance efficiency [15]. Particularly, the DC-DC converter regulates in PSM (also called *burst-mode* [16]) performing K subsequent switching cycles followed by M succeeding cycles with no operation. In this case, the power converter operates with a coil peak current set by REF_{SKIP}, and regulates V_{OUT} by modulating K and/or M. The term F_{SKIP} is simply used to refer to the converter repetition rate in PSM.

Given the requirements described in Section I, it is necessary to 1) smartly measure F_{SKIP} to detect if/when the converter is operating within a SB, and 2) find a corrective action that robustly allows it to hop away from the SB in a seamless way (i.e., without generating any transient on V_{OUT}) with no performance degradation.

1) Agile Detection: First of all, the idea is to monitor $COMP_{SKIP}$ and compare its behavior with a time reference signal to understand if the converter is operating with a repetition frequency F_{SKIP} that is not allowed. $COMP_{SKIP}$ is oversampled by exploiting an auxiliary clock, $CLOCK_{AUX}$, with a fixed frequency F_{CK}^{AUX} sufficiently higher than the highest F_{SB}^{MAX}. Specifically, if both the following conditions are satisfied, then it is possible to state that the DC-DC converter is operating within a SB (defined as the range of frequencies from F_{SB}^{MIN} to F_{SB}^{MAX}):

1) counting the number of auxiliary clock periods between two consecutive $COMP_{SKIP}$ rising edges

$$\left\lfloor \frac{F_{CK}^{AUX}}{F_{SB}^{MAX}} \right\rfloor \leq \text{number of } CLOCK_{AUX} \text{ periods} \leq \left\lceil \frac{F_{CK}^{AUX}}{F_{SB}^{MIN}} \right\rceil \quad (1)$$

2) in a sampling-window of duration t_{SW}

$$t_{SW} F_{SB}^{MIN} \leq \text{number of } COMP_{SKIP} \text{ rising edges} \leq t_{SW} F_{SB}^{MAX} \quad (2)$$

Condition (2) accounts for the average behavior of the converter within the sampling-window, but does not provide any information about the actual/instantaneous F_{SKIP}. Note that assessing only the second condition would be dangerous, since it does not provide any information about the density of $COMP_{SKIP}$ activity. In fact, condition (2) can be true for both the two following exemplary situations: 1) the converter is steadily performing in PSM with a given F_{SKIP1} that satisfies (2), and 2) the converter is initially performing with $F_{SKIP2} \gg F_{SKIP1}$ and then experiences a transient drastically lowering $F_{SKIP2} \ll F_{SKIP1}$. In the second case, in average F_{SKIP2} could still satisfy (2), but a corrective action would be required only in the first case, while in the latter the DC-DC converter should simply be allowed to settle, without the need of any action.

On the contrary, condition (1) provides insights about the present F_{SKIP}, but with a coarse resolution limited by F_{CK}^{AUX}. Moreover, not considering for a moment this limited resolution (i.e., ideally supposing to afford a super fast clock), relying only on condition (1) would still be deceptive, since it would not be possible to understand if the converter is in steady state or experiencing a transient (e.g., the DC-DC converter may "just be passing inside" the SB and eventually settling outside). Now it should be clear that checking only a single condition would be misleading and not sufficient to faithfully infer about the power converter's behavior, especially during transients. To increase the detection speed and maximize the performance during the converter transients, the sampling-window is continuously reset (i.e., shifted ahead in time) until condition (1) is not satisfied. When condition (1) is satisfied, it means that the present F_{SKIP} is coarsely within - or close to - the SB and thus a fine check is necessary. Here the sampling-window is started, and condition (2) is checked after t_{SW}. In other words, the precise evaluation is done only at the end of a sampling-window during which the converter has been operating with F_{SKIP} coarsely within or close to the forbidden band. Automatically, any transient is filtered out, avoiding misleading assessments.

The proposed algorithm is implemented[2] within the SB digital controller described in Section II-A.

2) Flexible Corrective Action: When the controller recognizes that the converter operation is within a SB, it initiates a

[1]The presented solution can be applied in the same way in valley-current-mode-control.

[2]For both the outlined conditions, a margin accounting for the non-idealities (e.g., limited clock frequency accuracy) has been applied.

corrective action by raising the flag SB in Figure 1 to increase $COUNTER_{REF}$ value. The idea is to slightly change the "programmed" coil peak current (i.e., REF_{SKIP}) and thus alter the skip behavior of the converter (i.e., change M and/or K). Iteratively modifying the added offset voltage V_{OFFSET} by means of a simple digital-to-analog converter (DAC), REF_{SKIP} is slightly changed until the converter finally operates outside of the SB. To minimize any transient on V_{OUT} when REF_{SKIP} is varied, the very same offset generator is also added at the error amplifier (EA) output (V_{EA}), which allows the system to automatically maintain V_C close to REF_{SKIP}. Proceeding by iteration allows minimal effects on the PSM performance, as the converter's working point is adjusted only as much as needed to move outside of the forbidden band. Such added offset gets iteratively increased until the converter is pushed out from the pre-selected SB. Besides, $COUNTER_{REF}$ is allowed to roll over, meaning that when REF_{SKIP} reaches its maximum it goes back to the minimum. This feature is key for the system to exit any future steady state condition in which the power converter may again operate within a SB[3]. The idea to proceed by iteration stems from the overwhelming complexity in understanding if a new SB violation is due to a new operative condition or a previous insufficient corrective action. For the sake of clarity, Table II provides an example of how the offsets are iteratively managed.

TABLE II
EXEMPLARY ITERATION VS OFFSET APPLIED

Iteration #	$COUNTER_{REF}$	V_{OFFSET}
0 (default)	0	0
1	1	+25 mV
2	2	+50 mV
3	3	+75 mV
4	4	+100 mV
5	5	-25 mV
6	6	-50 mV
7	7	-75 mV
8	back to iteration 1	

Practically, the offset steps are sized to exit from any SB in any operating condition, with a limited number of iterations (e.g., 7 in our case).

It is worth noting that as long as V_{EA} remains within the EA allowed output dynamic range, the voltage shift introduced by the programmable offset is not relevant for the DC–DC converter itself. In fact, the integral action present in the DC-DC converter loop forces the required compensator output V_C to maintain a specified regulation setpoint by changing the duty-cycle[4].

[3]In general, in PSM F_{SKIP} depends on the operative conditions (i.e., V_{IN}, V_{OUT}, I_{LOAD}) and the DC-DC converter parameters (e.g., L, C_{OUT}, etc.).

[4]This is always valid, no matter the DC-DC operating mode (i.e., CCM, DCM, PSM/PFM).

B. Digital Controller

The proposed algorithm has been implemented exploiting two asynchronous-finite-state-machines (A-FSM) [17], digital counters and combinatorial logic. The first A-FSM, labeled $AFSM_1$, is in charge of understanding if the actual burst is within the pre-selected SB (i.e., check the first condition) providing the feedback OK_1 to the second A-FSM ($AFSM_2$). This feedback gets reset when the present burst is outside the SB (i.e., condition (1) not satisfied). In Figure 2 the state-flow describing $AFSM_1$ and some of the additional logic controlled by it are depicted. In each state the corresponding outputs (colored numbers) are shown, while each arc is activated only as soon as the condition associated with the arc is true [18]. A counter ($COUNTER1$), is used to keep track of how many $CLOCK_{AUX}$ periods (i.e., rising edges) occur in a $COMP_{SKIP}$ period (i.e., between two consecutive $COMP_{SKIP}$ rising edges). This counter is initially enabled by $AFSM_1$ at the beginning of a switching cycle (i.e., $COMP_{SKIP}$ rising edge) and remains enabled and counting until: i) the next switching cycle, or ii) there is no need to wait for the next switching cycle since condition (1) cannot be satisfied[5]. Precisely, at the next switching cycle (i.e., $COMP_{SKIP}$ rising edge) condition (1) is evaluated[6], and the flag OK_1 is set high. Until F_{SKIP} of the actual burst remains within the SB, this flag remains set (i.e., $AFSM_1$ follows the states 1-2-3), while it gets reset as soon as a burst with F_{SKIP} outside the SB occurs.

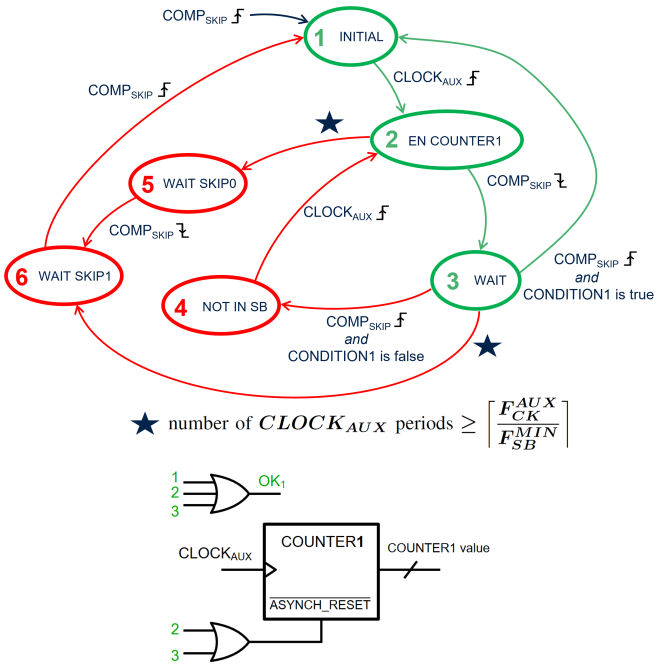

Fig. 2. State-flow describing $AFSM_1$ with some of the controlled logic.

[5]This is the case when the converter is operating with F_{SKIP} much below the SB.

[6]The combinatorial logic in charge of computing such evaluation, starting from the value of $COUNTER1$, is not shown.

The state-flow describing $AFSM_2$ is depicted in Figure 3. This state-machine is in charge of understanding: i) if within a sampling-window the number of $COMP_{SKIP}$ periods (i.e., $COMP_{SKIP}$ rising edges) falls within the SB (i.e., check the second condition), and ii) eventually decide if a corrective action is needed, outputting the flag SB = 1. To this end, $AFSM_2$ directly controls a burst counter ($COUNTER2$) that keeps track of how many $COMP_{SKIP}$ periods (i.e., rising edges) occur in a sampling-window lasting t_{SW}, while another counter clocked by $CLOCK_{AUX}$ is simply exploited as a timer for the sampling-window. Until $COMP_{SKIP}$ is 0, $AFSM_2$ remains in idle, looping in states 1 and 2. When $COMP_{SKIP}$ goes high (state 2), the timer and $COUNTER2$ are enabled to count. If the timer reaches its timeout, condition (2) is evaluated: if positive, the state-machine moves in state 3 setting SB = 1, otherwise, state 3 is reached and SB remains low. In both states 2 and 3 the timer and $COUNTER2$ are reset and the system is immediately ready for a new sampling-window. The presented behavior holds if the flag OK_1 remains set. In fact, in state 2 if the flag OK_1 goes to 0 there is no need to wait for the end of t_{SW} to understand if a corrective action is needed, since it is already acknowledged by $AFSM_1$ that the converter is performing outside the SB. The same applies if, before the timeout, the number of occurred $COMP_{SKIP}$ rising-edges goes above the maximum limit of $t_{SW}F_{SB}^{MAX}$.

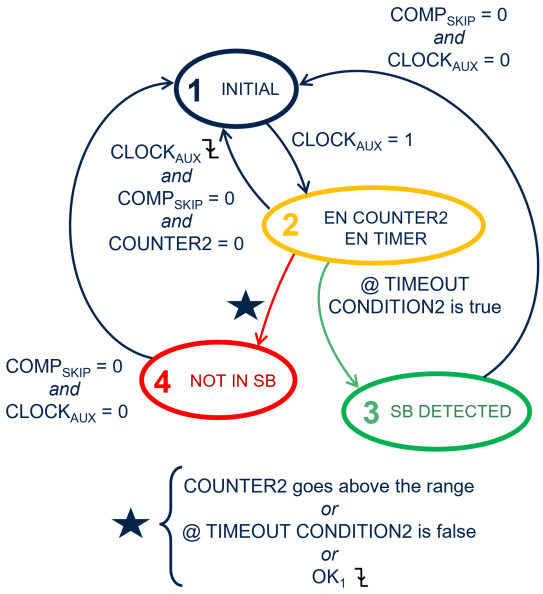

Fig. 3. State-flow describing $AFSM_2$.

To better understand the A-FSMs interactions, consider the following case in which the DC-DC converter is experiencing a transient (e.g., load, line, etc.). Depending on the perturbation's magnitude, F_{SKIP} changes typically over a wide range and finally settles at a given value. Even only a single burst that is recognized by $AFSM_1$ to be outside the SB is enough to promptly reset the sampling-window and the burst-counter (i.e., $COUNTER2$). In other words, $AFSM_1$ keeps shifting ahead the sampling-window until the actual F_{SKIP} is not coarsely within - or close to - the forbidden band. On the contrary, when $AFSM_1$ acknowledges that the actual F_{SKIP} is coarsely within the SB, the timer and $COUNTER1$ are enabled, since only at this point it is necessary to finely check if the averaged F_{SKIP} is within the SB. A filter rejecting the converter transients has been obtained, since the need to update the corrective action is evaluated only at the end of a steady state SW. When the SB is changed on-the-fly, both the state-machines are reset (i.e., back to their initial state).

C. Circuit Design

The proposed stop-band-management-system (SBMS) has been designed for a dual-phase inverting buck-boost (IBB) converter, which provides the negative supply rail (V_{OUT}) for the AMOLED display, from the Li-Ion battery (V_{IN}). This power converter has been designed within a custom power-management-integrated-circuit (PMIC) fabricated in a 180 nm BCD (bipolar-CMOS-DMOS) process. At light load, the IBB is operating only a single-phase (i.e., the second phase is disabled), and thus for the SBMS only the single-phase operation is relevant. An auxiliary clock with $F_{CK}^{AUX} = 3\,\text{MHz}$ has been exploited, since it is already available within the PMIC for other purposes, while the DC-DC converter is clocked at $F_S = 1.5\,\text{MHz}$ (i.e., $T_S = 666\,\text{ns}$). An open-loop-amplifier (OLA) Type-II compensator has been designed according to [19], while the clocked skip comparator is a P-type input StrongARM latch [20], [21]. As depicted in Figure 4, the digitally-controlled-offset-generators (DCOG) are implemented by means of a simple open-loop voltage buffer, made by a CMOS common drain stage [22] to decouple from the EA, followed by a programmable resistor (R_{OFFSET}) biased with a constant current I_{OFFSET}. Considering that this analog level-shifter retains the ability to only introduce programmable positive offsets, a baseline voltage is simply added to the values reported in Table II. As explained in Section II-A2, the absolute value of such baseline voltage is not relevant for the DC-DC converter, and neither for the SB corrective action.

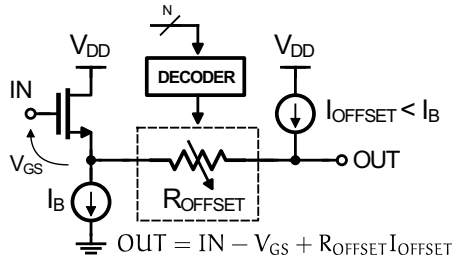

Fig. 4. Schematic of the digitally-controlled offset voltage generator.

D. Exemplary Simulation

In Figure 5 a simulation example shows the SBMS in action. The SB is programmed from 40 kHz to 60 kHz (top dashed black line boundaries) with a sampling-window of $t_{SW} = 0.5\,\text{ms}$. Initially, the SBMS is not enabled (EN = 0, second

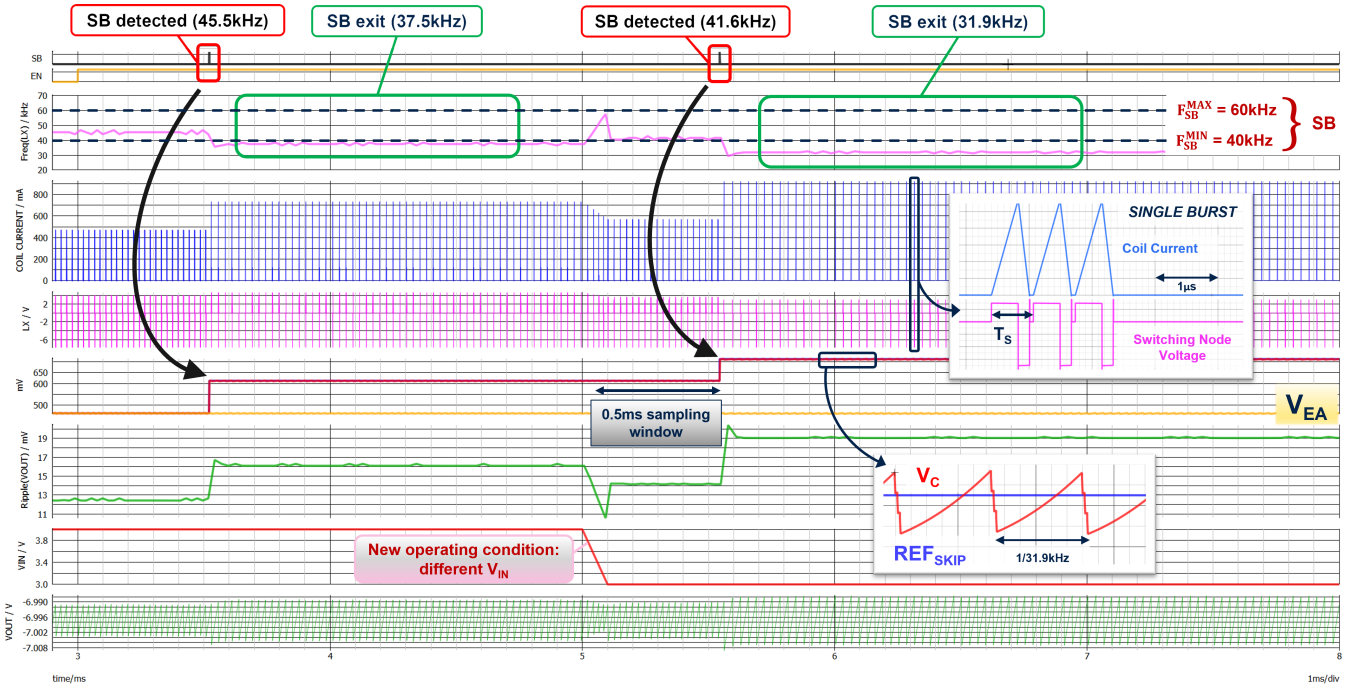

Fig. 5. Exemplary simulation of SBMS applied to an inverting buck-boost regulating $V_{OUT} = -7\,\text{V}$ in PSM with a load of $-6\,\text{mA}$: the SB is programmed from $40\,\text{kHz}$ to $60\,\text{kHz}$ ($t_{SW} = 0.5\,\text{ms}$).

waveform in yellow) and the IBB is steadily regulating V_{OUT} at $-7\,\text{V}$ (green bottom waveform) from $V_{IN} = 4\,\text{V}$ (red bottom waveform). With a load current of $-6\,\text{mA}$, the IBB is operating in PSM, as visible from the coil current (blue top waveform) and the switching node (magenta waveform in the middle), with F_{SKIP} around $45\,\text{kHz}$ (magenta top waveform). At $3\,\text{ms}$, the proposed solution is enabled (EN = 1), and after about $0.5\,\text{ms}$ (i.e., a sampling-window), it recognizes that a corrective action is needed (SB = 1 in the top black waveform). Consequently, REF_{SKIP} (blue waveform in the middle) is changed (increased in this case). This action proves effective in moving the IBB operation outside the SB, leading to $F_{SKIP} = 37.5\,\text{kHz}$. At $5\,\text{ms}$, a line transient occurs, which pushes back the IBB operation within the SB with $F_{SKIP} = 42.6\,\text{kHz}$. This is recognized by our solution (SB = 1) after $0.5\,\text{ms}$ of steady operation, and REF_{SKIP} is thus changed again. With this corrective action the IBB finally settles outside of the forbidden band, with $F_{SKIP} = 31.9\,\text{kHz}$ and the output voltage ripple is minimally affected (green waveform in the middle). Thanks to the replica V_{OFFSET} on the EA output, both V_{EA} (yellow waveform in the middle) and V_{OUT} do not experience any perturbation, guaranteeing the seamless specification.

III. Experimental Results

Figure 6 shows the die micrograph of the fabricated dual-phase IBB converter, with the SBMS key blocks highlighted in red. Considering the whole silicon area of the IBB controller (roughly $0.36\,\text{mm}^2$ for the single-phase), the SBMS area remains negligible (i.e., $\approx 6\,\%$). The dual-phase IBB converter is part of a PMIC for AMOLED power supply and is designed to regulate a programmed output voltage V_{OUT} in the range of -1 V down to -9 V, providing in single-phase up to -500 mA from an input supply V_{IN} varying between 2.2 V and 4.9 V. At light load the IBB operates in DCM/PSM, as exhibited from the oscilloscope capture of Figure 7. In this case, with $V_{IN} = 4.8\,\text{V}$ and an output load of -40 mA, V_{OUT} is regulated at -3 V with $F_{SKIP} \approx 73\,\text{kHz}$, and each burst is composed of 3 consecutive pulses.

Figure 8 showcases oscilloscope acquisitions of the IBB regulating in PSM with a programmed SB from $40\,\text{kHz}$ to $60\,\text{kHz}$ (V_{OUT} = -3 V, $V_{IN} = 4.3\,\text{V}$, I_{LOAD} = -6 mA). To

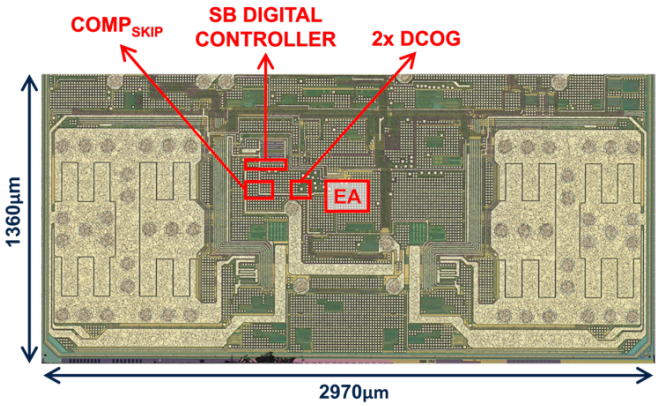

Fig. 6. Chip micrograph: dual-phase IBB with relevant SBMS blocks highlighted.

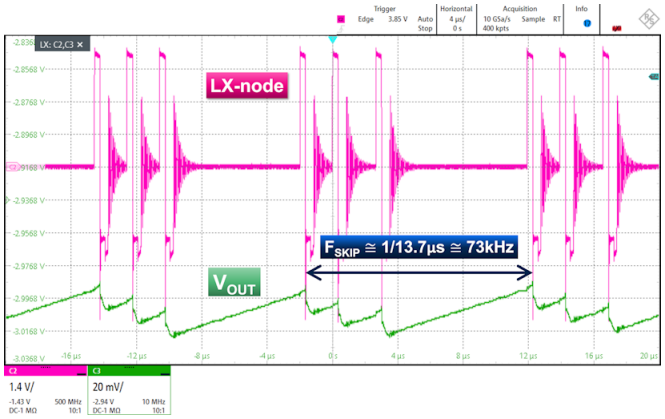

Fig. 7. Oscilloscope acquisition of the IBB operating in PSM at $F_{SKIP} \approx 73\,\text{kHz}$, with $V_{IN} = 4.8\,\text{V}$, $I_{LOAD} = -40\,\text{mA}$ and $V_{OUT} = -3\,\text{V}$ (green trace). The trigger is on the DC-DC converter switching node (magenta trace).

check the repetition period of the IBB burst (i.e., F_{SKIP}), the oscilloscope is triggered on the IBB switching node and set with display persistence of multiple acquisitions. The upper acquisition in Figure 8 shows that without enabling the proposed SBMS feature (EN = 0) the IBB is operating within the SB. On the contrary, with SBMS enabled (EN = 1) under the same IBB conditions, the absence of bursts around 1/50 kHz proves the effectiveness of our solution (bottom acquisition in Figure 8).

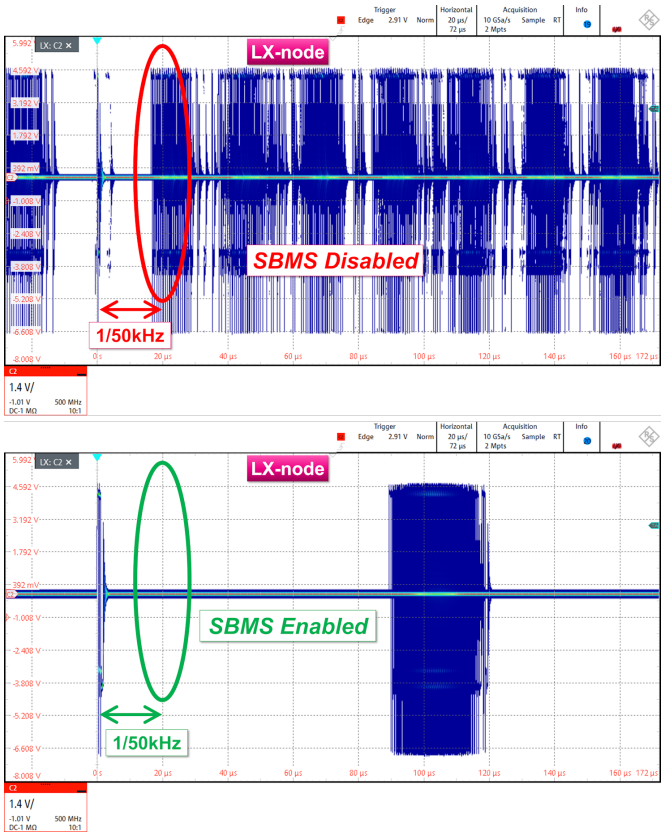

Fig. 8. Oscilloscope acquisitions of the IBB operating in PSM (trigger on the switching node): in the upper acquisition SBMS is disabled, while in the lower it is enabled with SB programmed from 40 kHz to 60 kHz.

To showcase how the proposed SBMS affects the power efficiency, in Figure 9 are presented two measured efficiency curves in the same operative conditions (i.e., $V_{IN} = 2.8\,\text{V}$, $V_{OUT} = -7\,\text{V}$, SBMS enabled and programmed SB from 40 kHz to 60 kHz). These measurements were performed on the very same sample by means of an automatic setup finely sweeping I_{LOAD}. During the first sweep-measurement (red trace) the SBMS applied a corrective action at about $-26\,\text{mA}$, as visible in the zoomed inset (visibile discontinuity). Immediately without resetting the PMIC, a second sweep-measurement (blue line) was performed. Here the SBMS did not trigger and from $-26\,\text{mA}$ the efficiency overlaps the trace from the previous sweep. In this case, at light load the efficiency variation is limited to 6 %.

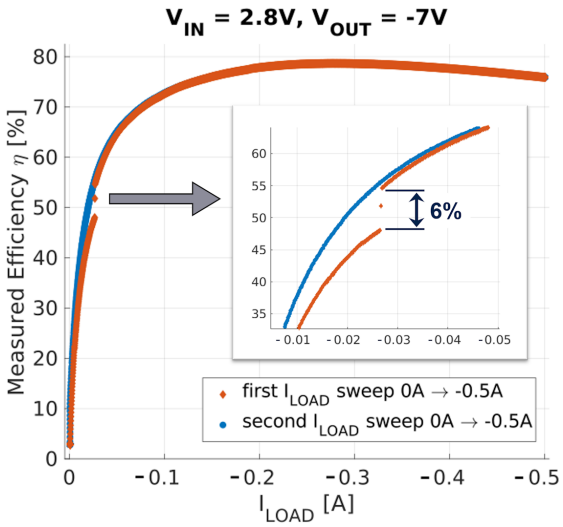

Fig. 9. Measured efficiency with $V_{IN} = 2.8\,\text{V}$ and $V_{OUT} = -7\,\text{V}$ when two automatic load-sweeps are performed consecutively: during the first sweep (red curve) at about $-26\,\text{mA}$ the SBMS apllies a corrective action.

IV. Conclusion

The presented solution proves effective in preventing the DC-DC converter from operating within forbidden frequency bands in DCM at light load. The switching activity of the converter is first oversampled, followed by a fine averaging within a sampling-window, which allows to finally understand if a programmed SB is violated. This dual-step check allows the oversampling operation to not require any high frequency clock signal, easing the implementation. An offset voltage changing the set DCM peak-current is applied as corrective action, in turn altering the converter switching activity. The application of the same offset voltage on the EA output allows to seamlessly maintain V_{OUT} unaffected, without any visible transient when a corrective action is exerted. Working in closed-loop, the obtained frequency-band-exclusion system is

robust against any process-voltage-temperature (PVT) variation, as well as operative conditions (e.g., V_{IN}, V_{OUT}, I_{LOAD}) and parameters (e.g., inductor, output capacitor, etc.). Thanks to its digital nature, there are no limitations on the number and range of SB, allowing maximum flexibility. The outlined algorithm properly filters out any transient that the power converter is experiencing, preventing any inappropriate and premature correction. Moreover, the iterative criteria allows to adapt the corrective action, minimally affecting the converter behavior and performance (e.g., output ripple, power efficiency). Furthermore, considering that the DCM peak-current value set by REF_{SKIP} is meaningless in CCM, the CCM stability and performance are not impacted by the SBMS. The presented SBMS is a digitally-assisted versatile add-on that can be applied to any DC-DC converter topology and light load operation mode (e.g., PFM and/or burst-mode). It has been designed and validated in a IBB converter providing a selectable output voltage in the range $-1\,\mathrm{V}$ to $-9\,\mathrm{V}$, fed from Li-Ion battery. This DC-DC converter is part of a PMIC for AMOLED display power supply, fabricated in a $0.18\mu m$ BCD technology.

REFERENCES

[1] F. Mao et al., "A hybrid single-inductor bipolar triple-output dc–dc converter with high-quality positive outputs for amoled displays," in *IEEE Trans. on Circ. and Sys. I*, vol. 70, no. 1, pp. 506–517, Jan. 2023.

[2] S. Forrset et al., "The dawn of organic electronics," in *IEEE Spectrum*, vol. 37, no. 8, pp. 2–34, 2000.

[3] M. K. Barwar et al., "Demystifying the Devices Behind the LED Light: LED Driver Circuits," in *IEEE Industrial Electronics Magazine*, vol. 17, no. 1, pp. 55–66, 2023.

[4] M. Kimura et al., "Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," in *IEEE Trans. on Elec. Dev.*, vol. 46, no. 12, pp. 2282–2288, 1999.

[5] Amir Besharati Rad et al., "An Ultra-Low-Noise Buck Converter for Noise-Sensitive Applications," in *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 2169–2178, February 2024.

[6] M. Alecci et al., "Noise Analysis in Voltage Mode Controlled DC-DC Converters," in *18th Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, June 2023.

[7] R. B. Ridley, "A New Small-Signal Model for Current-Mode Control," Ridley Engineering, Inc., 1999, https://ridleyengineering.com/education/books/books-current-mode-control.html.

[8] R. Erickson et al, Fundamentals of Power Electronics, 3nd ed., Springer, 2020.

[9] R. Sheehan et al., Switch-mode power converter compensation made easy, Sep. 2016.

[10] Wan-Rone Liou et al., "A High Efficiency Dual-Mode Buck Converter IC For Portable Applications," in *IEEE Trans. Power Electronics*, vol. 23, no. 2, pp. 667-677, March 2008.

[11] B. Sahue et al., "A high-efficiency, dual-mode, dynamic, buck-boost power supply IC for portable applications," in *18th International Conference on VLSI Design*, Jan. 2005.

[12] X. Zhou et al., "Improved lightload efficiency for synchronous rectifier voltage regulator module," in *IEEE Trans. Power Electronics*, vol. 15, no. 5, pp. 826-834, Sept. 2000.

[13] Alevoor et al, "A 95.2% Efficiency dc–dc Boost Converter Using Peak Current Fast Feedback Control (PFFC) for Improved Load Transient Response," in *IEEE Trans. Circuits Syst.—I*, vol. 70, no. 3, pp. 1097–1109, March 2023.

[14] Amir Besharati Rad et al., "A Wide-Input-/Output-Voltage-Range Buck Converter With Adaptive light load Efficiency Improvement and Seamless Mode Transition," in *IEEE Trans. on Power Elec.*, vol. 39, no. 2, pp. 2200–2212, February 2024.

[15] M. Zhao et al, "An Ultra-Low Quiescent Current Tri-Mode DC-DC Buck Converter With 92.1% Peak Efficiency for IoT Applications," in *IEEE Trans. Circuits Syst.—I*, vol. 69, no. 1, pp. 428–439, Jan. 2022.

[16] B. Yuan et al., "Hybrid Buck Converter With Constant Mode Changing Point and Smooth Mode Transition for High-Frequency Applications," in *IEEE Transactions on Industrial Electronics*, vol. 69, no. 1, pp. 1466–1474, February 2020.

[17] S. Dalle Feste et al., "A New Digital Flow for Automotive Robust Design of DC-DC Converters," in *AEIT International Conference of Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE)*, June 2019.

[18] R. Pellegrini et al., "A Seamless and Unified Flow for Robust Development of DC-DC Digital Controllers," in *18th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, June 2022.

[19] A. Bertolini et al., "Practical aspects for analog compensators design in integrated dc–dc converters," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 1, pp. 446–460, April 2024.

[20] B. Razavi, "The StrongARM latch [a circuit for all seasons]," in *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12-17, 2015.

[21] Abdullah Alshehri et al., "A 19 fJ/op, Low-Offset StrongARM Latch Comparator for Low-Power High-Speed Applications," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2024.

[22] B. Razavi, Design of Analog CMOS Integrated Circuits, 1st ed. McGraw-Hill Education, 2001, ch. Basic MOS Device Physics, pp. 21–36.