Multiphase Constant-On-Time Minimum-Deviation Controller for Modern Processors

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***Abstract*—In Voltage Regulator Module (VRM) applications, rapid dynamic load conditions often lead to significant output voltage deviation and negatively impact the dynamic efficiency of converters optimized for static efficiency. This paper proposes a novel multiphase Constant-On-Time Minimum Deviation (COT Min Dev) Controller to mitigate dynamic losses and reduce converter sizes. This marks the first application of a Minimum Deviation Controller in a multiphase system, validated on a 4-phase buck converter with a 12 V input and 1 V output, achieving a reduction in output voltage deviation from 280 mV to 80 mV during a 10 A - 90 A load step. Additionally, it was validated on a 3-level 4-phase buck converter prototype, where the output voltage deviation was reduced from 280 mV to 125 mV for the same load step, with input voltage initial drop eliminated. The experimental results demonstrate effective phase balancing, enhanced transient performance, and a reduction in converter size.**

***Index Terms*—Minimum Deviation Controller, flying capacitor, multilevel multiphase converter, Voltage Regulator Module (VRM)**

I. Introduction

The Constant-On-Time (COT) Controller [1]–[4] is one of the most popular controllers for modern Voltage Regulator Modules (VRMs). However, it has been increasingly challenged by the more rapidly fluctuating workloads, particularly in Graphics Processing Unit (GPU) applications. These rapidly changing conditions necessitate faster controllers to prevent large output voltage deviations, which negatively impact efficiency and stability.

The Minimum Deviation Controller [5], known for minimizing output voltage deviation by detecting both the rising and falling zero-crossing points of the output capacitor current and extending operation for D/2 and D'/2, has so far only been applied in single-phase applications. A direct implementation of the Minimum Deviation Controller in multiphase applications leads to phase balancing issues. Without effective phase sharing, certain phases may face a risk of reaching the inductor saturation point. At this point, the Minimum Deviation Controller becomes ineffective, resulting in reduced efficiency and potential instability.

To solve this problem, this paper introduces a novel multiphase Constant-On-Time Minimum Deviation (COT Min Dev) Controller. This controller is well-suited for conventional multiphase buck converters (Fig. 1), providing effective phase balancing, reducing output capacitor size, and improving dynamic efficiency, thereby achieving a lower environmental impact compared to a traditional Constant-On-Time (COT) controller [6].

Furthermore, the controller is adapted for use in multilevel multiphase buck converters (Fig. 9) [7], leveraging the growing interest in flying capacitor topologies [8]–[15]. This faster multiphase controller enables the reduction of both input bulk capacitor size and output capacitor size while minimizing dynamic losses.

II. Constant-On-Time Minimum Deviation for Multiphase Buck Converter

A. Open Loop Operation Of 4-phase Buck Converter

A conventional 4-phase buck converter was selected for this study due to its compatibility with the power requirements of our industry partner's product. Fig. 2 illustrates the open-loop operation of a conventional 4-phase buck converter. During the off time, all synchronous rectifiers conduct (state I in Fig. 1). During the on time, phases are turned on in sequential order and only one conducts at the time (state A-D in Fig. 1). The on time and off time are determined by the switching frequency and duty ratio just like the single-phase buck converter.

B. Phase Balancing Issue

A straight approach to implementing the Multiphase Minimum Deviation Controller would be to detect the rising and falling Zero-Crossing (ZC) points of the output capacitor current i_C and extend the operation for $D/2$ and $D'/2$ respectively, where D' is $1 - D$, as it is done in a single phase implementation [16]. Instead of firing all pulses with one phase, the operation rotates among the 4 phases. Note that the peaks in the i_C waveform come from different phases. However, this approach leads to phase balancing issues during both steady-state and transient operations.

During steady-state operation, phase balancing issues arise due to variations in PCB trace lengths from the output of each phase to the i_C sensing point, leading to differing delays in the i_C waveform peaks. This discrepancy results in unequal on-times across the phases. As illustrated in Fig. 3, phases 1 and 3 are located further from the i_C sensing point to accommodate the footprint of the 2-phase coupled inductors. This leads to

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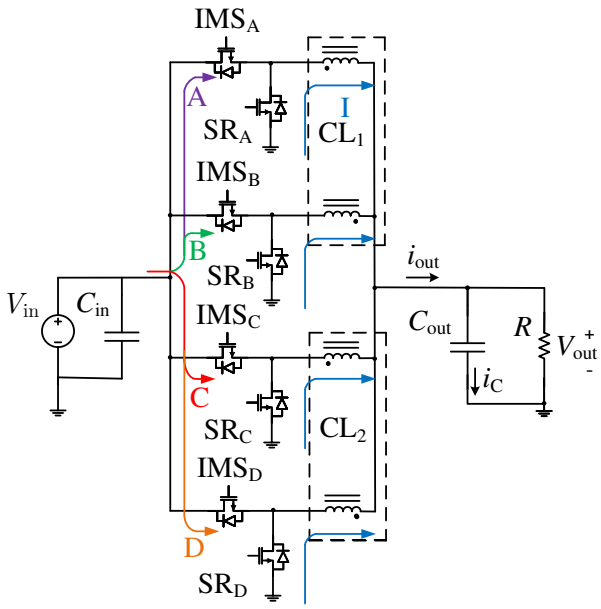

Fig. 1. Current flow diagram illustrating four on-time states (A–D), during which the total inductor current rises sequentially, and the off-time state (I), during which all synchronous rectifiers conduct. In each on-time state, only one phase is active, and one of the four states occurs after the off-time in a rotational manner. For simplicity, the input wire resistance and inductance are not shown here.

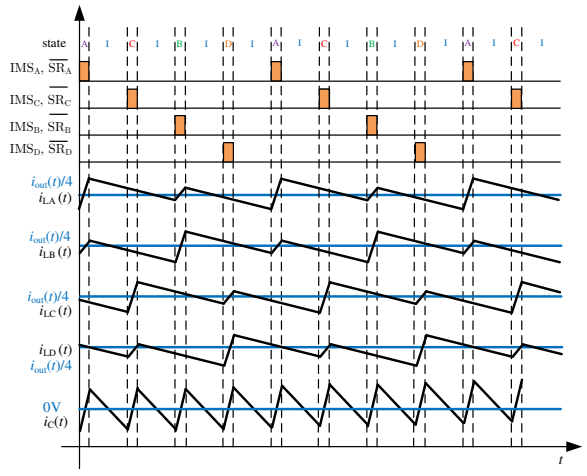

Fig. 2. Gating signals of converter with associated inductor current for each phase and total inductor current.

longer delays in their peaks, which causes longer on-times and higher currents compared to phases 2 and 4 (Fig. 4). The current balancing issue also occurs during transient response. When a transient event occurs, all 4 phases are turned on. However, when the total current of all phases reaches the new load value, the phases at that point have different values, leading to imbalanced current distribution. The experiment was conducted with an effective switching frequency of 1 MHz (a per-phase switching frequency of 250 kHz). While the severity of the phase balancing problem may be reduced with lower switching frequencies or an optimized PCB layout, it is unavoidable when employing a straightforward implementation approach.

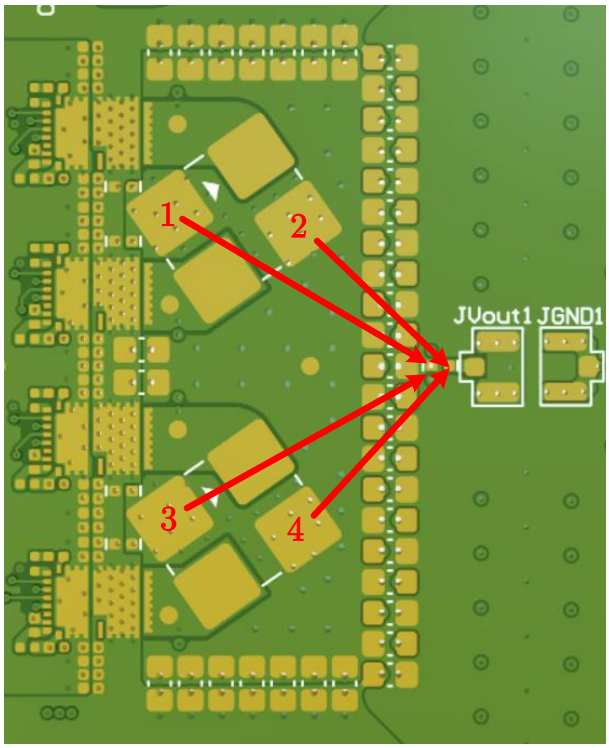

Fig. 3. PCB layout of the 4-phase buck converter with 2-phase coupled inductors. The couple inductor footprints were placed in a diagonal way, resulting in differences in distances from each phase to the differentiator sense point (labeled JVout1).

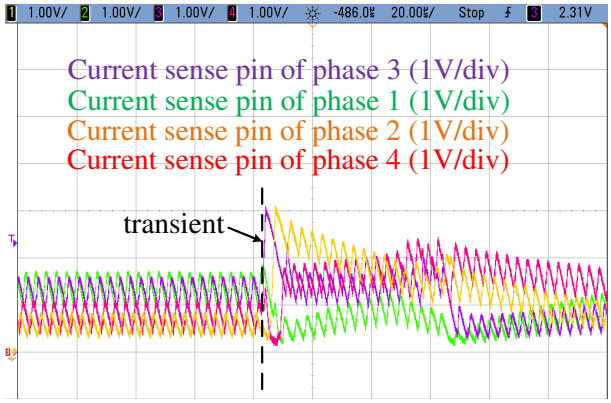

Fig. 4. Current sense pins of all phases of 4-phase buck converter with the straight implementation of Multiphase Minimum Deviation Controller at 10 - 50 A, 1/8 duty, 600 Hz load.

C. Principle of Operation

To address the phase balancing issues, the COT Min Dev Controller was introduced. During the on-time, the controller functions as a COT Controller, by issuing the same on-time

duration (D) for each phase (Fig. 6). During the off-time, it operates as a Minimum Deviation Controller, extending the duration for $D'/2$ after detecting the falling zero-crossing point on the output capacitor current i_C. By doing this, the controller utilizes information about the inductor current, to improve transient performance while ensuring phase balancing. Even when the zero-crossing points of each phase experience different delays due to PCB trace length variations, the controller ensures that, over a complete switching cycle, each phase has the same total on-time. Consequently, all phases contribute an equal amount of current to the load, maintaining balanced operation. During transients, the controller also provides stability, effective phase balancing, and improved performance (Fig. 5).

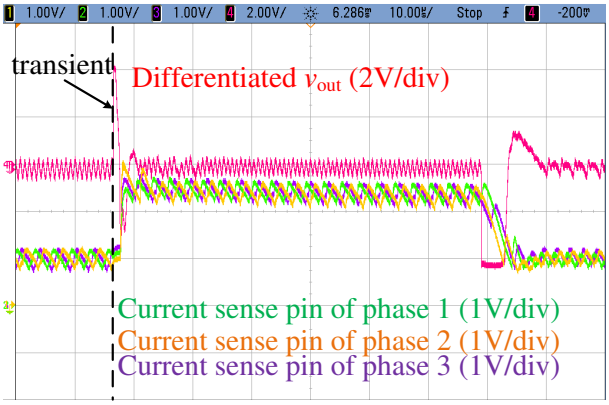

Fig. 5. Current sense pin of phase 1 (green), phase 2 (yellow), phase 3 (purple) and differentiated v_{out} (red) of 4-phase buck converter with COT Min Dev Controller at 10 - 150 A, 1/8 duty, 2 kHz load.

This method combines the best features of both Constant-On-Time and Minimum Deviation Controllers, operating with variable frequency. The upper frequency is bounded by the width of the constant-on-time pulses, while a maximum off-time counter limits the lower frequency. If the falling zero-crossing point is not detected within the maximum off-time duration, the controller progresses to the next state, the off-time second half (Fig. 8), ensuring continuous operation. During the off-time second half state, the zero-crossing signal should remain high. If it becomes low unexpectedly, the state reverts to the off-time first half. Once the zero-crossing signal is high again, the controller re-enters the off-time second half state, thereby maintaining continuous operation. This implementation has lower hardware requirements, compared to the approach of per-phase current sensing.

Transient is detected when i_c experience sudden drops and becomes lower than a valley value (Fig. 6). The valley value is typically set in the range of 3 to 5 times the i_c ripple. During transient, all 4 phases will be turned on, ensuring the fastest recovery rate. After the transient, a stored counter value is used to ensure that the phase interrupted by the transient will continue to finish the remaining time $(D - t_1)$ after transient. Therefore, the phase balancing is maintained even after transient.

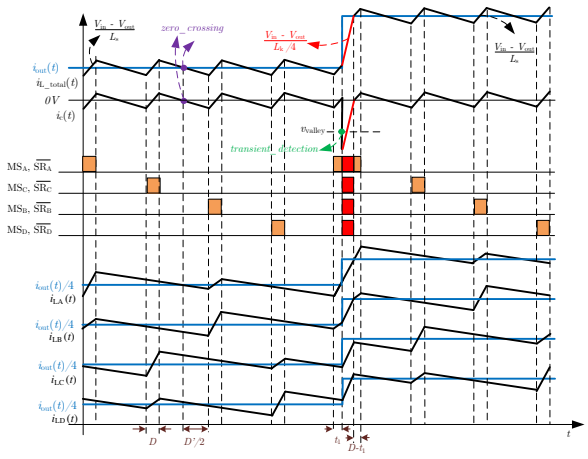

Fig. 6. Gating signals of the 4-phase converter during a light-to-heavy load step, illustrating the transient detection process and associated inductor currents for each phase, total inductor current and differentiated output voltage.

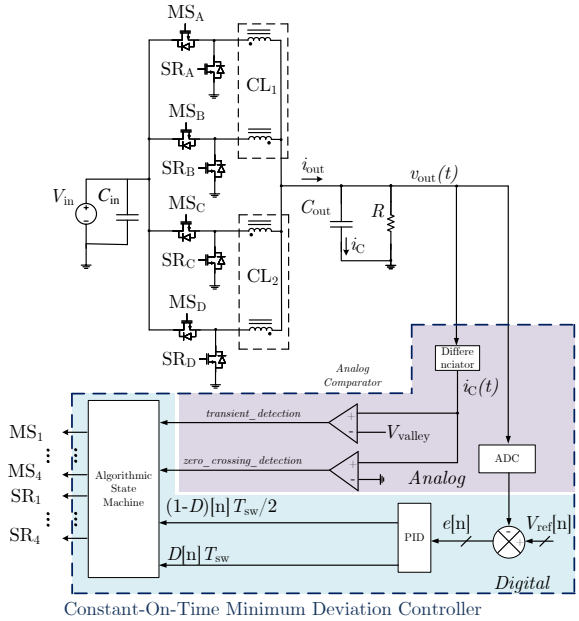

Fig. 7. Diagram of 4-phase buck converter and the implementation of its complementary COT Min Dev Controller.

The controller consists of both digital and analog circuits (Fig. 7). The analog circuits are employed for fast zero-crossing and transient detection, utilizing information from the output capacitor current (i_c). The output capacitor current is derived by differentiating the output voltage (v_{out}).

The digital logic is responsible for implementing the PID compensator to adjust the duty cycle D and generating the gating signals required for the converter's operation.

D. Couple Inductor

This controller can also benefit from the use of coupled inductors. When one of the phases is on (connected to V_{in}),

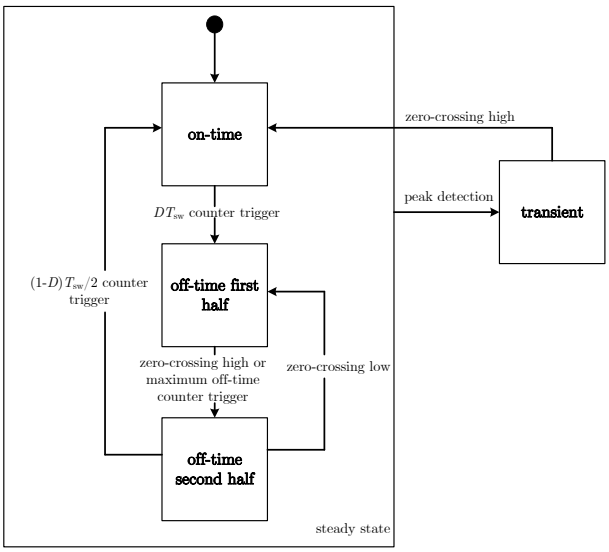

Fig. 8. The Algorithmic State Machine of the COT Min Dev Controller shown in Fig.7.

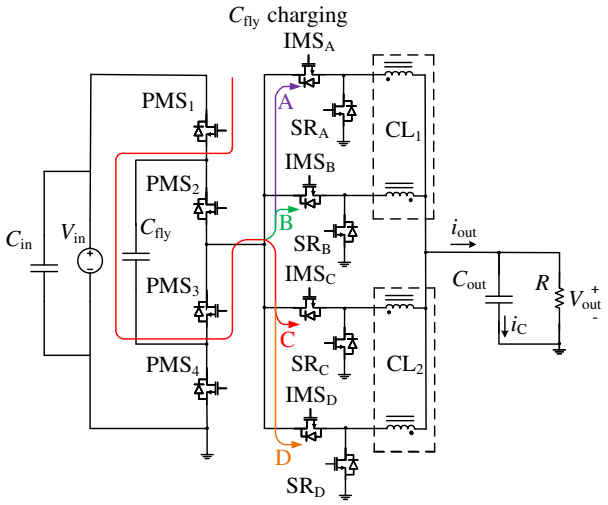

Fig. 9. Current flow diagram for 3-level 4-phase buck converter, with four different on-time states during the C_{fly} charging period. In each state, only one phase is active.

the other phases are off (connected to ground). The effective inductance is L_s, which is the sum of $L_m + L_k$, where L_s is the self inductance, L_m is the magnetizing inductance, and L_k is the leakage inductance. The phases that are off will experience a rise as well due to the negative coupling. This mechanism reduces current ripple and inductor volume during steady state. During transient, all 4 phases are turned on. If discrete inductors are used, the effective inductance becomes $L/4$ instead of L. In a coupled inductor configuration, when all phases are turned on, the mutual inductance L_m is effectively eliminated because the magnetic fields generated by each phase in the coupled inductor structure support each other. Instead of opposing each other (as in steady state with alternate phases on and off), they combine constructively. Therefore, effective inductance becomes $L_k/4$ instead of $L_s/4$ (L_m is eliminated), further increasing slew rate and, therefore, the speed of voltage recovery.

III. Constant-On-Time Minimum Deviation for Multilevel Multiphase Buck Converter

A. Open Loop Operation Of 3-level 4-phase Buck Converter

In the realm of power delivery for high-performance applications, the implementation of three-level multiphase buck converters has proven to be an important advancement [7]. Central to this topology is the inclusion of a Flying Capacitor (C_{fly}), nominally rated at 6V. This critical component effectively halves the switch node voltage swing from 12V to 6V, thereby reducing the voltage stress on the components, enhancing the overall efficiency of the system.

During start-up, the flying capacitor (Fig. 9) is charged to a voltage of 6 V. This operation ensures that the downstream buck converters receive an input voltage of 6 V. The mechanism of operation for these downstream buck stages closely mirrors that of a conventional buck converter, wherein the Intermediate Main Switches (IMS) and the Synchronous Rectifier (SR) are sequentially activated based on the predetermined duty ratio.

Fig. 11 shows how the three-level multiphase buck converter operates: the cycle begins with the charging state of the flying capacitor (C_{fly}) (Fig. 9). In this stage, every downstream buck converter sees 6 V at the phase node, and functions in a sequential manner, adjusting its SR and IMS according to their respective duty cycles. After 5 cycles, the system enters the C_{fly} discharging state where the 12 V input is disconnected and C_{fly} provides 6 V directly to the buck converters (Fig. 10). Each phase continues to operate in turns. After another 5 cycles, the system reverts to the charging state, reconnecting the 12 V input to recharge C_{fly} to 6 V, and the cycle restarts. Natural phase balancing can be achieved if the Primary Main Switch (PMS) operates at a frequency that is an odd fraction of the switching frequency of the downstream buck converters. This operating scheme also ensures natural voltage balancing at the flying capacitor. Additionally, the PMS employs Zero Current Switching (ZCS) to minimize switching losses.

During the off-time, all Synchronous Rectifiers (SRs) conduct similarly to their operation in a 4-phase buck converter (state I in Fig. 1), allowing the inductor current to decrease.

B. Principle of Operation

The novel COT Min Dev Controller adapted well to this 3-level topology. In steady state, the downstream IMS and SR function similarly to the conventional 4-phase buck converter described, utilizing the falling zero-crossing detection and COT pulses. The key difference lies in the flying capacitor C_{fly}, which is switched at 1/10 of the IMS frequency.

During transients, the behavior of the lower stream IMS mirrors that of multiphase converters (Fig. 12), with all four phases turning on simultaneously until the inductor current reaches the zero-crossing point, leveraging the advantages

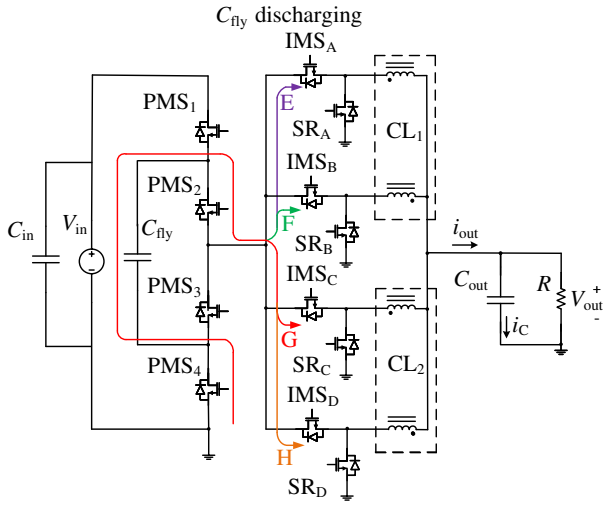

Fig. 10. Current flow diagram for 3-level 4-phase buck converter, with four different on-time states during the C_{fly} discharging period.

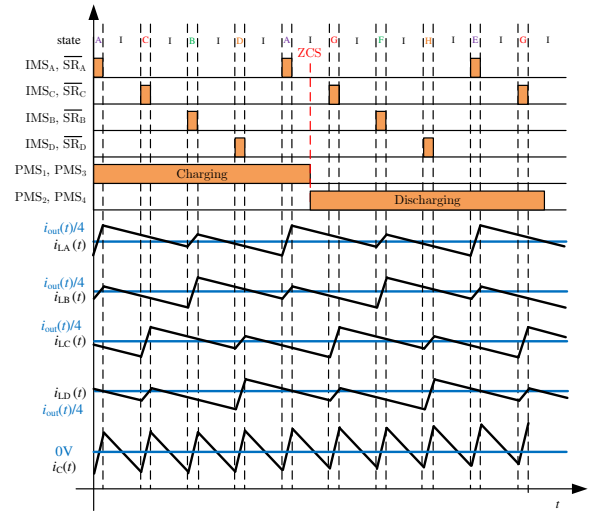

Fig. 11. Gating signals of 3-level 4-phase converter and associated inductor current for each phase and total inductor current [7].

of coupled inductors. For the PMS, each transient initiates the start of a discharging period, causing C_{fly} to experience a voltage deviation. This mechanism effectively decouples the input capacitor from the load during transients, thereby reducing the required input capacitor size.

This approach is preferred because there are regulations for V_{out} and V_{in} deviation but not for V_{cfly} deviation. Conventionally, for consumer GPU applications, input capacitors account for the majority of the total volume in the converter. This is essential to prevent significant input voltage drops during transients, which could lead to power supplies shutting down.

This method works also thanks to the inductor, when inductors are connected to the flying capacitor, there is no non-adiabatic charging loss. This innovative strategy of utilizing

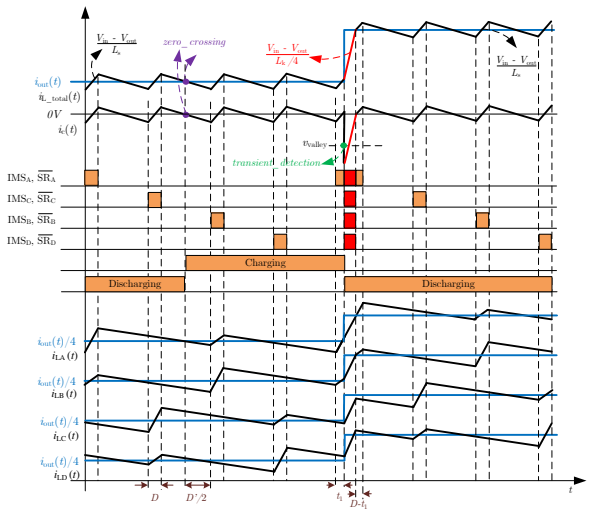

Fig. 12. Gating signals of 3-level 4-phase converter during a light-to-heavy load step with associated inductor current for each phase, total current ripple and differentiated output voltage.

C_{fly} to reduce the reliance on input bulk capacitors during transients is first presented in this paper.

The primary drawback of this approach is that the output capacitor needs to be doubled, as the slew rate is halved compared to connecting the phase node to the 12 V input, a method known as the C_{fly} bypass technique. However, the use of the COT Min Dev Controller mitigates this by enabling a faster transient response and reducing the overall output capacitance requirement.

The controller implementation for 3-level 4-phase buck converter is very similar to one for conventional multiphase buck converter, except that the additional combinational logic for PMS (Fig. 13).

IV. Experimental Results

A. Constant-On-Time Minimum Deviation Controller for Multiphase Converters

The concept is verified with a 3-level 4-phase buck converter prototype with 8 layers (Fig. 14), list of main components is shown in Table I. For experiments conducted on the 4-phase buck converter, PMS1 and PMS2 are turned on, while PMS3 and PMS4 are turned off.

The transient behavior of the COT Min Dev Controller is compared with the conventional COT Controller on the 4-phase buck converter, using identical output capacitors (9× 47 µF and 2× 22 µF). The output voltage deviation is significantly reduced, from 280 mV to 80 mV, for a 10 A - 90 A load step when using the COT Min Dev Controller (Fig. 15 and Fig. 16). It is important to note that during transient events, the COT Min Dev Controller turns on all phases simultaneously to maximize the transient response rate.

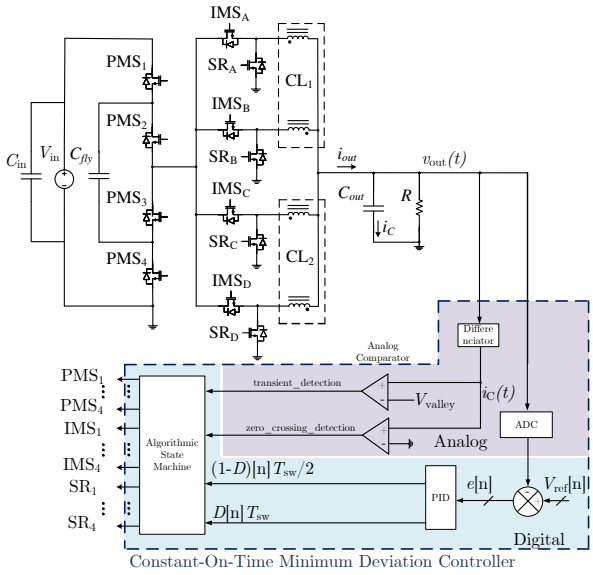

Fig. 13. Diagram of 3-level 4-phase buck converter and its complementary COT Min Dev Controller. For simplicity, the input wire resistance and inductance are not shown here.

TABLE I
LIST OF MAIN COMPONENTS USED IN THE EXPERIMENTAL PROTOTYPE

Component	Quantity & Main Parameters
Inductor	Intel's internal part (120 nH, 80 A)
Flying Capacitor	31x 22 µF / 16 V
Output Capacitor	9x 47 µF / 6.3 V, 4x 22 µF / 4 V
Input Capacitor	21x 1 µF / 16 V, 4x 560 µF / 16 V
Switches	4x MPS MP87006 (IMS) 4x BSZ031NE2LS5ATMA1 (PMS1) 5x BSZ031NE2LS5ATMA1 (PMS3) 5x IQE006NE2LM5 (PMS2) 4x IQE006NE2LM5 (PMS4)
Gate Drivers	4x LTC4440

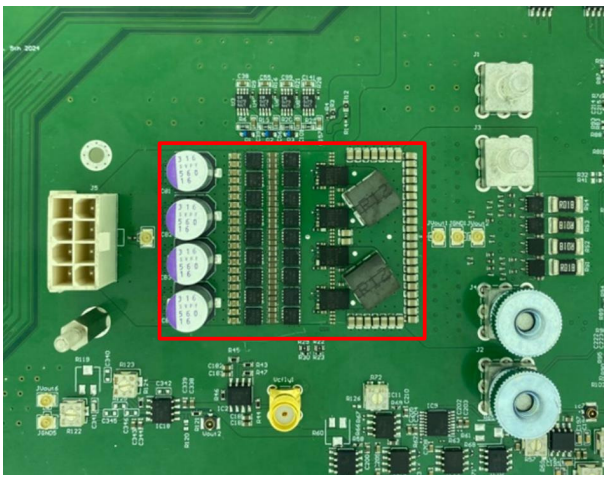

Fig. 14. Photo of assembled PCB of the 3-level 4-phase converters. The converter part (in red square) is 54 mm × 38 mm.

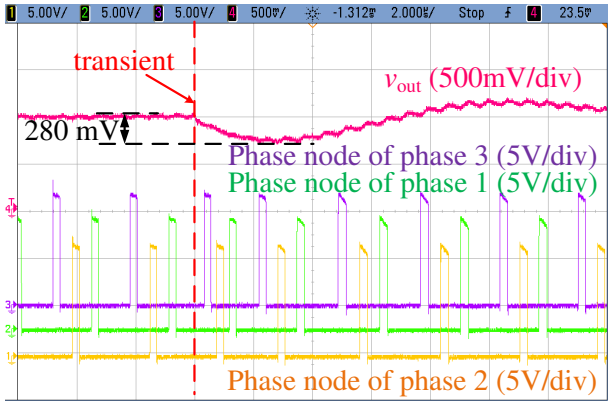

Fig. 15. Experimental output voltage deviation for load step 10 A - 90 A for 12 V - 1 V 4 phase buck converter with conventional COT Controller. Effective switching frequency is 1.7 MHz. Per-phase switching frequency is 417 kHz.

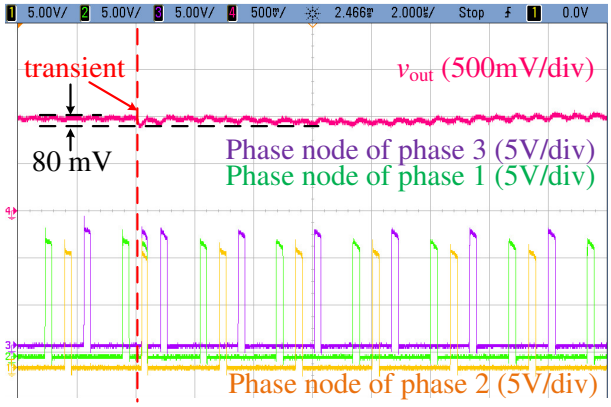

Fig. 16. Experimental output voltage deviation for load step 10 A - 90 A for 12 V - 1 V 4 phase buck converter with COT Min Dev Controller. Effective switching frequency is 1.7 MHz. Per-phase switching frequency is 417 kHz.

B. Constant-On-Time Minimum Deviation Controller for Multilevel Multiphase Converters

Fig. 17 and Fig. 18 illustrate the differences in input voltage drops during transient events occurring in the C_{fly} charging state and discharging states. A high D_0 signal indicates a charging period, while a low D_0 signal indicates a discharging period. It is observed that there is no instantaneous voltage drop at the input capacitor (C_{in}) if a transient occurs during the discharging period (Fig. 18). However, there is a larger input voltage ripple when the flying capacitor is connected to the input again in the subsequent charging period.

After a transient during a discharging period, it is observed that v_{cfly} drops below its nominal value of 6 V (Fig. 18). In the subsequent charging period, a higher voltage is seen at the phase node, allowing more charges to flow into the flying capacitor. As a result, v_{cfly} gradually rises back to its nominal value through a process known as the natural voltage balancing of C_{fly}.

Output voltage deviation is also compared between the conventional COT Controller and the COT Min Dev Controller

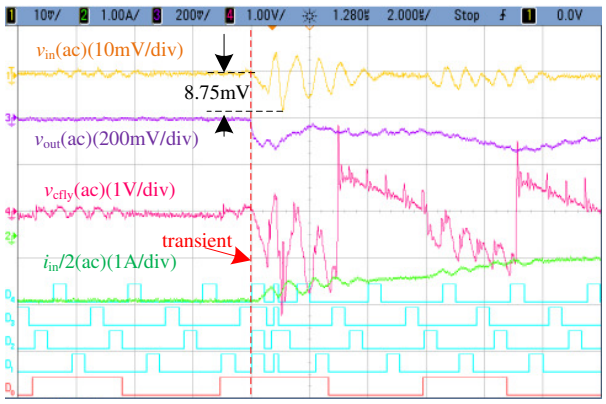

Fig. 17. Experimental v_{in}(ac), v_{cfly}(ac), v_{out}(ac), $i_{in}/2$(ac), IMS_A-IMS_D gating signals (D_1-D_4) and PMS_1 gating signal (D_0), of a 3-level 4-phase buck converter with the COT Min Dev Controller at 10 A - 160 A load step. Transient occurs in C_{fly} charging period. Please note that v_{out} will recover to the nominal voltage over time because it takes time for the PID compensator to adjust the duty ratio in response to the heavy load.

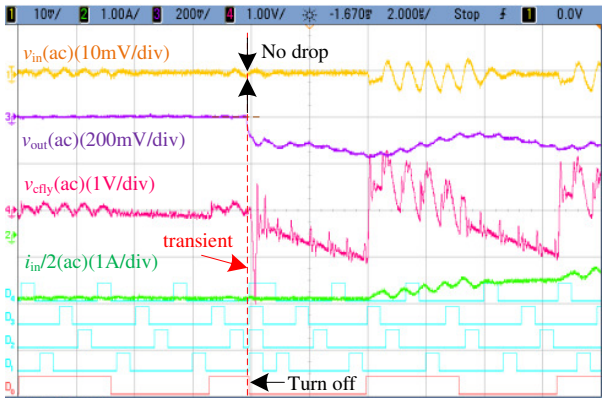

Fig. 18. Experimental v_{in}(ac), v_{cfly}(ac), v_{out}(ac), $i_{in}/2$(ac), IMS_A-IMS_D gating signals (D_1-D_4) and PMS_1 gating signal (D_0), of a 3-level 4-phase buck converter with the COT Min Dev Controller at 10 A - 160 A load step. Transient occurs in C_{fly} discharging period. Please note that v_{out} will recover to the nominal voltage over time because it takes time for the PID compensator to adjust the duty ratio in response to the heavy load.

on the 3-level 4-phase buck converter (Fig. 19 and Fig. 20). It is observed that the output voltage deviation is drastically reduced from 280 mV to 125 mV.

C. Volume Reduction

For 4-phase buck converters, experiments show that reducing an additional 200 mV of output voltage deviation requires increasing the output capacitance by a factor of at least five. This adjustment alters the overall volume and area distribution of the converter (Fig. 21 and Fig. 22), assuming the same output voltage deviation. The conventional buck converter used for comparison is based on an existing industry design provided by our industry partner. It is important to note that two extremes exist in this design space: one where the output capacitance remains constant to achieve smaller voltage deviation, and another, where the voltage deviation remains

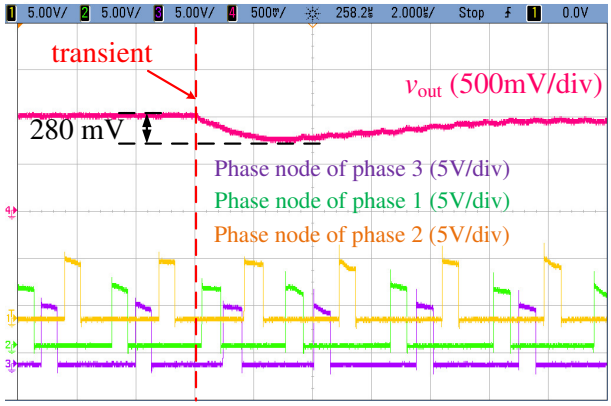

Fig. 19. Experimental output voltage deviation for load step 10 A - 90 A for 12 V - 1 V 3-level 4-phase buck converter with conventional COT Controller. Effective switching frequency is 1.7 MHz. Per-phase switching frequency is 417 kHz.

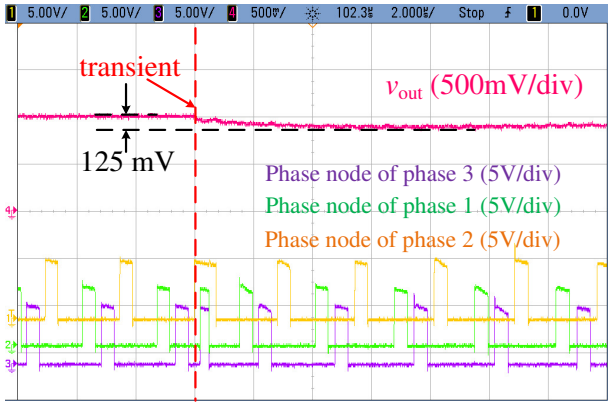

Fig. 20. Experimental output voltage deviation for load step 10 A - 90 A for 12 V - 1 V 3-level 4-phase buck converter with COT Min Dev Controller. Effective switching frequency is 1.7 MHz. Per-phase switching frequency is 417 kHz. Please note that v_{out} will recover to the nominal voltage over time because it takes time for the PID compensator to adjust the duty ratio in response to the heavy load.

constant to achieve a smaller output capacitance. In practice, a balance between these trade-offs can be selected [17].

For 3-level 4-phase buck converters with COT Min Dev Controller, the volume reduction is even more pronounced compared to conventional 4-phase buck converter with COT Controller. When comparing the required capacitance for a COT controller to achieve the same output voltage deviation, the output capacitor size can be reduced approximately to 1/5 of the original. However, with the flying capacitor discharging state in the 3-level topology, the slew rate is reduced by half during transient. This results in an output voltage deviation of 125 mV for the 3-level topology, nearly doubling the 80 mV seen in the 2-level topology. Consequently, the output capacitor needs to be doubled compared to the 2-level case, meaning it can only be reduced to 2/5 of the original size, given the same deviation.

On the other hand, the input capacitor can be reduced by half because the input voltage initial drop during transients

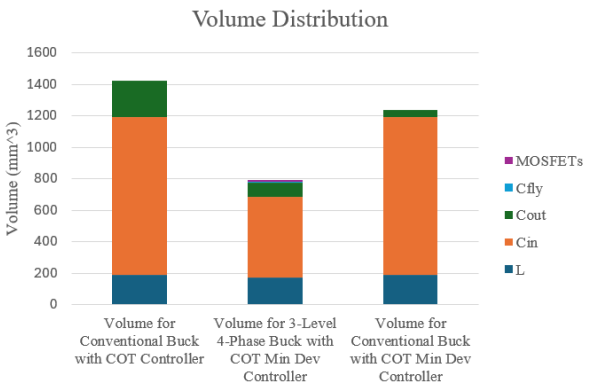

Fig. 21. Converter volume distribution of 4-phase buck converter with conventional COT Controller, 3-level 4-phase buck converter with COT Min Dev Controller and 4-phase buck converter with COT Min Dev Controller.

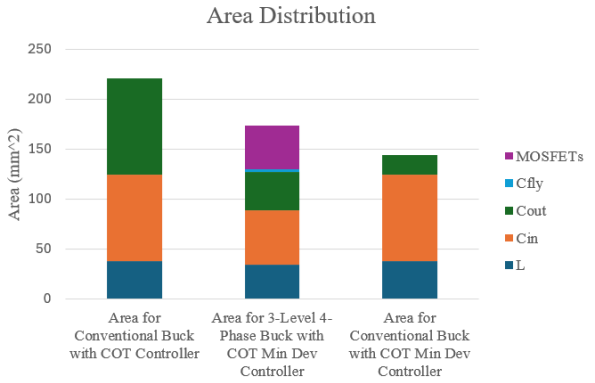

Fig. 22. Converter area distribution of 4-phase buck converter with conventional COT Controller, 3-level 4-phase buck converter with COT Min Dev Controller and 4-phase buck converter with COT Min Dev Controller. Note that the MOSFET area shown includes the packaging size of the discrete MOSFETs, not just the silicon area.

is eliminated. However, half of the input capacitance is still required because the input voltage experiences greater ripple during the subsequent charging state.

For the 3-level converter, reducing the phase node voltage from 12V to 6V allows the inductor value to be reduced to 10/11 of its original value, even with a larger duty ratio.

This 3-level topology, combined with the COT Min Dev Controller, enables significant reductions in overall size, even considering the additional MOSFETs and flying capacitors.

V. Conclusion

In conclusion, this paper presents a novel multiphase Constant-On-Time Minimum Deviation Controller. Previous Min Dev Controllers were limited to single-phase applications. The unique transient techniques of the controller successfully minimized v_{out} deviation, resulting C_{out} reduction. The implementation on the COT Min Dev Controller with the 3-level topology eliminates initial v_{in} drop during transients and significantly reduces input capacitor size. Furthermore, the versatility of this controller allows for broader applications across systems with any number of phases. In configurations exceeding 6 phases for a 3-level topology, or 12 phases for a 2-level topology, the overlap of Pulse Width Modulation (PWM) signals may interfere with zero-crossing detection of the output capacitor current. In such cases, phase synchronization can be employed as a potential solution.

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