Mixed-Signal Sliding Mode Controller for Non-Inverting Buck-Boost Photovoltaic DC Optimizers

Anurag Singh, Sayan Paul, Dragan Maksimović and Luca Corradini
Department of Electrical, Computer and Energy Engineering
University of Colorado, Boulder, CO 80309
Email: {anurag.singh-1, sayan.paul, maksimov, luca.corradini}@colorado.edu

***Abstract*—Photovoltaic (PV) dc optimizers require input voltage regulation over a wide range to maximize power extracted from PV panels. As such, seamless reference tracking and robust stability are required under all operating conditions. This work introduces a mixed-signal sliding mode controller for non-inverting Buck-Boost (NIBB) dc optimizers to address these challenges. The controller, implemented around a low-cost DSP platform, achieves seamless reference tracking in pass-through mode – where the input voltage is close to the output voltage – while retaining the reduced inductor and switch current stresses typical of multi-mode NIBB modulations. Design guidelines for the implementation are outlined, and experimental results validate the effectiveness of the proposed controller on a 600 W NIBB converter.**

***Index Terms*—sliding mode control, dc optimizers**

I. Introduction

In residential photovoltaic (PV) systems, PV panels can be interfaced with a grid-tied inverter through series-stacked *dc optimizers* [1], [2], as shown in Fig. 1. Each dc optimizer performs Maximum Power Point Tracking (MPPT) by varying the voltage at the PV panel terminals. The input voltage V_g of the optimizer varies over an extensive range depending on the panel's irradiance, operating temperature, and conditions such as partial shading, while the inverter regulates the dc bus voltage. The non-inverting Buck-Boost (NIBB) converter, with its topological versatility and capability for step-up and step-down operation, is often used to implement dc optimizers.

Due to the practical limitations of pulse width modulators, multi-mode controllers for NIBB topologies invariably face challenges around the so-called *pass-through region* when the conversion ratio $M = V_o/V_g$ is close to 1. This typically leads to pulse skipping, chattering of controlled state variables, and potential instability [3]–[7]. This work proposes a *Mixed-Signal Sliding Mode Controller* (MS-SMC) capable of achieving smooth operation around the pass-through region while retaining the advantages of the reduced inductor and switch current stress commonly seen in multi-mode NIBB modulations. The controller architecture, depicted in Fig. 2, is constructed around the mixed-signal resources of a low-cost commercial DSP platform [8]. A fast, analog-based, but digitally programmable sliding mode control layer implements the cycle-by-cycle control of the NIBB. Here, the sliding surface function $\sigma(t)$ is analog-compared to generate the basic switching events for the converter, while a fast digital logic implemented using the platform's Configurable Logic Block (CLB) provides the additional processing required for the applied gate signals in different operating modes. A slower digital layer, controlled by the DSP, programs the sliding surface and controller set-point and provides higher-level functions such as MPPT, communication, telemetry, and other ancillary features. By combining analog and digital resources in a versatile and programmable manner, the proposed archi-

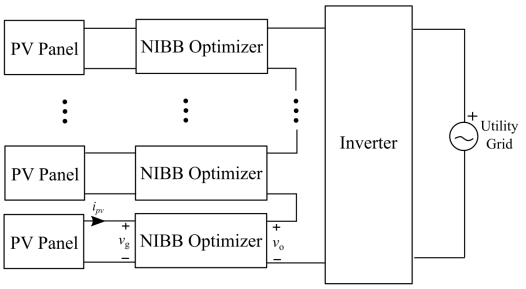


Fig. 1: Photovoltaic system based on several series-connected dc optimizer modules interfacing with a grid-tied inverter.

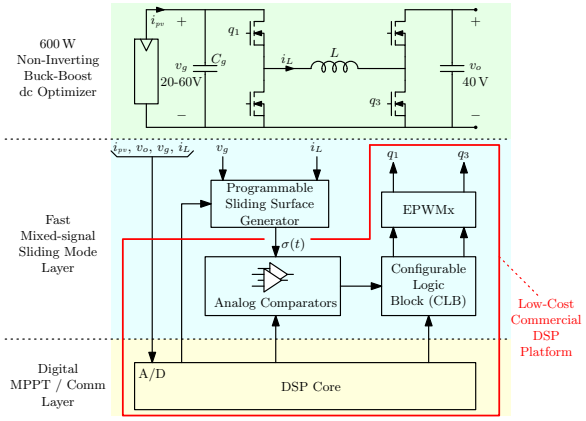
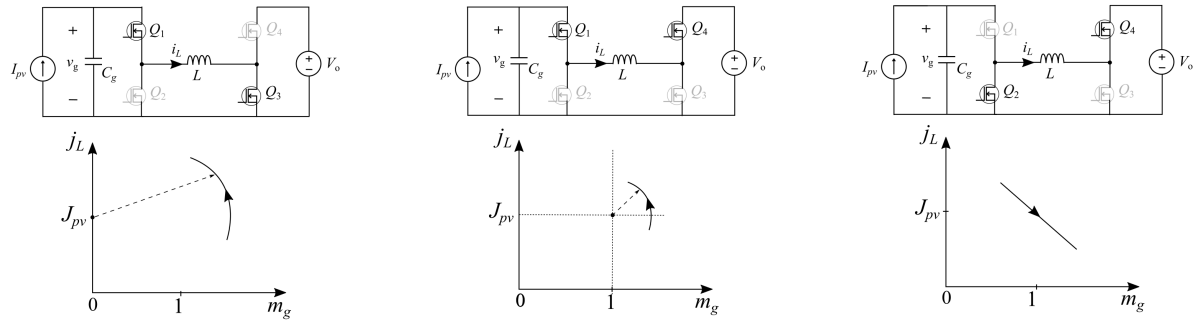


Fig. 2: High-level depiction of the proposed mixed-signal sliding mode controller, with general case study specifications.



(a) State A (b) State B (c) State C

Fig. 3: The three switching states of the NIBB converter with accompanying normalized state-plane trajectories.

tecture reduces the computational latency and attains a faster switching rate in a low-cost implementation when compared to its purely digital counterparts [9]–[11].

The rest of the paper proceeds as follows: Section II describes the operation and general implementation of the proposed mixed-signal sliding mode controller, while Section III outlines the design methodology adopted for the specific NIBB dc optimizer case study considered in this work. Section IV illustrates the experimental validation of the proposed implementation on a 600 W NIBB converter prototype operated as a dc optimizer.

II. Proposed Mixed-Signal Sliding Mode Control

In all generality, the instantaneous dynamic equations of the converter can be expressed as

$$\frac{di_L}{dt} = \frac{1}{L}\left(v_g q_1 - V_o(1-q_3)\right) \tag{1a}$$

$$\frac{dv_g}{dt} = \frac{1}{C_g}\left(I_{pv} - \frac{v_g}{R_g} - i_L q_1\right), \tag{1b}$$

with q_1 and q_3 as the gate signals for Q_1 and Q_3, respectively.

There are a total of four possible converter states depending on the switches q_1 and q_3 switch states. The three states involved in direct power transfer are highlighted in Fig. 3. Note that the axis of the plots are normalized with $V_{base} = V_o$ and $I_{base} = V_{base}/R_0$, where $R_0 = \sqrt{L/C_g}$ is the characteristic impedance. State trajectories associated with the resonant states A and B can be drawn as a family of circles centered at $(0, J_{pv})$ and $(1, J_{pv})$, respectively, while state C generates a linear trajectory with slope $-1/J_{pv}$. With this normalization, the large-signal behavior of the converter can be conveniently studied using purely geometrical arguments [12], [13].

A. Operation of the Proposed Sliding Mode Controller

The sliding surface equation is defined as

$$\sigma \triangleq \boldsymbol{K}\left(\boldsymbol{x} - \boldsymbol{x}_{ref}\right) = 0, \tag{2}$$

where $\boldsymbol{K} \triangleq [K_1\ K_2]$, $\boldsymbol{x} \triangleq [v_g\ i_L]^T$, and where $\boldsymbol{x}_{ref} \triangleq [v_{g,ref}\ i_{L,ref}]^T$ is the controller set-point [14]–[17]. The $i_{L,ref}$ set-point is obtained as a low-pass version of the sensed inductor current. For given $v_{g,ref}$, the operating $i_{L,ref}$ can be found geometrically as the point where the trajectories have opposing tangents when crossing the sliding surface ($\sigma = 0$) for a two-state modulation. The proposed controller operates across three main operating regions:

- *Boost region*, defined as $v_g < V_{\text{g,bst-pt}} < V_o$;
- *Buck region*, defined as $V_o < V_{\text{g,bck-pt}} < v_g$;
- *Pass-through region*, defined as $V_{\text{g,bst-pt}} < v_g < V_{\text{g,bck-pt}}$.

where $V_{g,\text{bst-pt}}$ and $V_{g,\text{bck-pt}}$ denote the pass-through region boundaries on the boost and the buck sides, respectively.

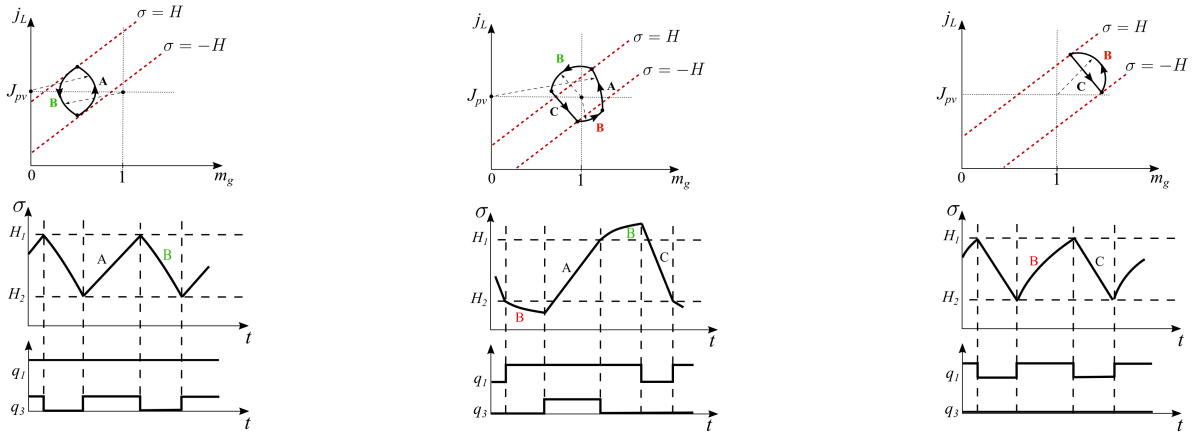
The normalized state-plane trajectories in the three modes of operations are depicted in Fig. 4. In boost mode (Fig. 4(a)), the converter alternates between states A and B, resulting in the steady-state trajectory translating along the $j_L = J_{PV}$ line; in buck mode (Fig. 4(c)), on the other hand, the converter alternates between states B and C, causing the steady-state trajectory to shift along $j_L = J_{PV} m_g$.

Within the pass-through region (Fig. 4(b)), states A and C terminate when $\sigma(t)$ crosses thresholds H_1 and H_2, respectively. However, the two distinct instances of state B – color-coded red and green in Fig. 4(b) – are each terminated by separate digital counters, c_1 and c_2, upon reaching thresholds $t_{c1} \in [0, T_{c1}]$ and $t_{c2} \in [0, T_{c2}]$. Use of counters c_1 and c_2 in pass-through mode is illustrated in greater detail in Fig. 5. As V_g increases, t_{c1} rises while t_{c2} falls, shifting dominance from the green to the red instance of state B. The counter thresholds for these two instances of state B adjust as follows,

$$t_{c1} = \alpha \cdot T_{c1}, \quad t_{c2} = (1-\alpha) \cdot T_{c2}, \tag{3}$$

where $\alpha = (V_{\text{g,ref}} - V_{\text{g,bst-pt}}) \,/\, (V_{\text{g,bck-pt}} - V_{\text{g,bst-pt}})$.

State-plane analysis of each operational mode reveals that the converter's trajectory consistently forms a closed figure and the average value of the controlled variable, specifically v_g, is determined by the geometry of this closed trajectory. The approach here relies on the principle that, as the operating point transitions from the boost region, through the pass-through region, and into the buck region, the shape of the closed trajectory should evolve gradually, thereby avoiding abrupt changes in the average value. Furthermore, the proposed modulation scheme ensures that the converter operates



(a) Boost Operation (b) Pass-through Operation (c) Buck Operation

Fig. 4: Normalized state plane trajectory for the three modes of operation.

at a significantly reduced $i_{L,\text{ref}}$ compared to standard buck-boost modulation, as illustrated in Fig. 6.

Interestingly, the counter-based implementation discussed above is an extension of the conventional, hysteresis-based SMC, with the key difference that the hysteresis is a level-based threshold, whereas the counters are time-based thresholds. Counter-termination events $c_1 = t_{c1}$ and $c_2 = t_{c2}$ act as additional inputs to the SMC controller, making switching between the three states possible in the pass-through region.

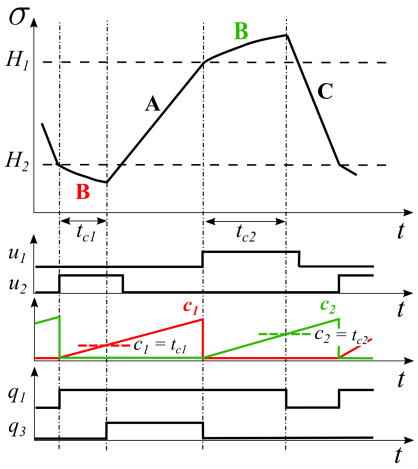


Fig. 5: Modulation scheme in pass-through operation.

B. Hardware Implementation

Implementation of the mixed-signal controller of Fig. 2 is conducted around Texas Instruments LAUNCHXL F280049C development board [8]. A detailed diagram of the controller architecture is shown in Fig. 7. The sliding surface function $\sigma(t)$ is generated in the analog domain via external instrumentation and summing amplifiers. A digital potentiometer functions as an adjustable gain resistor in the instrumentation amplifier

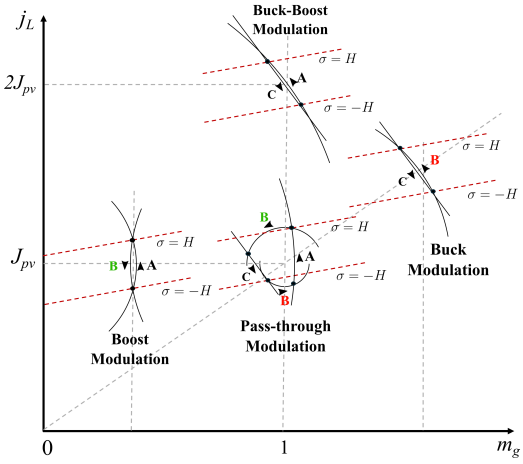


Fig. 6: Comparison of the proposed pass-through modulation with the traditional buck-boost modulation. States A and B are circular arcs centered at $(0, J_{pv})$ and $(1, J_{pv})$, respectively.

stage. It is programmable via SPI by the microcontroller, enabling modification of the sliding surface coefficients K_1 and K_2.

The analog signal $\sigma(t)$ is fed to the onboard CMPSS (Comparator Sub-system), where each module includes two comparators and internal DACs for hysteresis thresholds H_1 and H_2. The CMPSS also performs digital filtering to mitigate switching noise from the sensed $\sigma(t)$, ensuring stable operation. In the subsequent CLB (Configurable Logic Block) stage, sequential logic uses the comparator outputs u_1 and u_2, along with internal counter termination events c_1 and c_2, to generate gate logic signals q_1 and q_3. These logic signals are then fed to the EPWM module, which adds the required dead times to produce the final gate signals $q_{1,\text{PWM}}$ and $q_{3,\text{PWM}}$. The q_1 and q_3 signals are also fed to the ECAP module to measure switching frequency in real-time, allowing for on-the-

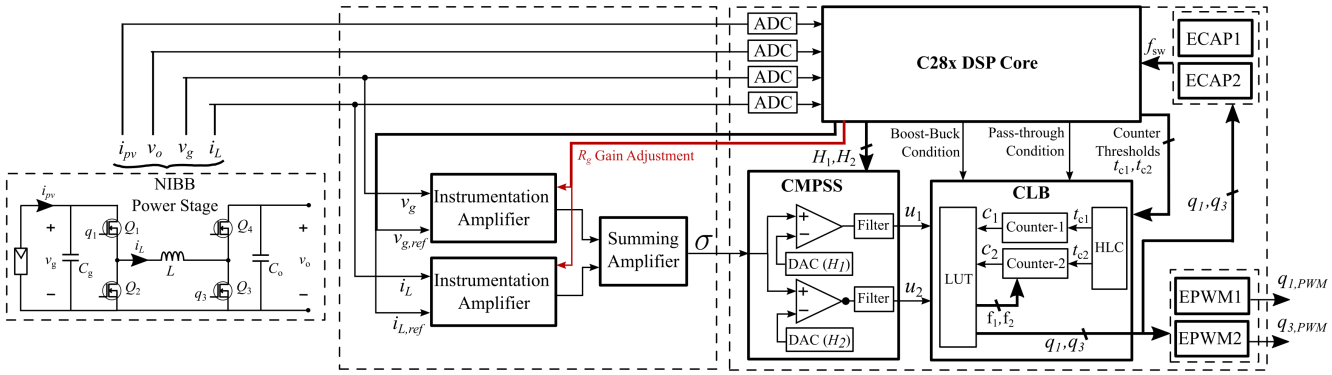


Fig. 7: Hardware implementation of the mixed-signal sliding mode controller using resources of a low–cost DSP platform [8].

fly adjustment of hysteresis thresholds to specifically limit the maximum switching frequency in boost and buck modes. The implementation described above provides complete run-time control over all parameters used in the sliding mode controller, leading to enhanced system programmability over traditional SMC implementations and enabling support of diverse options for advanced modulation schemes.

C. Generation of the gate logic signals

The CLB has three central units utilized in the implementation: the Look-up Tables (LUTs), Counters, and High-Level Controller (HLC). The sequential logic that generates the gate logic signals q_1 and q_3 is depicted as a finite state machine in Fig. 8a. The sequential logic for gate logic signals can be derived for the pass-through region (4a), boost region (4b), and buck region (4c). The counter enable flags, f_1 and f_2, corresponding to counter-1 and counter-2 (4d), respectively, activate the appropriate counter during state B based on the context of the preceding state. This ensures that the two instances of state B are terminated after the appropriate durations.

$$\begin{cases} q_1' = q_1 \cdot q_3 + \overline{q_1} \cdot \overline{q_3} \cdot u_2 + q_1 \cdot \overline{q_3} \cdot (c_2 + \overline{u_1} \cdot f_1) \\ q_3' = q_1 \cdot q_3 \cdot \overline{u_1} + q_1 \cdot \overline{q_3} \cdot (c_1 + u_2 \cdot f_2) \end{cases} \tag{4a}$$

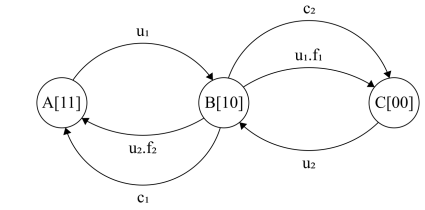
$$\begin{cases} q_1' = 1 \\ q_3' = q_1 \cdot q_3 \cdot \overline{u_1} + q_1 \cdot \overline{q_3} \cdot u_2 \end{cases} \tag{4b}$$

$$\begin{cases} q_1' = q_1 \cdot \overline{q_3} \cdot \overline{u_1} + \overline{q_1} \cdot \overline{q_3} \cdot u_2 \\ q_3' = 0 \end{cases} \tag{4c}$$

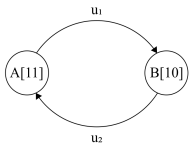
$$\begin{cases} f_1' = \overline{f_2} \cdot (\overline{u_1} + u_2) + \overline{u_1} \cdot u_2 \\ f_2' = \overline{f_1} \cdot (u_1 + \overline{u_2}) + u_1 \cdot \overline{u_2} \end{cases} \tag{4d}$$

III. Design Guidelines

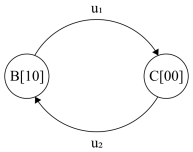
In the subsequent sections, we explore the selection of the hysteresis levels (H_{min}, H_{max}) and the maximum counter times (T_{c1}, T_{c2}) based on a given specification of sliding surface coefficients: $K_1/K_2 = 0.8$, pass-through region limits $(V_{g,\text{bst-pt}} = 35\,\text{V}, V_{g,\text{bck-pt}} = 45\,\text{V})$, and f_{sw} limits: (100 kHz - 200 kHz). It is important to note that these limits, here taken as inputs to the design procedure, involve several trade-offs including converter efficiency as well as reachability/existence requirements for state B. As such, they should be subsequently refined based on simulation and/or experimental evaluation.



(a) Pass-through Region



(b) Boost Region



(c) Buck Region

Fig. 8: Finite State Machine (FSM) illustrating state transitions, with each state uniquely defined by the gate logic values $[q_1,\ q_3]$.

TABLE I: Summary of Design Parameters

Parameter	Value	
	Initial Design	Final Design
K_1'/K_2'	0.8	0.83
f_{sw}	100 kHz to 200 kHz	80 kHz to 200 kHz
$V_{g,\text{bst-pt}}, V_{g,\text{bck-pt}}$	(35 V, 45 V)	(35 V, 45 V)
H_{min}	0.4	0.4
T_{c1}, T_{c2}	$(6.5\mu s, 8\mu s)$	$(7\mu s, 9\mu s)$

A. Sliding Surface Coefficients

Let the sensor gains for v_g and i_L be $G_{v_g,\text{sns}}$ and $G_{i_L,\text{sns}}$ respectively. Similarly, assume the instrumentation amplifier gains to be $G_{v_g,\text{IA}}$ and $G_{i_L,\text{IA}}$ along each path. The imple-

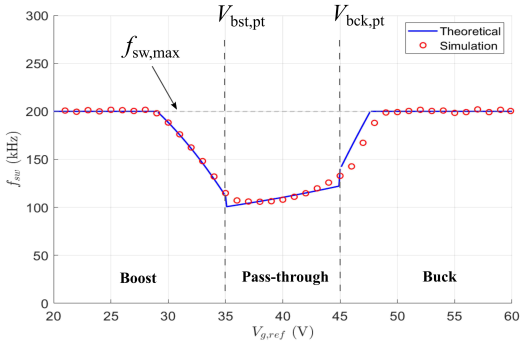


Fig. 9: Theoretically estimated vs. simulated switching frequency (f_{sw}) variation across boost, buck, and pass-through regions, based on the approximate expressions reported in the Appendix, including the maximum switching rate limitation.

mented coefficients can be written as

$$K_1' = G_{v_g,\text{sns}} \cdot G_{v_g,\text{IA}} \tag{5a}$$
$$K_2' = G_{i_L,\text{sns}} \cdot G_{i_L,\text{IA}} \tag{5b}$$

The modified sliding surface equation then becomes $\sigma = K_1'(v_{g,sns} - v'_{g,ref}) + K_2'(i_{L,sns} - i'_{L,ref})$ where the reference values $v'_{g,ref} = G_{v_g,\text{sns}} \cdot v_{g,ref}$ and $i'_{L,ref} = G_{i_L,\text{sns}} \cdot i_{L,ref}$ are sensor gain adjusted values provided by the microcontroller's DAC. The designer can choose the $G_{v_g,\text{IA}}$ and $G_{i_L,\text{IA}}$ such that the the implemented gain ratio K_1'/K_2' equals K_1/K_2.

B. Choosing the hysteresis levels

Across the pass-through region, hysteresis thresholds are kept fixed at H_{min}, which can be evaluated from (6) for a given choice of minimum switching frequency $f_{sw,min}$ at the pass-through region boundaries.

$$f_{sw,min} = \min \left\{ \left(\frac{1}{T_{bst}}\right)_{V_{bst,pt}}, \left(\frac{1}{T_{bck}}\right)_{V_{bck,pt}} \right\} \tag{6}$$

Here, $T_{\text{bst}}(H, V_{g,\text{ref}}) = t_{A,\text{bst}} + t_{B,\text{bst}}$ and $T_{\text{bck}}(H, V_{g,\text{ref}}) = t_{B,\text{bck}} + t_{C,\text{bck}}$ represent the steady-state periods for boost and buck operations, respectively. These periods are functions of the hysteresis levels (H) and the input voltage reference ($V_{g,\text{ref}}$) (see Appendix).

C. Determination of Counter Thresholds

The counter thresholds $t_{c1} \in [0, T_{c1}]$ and $t_{c2} \in [0, T_{c2}]$ vary with the reference voltage $V_{\text{g,ref}}$ within the pass-through region defined by boundaries $V_{\text{g,bst-pt}}$ and $V_{\text{g,bck-pt}}$. The maximum counter thresholds T_{c1} and T_{c2} are chosen to keep the duration of state B duration continuous across these boundaries.

$$T_{c1} = t_{B,bck}|_{V_{g,bck-pt}}, \quad T_{c2} = t_{B,bst}|_{V_{g,bst-pt}}, \tag{7}$$

where the expressions for $t_{B,bck}$ and $t_{B,bst}$ are provided in the Appendix.

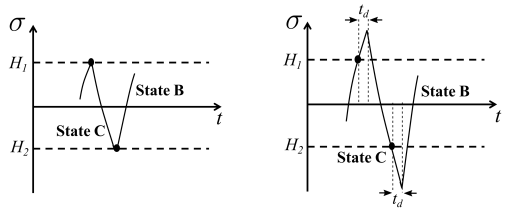


Fig. 10: Effect of delays on σ: (a) shows transitions without delays, and (b) shows transitions with delays.

D. Limiting maximum switching frequency

Fig. 9 illustrates the variation of the switching rate across the input voltage range. As seen in the plot, the switching frequency is minimum around the pass-through region, and tends to rapidly increase as soon as the converter enters buck or boost mode of operation. Limiting the switching frequency is usually desirable to reduce switching losses and maintain efficiency. For this reason, a switching frequency limitation mechanism is embedded in the proposed controller, which dynamically adjusts the hysteresis band H to prevent the switching rate from exceeding $f_{\text{sw,max}} = 200\,\text{kHz}$. This control can be implemented using an ECAP module to measure the clock cycles between consecutive rising edges of gate signals q_1 or q_3, providing real-time switching frequency estimates. The hysteresis bandwidth H is then dynamically adjusted based on the measured frequency f_{meas} relative to the maximum frequency $f_{\text{sw,max}}$, governed by periodic adjustments as in (8).

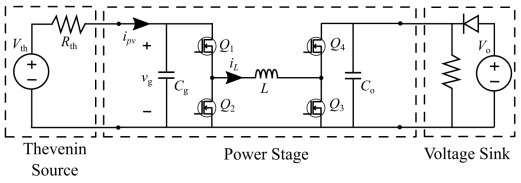
$$H = \begin{cases} \min(H + \Delta H, H_{\text{max}}), & \text{if } f_{\text{meas}} > f_{\text{sw,max}} \\ \max(H - \Delta H, H_{\text{min}}), & \text{if } f_{\text{meas}} < f_{\text{sw,max}} \\ H, & \text{otherwise} \end{cases} \tag{8}$$

where ΔH is the step adjustment for H, and H_{min} and H_{max} represent the minimum and maximum hysteresis values, respectively. H_{min} is determined earlier in Section III-B on selecting appropriate hysteresis levels, while H_{max} is constrained by the reference voltage of the internal DACs within the CMPSS sub-module.

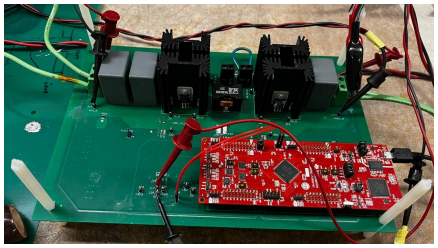
As seen in Fig. 9, the switching frequency limitation kicks in when the converter is deep into the buck or boost modes of operation, effectively limiting f_{sw}. Near and inside the pass-through region, on the other hand, the switching rate is not constrained and is estimated using the expressions reported in the Appendix. Fig. 9 compares the theoretically expected f_{sw} variation with the simulated one, confirming the effectiveness of both the switching rate limitation mechanisms, and the good accuracy of the provided expressions, valid for $f_{sw} < f_{sw,max}$.

E. Effect of delays on the state durations

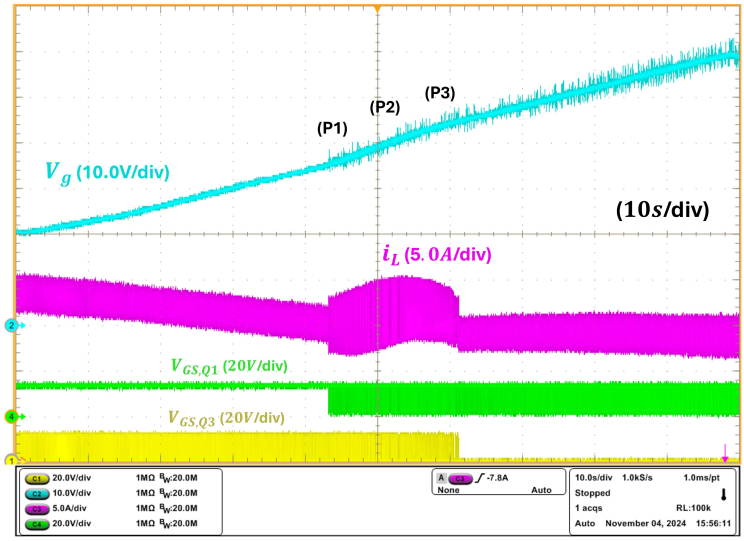
The design methodology is based on the knowledge of state durations in boost and buck modes. In practical implementa-



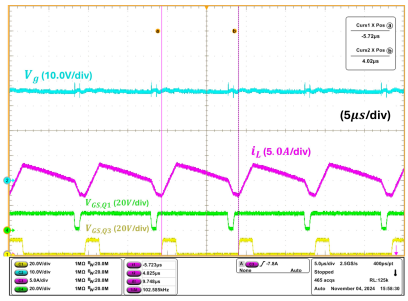
(a) Experimental Setup



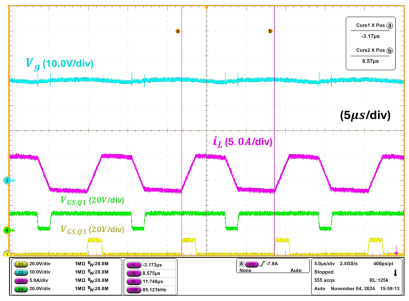
(b) NIBB 600 W Prototype



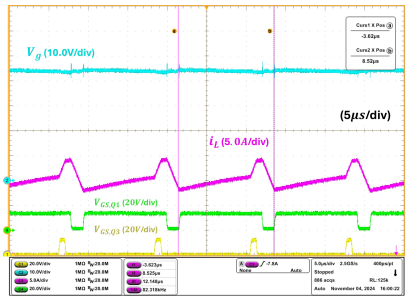
(c) Input voltage sweep from V_g = 20 V to 60 V



(d) Operating point P1
$V_{g,ref}$ = 36 V



(e) Operating point P2
$V_{g,ref}$ = 40 V



(f) Operating point P3
$V_{g,ref}$ = 44 V

Fig. 11: Experimental results for input voltage sweep with input Thévenin source $V_{g,th}$ = 104 V and $R_{g,th}$ = 4.5 Ω (set up for P_{max} = 600 W at V_g = 52 V), and fixed output voltage V_o = 40 V.

tions, factors such as dead times, digital filtering, and propagation delays cause the actual steady-state periods to deviate from theoretical estimates. The magnitude of these deviations depends on the specific constituent states within each mode and the operating point. Fig. 10 illustrates the impact of delays by comparing two scenarios: one with delays and one without. During each comparison event, the *extended state* exceeds the hysteresis level by $\Delta\sigma$ during t_d, requiring the *return state* to compensate for the overshoot. Consequently, this results in deviations in the switching period, which becomes more pronounced when the *extended state* changes faster than the *return state*. Adjustments to the initial design parameters are therefore necessary to mitigate these effects. For reference, Table I summarizes the finalized design parameters for the case study discussed.

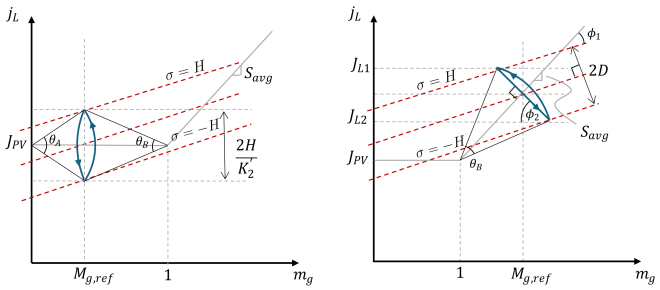
TABLE II: Component Values for NIBB Converter

Component	Value
Input Capacitor (C_g)	20 μF
Inductor (L)	10 μH
Switching MOSFETs (Q_1 to Q_4)	FDP083N15A
Gate Driver	1EDB8275FXUMA1
Current Sense Amplifier	INA241A4 (100V/V)
Voltage Sense Amplifier	ADA4851-2Y
Instrumentation Amplifier	INA849
Digital Potentiometer	MAX5394LATA+
Control Platform	TI F280049C
Switching Frequency	80-200 kHz
Power Ratings	600W max, 20-60V input

IV. Experimental Results

The NIBB experimental prototype is shown in Fig. 11a, and a list of main components used to implement the proposed mixed-signal controller is reported in Table II.

In the following tests, the converter operates off a Thévenin input source set for a maximum power of 600 W at V_g =52 V, and with V_o fixed at 40 V. An input voltage sweep between 20 V and 60 V is illustrated in Fig. 11c. The converter transitions smoothly through the pass-through region – here defined by a ±5 V window around V_o – with a limited excursion of the average inductor current. Throughout the sweep, the converter switching frequency ranges between 80 kHz and



(a) Boost Mode (b) Buck Mode

Fig. 12: Typical steady-state state plane trajectories.

200 kHz. Fig. 11(d)–(f) present a sequence of three steady-state operating points, illustrating how the q_3 pulse shifts from left to right as V_g increases. This shift reflects changes in t_{c1} and t_{c2}—the thresholds of counter-1 and counter-2, respectively—that determine the duration of the two instances of state B.

V. Conclusion

This work presents a mixed-signal sliding mode controller for NIBB-based PV dc optimizers. The approach enables seamless tracking of the input voltage reference throughout the converter's operating range. It provides an advanced modulation in the pass-through region, which reduces the inductor and switch current stresses. The controller is implemented around a low-cost commercial DSP platform and uses mixed-signal resources to get configurable parameters and minimal delay from the sensing to output. Experimental results on a 600 W NIBB converter operated as a dc optimizer are presented to validate the proposed controller architecture.

Appendix A
Theoretical Estimation of State Durations

The first step in calculating the state durations in the boost and buck modes is to translate the sliding surface equation (2) onto the normalized state plane (m_g vs j_L),

$$\sigma = K_{1,\text{norm}}(m_g - M_{g,\text{ref}}) + K_{2,\text{norm}}(j_L - J_{L,\text{ref}}), \quad (9)$$

where $K_{1,\text{norm}} = K_1 V_{\text{base}}$ and $K_{2,\text{norm}} = K_2 I_{\text{base}}$.

A. Boost Operation

Referring to Fig. 12(a), in boost operation, the converter alternates between states A and B. The vertical distance between the two switching instants on the state plane is given by $2H/K_{2,\text{norm}}$. The durations of states A and B are derived as shown in (10).

$$t_{A,\text{bst}} = \frac{\theta_A}{\omega_0} = 2\sqrt{LC_g}\tan^{-1}\left(\frac{H/K_{2,\text{norm}}}{M_{g,\text{ref}}}\right), \quad (10a)$$

$$t_{B,\text{bst}} = \frac{\theta_B}{\omega_0} = 2\sqrt{LC_g}\tan^{-1}\left(\frac{H/K_{2,\text{norm}}}{1 - M_{g,\text{ref}}}\right). \quad (10b)$$

B. Buck Operation

In buck operation, as shown in Fig. 12(b), the converter alternates between states B and C. The slope of the state C trajectory is given by:

$$\frac{dj_L}{dm_g} = -\frac{1}{J_{PV}} = \tan(\pi - \phi_2). \quad (11)$$

Using input-output power balance, it can be shown that the reference inductor current is related to the photovoltaic current by $J_{L,\text{ref}} = J_{PV} M_{g,\text{ref}}$. For $M_{g,\text{ref}} > 1$, the slope of the ideal average inductor current trajectory becomes:

$$S_{\text{avg}} = \frac{J_{L,\text{ref}} - J_{PV}}{M_{g,\text{ref}} - 1} = J_{PV}. \quad (12)$$

This implies that the state C trajectory is perpendicular to the ideal average trajectory, $j_{pv} = J_{PV} m_g$, shown as a line on the state plane. Let ϕ_1 denote the angle between the average $J_{L,\text{ref}}$ trajectory (line $j_{pv} = J_{PV} m_g$) and the sliding surface (defined by $K_{1,\text{norm}}$ and $K_{2,\text{norm}}$). The angle ϕ_1 is expressed as:

$$\phi_1 = \tan^{-1}\left(-\frac{K_{1,\text{norm}}}{K_{2,\text{norm}}}\right) - \tan^{-1}(J_{PV}). \quad (13)$$

The perpendicular distance between the switching boundaries $\sigma = H$ and $\sigma = -H$ is defined as $2D$, where:

$$D = \frac{H/K_{2,\text{norm}}}{\sqrt{1 + \left(\frac{K_{1,\text{norm}}}{K_{2,\text{norm}}}\right)^2}}. \quad (14)$$

Assuming that the average trajectory $(M_{g,\text{ref}}, J_{L,\text{ref}})$ lies on the state C trajectory, and noting that $(J_{L1} - J_{L2}) = 2D\sec(\phi_1)\sin(\phi_2)$, the durations of states B and C are given in (15).

$$t_{B,\text{bck}} = 2\sqrt{LC_g}\tan^{-1}\left(\frac{D\sec(\phi_1)}{\sqrt{(M_{g,\text{ref}} - 1)^2 + (J_{L,\text{ref}} - J_{PV})^2}}\right), \quad (15a)$$

$$t_{C,\text{bck}} = 2D\sqrt{LC_g}\sec(\phi_1)\sin(\phi_2). \quad (15b)$$

C. Pass-through Operation

For estimating the steady-state period in this mode, the following simplifying assumptions are made: during the two instances of state B, the change $\Delta\sigma \approx 0$, and states A and C exhibit constant $d\sigma/dt$,

$$t_{A,\text{pt}} = \frac{2H}{\dot{\sigma}_A}, \quad t_{C,\text{pt}} = \frac{2H}{\dot{\sigma}_C}, \quad (16)$$

where $\dot{\sigma}_A$ and $\dot{\sigma}_C$ represent $d\sigma/dt$ for states A and C, respectively, evaluated at the equilibrium point $(M_{g,\text{ref}}, J_{L,\text{ref}})$. The durations of the two instances of state B are determined by the counter thresholds t_{c1} and t_{c2}, as defined in (3).

REFERENCES

[1] G. Walker and P. Sernia, "Cascaded dc-dc converter connection of photovoltaic modules," in *Proc. 33rd IEEE Power Electronics Specialists Conference (PESC)*, vol. 1, 2002, pp. 24–29.

[2] L. Linares, R. W. Erickson, S. MacAlpine, and M. Brandemuehl, "Improved energy capture in series string photovoltaics via smart distributed power electronics," in *Proc. 24th IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2009, pp. 904–910.

[3] R. Paul and D. Maksimović, "Analysis of PWM nonlinearity in non-inverting buck-boost power converters," in *Proc. 39th IEEE Power Electronics Specialists Conference (PESC)*, 2008, pp. 3741–3747.

[4] P.-C. Huang, W.-Q. Wu, H.-H. Ho, and K.-H. Chen, "High efficiency and smooth transition buck-boost converter for extending battery life in portable devices," in *Proc. 1st IEEE Energy Conversion Congress and Exposition (ECCE)*, 2009, pp. 2869–2872.

[5] C. Restrepo, T. Konjedic, J. Calvente, and R. Giral, "Hysteretic transition method for avoiding the dead-zone effect and subharmonics in a non-inverting buck–boost converter," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3418–3430, 2015.

[6] N. Zhang, G. Zhang, and K. W. See, "Systematic derivation of dead-zone elimination strategies for the noninverting synchronous buck–boost converter," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 3497–3508, 2018.

[7] C.-H. Tsai, Y.-S. Tsai, and H.-C. Liu, "A stable mode-transition technique for a digitally controlled non-inverting buck–boost dc–dc converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 1, pp. 475–483, 2015.

[8] *TMS320F28004x Real-Time Microcontrollers*, Texas Instruments, 2023, rev. G. [Online]. Available: https://www.ti.com/lit/gpn/tms320f280049c

[9] S. Narula, L. Corradini, and D. Maksimović, "Unified sliding-mode control of non-inverting buck-boost converters," in *Proc. 24th IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2023, pp. 1–7.

[10] J. Celikovic, P. Cavallini, S. Abedinpour, and D. Maksimović, "Minimum-deviation transient response in non-inverting buck-boost dc-dc converters," in *Proc. 21st IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–8.

[11] M. Oppenheimer, I. Husain, M. Elbuluk, and J. De Abreu Garcia, "Sliding mode control of the Cuk converter," in *Proc. 27th IEEE Power Electronics Specialists Conference (PESC)*, vol. 2, 1996, pp. 1519–1526.

[12] R. Munzert and P. Krein, "Issues in boundary control [of power convertors]," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, vol. 1, 1996, pp. 810–816 vol.1.

[13] M. Greuel, R. Muyshondt, and P. Krein, "Design approaches to boundary controllers," in *PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*, vol. 1, 1997, pp. 672–678 vol.1.

[14] V. Utkin, "Variable structure systems with sliding modes," *IEEE Transactions on Automatic Control*, vol. 22, no. 2, pp. 212–222, 1977.

[15] H. Sira-Ramirez, "Sliding motions in bilinear switched networks," *IEEE Transactions on Circuits and Systems*, vol. 34, no. 8, pp. 919–933, 1987.

[16] P. Mattavelli, L. Rossetto, G. Spiazzi, and P. Tenti, "General-purpose sliding-mode controller for dc/dc converter applications," in *Proc. 24th IEEE Power Electronics Specialist Conference (PESC)*, 1993, pp. 609–615.

[17] R. Venkatramanan, "Sliding mode control of power converters," Ph.D. dissertation, California Institute of Technology, Pasadena, California, May 1986.