Self-Calibrated Digital Current Emulation for High-Frequency Hysteretic Current-Mode Control in GaN PFC Converters

Mohammad Shawkat Zaman and Olivier Trescases
The Edward S. Rogers Sr. Department of Electrical & Computer Engineering, University of Toronto, Canada
E-mail: Shawkat.Zaman@utoronto.ca

***Abstract*—This work presents a digital emulation technique that reproduces the switching-frequency behaviour of the inductor current in a power converter, enabling high-frequency (HF) cycle-by-cycle hysteretic current-mode control for applications with limited current-sensing opportunities. The proposed technique leverages lower-bandwidth current sensors to opportunistically self-calibrate the emulator, alleviating its dependence on preset system parameters. Removing the need for high-bandwidth sensors enables low-inductance power loops, critical for maximizing performance in HF converters. The design is demonstrated in a 240-V_{rms}-to-450-V all-GaN totem-pole PFC converter operating at 4 kW.**

***Index Terms*—Digital Current Emulation, Current Observer, Self Calibration, Current Mode Control, Power Factor Correction, Totem Pole, Bridgeless Rectifier, GaN.**

I. Introduction

The market for gallium nitride (GaN) power transistors is expected to grow from $46M in 2020 to $1B in 2026, thanks to their superior electrical and thermal performance [1], with promising outlooks in electric-vehicle (EV) applications in the 400-V range [2]. Grid-facing EV power systems, like the onboard chargers (OBCs) with power-factor correction (PFC), benefit from current-mode control (CMC) for precise current-shaping, enhancing efficiency and minimizing input-filter size [3], [4]. While GaN devices operating in the medium- to high-voltage (HV) range ($\geq$ 200 V) are capable of faster switching speeds compared to their Silicon (Si) counterparts [2], current-sensing becomes increasingly challenging at higher switching frequencies ($\geq$ 300 kHz) and power levels ($\geq$ 500 W). High-bandwidth sensing requires the insertion of current sensors in the power loop, which worsens parasitic inductances and limits the achievable switching frequency. Furthermore, while resistive current sensors can have bandwidths in the GHz range (compared to a few MHz for magnetic ones), they suffer from significant conduction losses in high-power applications [5]. SenseFET-like indirect sensing schemes can avoid these issues [6], [7], but must contend with isolation and noise constraints at HV.

To circumvent these current-sensing challenges, various aspects of the desired current waveform have been emulated using more easily sensed quantities, such as input and output voltages [5], [8]–[15]. However, many such designs only emulate the average inductor current [8]–[12], without capturing the switching-frequency ripple, preventing their use in high-frequency control techniques. Moreover, emulators that do reproduce the ripple [5], [13]–[15] have only been demonstrated for lower-voltage and -power ($\leq$ 200 V, 200 W) systems, unsuitable for the 400-V, kW-level converters in EV onboard chargers (OBCs). In particular, [5] is implemented in an ac-dc PFC converter, but operating at only 100 kHz, while [13] is demonstrated at a fixed frequency of 500 kHz, but only for dc-dc conversion. They also rely on the precise inductance value (which may vary by up to $\pm 20\%$), requiring manual adjustment of the emulator parameters for every sample.

This work presents a digital emulator that reproduces the switching-frequency behaviour of the inductor current. To alleviate the need for precise knowledge of system parameters, a novel calibration technique leveraging current sensors with relatively low bandwidth is proposed. The emulator design is validated in a 240-V_{rms}-to-450-V all-GaN totem-pole PFC converter operating at 4 kW by enabling cycle-by-cycle hysteretic current-mode control (HCMC).

II. Proposed Design

Fig. 1 shows the proposed system with the emulator-based control architecture. It consists of an all-GaN totem-pole PFC converter and an FPGA-based digital controller employing HCMC via inductor emulation.

A. Totem-Pole PFC converter with HCMC

The proposed PFC converter is implemented using an all-GaN totem-pole topology, as shown in Fig. 1, to leverage the low ON-resistance and switching loss of GaN devices and eliminate the lossy diode bridge required for conventional boost PFC converters [16]. $M_{x\text{S-LF}}$ form the low-frequency (LF) leg of the totem pole that commutates based on the polarity of the ac-line voltage, v_{ac}, while $M_{x\text{S-HF}}$ form the high-frequency (HF) leg that switches at a frequency, $f_{\text{sw}} \gg$ the line frequency, f_{ac}, to shape the inductor current, i_L. v_{ac} and the dc-link voltage, V_{link}, are digitally sampled using independent analog-to-digital converters (ADCs). A Hall-effect-based sensor placed at $V_{X\text{-LF}}$, along with a comparator and a digital reference, is used to sample the inductor current and correct emulator mismatches.

The PFC design employs variable-frequency HCMC, which controls both peak and valley of the inductor current and avoids the need for slope compensation inherent with fixed-frequency peak- or valley-current-mode control. The controller automatically switches between boundary and continuous conduction modes (BCM and CCM) to optimize efficiency, similar to the Silicon-Carbide-based design in [4], which operated

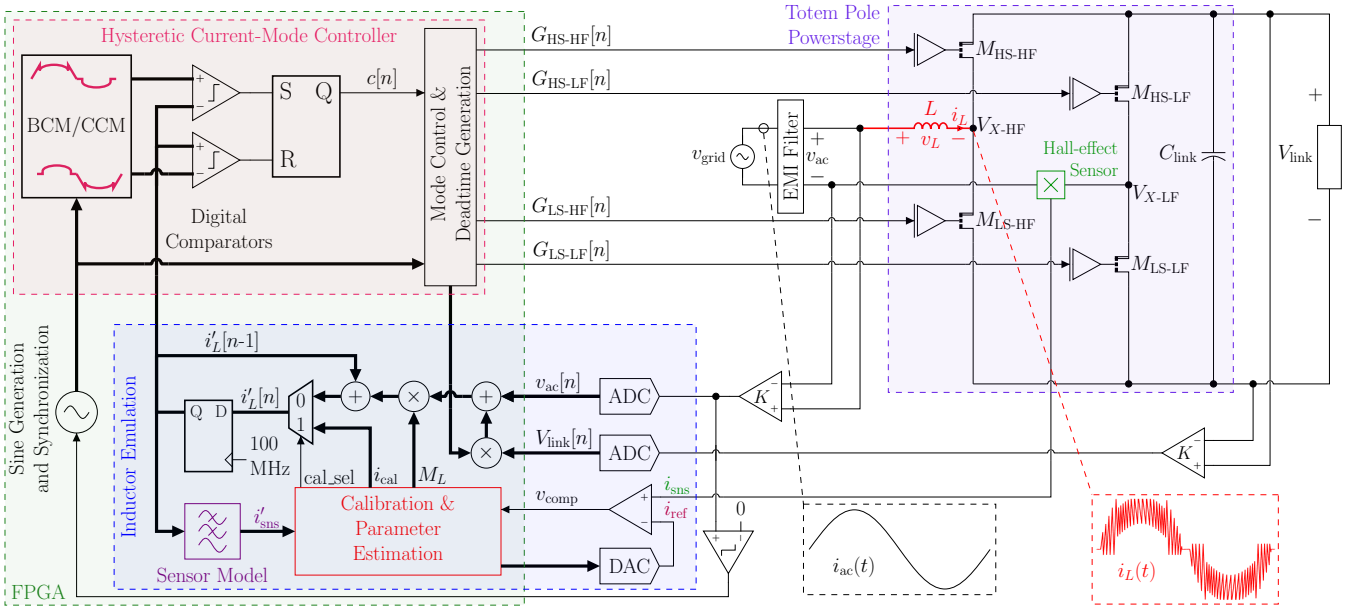


Fig. 1. PFC converter system diagram showing the power-stage, sensing circuitry, and the FPGA-based inductor-current emulator and controller. A thick line indicates a multi-bit digital signal. The outer voltage loop that regulates the PFC input-current amplitude is not shown for simplicity.

at up to 300 kHz. BCM operation at low input currents reduces switching losses by enabling zero-voltage switching (ZVS) for both HF switches, while CCM at high currents optimizes conduction losses. This design utilizes the high-resolution emulated current to perform HCMC, which enables higher-frequency operation, as the emulated waveform is free of the ubiquitous switching noise that otherwise limits the performance of converters with CMC, especially in ac-dc conversion with wide duty-cycle ranges.

B. Inductor Emulator

Fundamentally, the inductor current, $i_L(t)$, is related to the integral of its voltage, $v_L(t)$:

$$i_L(t) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{t} v_L(\tau)d\tau \tag{1}$$

For the totem-pole topology, $v_L(t)$ is given by

$$v_L(t) = v_{\text{ac}}(t) + \Big[S_{\text{LF}}(t) - S_{\text{HF}}(t)\Big]V_{\text{link}}(t) \pm V_{\text{loss}}(t) \tag{2}$$

where $S_{\text{LF}}(t)$ and $S_{\text{HF}}(t)$ represent the states of the LF and HF legs of the totem pole, respectively:

$$S_x(t) = \begin{cases} 1 & \text{if } M_{\text{HS-}x} \text{ is conducting} \\ 0 & \text{if } M_{\text{LS-}x} \text{ is conducting} \end{cases}, x \in \{\text{LF}, \text{HF}\}$$

given that the $\big(M_{\text{HS-}x}, M_{\text{LS-}x}\big)$ pairs always switch in a complementary fashion. During deadtime (i.e., when both switches in a leg are OFF), conduction states can be inferred from the direction of i_L and the reverse-conduction capability of the switches.

$V_{\text{loss}}(t)$ represents the current-dependent conduction losses due to component resistances. In this system, i_L scales with v_{ac} (due to PFC operation), and the total resistance contributing to V_{loss} is $<100\,\text{m}\Omega$. Consequently, this term is ignored in the proposed design for computational simplicity.

For a sufficiently small computation interval, T_{comp}, $v_L(t)$ can be assumed to be constant, and estimated using the sampled v_{ac} and V_{link} voltages:

$$v'_L[n] = v_{\text{ac}}[n] + \Big(S_{\text{LF}}[n] - S_{\text{HF}}[n]\Big)V_{\text{link}}[n] \tag{3}$$

The integral from (1) can then be approximated by a product, and $i_L(t)$ can be emulated by

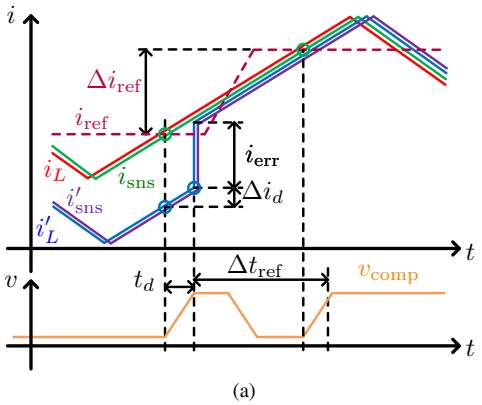
$$\begin{aligned} i'_L[n] &= i'_L[n-1] + \frac{1}{L}\Big(v'_L[n]\Big)\Big(T_{\text{comp}}\Big) \\ &= i'_L[n-1] + M_L v'_L[n] \end{aligned} \tag{4}$$

where $M_L = \frac{T_{\text{comp}}}{L}$ is used as the adjustable slope parameter, instead of L, for ease of computation.

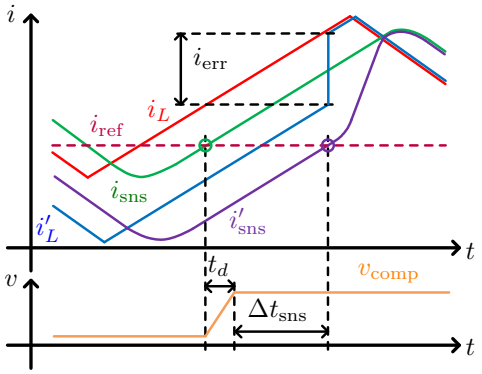
In this design, $T_{\text{comp}} = 10\,\text{ns}$ is chosen to ensure 0.5% or better temporal resolution at the highest targeted f_{sw} of 500 kHz. $S_x[n]$ can be determined from the digital gating signals, $\Big(G_{\text{HS-}x}[n], G_{\text{LS-}x}[n]\Big)$, generated by the current-mode controller, after accounting for gate-driver delays. The proposed design samples $v_{\text{ac}}(t)$ and $V_{\text{link}}(t)$ at $f_{\text{samp}} \approx 1\,\text{MHz}$ using 10-bit serial ADCs in order to balance voltage and timing resolutions, leading to a worst-case change in the measured voltages $\ll V_{\text{LSB}} \approx 0.7\,\text{V}$ between samples under typical operating conditions. Since $T_{\text{comp}} \ll 1/f_{\text{samp}}$, a sample-and-hold approach is utilized for generating the intermediate voltage samples between consecutive measurements. While extrapolation using past samples can improve emulation accuracy, the added computational complexity was deemed unjustified given the slow voltage dynamics in this application.

C. Emulator Calibration

In order to limit the deviation of (4) from reality over time due to measurement noise and component variations, occasional sensing is required to calibrate i'_L and M_L. Unlike direct



(a)



(b)

Fig. 2. Idealized waveforms of (a) direct and (b) indirect calibration of the emulator with high- and low-bandwidth sensors, respectively. While a positive correction is shown in each case, both positive and negative errors can be corrected in either approach.

current-sensing for conventional CMC, these calibrations need not be performed every cycle, though there is a direct relationship between the frequency of calibration and the maximum accumulated error in the emulated waveform. For example, a 1-LSB error in the voltage measurement ($\approx 0.7\,\mathrm{V}$ in this design) leads to a current error of approximately 177 mA over one period at the lowest targeted f_{sw} of 200 kHz, which is less than 0.5% of the rated operating current. In a variable-frequency control scheme such as PFC with HCMC, calibration can be performed during lower-frequency periods in the operating cycle, enabling higher-frequency operation without direct sensing elsewhere.

If the current sensor has a bandwidth, $f_{\mathrm{BW}} > 5f_{\mathrm{sw}}$, it preserves the most significant harmonics of the triangular inductor current waveform, i_L, and the sensed waveform, i_{sns}, closely matches i_L, as shown in Fig. 2(a). This allows *direct calibration* by comparing i_{sns} with a reference level, i_{ref}. When i_{sns} crosses i_{ref}, as detected by the comparator output, v_{comp}, the emulated current, i'_L, is set to

$$i_{\mathrm{cal}} = i_{\mathrm{ref}} + \Delta i_d \tag{5}$$

where Δi_d accounts for the comparator delay, t_d, as given by

$$\Delta i_d = M_L \sum^{t_d} v'_L[n] \tag{6}$$

where the summation term represents the sum of all v'_L samples over the t_d duration preceding the detection instant. This notation is used in the following equations as well.

By changing i_{ref} during the same switching state and performing a second comparison, M_L can also be estimated, as shown in Fig. 2(a). If i_{ref} is changed by Δi_{ref}, and the duration between the two detection instants is Δt_{ref}, M_L is approximated by

$$M_L \approx \frac{\Delta i_{\mathrm{ref}}}{\sum^{\Delta t_{\mathrm{ref}}} v'_L[n]} \tag{7}$$

While this measurement requires the switching state to be sufficiently long to allow the changing and settling of i_{ref}, it is only needed infrequently, and can be performed opportunistically in operating conditions with the largest ripple.

In contrast, if $f_{\mathrm{BW}} \leq 5f_{\mathrm{sw}}$, as in this design, loss of the higher harmonics introduces peak distortion and phase delay in i_{sns}, as shown in Fig. 2(b). This makes direct calibration infeasible, and requires an *indirect calibration* approach to be used for correcting i'_L. The current error, i_{err}, is defined as

$$i_{\mathrm{err}} = i_L - i'_L \tag{8}$$

To estimate i_{err}, the low-pass current-sensor behaviour must also be emulated, as shown in Fig. 2(b). This is modelled as a digital transfer function that replicates the frequency response of the sensor, which can be obtained from the manufacturer datasheet, or experimentally measured. Both i_{sns} and the emulated sensor waveform, i'_{sns}, is compared against the same i_{ref} during one switching state, and the duration between the two crossings, Δt_{sns}, is measured. Note that detection of the i'_{sns} crossing is effectively instantaneous, since it is an internally generated signal and free from analog delays. Then i_{err} is given by

$$i_{\mathrm{err}} \approx M_L \left(\sum^{\Delta t_{\mathrm{sns}} + t_d} v'_L[n] \right) \tag{9}$$

i'_L is then set to

$$i_{\mathrm{cal}} = i'_L + i_{\mathrm{err}} \tag{10}$$

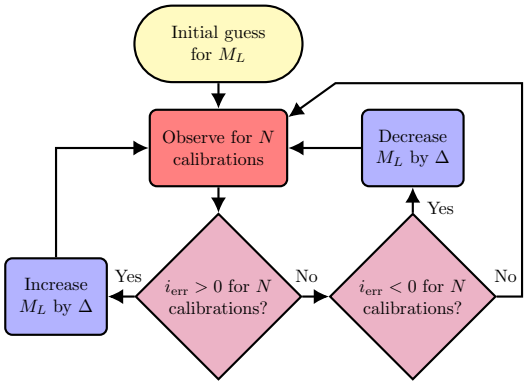


Fig. 3. Perturb-and-observe approach for estimating the slope parameter, M_L, with a low-bandwidth sensor. N and Δ are design parameters dependent on converter operating modes.

To estimate M_L with a low-bandwidth sensor, the converter can be occasionally operated in an LF mode to employ the direct-calibration method, or a perturb-and-observe approach may be used, as shown in Fig. 3. For example, in PFC operation with HCMC, the lowest operating frequencies occur in the BCM region near the BCM-CCM crossover point, as shown in Fig. 1, which presents a convenient opportunity for M_L estimation.

III. Experimental Results

A prototype converter with the specifications shown in Table I was built to demonstrate the proposed current-emulation technique, as shown in Fig. 4. The power-stage uses the 650-V-rated `GS66516T` devices to leverage their near-chip-scale packaging with convenient top-side cooling surface, which enables heat extraction without interfering with the electrical layout. The `ACS733` isolated hall-effect sensor, having a bandwidth of 1 MHz, is used for sensing the inductor current.

TABLE I
PFC Converter Specifications

Parameter	Value	Unit
AC-Line Voltage, v_{ac}	120-240	V_{rms}
AC-Line Frequency, f_{ac}	60	Hz
AC-Line Inductance, L	6×3.3	µH
DC-Link Voltage, V_{link}	300-450*	V_{dc}
DC-Link Capacitance, C_{link}	5×120	µF
Rated Output Power, P_{out}	4	kW
Switching Frequency, f_{sw}	200-500	kHz
Power Device, M_x	650 V, 25 mΩ	

* Dependent on ac-line voltage.

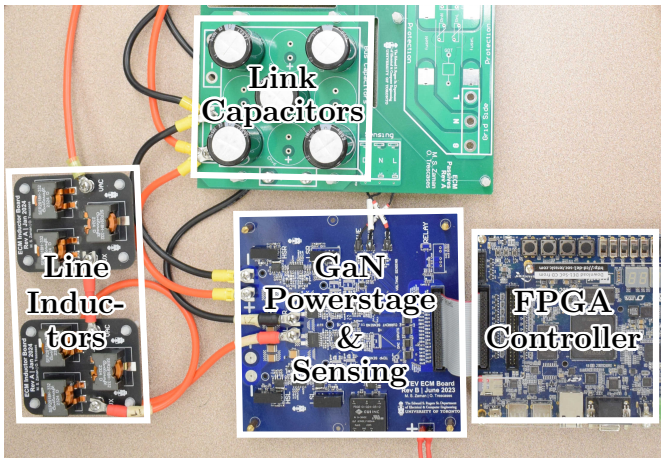


Fig. 4. Prototype PFC converter with emulator-based HCMC. The ac-line inductance is implemented with series-connected 3.3-µH SER2918H units in order to achieve the required saturation current. The power-stage is located on the underside of the PCB, along with the off-the-shelf liquid-cooled copper heatsink.

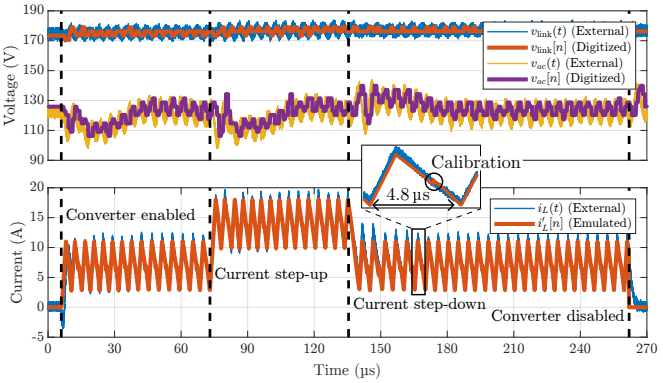
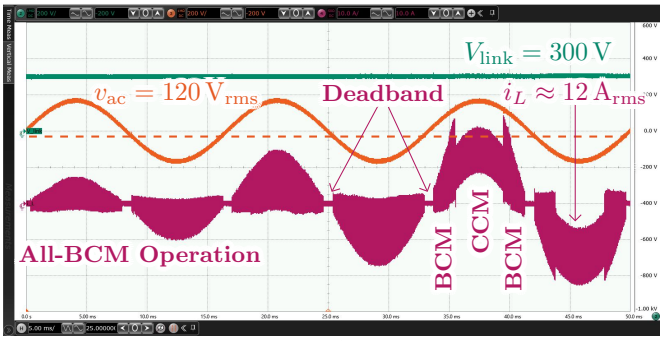
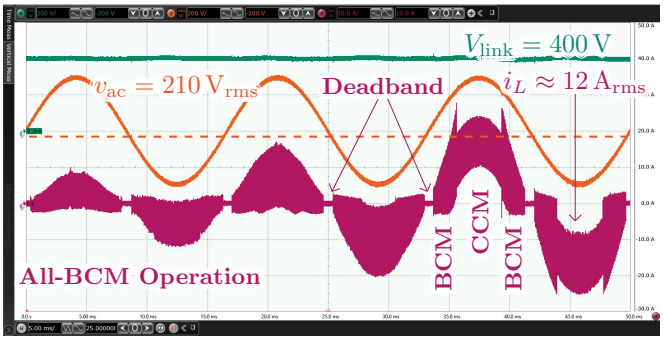


Fig. 5. Comparison between external (as measured by an oscilloscope) and digitized internal waveforms of the converter from an approximately 260-µs test run in dc-dc boost mode with $v_{ac} = 120\,V_{dc}$, $V_{link} = 175\,V_{dc}$, and current steps between 7 A and 14 A.



(a)

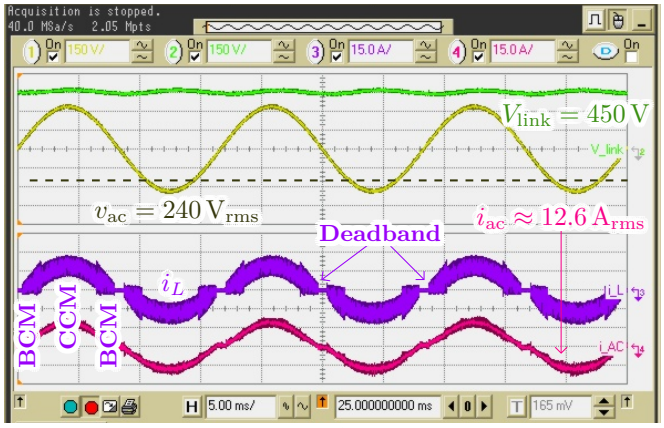


(b)

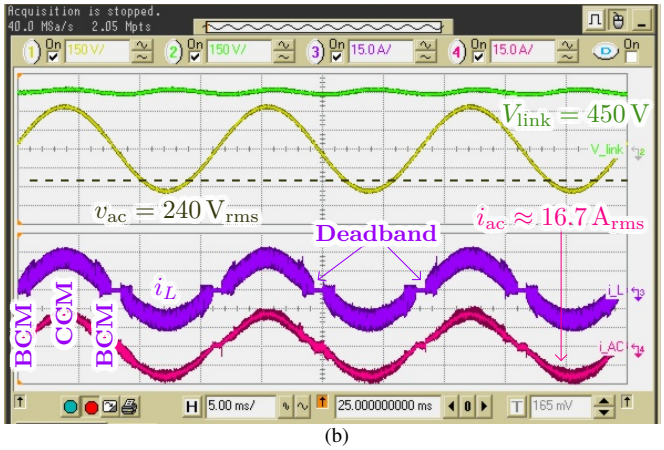
Fig. 6. Measured converter waveforms in ac-dc mode with an input current of up to $12\,A_{rms}$, and (a) $v_{ac} = 120\,V_{rms}$, $V_{link} = 300$ V, and (b) $v_{ac} = 210\,V_{rms}$, $V_{link} = 400$ V, showing sinusoidal current shaping, and automatic BCM-CCM transition based on operating current.

To verify the effectiveness of the proposed emulator and control technique, the converter was first operated in dc-dc boost mode, as shown in Fig. 5. The controller is able to reach steady-state operation in a single switching cycle, both at startup and subsequent current up- and down-steps, demonstrating the advantages of HCMC. The emulator makes this possible without peak- and valley-current sensing by providing a faithful representation of the inductor current, despite transient variations in v_{ac}.

The measured waveforms of the converter when operating in ac-dc PFC mode are shown in Figs. 6 and 7. In all cases, the inductor current is sinusoidally shaped and synchronized to

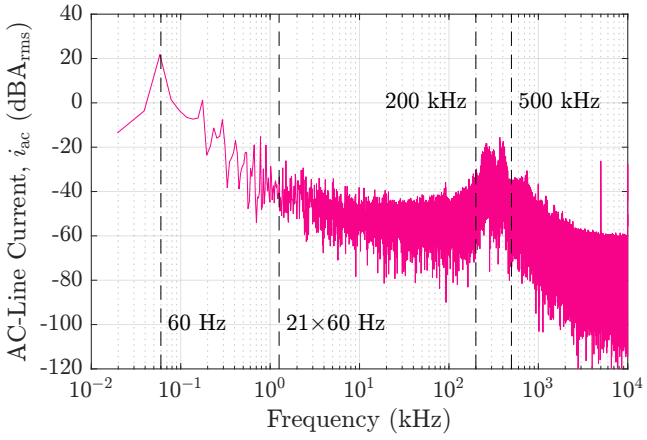


(a)

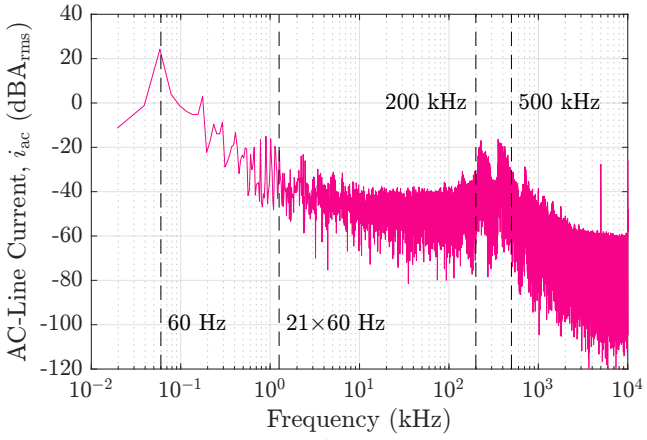


(b)

Fig. 7. Measured converter waveforms in steady-state ac-dc operation with $v_{\text{ac}} = 240\,\text{V}_{\text{rms}}$, $V_{\text{link}} = 450\,\text{V}$, and an input power of approximately (a) 3 kW, and (b) 4 kW. BCM-CCM transitions occur at different points in the cycle for different power levels due to the fixed current threshold. The ac-line current, i_{ac}, is measured with a 5-µF filter capacitance.



(a)



(b)

Fig. 8. Magnitude spectrum of the ac-line current, i_{ac}, when the converter is operated with $v_{\text{ac}} = 240\,\text{V}_{\text{rms}}$, $V_{\text{link}} = 450\,\text{V}$, and an input power of approximately (a) 3 kW, and (b) 4 kW. i_{ac} is measured with a 5-µF filter capacitance.

the input voltage, thanks to cycle-by-cycle CMC. Automatic mode transitions between BCM and CCM operation occurs based on a preset average-current threshold, and a slightly negative valley current is used in BCM to enable ZVS on all switches. The converter is disabled near the zero-crossings of the line cycle (the *deadband*) to avoid inefficient operation at very high frequencies and input-to-output ratios.

Thanks to the sinusoidal current-shaping, the unwanted frequency content of the current drawn from the ac line, i_{ac}, is relatively low, even with minimal filtering (only 5 µF in this case), as shown in Fig. 8. In particular, the total harmonic distortion (THD) at 4 kW is approximately 10.3%, using the first 20 harmonics. For comparison, the all-GaN totem-pole topology in [17] operating exclusively in BCM achieved a THD between 7.5%–18% over 0.3-3.3 kW, but with additional filtering. The variable-frequency operation results in a pair of distributed peaks between the designed minimum and maximum f_{sw}, which are approximately 40 dB below the fundamental component at 4 kW. This implies the need for reduced input filtering to meet electromagnetic interference (EMI) standards compared to fixed-frequency modulation schemes with a high-amplitude peak at a single frequency. The power-stage achieved a peak efficiency of approximately 95.5% at 3 kW.

IV. Conclusion

This work presents a digital emulator that reproduces the switching-frequency ripple of the power inductor, and leverages a 1-MHz-bandwidth current sensor to opportunistically self-calibrate the emulated waveform and avoid the impact of noise from converter switching transitions. The HF emulation enables cycle-by-cycle CMC, and allows the power loop to be better optimized since no high-bandwidth sensors are needed. A 240-V$_{\text{rms}}$-to-450-V all-GaN totem-pole PFC converter, operating at 4 kW with HCMC and automatic BCM-CCM transitions for loss optimization over the full operating range, demonstrates the effectiveness of the proposed emulation technique. To the best of the authors' knowledge, this work provides the first demonstration of HF emulation in an ac-dc converter at 450 V and above 2 kW power levels.

Acknowledgment

This work was supported by the Natural Sciences and Engineering Research Council (NSERC) of Canada and the Taiwan Semiconductor Manufacturing Company (TSMC).

REFERENCES

[1] A. B. Slimane and P. Chiu. (2021, May) GaN Power 2021: Epitaxy, Devices, Applications and Technology Trends. [Online]. Available: https://www.yolegroup.com/press-release/the-gan-power-market-will-surpass-1-billion-in-2026/

[2] M. Buffolo *et al.*, "Review and Outlook on GaN and SiC Power Devices: Industrial State-of-the-Art, Applications, and Perspectives," *IEEE Transactions on Electron Devices*, vol. 71, no. 3, pp. 1344–1355, Mar. 2024.

[3] R. Fernandes and O. Trescases, "A Multimode 1-MHz PFC Front End With Digital Peak Current Modulation," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5694–5708, Aug. 2016.

[4] M. Nasr, K. Gupta, C. da Silva, C. H. Amon, and O. Trescases, "SiC Based On-Board EV Power-Hub with High-Efficiency DC Transfer Mode through AC Port for Vehicle-to-Vehicle Charging," in *Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 3398–3404.

[5] M. E. Ahmad, F. Schafmeister, and J. Böcker, "Digital Implementation of a Current Observer with On-Line Current Sample Correction for PFC Rectifiers," in *Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2023, pp. 2867–2873.

[6] M. Biglarbegian, N. Kim, T. Zhao, and B. Parkhideh, "Development of Isolated SenseGaN Current Monitoring for Boundary Conduction Mode Control of Power Converters," in *Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, Apr. 2018, pp. 2725–2729.

[7] M. S. Zaman *et al.*, "Integrated SenseHEMT and Gate-Driver on a 650-V GaN-on-Si Platform Demonstrated in a Bridgeless Totem-pole PFC Converter," in *International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Vienna, Austria, Sep. 2020.

[8] Q. Zhang, Q. Tong, and H. Zhang, "An Inductor Current Observer Based on Improved EKF for DC/DC Converter," in *International Symposium on Computer, Consumer and Control*, Jun. 2014, pp. 892–895.

[9] J.-M. Choe, B.-J. Byen, S. Moon, and J.-S. Lai, "A capacitor current control for stand-alone inverters using an inductor current observer," in *International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Jun. 2015, pp. 1143–1148.

[10] L. Liu, Y. Zhao, Y. Yin, and J. You, "Current Sensor-less Control for Boost DC-DC Converter Based on Switched Observer," in *Annual Conference of the IEEE Industrial Electronics Society (IECON)*, Oct. 2018, pp. 1122–1127.

[11] J. Lin and G. Weiss, "Current sensorless control of bidirectional converters under mixed conduction mode," in *Conference on Decision and Control (CDC)*, Dec. 2019, pp. 8118–8123.

[12] A. Aillane *et al.*, "An Observer-Based Inductor Current Control for a Bifunctional Three-Phase DG-Inverter," in *International Ccnference on Sciences and Techniques of Automatic Control and Computer Engineering (STA)*, Dec. 2022, pp. 566–571.

[13] F. Mezger and D. Killat, "Digital observer based current loop control for buck converters - Prototype implementation on an FPGA," in *International Symposium on Industrial Electronics (ISIE)*, Jun. 2014, pp. 1336–1341.

[14] Y. Lee *et al.*, "A High-Efficiency High-Voltage-Tolerant Buck Converter With Inductor Current Emulator for Battery-Powered IoT Devices," *IEEE Transactions on Power Electronics*, vol. 38, no. 9, pp. 10 917–10 932, Sep. 2023.

[15] E. Pazouki, J. A. De Abreu-Garcia, and Y. Sozer, "Fault Diagnosis Method for DC-DC Converters Based on the Inductor Current Emulator," in *Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–6.

[16] H. Ademane, R. Attanasio, and G. Vitale, "A GaN based Totem Pole Bridgeless Power Factor Correction Circuit," in *Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, Feb. 2024.

[17] J. K. Han, "Efficiency and PF Improving Techniques with a Digital Control for Totem-Pole Bridgeless CRM Boost PFC Converters," *Energies*, vol. 17, no. 2, p. 369, Jan. 2024.