Concurrent Charge Distribution and Time-Optimal Control for Unordered Single-Inductor Dual-Output Converter

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***Abstract*—Single-inductor-multiple-output (SIMO) converters are pivotal for providing versatile V-F domains and fine-grained DVFS for many-core XPUs under stringent cost and size constraints. However, acceptable cross-regulation (CR) can only be promised in scenarios with less than 50% current discrepancies between output channels, making previous work unfeasible for frequent sleep/wake-up demands. Charging sequence reordering has emerged as a promising technique for mitigating last-channel CR in SIMO converters. However, conventional unordered control techniques introduce unwanted preceding-channel cross-regulation issues. The root cause is the mismatch in the loop response between the peak current (PC) control loop for the half-bridge and the channel-wise charge-driven loop. Although response mismatches can be alleviated through real-time calibration, significant CRs still occur during load transients with extreme channel discrepancies and hinder practical applications. To address these limitations, we introduce a calibration-free concurrent charge distribution and time-optimal control (CCD-TOC) technique. Moreover, a comparative study has explored the stability boundary and the benefits of an unfixed charging sequence. The experimental results of the single-inductor dual-output (SIDO) prototype demonstrate a transient CR of 0.176 mV/mA and a 92-mV (3.1%) undershoot against a 500-mA load step and a 400-mA (66.7%) channel discrepancy.**

***Index Terms*—SIMO Buck converters, cross-regulation, sequence re-ordering, charge expectation, digital control, time-optimal control**

I. Introduction

In typical many-core XPU designs, fine-grained DVFS and sleep/wake-up are enabled using per-core fully integrated VRs (FIVRs) or linear VRs and PLLs, thus posing major challenges to integrating many high-Q inductors within the thin package or degraded efficiency in high dropout channels. Single-inductor-multiple-output (SIMO) converters are naturally favorable for providing versatile V-F domains under stringent cost and size constraints. However, acceptable cross-regulation can only be promised in scenarios with less than 50% workload discrepancies among output channels, making prior work unfeasible for frequent sleep/wake-up demands. Fig. 2 illustrates the last-channel cross-regulation (CR) issue in ordered SIDO converters and the preceding-channel CR issue in unordered SIDO converters. In a conventional SIDO converter with a fixed charging sequence, the last channel may receive insufficient or surplus energy [1]. Therefore, the victim-last

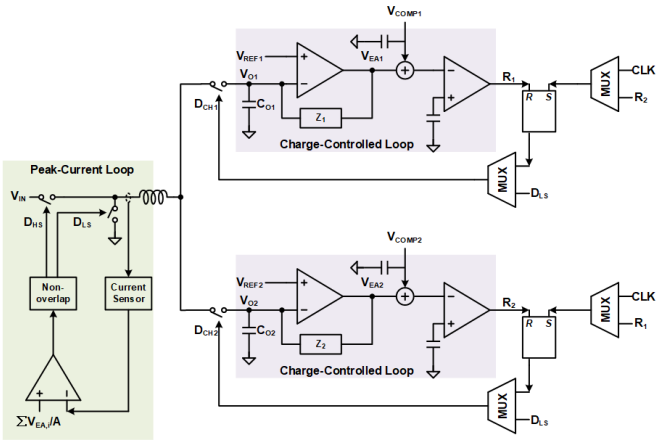

Fig. 1. General diagram of ordered/unordered SIDO Converter.

control senses which channel has the transient load and then dispatches the victim to the last place in the charging sequence [2]. Although the victim-last control addresses the last-channel CR, it introduces CR to the preceding channel, caused by the mismatch between the PC control loop and the channel-wise charge-driven loop. The duty stretching/shrinking strength of the half-bridge is intentionally bounded in time-multiplexing SIMO converters to prevent conflicts with the charged-based domain duty calculation. This conflict limits the cycle time for load transient recovery, especially when a large channel discrepancy exists. In this paper, we present an all-digital solution to supply independent V-F domains with reduced cross-regulation issues, even with a 400-mA (66.7%) channel discrepancy, via a SIMO Buck converter.

The rest of this article is organized as follows. The operation principle of the proposed concurrent charge distribution and time-optimal control is presented in Section II. The instability phenomena of ordered SIDO Buck converters are revealed by bifurcation analysis, including the effect of load parameters on stability boundaries. In Section IV, the working principle of the inductor current estimator is discussed, and the parameters are investigated for calibration. Section V gives the experimental results of the studied converter to verify the theoretical anal-

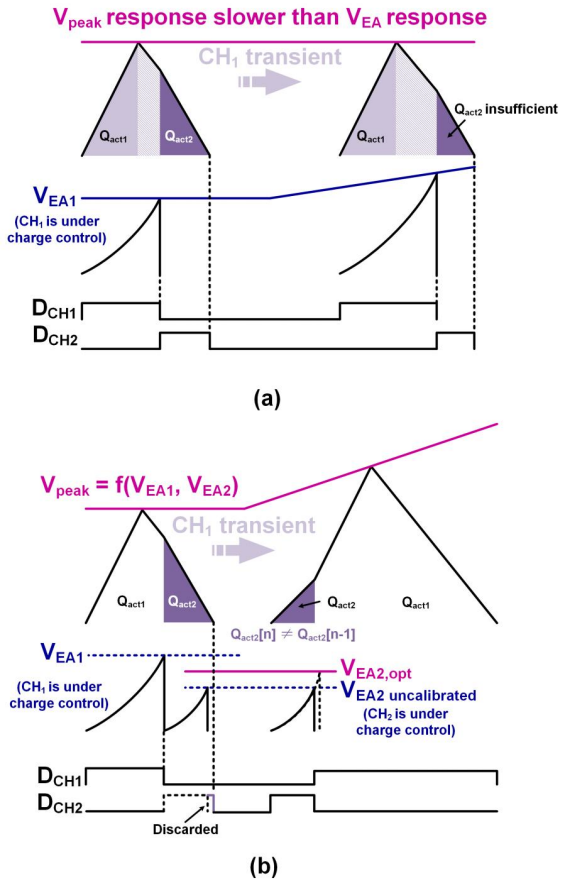

Fig. 2. Cross-regulation issues of (a) ordered and (b) unordered SIDO converters.

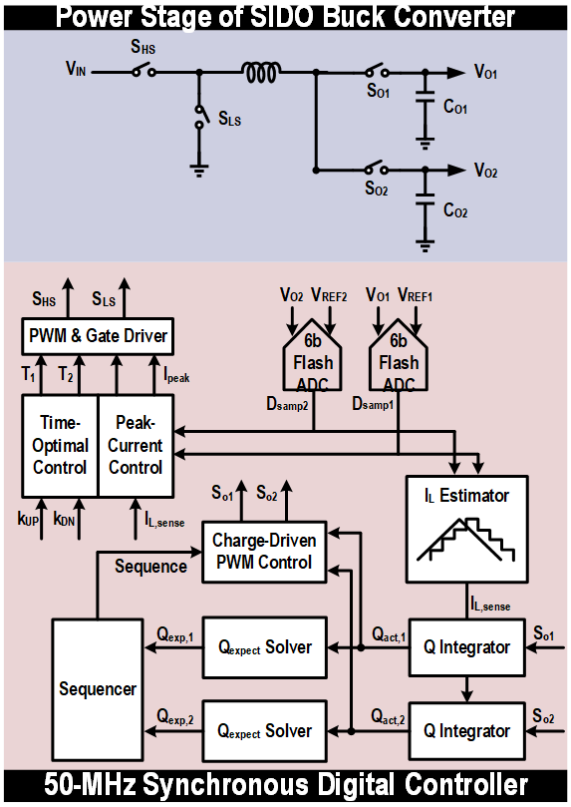

Fig. 3. Diagram of proposed SIDO architecture.

ysis, followed by the conclusion in Section VI.

II. Proposed Concurrent Charge Distribution and Time-Optimal Control

To address the above problems and unleash the full benefits of an unfixed charging sequence, we propose a concurrent charge distribution and time-optimal control (CCD-TOC) strategy with all-digital implementation. Independent control loops are assigned to the half-bridge and load switch in each channel [5]. For the half-bridge, a peak current control loop compares the estimated instantaneous inductor current and the PID-regulated reference code $I_{L,REF}$ to update the duty ratio.

$$\begin{cases} I_{L,REF}[z] = K_P \sum_{i=1}^{2} V_{err,i}[z] + \frac{K_I \sum_{i=1}^{2} V_{err,i}[z]}{z-1} \\ V_{err,i}[z] = K_q(V_{REF,i} - v_{OUT,i}[z]) \\ K_q = \frac{1}{V_{res}} \end{cases} \quad (1)$$

where V_{res} is the resolution of the ADC.

The design and calibration of the digital inductor current estimator follow [6]-[9] and will be discussed in Section IV. At each load point, a digital integrator records the charge received from the given channel in each period, which is used for calculating the charge expectation [10][11]. Unlike the victim-last control strategy [1][2], the charge expectations (Eq. 1) are resequenced at the beginning of the new period to determine the charging sequence.

$$Q_{exp}[n] = Q_{act}[n-1] + 2C_L V_{err}[n] - C_L V_{err}[n-1] \quad (2)$$

where Q_{act} and Q_{exp} are the per-channel received charge and charge expectation, respectively. For the preceding channel under charge iteration, Q_{act} is the same as Q_{exp}. When load transients between low load and rated load cause voltage undershoots/overshoots at any channel, the time-optimal control (TOC) loop takes over the regulation. During the TOC phase, the inductor current is directed to the unloaded channel at the beginning of the inductor charging/discharging sub-phases. The transient channel is always placed in the last order of voltage regulation to minimize CR in light-load channels. The charge iteration equation of the new preceding channel is derived from Eq. 1 and rewritten as shown in Eq. 2.

$$Q_{exp} = \frac{T_2}{T_1} Q_{act} + (1 + \frac{T_2}{T_1}) C_L V_{err}[n] - \frac{T_2}{T_1} C_L V_{err}[n-1] \quad (3)$$

For a large load step, the proposed TOC response involves (1) maximally slewing I_L beyond I_{load} to stop and reverse the voltage droop until T_1; (2) slewing I_L back toward I_{load}

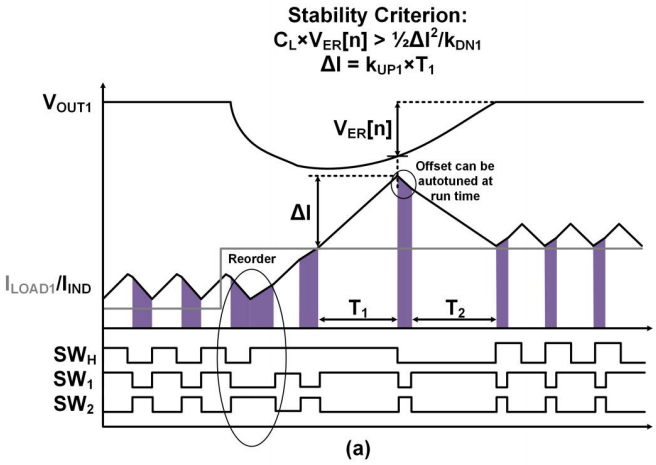

Fig. 4. Proposed CCD-TOC technique.

until T_2; (3) I_L tracks I_{load} after T_2, and the linear controller regains the overall regulation with a preset duty constant for smooth transition between the transient state and the steady state. The time intervals (denoted as T_1 and T_2 in Fig. 4) of the inductor charging/discharging subphases are recorded starting from the current crossing point where the voltage recovery begins [12][13]. Timing T_1 and T_2 precisely is pivotal for optimal response and is achieved by tracking the surplus charge $Q_{surplus}$:

$$Q_{surplus} = 1/2(k_{UP}T_1)^2/k_{DN} \tag{4}$$

where k_{UP} and k_{DN} are the slew rate of the inductor charging/discharge subphases. An optimal response is achieved when $Q_{surplus}$ provides just the right quantity of charge to restore V_{OUT} without overshooting, and it is guaranteed by continuous evaluation of the stability constraint:

$$Q_{surplus} <= C_L V_{err} \tag{5}$$

Our proposed CCD-TOC technique relaxes the matching requirement between the PC control and the channel-wise charge control, allowing the former to operate at a moderate bandwidth and achieve a wider load range without stability issues. Despite the vast adoption of time-optimal control (TOC) in single-channel digital Buck or LDO converters, this is the first work to use TOC for a SIMO converter. The details of the stability analysis will be discussed in the following section.

III. Discrete-Time Map Model and Stability Boundaries

In this section, bifurcation diagrams are utilized to explore the stability limits of conventional ordered SIDO converters. The derivation of the discrete-time map model follows [14][15]. An ordered SIDO converter with two output channels has four available switching states, which is defined by Eq. 6-9 and shown in Fig. 5.

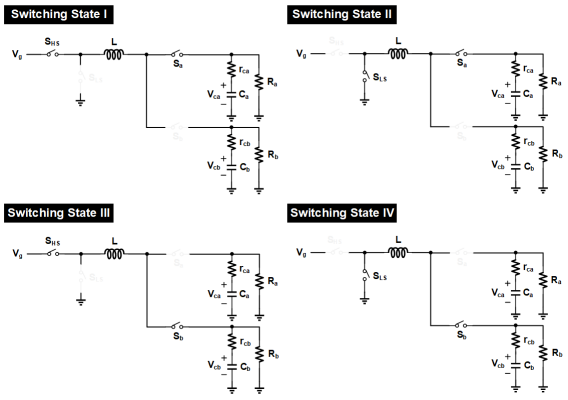

Fig. 5. Switching states of ordered SIDO converter..

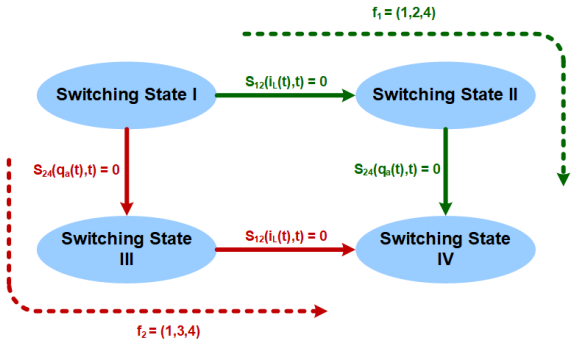

Fig. 6. Two switching state sequences.

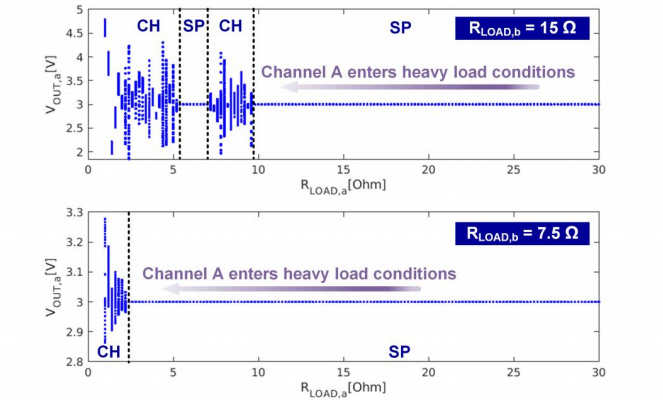

Fig. 7. Bifurcation diagrams of ordered SIDO converter.

$$\begin{cases} \frac{di_L}{dt} = \frac{V_g}{L} - \frac{R_a r_{ca} i_L}{L(R_a+r_{ca})} - \frac{R_a v_{ca}}{L(R_a+r_{ca})} \\ \frac{dv_{ca}}{dt} = \frac{R_a i_L}{C_a(R_a+r_{ca})} - \frac{v_{ca}}{C_a(R_a+r_{ca})} \\ \frac{dv_{cb}}{dt} = -\frac{v_{cb}}{C_b(R_b+r_{cb})}. \end{cases} \tag{6}$$

$$\begin{cases} \frac{di_L}{dt} = -\frac{R_a r_{ca} i_L}{L(R_a+r_{ca})} - \frac{R_a v_{ca}}{L(R_a+r_{ca})} \\ \frac{dv_{ca}}{dt} = \frac{R_a i_L}{C_a(R_a+r_{ca})} - \frac{v_{ca}}{C_a(R_a+r_{ca})} \\ \frac{dv_{cb}}{dt} = -\frac{v_{cb}}{C_b(R_b+r_{cb})}. \end{cases} \tag{7}$$

$$\begin{cases} \frac{\mathrm{d}i_L}{\mathrm{d}t} = \frac{V_g}{L} - \frac{R_b r_{cb} i_L}{L(R_b+r_{cb})} - \frac{R_b v_{cb}}{L(R_b+r_{cb})} \\ \frac{\mathrm{d}v_{ca}}{dt} = -\frac{v_{ca}}{C_a(R_a+r_{ca})} \\ \frac{\mathrm{d}v_{cb}}{\mathrm{d}t} = \frac{R_b i_L}{C_b(R_b+r_{cb})} - \frac{v_{cb}}{C_b(R_b+r_{cb})}. \end{cases} \tag{8}$$

$$\begin{cases} \frac{\mathrm{d}i_L}{\mathrm{d}t} = -\frac{R_b r_{cb} i_L}{L(R_b+r_{cb})} - \frac{R_b v_{cb}}{L(R_b+r_{cb})} \\ \frac{\mathrm{d}v_{ca}}{dt} = -\frac{v_{ca}}{C_a(R_a+r_{ca})} \\ \frac{\mathrm{d}v_{cb}}{\mathrm{d}t} = \frac{R_b i_L}{C_b(R_b+r_{cb})} - \frac{v_{cb}}{C_b(R_b+r_{cb})}. \end{cases} \tag{9}$$

As shown in Fig. 6, the independent control of the half-bridge and channel-wise conduction time leads to two potential switching sequences. The transition between adjacent switching states occurs when meeting Eq. 10 or Eq. 11.

$$\begin{cases} S_{12}(i_L(t), t) = i_L(t) - i_{L,REF} = 0 \\ S_{24}(q_a(t), t) = q_a(t) - q_{a,REF} = 0. \end{cases} \tag{10}$$

$$\begin{cases} S_{13}(q_a(t), t) = q_a(t) - q_{a,REF} = 0 \\ S_{34}(i_L(t), t) = i_L(t) - i_{L,REF} = 0. \end{cases} \tag{11}$$

TABLE I
RATED CIRCUIT PARAMETERS OF SIDO BUCK CONVERTER

Variable	Definition	Value
V_g	Input Voltage	8 V
R_a, R_b	Load resistors of channel a and channel b	30 Ω, 15 Ω
V_{ca}, V_{cb}	Output voltages of channel a and channel b	3.3 V, 5 V
L	Inductor	3.9 µH
C_a, C_b	Capacitors of channel a and channel b	20 µF
r_{ca}, r_{cb}	ESR resistors	2.5 mΩ
K_P, K_I	Proportional and integral parameters	0.01, 0.001
K_q	Quantization gain	1

Bifurcation diagrams with the variation of load parameters are presented based on the established discrete iterative map model. The rated parameters are listed in Table. I, extracted from the prototype in Section IV. The iterative calculation begins from $x_1 = 0$ and stops at the 5000^{th} period with a 2-ns step. Finally, the last 50 points at the end of the simulation are used to draw the bifurcation diagram. As shown in Fig. 7, the motion orbit mutates from stable period-1 (SP) to chaos (CH) via border-collision bifurcation as the leading channel enters heavy-load conditions. When the trailing channel has a 15-Ω resistive load (333 mA), the collision point is around 300 mA. When the trailing channel has a 7.5-Ω resistive load (666 mA), the collision point is around 1.2 A. In conclusion, the border collision occurs as the channel discrepancy increases. This transition hinders the dynamic range of ordered SIDO converters and highlights the superiority of the proposed charge-expectation-driven reordering technique.

IV. DIGITAL INDUCTOR CURRENT ESTIMATION

DCR current sensing is one of the main methods of analog current sensing, and the working principle expression is shown as Eq. 12:

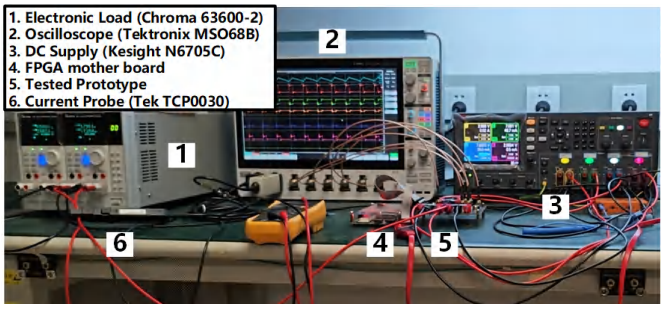

Fig. 8. Experimental setup.

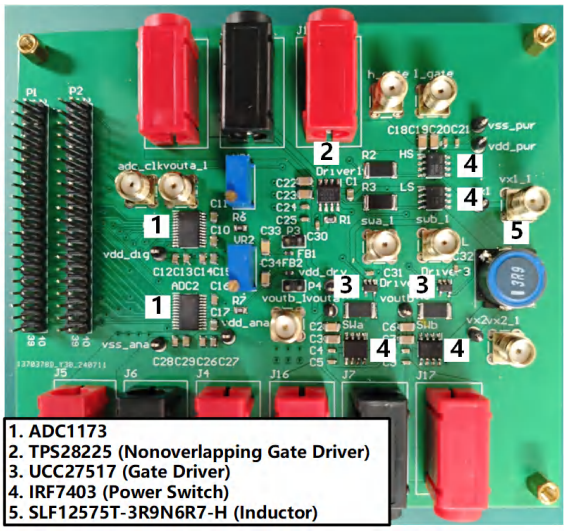

Fig. 9. Tested Prototype.

$$I_{sense} = \frac{V_L(s)}{sL_e + R_{Le}} \frac{I_L(s)R_L}{R_{Le}} \frac{1 + s\frac{L}{R_L}}{1 + s\frac{L_e}{R_{Le}}} \tag{12}$$

where L_e and R_{Le} are the estimated inductance and DCR value set in the filter, respectively. By manipulating and applying the bilinear transformation, the digital equivalence of Eq. 12 can be obtained as given in [8]. The calibration procedure of the parameters (L_e and R_{Le}) consists of two steps: (1) gain calibration and (2) time constant calibration. Similar to [7], a 50-MHz sampling clock (100 times the switching frequency) with low-pass filtering is used to eliminate the estimation error of the averaged duty cycle D for accurate calculation of V_L:

$$V_L[n] = D \times V_g[n] - V_o[n] \tag{13}$$

To track the channel-wise R_{ds} of the power switches, while a test current sink circuit with known load change ΔI_{test} is applied in one channel, the other channel will be disabled and disconnected from the half-bridge. The online calibration procedure will be repeated twice and the estimated equivalent resistance R_{eq} of the entire converter becomes:

$$R_{eq} = R_L + D_{CH1}[n]R_{ds,1} + D_{CH2}[n]R_{ds,2} \tag{14}$$

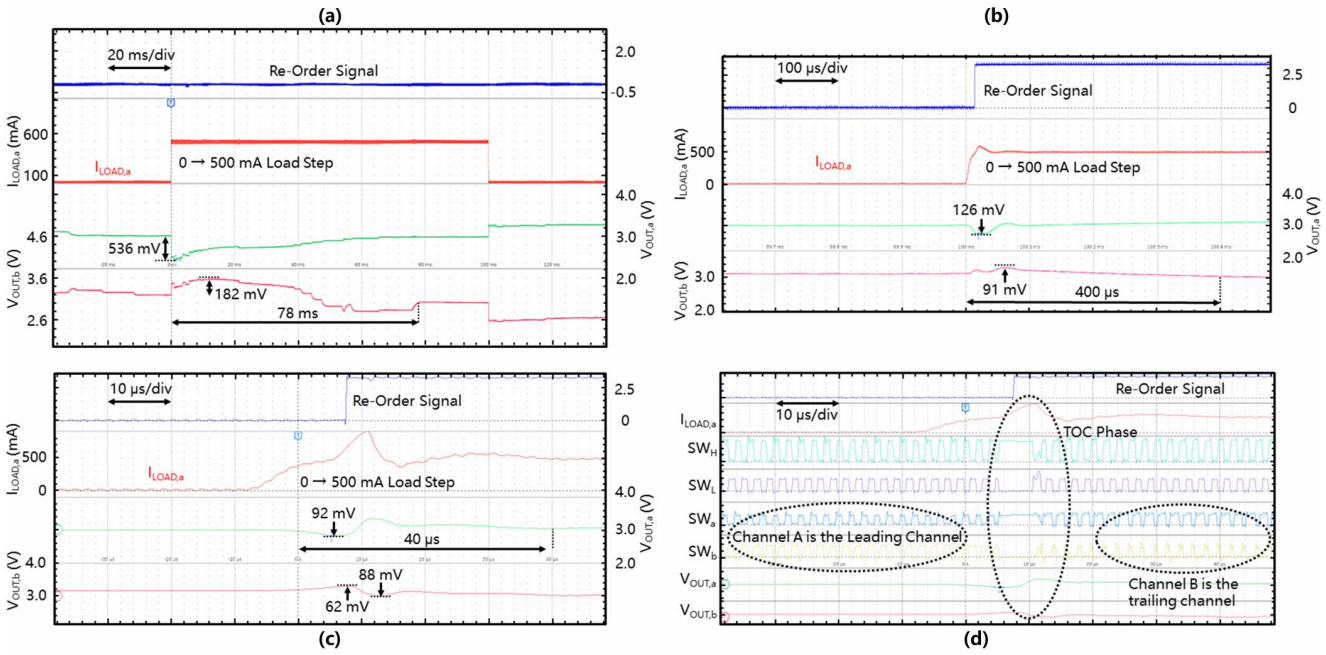

Fig. 10. Waveforms of load transient responses (a) without sequence re-ordering or time-optimal control (TOC); (b) with sequence reordering and well-tuned PID control; (c) with sequence reordering and TOC and (d) its detailed gate driving signals (right).

where D_{CH1} and D_{CH2} are the average conduction time of each channel within a switching period. Eq. 14 is used to replace R_L in Eq. 12 and regard R_{ds} of the power switch as a part of the DCR resistance.

V. Experiment Verification

An experimental prototype of a SIDO CCM buck converter is implemented with IRF7403 MOSFET as power switches, TPS28225 and UCC27517 as gate drivers. The 500-kHz gate driving signals are generated by FPGA with a 6.25-MHz ADC sampling frequency. Figs. 10 (a)-(d) present the experimental waveforms of output voltages, current loads, and gate driving signals of the tested prototype. The resistive loads of each channel are 30 Ω and 15 Ω, respectively. Compared Fig. 3(b) with the baseline in Fig. 3(a), channel sequence reordering prevents the response mismatches between the peak-current control loop and channel-wise charge iteration loops. When applying a 500-mA load step to the original preceding channel A, the voltage undershoot (V_{US}), the cross-regulation (CR), and the settling time (T_{SETTLE}) are reduced to 126 mV, 91 mV, and 400 μs by dispatching the unloaded channel B as the new leading channel. As shown in Fig. 3(c)-(d), concurrent sequence reordering and time-optimal control further reduce V_{US} and T_{SETTLE} to 92 mV and 40 μs without deterioration in CR. Table II lists the parameters of previous works with the standalone charge control, the standalone unordered control, and the standalone time-optimal control. Owing to the concurrent utilization of unordered charge control and time-optimal control, this work achieved one of the best undershoots and CR against one of the largest load steps and channel discrepancies.

VI. Conclusion and Future Work

The major contributions of our work are concluded here:

- We proposed a calibration-free concurrent charge distribution and time-optimal control (CCD-TOC) technique to address both the last-channel CR issue of ordered SIDO converters and the preceding-channel CR problem introduced by conventional reordering techniques.
- We rendered a charge-expectation-driven reordering technique and conducted analytical models to explore the stability boundaries.
- We introduced channel discrepancy as a supplement to cross-regulation to give a comprehensive performance evaluation of SIDO converters for real-world applications.

Although the proposed CCD-TOC technique was verified by a simple Buck prototype with only two output channels, neither the converter topology nor the number of output channels is a fundamental constraint. The following methodologies are proposed for future investigation to exploit the positive impact of out-of-order control on performance and power efficiency in practical applications.

- To support concurrent load changes in more than one channel, the victim channels should be bundled during the time-optimal control phase. The reordering within the bundle will be executed at a higher frequency to guarantee the channel-wise crossing points are close to each other for precise timing of T_1 and T_2.
- With a proper decomposition of the I_L estimation error [6], iterative correction of the current estimator can be achieved without interrupting the converter operation.

TABLE II
COMPARISON TABLE WITH PRIOR WORKS

Parameter	*TPE'12 [6]*	*ISSCC'21 [10]*	*TIE'21 [1]*	*APEC'24① [16]*	*TCAS-I'24 [2]*	***This work***
No. of channels	2 Boost	4 Buck	2 Buck	2 Boost	4 Buck	**2 Buck**
Control Scheme	Ordered Charge Control (Digital)	Ordered Charge Control (Digital)	Unordered TOC Control (Digital)	Ordered Charge Control (Analog)	Unordered Charge Control (Analog)	**Unordered Charge & TOC Control (Digital)**
Supply Voltage	2.5 V	1.8 V	3.3 V	2.7 V – 4.5 V	5 V	**5 V – 12 V**
C_{OUT} / L_{IND}	10 µF / 4.7 µH	1 µF / 10 µH	10 µF / 4.7 µH	22 µF / 1 µH	22 µF / 1 µH	**20 µF / 3.9 µH**
F_{SW}	390 kHz	2.5 MHz	1 MHz	2 MHz	1.5 MHz	**500 kHz**
Load Step / Undershoot	350 mA / 500 mV (12.5 %)	78 mA / 33 mV (3.3 %)	190 mA / 95 mV (5.3 %)	600 mA / 69 mV (1.1 %)	225 mA / 145 mV (9.7 %)	**500 mA / 92 mV (3.1 %)**
Channel Discrepancy②	200 mA / 430 mA (46.5 %)	106 mA / 101 mA (105 %)	N/A	350 mA / 600 mA (58.3 %)	380 mA / 375 mA (101.3 %)	**200 mA / 600 mA (33.3 %)**
Cross Regulation	0.429 mV/mA	0.359 mV/mA	0.05 mV/mA	0.060 mV/mA	0.057 mV/mA	**0.176 mV/mA**
FoM③	0.199 mV/mA	0.377 mV/mA	N/A	0.035 mV/mA	0.058 mV/mA	**0.058 mV/mA**

[1]SIMPLIS simulation results; [2]Channel Discrepancy = The current sum of unloaded channels / The maximum load of the victim channel; [3]FoM = Cross Regulation × Channel Discrepancy.

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