An USB Cable Based Extended Conversion Range L-First Hybrid-Converter using Valley-Virtual-Inductor-Current-Mode Control with Auto-Tracking Slope Compensation against ±50% Inductance Variation

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***Abstract*—This paper introduces an L-first hybrid converter with extended conversion ratio that uses an USB cable as the power inductor to maximize power density both on-chip and on-PCB. The inductor current, reduced by the conversion ratio, naturally equals the input current, enabling the USB cable to function effectively as an inductor despite its parasitic resistance. The converter achieves an estimated power density of 3.3 W/3mm³ with a peak efficiency of 95%. To accommodate varying USB cable lengths, a valley-virtual-inductor-current mode control with auto-tracking slope compensation is proposed. This scheme eliminates the need for inductor current sensing and adjusts slope compensation based on changes in voltage and inductance. A 5 V input and 1.8–3.3 V output prototype, implemented in a 180 nm BCD process, covers inductances from 500 nH to 1 µH, corresponding to USB cable lengths of 1 to 2 meters.**

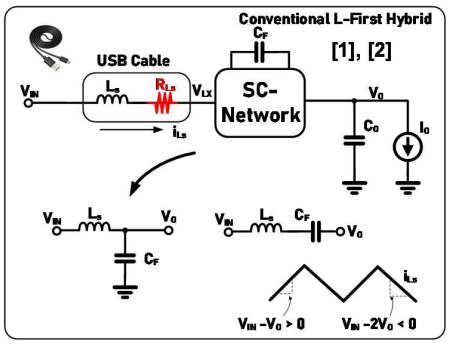
Keywords—Hybrid converter, USB cable, auto-tracking slope compensation, valley-virtual-inductor-current

I. Introduction

Modern mobile and IoT devices require efficient, compact power management solutions that can operate directly from a USB cable (5 V) for charging and discharging batteries. Conventional buck converters struggle to achieve both high power density and efficiency due to increased DCR and conduction losses from miniaturized inductors, particularly on the high-current side. To mitigate these losses, inductor-first topologies [1]–[3] place the inductor on the input side, where it handles lower current, reducing conduction losses. Some L-first designs even use the USB cable as the inductor to boost power density [1]. However, these traditional L-first topologies face challenges, including a limited conversion ratio of 0.5–1 and controller design difficulties for varying USB cable inductances. This digest extends the traditional L-first converter [1] from a dual-path to a triple-path design, expanding the conversion ratio to 1/3–1 by adding a flying capacitor and switch network. A virtual-inductor-current (VIC) technique is employed to enable valley current mode modulation, eliminating the need for current sensing circuitry, which is challenging in L-first converters. Additionally, an auto-tracking slope compensation technique is developed to handle large inductance variations.

II. USB-Cable Based L-First Converter With Extended Conversion Range

Fig. 1(a) illustrates the basic concept of a traditional L-first hybrid converter, which uses an output switching network to transfer the switching node V_{LX} toggling between V_O and $2V_O$ for inductor charging and discharging. This approach limits the conversion ratio to a range of 0.5 to 1, as determined by the volt-second balance. By simply modifying the switching network, following the concept in Fig. 1(a), a new L-first converter that operates with can be developed, extending the conversion range to 1/3 to 1, making it suitable for mobile devices powered by a USB cable. The actual implementation of the converter and its operating states are shown in Fig. 2. Notably, the inductor current is equal to the input current, which reduces the inductor current stress by the conversion ratio M (= 1/(3-2D)). A comparison of inductor current stress, inductor current ripple, estimated inductor volume, additional on-board capacitor requirements, and total volume for various converters, including buck, 3-level, and double-step-down converters, is provided in Table I. Since this architecture uses the USB cable as a parasitic inductance along with appropriate control methods, there's no need for an external inductor. Consequently, compared to other converters, the power density can be significantly increased. An estimated volume of 3 mm³ by accounting passive devices and power density of 3.3 W / 3 mm³ is achieved and gradually superior to conventional converter!!



(a)

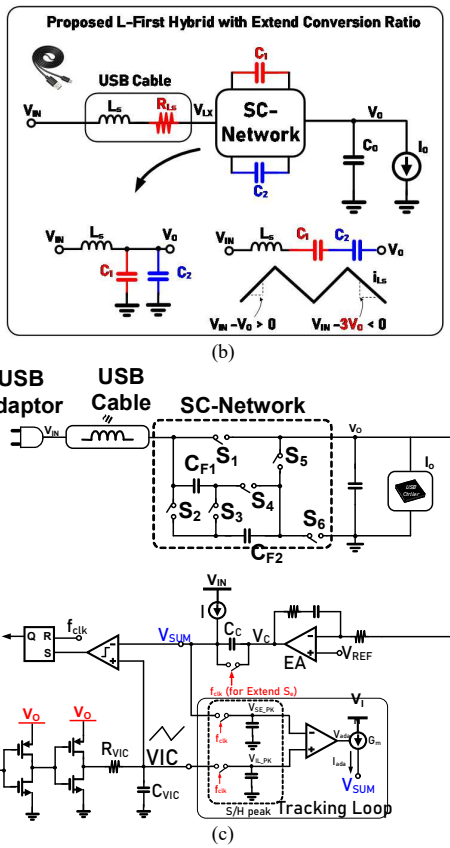


Fig. 1. concept of (a): conventional L-first converter, (b): proposed L-first with extended conversion ratio, (c): architecture of the proposed converter

TABLE I.
COMPARISON OF TOPOLOGY

Topology	i_{LS}/I_O	Δi_{LS}	Estimated L	C_F / C_O	Total Volume
Buck	1	$\frac{V_{IN}(1-M)M}{L_s F_{SW}}$	500nH, 4mΩ DCR 100 mm^3	0 / 1 mm^3	100 mm^3
3-L Buck [4]	1	$\frac{V_{IN}(1-M)M}{2L_s F_{SW}}$	250nH, 4mΩ DCR, 25 mm^3	1 / 1 mm^3	26 mm^3
DSD Buck [5]	1/2	$\frac{V_{IN}(1-2M)M}{L_s F_{SW}}$	250nH X 2, 4mΩ DCR, 50 mm^3	1 / 1 mm^3	52 mm^3
Proposed	M	$\frac{V_{IN}(1-M)M}{L_s F_{SW}}$	500nH – 1000nH, 50mΩ DCR (USB Cable)	2 / 1 mm^3	3 mm^3

III. The Concept Of The Proposed Converter

The proposed triple path converter is illustrated in Figure. 1(c). Since the inductor is connected to Vin, the inductance can be implemented using the parasitic inductance of a USB cable, leading to a significant improvement in power density. It is evident that the parasitic inductance value is related to the cable length and independent of the cable shape [5], indicating the stability of the parasitic inductance value. We measured one testing cable's inductance using an Impedance Analyzer and found it to be 750nH with a DC resistance of 10mΩ. Subsequent derivations of L are based on this set of data.

A. Operating principle

Fig. 2 depicts the two states of the circuit in normal mode. As shown in Fig. 2(a) , In state A, capacitors C_1 and C_2 are connected in parallel with V_o. From this, it can be inferred that when the switching frequency is sufficiently high, C_1 and C_2 will be approximately equal to V_o and can achieve auto balance. Inductor and capacitors supply I_o through the parallel connection of V_o. And in state B, I_{LS} charges C_1 and C_2 to maintain the principle of capacitor charge balance in one cycle.

The voltage conversion ratio can be calculated based on charge flow analysis [9]. The deduced result is consistent with using voltage second balance. First, we assume output capacitor is very large. Then, calculate the conversion ratio by dividing the total input charge by the total output charge.
It follows that:

$$q_{in}^A = I_{Ls}DT \quad , \quad q_{in}^B = I_{Ls}(1-D)T \tag{1}$$

$$q_o^A = q_{in}^A + 2q_{in}^B \quad , \quad q_o^B = q_{in}^B \tag{2}$$

$$\text{Conversion ratio (M)} = \frac{q_{in}^A + q_{in}^B}{q_o^A + q_o^B} = \frac{1}{3-2D} \tag{3}$$

By using the formula in ideal case $P_{in} = P_{out}$ and $I_{in} = I_{Ls,DC}$, we can derive:

$$I_{in} = I_{Ls,DC} = MI_o \tag{4}$$

$$\Delta I_{Ls} = \frac{1}{L}(V_{in} - V_O)DT = \frac{V_{in}}{L}T(1-M)\left(\frac{3}{2} - \frac{1}{2M}\right) \tag{5}$$

With the derivations provided above, we can easily observe that $I_{Ls,DC}$ is reduced by a factor of M when compared to the conventional buck converter and 3-level buck converter, and this reduction is directly related to DCR loss.

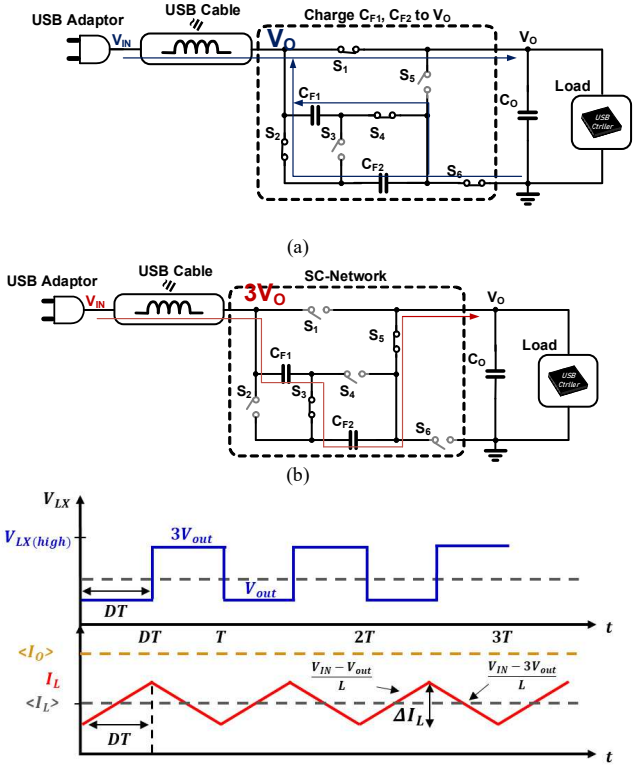


Fig. 2. The proposed converter: (a)State A (b)State B (c)Steady State Waveform

B. Conduction Loss Analysis and Cflly hard charging Loss

Because of the hard-charging issue with C_1 and C_2, it is difficult to analyze Ro using conventional methods. Thus, charge flow analysis is applied to estimate the hard-charging average current and determine Ro. A charge-flow analysis framework is presented as follows: From Fig .2 , we derive the charge flows of the two states at (1), encompassing input (q_{in}^A, q_{in}^B). Next, by utilizing the charge flowing through the switch and the conduction time, we can calculate the average current during each switch conduction. Substituting this into the energy formula $E = I^2R * t_{on}$, we can obtain the losses on each switch. Then, by using the relationship between $I_L$and I_o, we can determine the equivalent output resistance $R_{o,cond}$. Fig. 3 presents the graph of Ro corresponding to f_{sw}, serving as a reference for selecting the switching frequency.

$$R_{o,cond} = R_{o,FSL} = \left(\frac{1}{3-2D}\right)^2 \left(\frac{(2-D)^2}{D}R_{SW1} + \frac{(1-D)^2}{D}R_{SW2} + (1-D)R_{SW3} + \frac{(1-D)^2}{D}R_{SW4} + (1-D)R_{SW5} + \frac{(1-D)^2 * 4}{D}R_{SW6}\right) \quad (6)$$

The SSL loss analysis:

$$\frac{\Delta q^2}{2CT} = I_O^2 R_{o,SSL}\,, \Delta q = I_L(1-D)T \quad (7)$$

By using (3),(4) and (7):

$$R_{o,SSL} = \frac{(1-D)^2}{C_{flyF_{SW}}(3-2D)^2} \quad (8)$$

$$R_{O,total} = \sqrt{{R_{o,cond}}^2 + {R_{o,SSL}}^2} \quad (9)$$

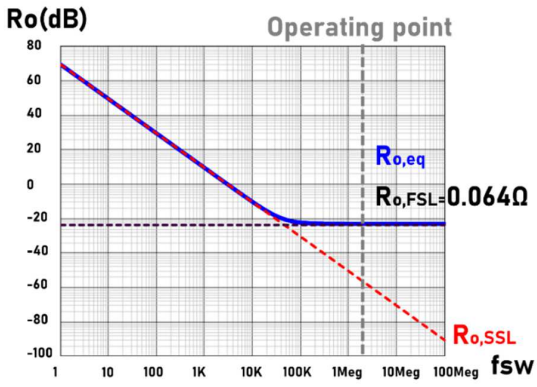


Fig. 3 Conduction loss contribution of Switches and C_1, C_2 charging loss.

IV. Valley VIC Control With Auto-Tracking Slope Compensation

To address the challenges of inductance variation when using a USB cable, we propose a valley virtual-inductor-current (VIC) mode control with auto-tracking slope compensation. Fig. 3 illustrates the control loop of the proposed scheme, which is a modification of conventional valley current mode control [6]. Instead of using the actual inductor current, a "virtual-inductor-current" [7] is generated by passing the duty cycle through two inverters, sourced by the output voltage V_O, to create an inductor current-shaped signal. An error amplifier senses the output voltage and compares it to a reference voltage V_{REF}, generating V_C for modulation. Slope compensation is applied directly to V_C using a stacked capacitor C_C and a charging current source, eliminating the need for a current sensor while maintaining the control dynamics and type-II compensation. This approach is particularly suitable for L-first hybrid converters, where inductor current sensing is challenging. The slope compensation is implemented at the output of the type-II compensation with a stacked current source charging the capacitor, reducing the need for an additional analog adder and enabling adaptive slope compensation.

The adaptive slope compensation tracks the modulation waveform to ensure stability across varying inductance and V_{IN}/V_O conditions. Based on the modulation waveform shown in Fig. 4(a):

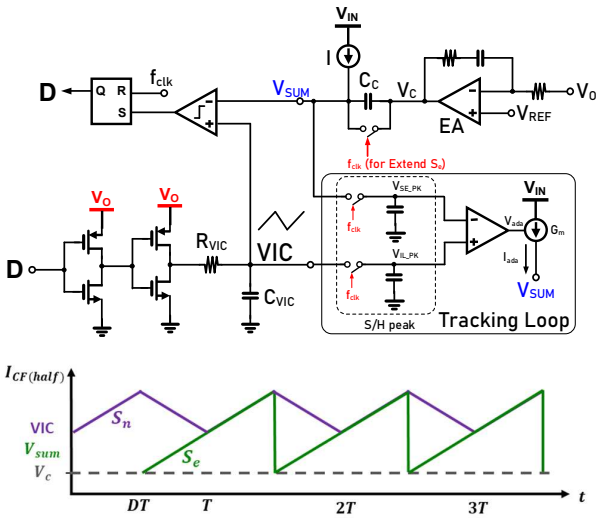
$$VIC_{max} = V_c + S_e * (1-D)T + S_n * DT \quad (10)$$

If $S_e = S_n$:

$$V_{SUM,max} = V_c + S_e * T = VIC_{max} \quad (11)$$

Based on the (11), the automatic tracking loop samples the peak value of V_{SUM} and VIC at the clock edge and adjusts the slope compensation to match the modulation current ramp's rising slope S_n. If $V_{SUM,max} > VIC_{max}$, V_{ada} will decrease, so the current flow into C_c is decreased which cause $V_{SUM,max}$ decrease. By the same concept if $V_{SUM,max} < VIC_{max}$, V_{ada} and $V_{SUM,max}$ will increase.

This tracking loop ensuring $S_e = S_n$ [8], which prevents subharmonic oscillation under all operating conditions, even with ±50% inductance variation. The simulated control-to-output transfer function G_{vc} in Fig. 4 confirms the absence of subharmonic instability, as indicated by the lack of $f_{sw}/2$ complex poles.



(a)

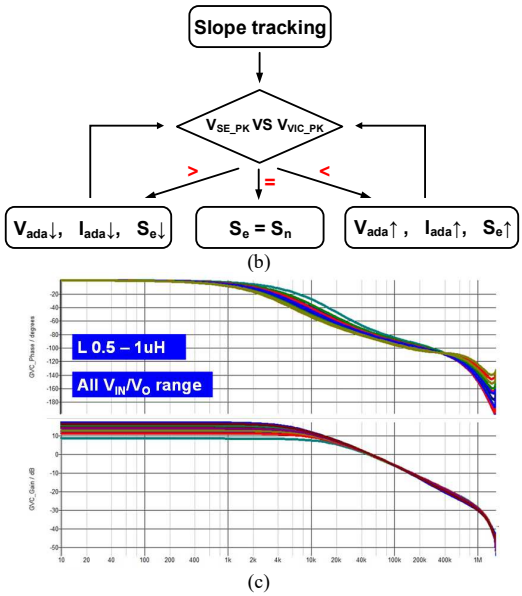


Fig. 4 The Valley VIC control with auto-slope compensation tracking technique

V. Simulation Results

Fig. 5 (a) shows the load transient response of valley VIC control. During load transients, V_{sum} decreases due to the feedforward action of V_o. At the same time, V_c rises as the error between V_o and V_{REF} becomes large, especially when V_o experiences a significant drop under heavy load. This causes the duty cycle to be activated quickly.

From Fig. 5(b), it shows the waveform with an inductance variation of 50%. This waveform shows that the system remains stable in every condition. Besides, when the output current (Io) ranges from 0 to 1 A, the settling time is 12 us in the worst-case scenario.

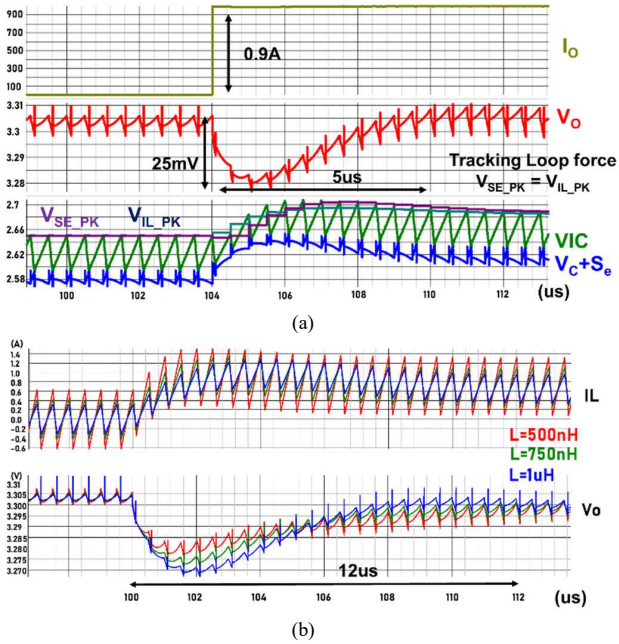


Fig. 5. Simulation waveform: (a)load transient response (b)load transient response with inductance variation

We first build up a PCB prototype design with a measured efficiency of 5 V to 3.3 V after whole chip tape out shown in Fig. 6 to verify the converter. The peak efficiency is 95.7% of this prototype PCB. The on-chip version will increase the maximum loading current to 3 A and the power density will be increased to around 10 W / 3mm^3 with flying capacitor and output capacitor mounted on die.

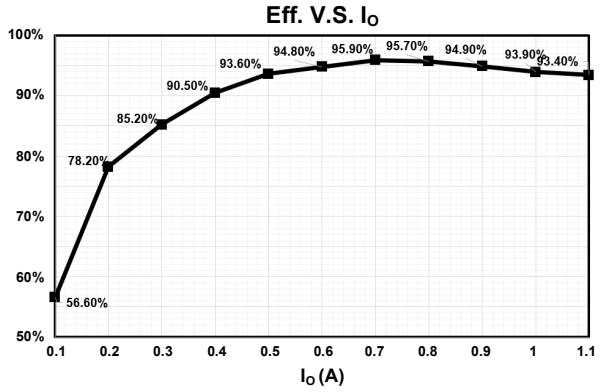


Fig. 6 Efficiency measured on prototype PCB version proposed converter

VI. Conclusion

This paper presents an L-first hybrid converter with extended conversion ratio and generalized valley-VIC-control scheme with auto-tracking slope compensation against USB cable ±50% inductance variation. The converter has been implemented a 180 nm BCD process, achieving a peak efficiency of 95.7% and 3.3 W / 1mm^3 power density. The chip fabrication process and measurement are in progress.

	[1] TIE 2020	[3] JSSC 19	[11] ISSCC 23	[10] JSSC 24	This work
Technology	DSP Ctrller	130nm	180nm	180nm	180nm
Topology	L-1st 1C_F	L-1st 1C_F 3C_o	L-1st 1C_F	2Phase L-1st 2C_F	L-1st 2C_F
Control scheme	V-mode	V-mode	V-mode	V-mode	V-VIC
V_O(V)/ V_{IN}(V)	3.3 / 5	3 - 4.2 / 9	8 - 12.6 / 12-20	0.8 - 1.8 / 1.5 - 3.3	1.6–3.3 /5
f_{sw}(MHZ)	2	2	5	0.5	2
Ls(uH) / Co(uF)	Cable (1) / 13.2	Cable (0.5)/4.4	Cable (1) / N.A.	1*2 /4*4.7	Cable (0.75) / 10
Inductance Variation Tolerance	X	X	X	X	50%
Peak-Eff(%)	90	96	95.1	97.3	95.9
$I_{o,MAX}$(A)	3.9	3	3.3	3.3	4

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References

[1] G. -S. Seo and H. -P. Le, "S-Hybrid Step-Down DC–DC Converter—Analysis of Operation and Design Considerations," *IEEE Tran.s on Industrial Electronics*, vol. 67, no. 1, pp. 265-275, Jan. 2020.

[2] A. Abdulslam and P. P. Mercier, "A Battery-Connected Inductor-First Flying Capacitor Multilevel Converter Achieving 0.77W/mm2 and 97.1% Peak Efficiency," in *Proc. 2021 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, USA, 2021, pp. 1-2.

[3] Casey Hardy, Yogesh Ramadass, Kevin Scoones, Hanh-Phuc Le, "A Flying-Inductor Hybrid DC–DC Converter for 1-Cell and 2-Cell Smart-Cable Battery Chargers", *IEEE Journal of Solid-State Circuits*, vol.54, no.12, pp.3292-3305, 2019.

[4] X. Liu, P. K. T. Mok, J. Jiang and W. -H. Ki, "Analysis and Design Considerations of Integrated 3-Level Buck Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 5, pp. 671-682, May 2016.

[5] J. Yuan, Z. Liu, F. Wu and L. Cheng, "A 12V/24V-to-1V DSD Power Converter with 56mV Droop and 0.9\mu \mathrm{S}$ 1% Settling Time for a 3A/20ns Load Transient," in *Proc. 2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 1-3.

[6] J. Li and F. C. Lee, "Modeling of V2 Current-Mode Control," in *Proc. 2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, USA, 2009, pp. 298-304.

[7] Y.-C. Lin, C.-J. Chen, D. Chen, B. Wang, "A Ripple-Based Constant On-Time Control With Virtual Inductor Current and Offset Cancellation for DC Power Converters," *IEEE Transactions on Power Electronics*, Vol. 27, No.10, pp. 4301 - 4310, 2012.

[8] P. -H. Liu, Y. Yan, F. C. Lee and P. Mattavelli, "External ramp autotuning for current mode control of switching converters," in *Proc. 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, 2013, pp. 276-280.

[9] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," in IEEE *Trans. on Power Electronics*, vol. 23, no. 2, pp. 841-851, March 2008.

[10] X. Zhang et al., "An Outphase-Interleaved Switched-Capacitor Hybrid Buck Converter With Relieved Capacitor Inrush Current and COUT-Free Operations," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 4, pp. 1078-1092, April 2024.

[11] Z. Tong, J. Huang, Y. Lu and R. P. Martins, "A 42W Reconfigurable Bidirectional Power Delivery Voltage-Regulating Cable," in *Proc. 2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 192-194.