Design and Control for Switch-Mode Voltage Regulation by Gyrator Resonant Switched-Capacitor Converters

Thesis submitted in partial fulfillment

of the requirements for the degree of

"DOCTOR OF PHILOSOPHY"

By

Alon Cervera

Submitted to the Senate of Ben-Gurion University

of the Negev

14.10.2018

Beer-Sheva

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Approved by the advisor:
Prof. Mor Mordechai Peretz

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Prof. Dudy Bar-Zvi

14.10.2018

Beer-Sheva

This research was carried out under the supervision of:

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The Center of Power Electronics and Mixed-Signal IC (PEMIC)

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Research-Student's Affidavit when Submitting the Doctoral Thesis for Judgment

I___Alon Cervera_____, whose signature appears below, hereby declare that

(Please mark the appropriate statements):

_✓_ I have written this Thesis by myself, except for the help and guidance offered by my Thesis Advisors.

_✓_ The scientific materials included in this Thesis are products of my own research, culled from the period during which I was a research student.

___ This Thesis incorporates research materials produced in cooperation with others, excluding the technical help commonly received during experimental work. Therefore, I am attaching another affidavit stating the contributions made by myself and the other participants in this research, which has been approved by them and submitted with their approval.

Date: ___14.10.2018____ Student's name: ___Alon Cervera___

Signature:_____

Acknowledgements

First, I would like to thank my advisor Prof. Mor Mordechai Peretz for six years of support and extreme dedication to my establishment as a researcher. In these six years we have travelled a long way together with him not only being a tutor, but also a true supporting friend, helping me out when in need.

Next, I would like to personally thank Eli Abramov, my colleague and friend for the last three years at the 'Power-electronics and mixed-signal IC' (PEMIC). We have made great achievements through mutual support. Although our research interests were different, we spent hours discussing our research to solve the latest problems each one had. I would also like to thank Or Kirshenboim, who was also part of PEMIC in my study years, in which we had big collaborations. In our different take on things we managed to produce outstanding results.

Many thanks to the rest of the staff, Dr. Michael Evzelman and Mr. Azrikam Yehieli - I have learnt many practices from each of you guys, which I'm taking with me today. I would also like to thank some particular junior graduate and undergraduate students: Alex Mindel, Bar Halivni, Hagit Perets, and Sivan Aharon: we've formed true friendships together, you guys have provided lots of liveliness to PEMIC and allowed me to acquire key management skills which I put to practice today.

Most importantly, I would like to thank my wife, Moran: Thank you for eighteen constructive years of loving friendship, which have shaped me to the person I am today.

Last but not least, I would like to thank Vishay Siliconix for supporting this work.

Dedicated to my wife, Moran

♥

Abstract

Following the recent proliferation of portable electronics, constant research and development efforts aim to obtain more compact, light, energy efficient and economical power sources. State-of-the-art power-supplies developers manage to obtain relatively small size with reasonable power processing efficiency by using improved components and design techniques, combined with the flexibility of digital control. However as this trend continues, the requirements become ever-challenging: tighter output voltage regulation, faster response times to load and input voltage changes and lower volume are of major concern in the design of present-day power management hardware and pose a constant bottleneck in the advancement of current technology.

Present-day switched capacitor converters (SCC) have become an attractive alternative to the switched-inductor based conversion solutions, for volume-sensitive applications, featuring high efficiency and economical implementation. A major drawback of the SCC family is that regardless of the voltage regulation scheme, the efficiency of a SCC is inherently tied to the ratio between the output voltage and designed target voltage (unregulated open circuit voltage), similarly to linear regulators. The linear dependency stems from the rigid proportionality between the input and output charges.

Several solutions reduce this penalty by generating multiple target voltages using multiple flying-capacitor cells. The effective operation range can be increased at the cost of a complex connectivity scheme for the flying capacitor cells. However, even with multiple cells the efficiency characteristics of the converter retain a discrete nature.

Precise regulation is then achieved to match the required output either by varying the SCC parameters, or by inserting a post regulation stage, or by combining a switched-inductor forming a hybrid topology. A new conversion scheme will have an advantage over existing converters if it can maintain the properties and merits of a SCC and allow for continuously-efficient power-conversion, similar to that of switched-inductor based conversion solutions.

The objective of this PhD research program is to provide and detail a generalized power management scheme for high-efficiency power conversion and continuous output voltage regulation using switched-capacitor technology for a wide variety of

applications. Efficient power conversion is achieved without or with significantly reduced magnetics, by utilizing capacitive elements as the energy transfer vehicle. This ultimately allows for high power-density and is the key to power-integration.

A gyrator resonant switched-capacitor converter (GRSCC) is introduced with a high-efficiency profile, detached from the linear dependency which characterizes the SCC family. A compact voltage-regulator based on the GRSCC, which showcases zero-order load transient response and enables significant miniaturization of both the magnetic-element and the capacitor filters, is presented. A new voltage regulator module (VRM) which merges a highly efficient switched-inductor converter with a load-connected GRSCC to assist during load transient events is then introduced. The resulting VRM exhibits improved dynamic performance for both loading and unloading transient events, while maintaining a compact design with reduced output capacitance.

An envelope tracking power supply which enhances the performance and reduces the overall volume of RF transmitter modules is presented. This realization utilizes the bi-directionality and natural current-sourcing attributes of the GRSCC alongside its virtually instantaneous response to form the desired envelope to be fed to the transmitter.

A new topological family of the GRSCC is introduced and thoroughly analyzed. The extended version of the GRSCC enables further modes of operation, allowing the efficiency characteristics of the converter to be shaped shifting peak efficiency to various conversion ratios. A general behavioral model for multi-port switched-resonant and soft-switched capacitor converters is developed. The model defines a systematical framework for multiport network impedance representation of converters with multiple switching-states. In particular the model includes the effect of losses on the converter's efficiency as well as performance and characteristic features.

This thesis signifies a leap in power-processing by switch-capacitor technology as it provides a comprehensive methodology to realize switched-capacitor converters with high-efficiency over a wide and continuous voltage-range, for the first time. Innovative theoretical analysis provides new foundations, reexamining the way in which switched-capacitor converters are designed and examined. The thesis provides fertile ground for new applications, demonstrated by voltage-regulation and envelope-tracking applications with unprecedented properties such-as droop-elimination, efficiency-curve shaping and continuous envelope-shaping.

The outcome of the PhD research sums an academic contribution of six journal papers [1]-[6] submitted and published in the IEEE Transactions on Power Electronics (TPEL) and the Journal of Emerging and Selected Topics in Power Electronics (JESTPE); six more leading conference papers [7]-[12] – all presented in the IEEE Applied Power Electronics Conference (APEC) and the Energy Conversion Conference and exposition (ECCE). The results of which have been awarded several prestigious distinction awards, including TPEL 2nd best paper award for 2017 [4], APEC best presentation award [11], and Wolf foundation prize scholarship for research students. The derivatives of this program have already contributed to several more publications in the fields of digital control [13], [14] and chip-integration [15], [16] based on the GRSCC as the power scheme

Keywords – power-electronics; voltage-regulation module; resonant switched-capacitor converter; gyrator; digital power-control;

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CHAPTER 1: Introduction

1.1 DC Voltage-Regulation and Power-Conversion at-a-Glance

This chapter provides a short overview on relevant terms in power electronics, reviews some differences between different methods of energy-efficient power conversion, and provides details on latest research efforts. An emphasis is given to switched-capacitor based converters as the foundation of this thesis, alongside the state-of-the-art and present-day challenges.

1.1.1 Linear regulation

The simplest means for controlled voltage regulation is linear power supplies. An operational amplifier feedback network creates a controllable series resistance between a rectified filtered supply and a load, regulating the output voltage by feedback to a series transistor (Fig. 1). As a given load draws more current, the output voltage drops, feeding back to error compensation circuitry that, in turn, decreases the series resistance, which amends the output voltage.

The series resistance in linear supplies introduces losses that are proportional to the required voltage drop between the input and output voltages. The relationship can be described by (1),

$$\eta = \frac{P_2}{P_1} = \frac{V_2}{V_1}, \tag{1}$$

where P_1 and P_2 are the input and output powers, respectively, and V_1 and V_2 are the input and output voltages, respectively. This equation is true when the connection is in series, i.e. the input and output currents are the same. This power regulation method's efficiency profile is a steep linear drop, making it an effective method for regulation when only a small voltage drop is needed. On the other hand, linear converters provide a precise output voltage with little to no output ripple.

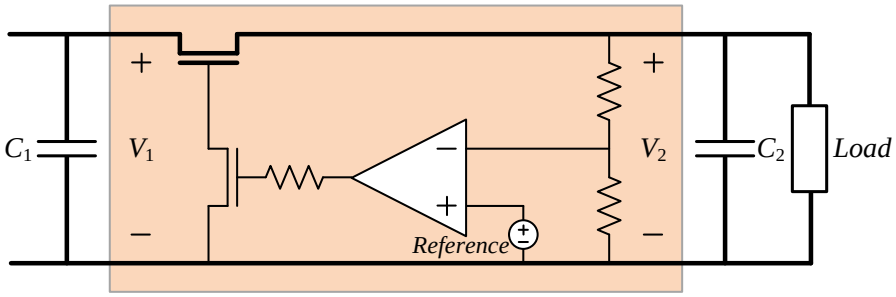


Fig. 1 Basic linear regulator example.

1.1.2 Switched-mode power supplies

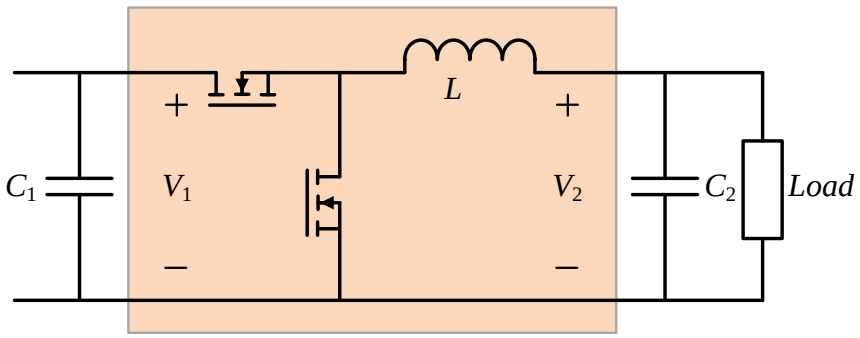
A switched-mode power supply (SMPS) operates with high frequency switching in order to reduce component size. In its simplest form, a reactive element is switched in between the input and output, charging and discharging, respectively. Topology-wise, dc-dc power converters can be roughly categorized in to two groups by the dominant power-processing element in the converter – an inductor, i.e. switched-inductor converter (SIC) or a capacitor, i.e. switched capacitor converter (SCC). There are also switched-resonant converters (SRC) which utilize a resonant tank composed of both a capacitor and inductor, however many times there is one dominant element used for the energy-transfer. Therefore In these cases the SRC can be categorized as a resonant SCC or SIC, depending on the dominant *power-transfer element*.

Even though both groups have been investigated over the years, an inductor has been (and still is) the most commonly used choice as the main reactive element in a SMPS. Historically, SICs were preferred due to efficiency, cost, simplicity and reliability concerns. Creating an inductor requires winding a coil around a ferromagnetic element. This is a simple and reliable form of energy storage. Storing the same amount of energy in a capacitor required bulky electrolytic capacitors having short lifespans. But most importantly, as will be explained in the following chapters, a method enabling a wide range of conversion ratios maintaining high efficiencies for SCCs was yet to be discovered. SCCs suffer from linear efficiency drops and in some cases have no advantage in terms of efficiency over linear regulators.

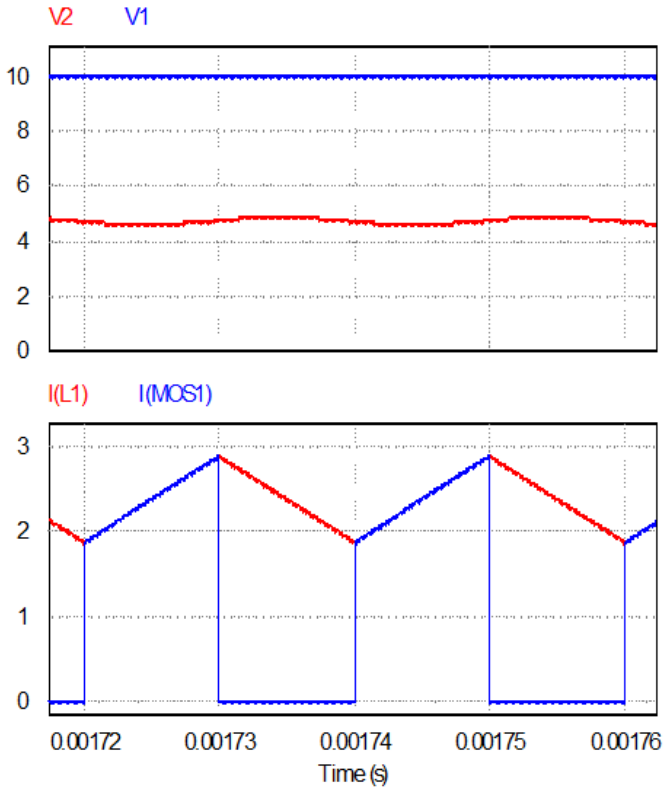
A. SIC example - Buck

An example of an inductor-based converter is given in Fig. 2, depicting a “Buck” converter – a simple, efficient and commonly used step-down converter. The converter sets a voltage conversion ratio by using an inductor that serves as a low-pass filter fed by a pulsed voltage source, delivering the average dc component of the pulse. The pulsed source is produced by repeatedly switching the input voltage, creating the high level of the input signal. The low-level is created by connecting a freewheeling diode between the switched input and the ground, or actively shorting the switched node to ground via a second switch. The diode naturally conducts as the input is disconnected due to current continuity demands of the inductor. The switching frequency depends on hardware capabilities, e.g. MOSFET turn-on and turn-off times, driving components’

speed, etc. Raising the frequency decreases the required inductance, significantly shrinking the inductor's volume, but comes at the cost of increased losses.



(a)



(b)

Fig. 2 (a) A typical synchronous Buck converter. The transistor Q_2 can either be a switch (synchronous mode) or a freewheeling diode. (b) Traces showing the operation of a Buck converter. The input and output voltages are shown in the top graph and the current seen by the input and output is shown in the bottom graph.

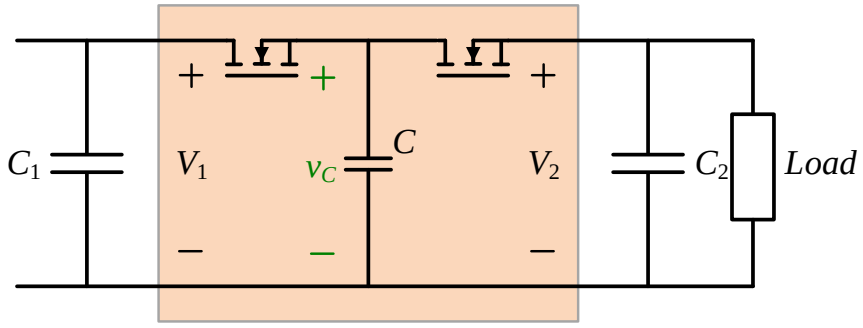
Knowledge about inductor-based SMPS has evolved to a point that high efficiency is easily obtained, especially when implementing soft-switching techniques, but size reduction remains somewhat limited. Miniaturization is strongly pursued in current and emerging technologies, and CMOS-only realizations are pursued in order to completely embed power supplies on-chip. This poses a problem for inductor technology, while

attempts have been made to create on-chip SICs [17], [18], a way to efficiently mass produce IC inductors retaining high efficiency has yet to be found.

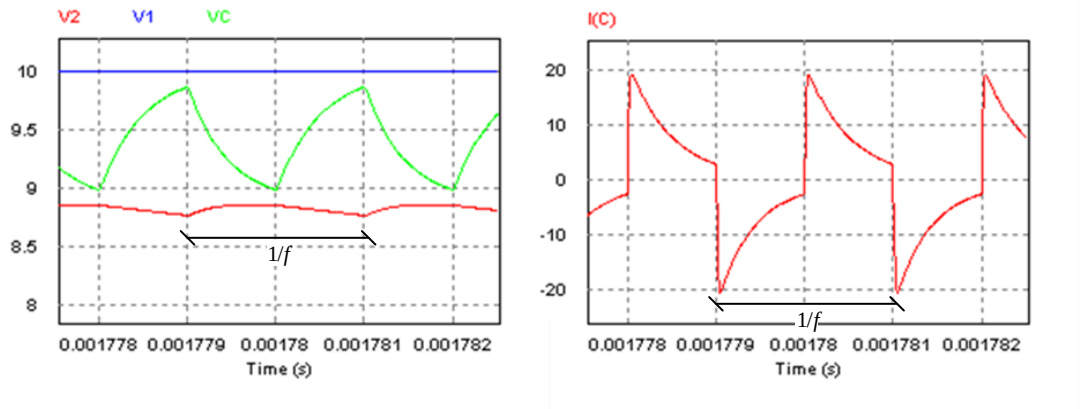
B. SCC example #1: 1:1

A switched capacitor-based converter (SCC) operates based on the principle of voltage potential leveling. In its most simplistic version, shown in Fig. 3, a flying capacitor is alternately switched in between the input and the output and transfers charge from the higher to the lower potential, aiming to level the potentials. As in most switched converters, if the output load is resistive, an additional capacitor is needed to maintain a steady dc output voltage while the flying capacitor is charging at the input. To reduce the required size of the flying and output capacitors, the switching frequency is increased, to maintain low ripple.

There are many variations to the switched capacitor topology that are able to provide multiple output levels by manipulating multiple flying capacitors, alternating between parallel, series, or mixed parallel-series connections. These yield discrete fractional options for voltage conversion and will be discussed further in section 1.2.



(a)



(b)

Fig. 3 A 1st order SCC: (a) layout (b) traces of the voltages and currents (with some ESR added to the resonant tank).

In recent years, research on miniaturization has focused on integrating the SCC with SIC post-regulation. According to one approach, the current path for the SCC can be optimized to minimize losses. By introducing GaN technology, recent publications have obtained unprecedented power densities ranging from 500 to 2200 W/in^3 (30 to 130 kW/dm^3) for fixed conversion ratios [32,33]. The SCC is then preceded by a small buck stage for post-regulation.

C. SCC Example #2: Soft-switching

In order to reduce switching losses, operating in a resonant mode has been suggested. Adding an inductive element in series with the flying capacitor changes the charge and discharge profiles from an exponential to a second-order profile. Switching at (or close to) resonance, when the current crosses a zero value creates a sinusoidal shaped current, as seen from the traces in Fig. 4b, and switching can occur at (or close to) zero current.

A major drawback in using soft-switched SCC is the inability to create an output voltage that is different from its natural target voltage (1:1, 2:1, etc.). In soft-switched SCC, the resultant charge-balance of the flying capacitor(s) differs from zero after a charge/discharge cycle when $V_2 \neq V_1$. The residual charge left in the flying capacitor(s) impacts the average current and causes it to diverge, which, in turn, eventually increases/decreases the output voltage such that the charge-balance of all the capacitors will be satisfied. The result is that the system naturally drifts back to the target voltage. To better view this problem, consider a generic 1:1 resonant SCC (Fig. 4) with a "forced" output voltage of $V_2 < V_1$. The flying capacitor voltage and current are illustrated in Fig. 5. The current waveform shows that although ZCS is obtained, the charge received from the source is not equal to the one delivered to the output. This translates into an unbalanced capacitor charge that continues to accumulate in each cycle, in turn increasing the output current until the target voltage is reached, where charge-balance is obtained.

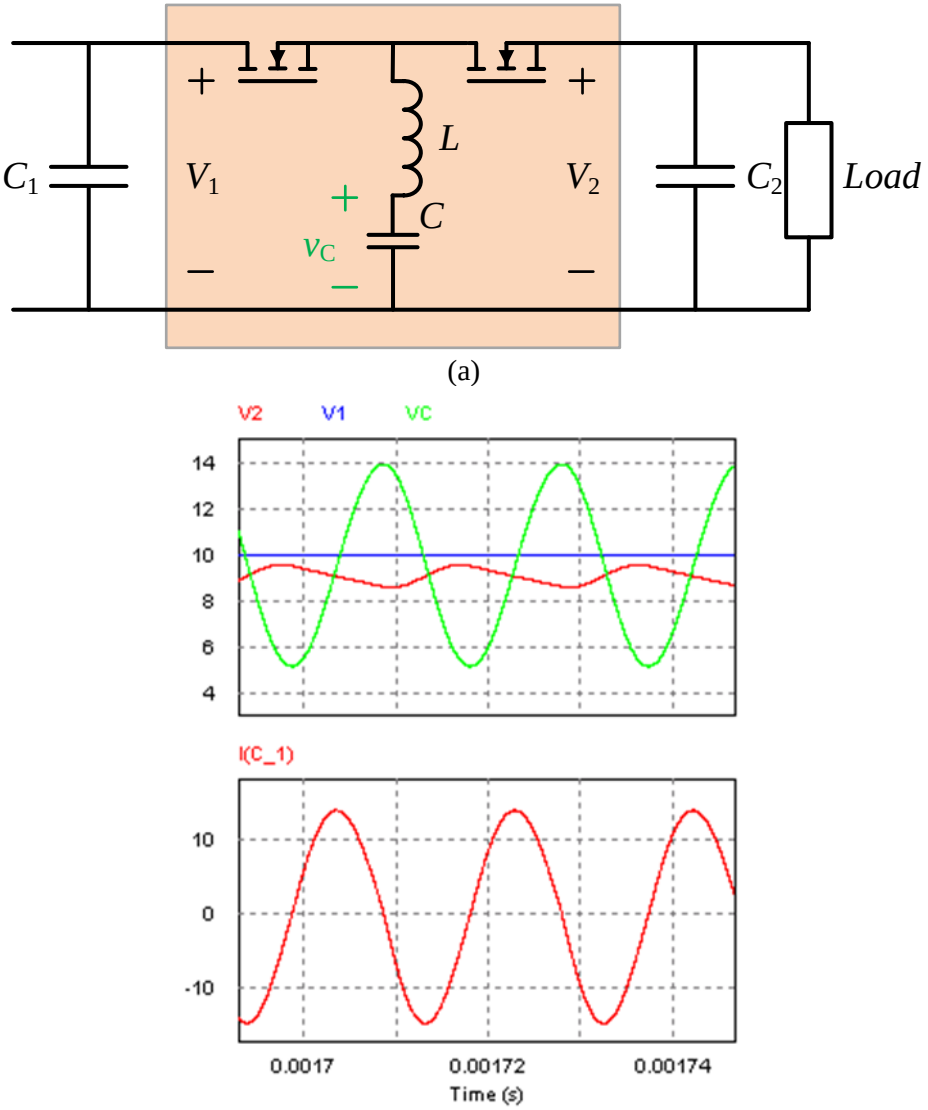


Fig. 4 A 2nd order SCC: (a) layout (b) traces of the voltages and currents (with some ESR in the resonant tank).

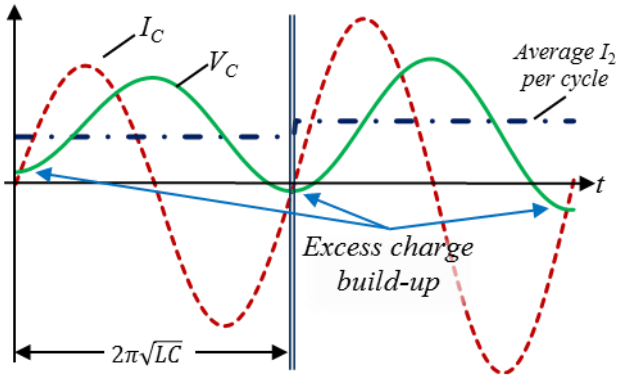


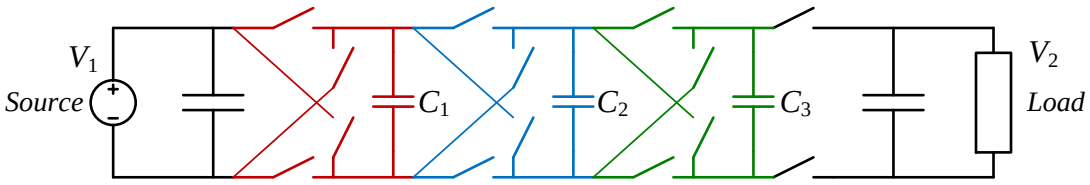
Fig. 5 Unbalanced waveforms of the flying capacitor in the RSCC described in Fig. 4a: dashed line - I_C , solid line - V_C , flat step - average I_2 corresponding to each switching cycle

1.2 Overcoming Efficiency Issues in Switched-Capacitor Converters – An Overview

Due to the voltage balancing nature of the basic SCC configurations, these converters lack regulation capabilities that do not introduce direct losses, similar to the linear power supplies. In first-order SCCs, losses can be introduced by adjusting the switching frequency or duty cycle [19] and thereby increasing R_s. second-order soft-switched SCCs cannot be tweaked in the same manner if soft-switching is to be maintained, effectively locking the conversion ratio. This was a major problem, and due to this challenge, combined with the limited variety of available capacitors having high capacitance and long-term durability, SCCs were rarely used.

Miniaturization demands and advances in capacitor technology reignited the interest in SCC technology and research in the field resurfaced. Most of which accepted the need to compromise on efficiency, some focused on working with limited conversion ratios where efficiency is high or on creating multiple conversion ratios, and some aimed to find ways to break this rigid relationship between the conversion ratio and the efficiency. The following sub-sections review the latest relevant advancements in this field.

1.2.1 Extended binary / Fibonacci multilevel schemes



(b)

Fig. 6 The EXB/Fibonacci converter topology

Research conducted in [20], [21] introduced a family of multi-level converters that use a number of flying capacitors which have multiple connectivity options. The capacitors can be switched in between the input and the output in various combinations following a specific algorithm that effectively results in the output being some fraction of the input. Using only the extended binary algorithm, for example, a converter consisting of n flying capacitors can yield 2^{n+1}–1 conversion ratios ranging from $V_2 = \frac{1}{2^n} V_1$ to $V_2 = \frac{2^{n+1}-1}{2^n} V_1$.

Three flying capacitors configured as shown in Fig. 6 are sufficient for creating 15 different conversion ratios. If the SCC is of first-order, the duty cycle can be tweaked to enable voltage regulation.

The down side of this converter is the low achievable nominal efficiency. The required number of transistors is large: all transistors must be four-quadrant, requiring a total of 8 MOSFETs per flying capacitor. Furthermore, current flows through a large and varying number of the transistors at each state, making it hard and expensive to lower the equivalent series resistance.

Similar approaches to this converter family are also worth mentioning, which for the matter of this work can be similarly categorized: the gearbox capacitive converter [22] and the general transposed series-parallel (GTSP) [23], [24].

1.2.2 A resonant switched capacitor converter for voltage balancing of series-connected capacitors [25]

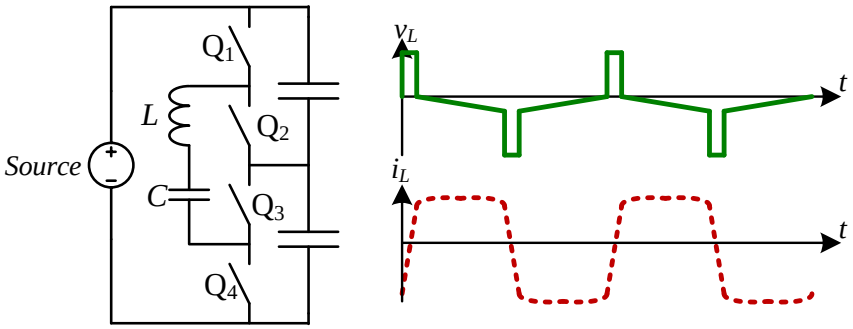


Fig. 7 (a) The circuit proposed by Sano *et al.* (b) voltage and current waveforms on *L*.

The research published in [25] describes a topology that is a hybrid between SCCs and SICs. The circuit is designed for serial cell-balancing, transferring energy between one cell and its neighbor. The cells can be a series of batteries or capacitors supporting a dc bus, or photovoltaic elements in a solar array. In the proposed configuration shown in Fig. 7 a flying capacitor is switched between the two adjacent cells, but instead of charging and discharging in a 1st or 2nd order manner, the energy is transferred as a relatively constant current by a series inductor that is pre-charged to the desired current.

This pre-charging can occur due to the available options of feeding the L-C tank with the voltage of the two cells together, or shorting the tank to itself. Assuming that the flying capacitor is large enough to maintain a relatively constant voltage value roughly equal to the voltage of one cell, connecting the tank to the cells in series creates a positive voltage on the inductor, charging it in one direction. Shorting the tank

reverses the voltage across the inductor, forcing current to flow the other way. Once the tank is connected to only one cell, the voltage across the inductor is relatively small, leaving the current constant for a considerable amount of time.

This mode of operation becomes problematic once the voltage difference between cells becomes substantial. This creates a voltage drop across the inductor, causing a rapid decrease in current. This means that the time of current inversion (Fig. 7b), where no energy is transferred, becomes dominant, raising the overall rms current and decreasing the efficiency. In addition, soft-switching does not occur in all stages

1.2.3 Analysis of a step down resonant switched capacitor converter with a sneak circuit state [26]

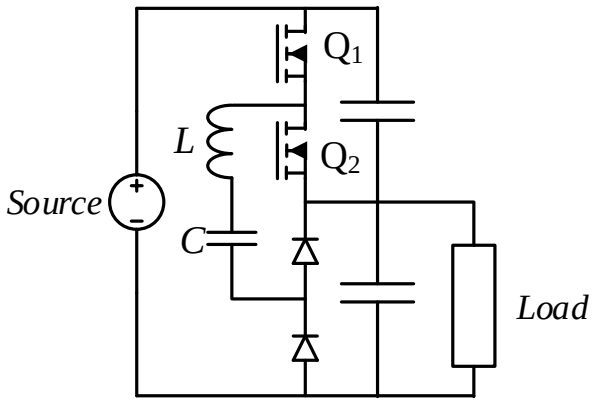


Fig. 8 The examined RSCC given in [26].

In [26], a 2:1 step down RSCC, implemented as shown in Fig. 8, was examined. The study revealed a phenomenon that occurs when using two-quadrant MOSFETs and diodes while switching above or below resonance. Results show that unmatched frequency leads to undesired current circulation paths named *sneak circuits*. When switching above resonance, V_2/V_1 stays relatively constant for a given load, R_L, but if f_s is lower than the resonant frequency and R_L is small enough to create significant resonant current, the result will be a dramatic decline in V_2/V_1, as can be seen in Fig. 9, due to the voltage of the resonant capacitor exceeding the clipping voltage of the diodes (this is discussed throughout the following chapters). Reading the study with an efficiency-oriented view, one might intuitively assume that the efficiency declines linearly with the drop in V_2, but simulations suggest otherwise (Fig. 10). In fact, the circulating currents recycle some excess charge, resulting in lower output currents than expected. The direct result is $\eta = P_2 / P_1 > 2V_2 / V_1$, meaning that the rigid relationship

between the input and output voltages and the efficiency does not hold, resulting in better-than-expected efficiencies.

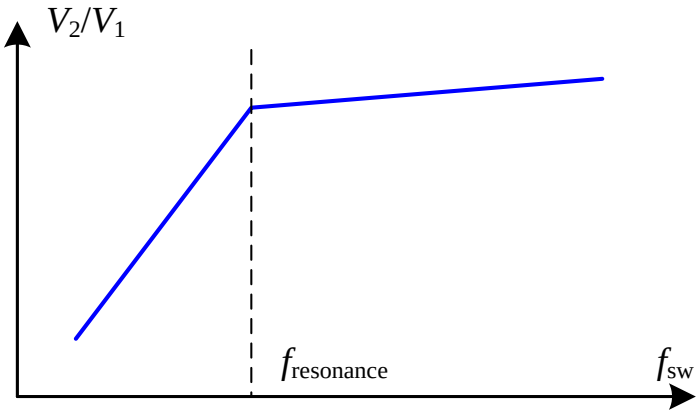


Fig. 9 Typical behavior of the conversion ratio as a function of the switching frequency f_{sw}

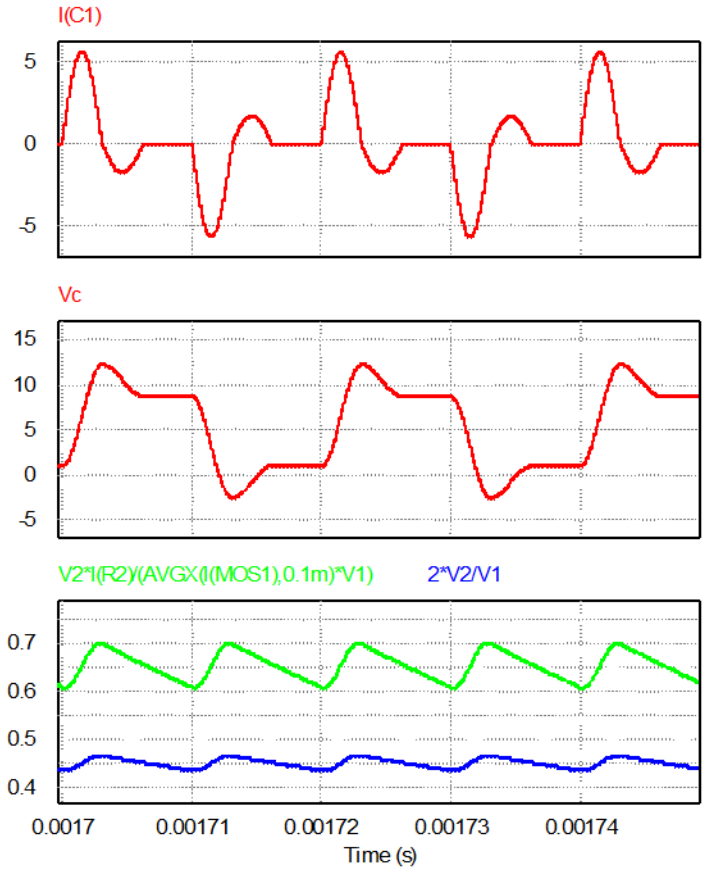


Fig. 10 Circuit traces showing a case of $\eta > V_2/V_1$. The bottom graph shows the actual efficiency (upper trace) above the V_2/V_1 (lower trace) conducted in PSIM.

1.2.4 Unified analysis of switched resonator converters [27]

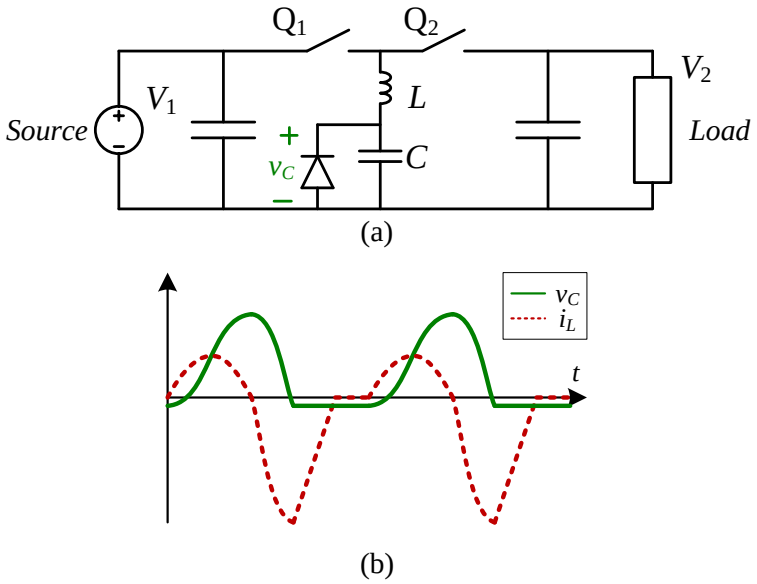


Fig. 11 The examined resonator: (a) topology; (b) typical traces.

The study in [27] proposes a family of switched capacitor converters, focusing mainly on the topology of a step down converter. The whole family manages to detach the correlation between the output voltage and the efficiency, with the theoretical efficiency being 100% for all conversions for all output voltages in the conversion range. The proposed topology consists of a standard 1:1 RSCC with an added diode connected antiparallel to the flying capacitor, as seen in Fig. 11. In this manner, if $V_2 < V_1$, once the capacitor discharges to the output it depletes of energy, i.e. reaches 0V, before the discharge current reaches zero. In this case, the antiparallel diode conducts and lets the inductor discharge any residual energy it maintains. This creates a split discharge profile starting with a resonant shape and ending with linear discharge. The resonant tank meets V_1 empty of any charge, regardless of any occurrence at the output. This means that as long as a whole switching sequence (charge and full discharge or DCM) occurs, the power output will be constant and R_L will dictate the output voltage and current. In this operation mode, power and current or voltage regulation can be achieved by applying pulse-density modulation (PDM).

In [27], many derivatives were presented for the proposed configuration. A drawback of the topology is the inability to maintain small conversion ratios (close to 1:1), and conversion ratios above 1:1. As the output voltage gets closer to the input voltage, the linear discharge through the diode takes longer, limiting the frequency and the average current that can be transferred.

1.3 Thesis Outline

The introduction above provides background for the following chapters as-well-as the motivation for the research. The rest of the chapters detail the following:

Chapter 2: Introduces a new efficient method for voltage conversion over a wide and continuous conversion-ratio by using an SCC alone. By using the new topology called a gyrator resonant switched-capacitor converter (GRSCC), it is demonstrated that an SCC can be detached from its linear efficiency dependence by utilizing resonant characteristics with a new switching scheme.

Chapter 3: A compact voltage-regulator using the introduced GRSCC and a comparator-based control-scheme is presented. It features zero-order response characteristics to load and line transients, similar to SICs operating discontinuous current-mode (DCM). Large- and small-signal average-behavioral-models are developed and verified.

Chapter 4: Two applications are presented to demonstrate the capability of the GRSCC to surpass the performance of state-of-the-art. A hybrid voltage-regulation module (VRM) combines the unparalleled efficiency of a buck-converter with the responsiveness of the GRSCC. The presented VRM is effectively immune to droops caused by load-transients and allows one to drastically reduce the required output capacitance. An envelope-tracking power supply which facilitates miniaturization of radio-frequency (RF) transmitters by drastically improving their efficiency is then presented. The fast envelope-tracker feeds optimized amplitude levels to the linear RF power-amplifier thus reducing total losses.

Chapter 5: The theorem behind the GRSCC is revisited. First, a new topology which expands the operation of the original GRSCC, allowing the peak efficiency of the converter to be shifted towards the desired operating point, is presented. Then, a multiple input/output theorem is conceived which lays the foundations to more applications modes of operation based on the GRSCC. A conduction-path based loss analysis is performed on the expanded theorem to provide accurate optimization tools for the presented research.

Chapter 6 concludes the thesis.

1.4 Contributions of this Research

Chapter 2 summarizes content that is published in a paper named "A high-efficiency resonant switched capacitor converter with continuous conversion ratio" in *IEEE Transactions on Power Electronics* (TPEL) [5], presented in *IEEE Energy Conversion Congress and Exposition* (ECCE) [12] under the same title.

Chapter 3 summarizes content that is published in a paper named "Resonant switched-capacitor voltage regulator with ideal transient response" in TPEL [6] and presented inthe *IEEE Applied Power Electronics Conference* (APEC) [11] under the same title, ***winning best presentation award.***

Chapter 4 summarizes content from several separate publications: "Improving loading and unloading transient response of a voltage regulator module using a load-side auxiliary gyrator circuit" published in TPEL [4], ***winning Second Place Prize Paper Award for 2017*** and presented in APEC [10] under the same title; "Envelope tracking power supply for volume-sensitive low-power applications based on a resonant switched-capacitor converter" presented in APEC [9].

Chapter 5 summarizes content from four separate publications: "A Generic and Unified Global-Gyrator Model of Switched-Resonator Converters" published as a letter in TPEL [3]; "A family of switched-resonant converters with wide conversion ratio and controlled sourcing features for volume-sensitive applications" accepted for publication in the *IEEE Journal of Emerging and Selected Topics in Power Electronics* (JESTPE) [2]; "Single-stage switched-resonator converter topology with wide conversion ratio for volume-sensitive applications" presented in APEC [8]; "Performance analysis of gyrator behavior in multi-port resonant switched capacitor converters", to be submitted to TPEL[1].

The research also contributed to additional publications based on the findings: "Enhanced differential power processor for PV systems: Resonant switched-capacitor gyrator converter with local MPPT" published in JESTPE [13]; "Plug-and-play electronic capacitor for VRM applications" presented in APEC [14]; "Digital self-tuning controller for ZCS resonant converters operating in the 10MHz-range" presented in the Control and Modelling of Power Electronics (COMPEL) workshop [7]; "Optimal design of a voltage regulator based on gyrator switched-resonator converter IC" published in JESTPE [15] and presented in APEC [16] under the same title.

CHAPTER 2:
Gyrator Switched-Resonant Converter

2.1 Introduction

In this chapter a method for efficient voltage conversion over a wide and continuous range using SCC technology alone is presented and analyzed; a method which *disengages the efficiency of an SCC from its conversion ratio*. A new gyrator resonant switched-capacitor converter (GRSCC), which is a topological modification of a conventional soft-switched RSCC [19], [28]-[33], is presented.

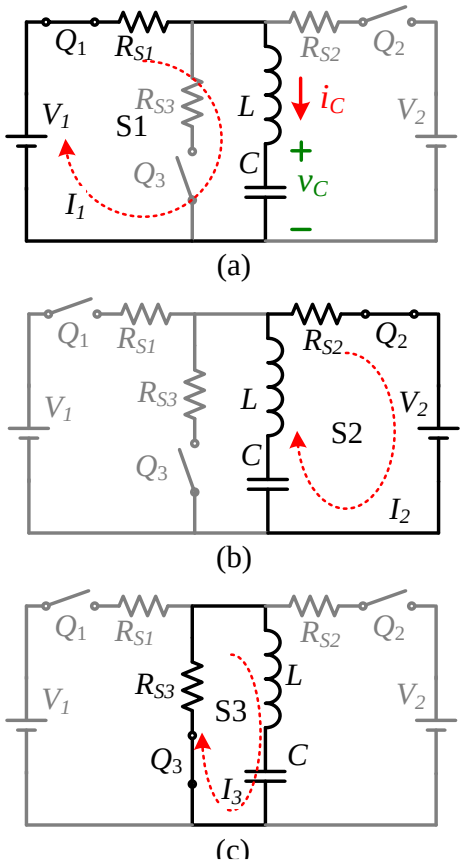


Fig. 12 The introduced RSCC configuration and operation principle: (a) *charge*, (b) *discharge*, and (c) *balance* states.

The physical modification (presented in Fig. 12 in simple form), along with a new switching scheme, alters the converter's power-processing properties. By doing so the converter acts as a natural voltage-dependent current source (gyrator). Thanks to its resonant nature, the GRSCC maintains soft-switching for the entire operation range, and exhibits bi-directional power flow with wide range of voltage gains. The converter's efficiency may be very high, and depends primarily on the conduction losses.

2.2 Principle of Operation

The GRSCC includes two switches and a resonant tank, similarly to the classical RSCC design. An additional switch S_3 is added to introduce an alternative resonant current path to balance the residual charge of the flying capacitor, i.e., the resonant current path allows current to restore the flying capacitor voltage to its original state by reversing its polarity. The mechanism of polarity reversal (charge balancing) lays the foundations for breaking the rigid connection of input/output voltage and efficiency dependency. Controlling the sequence of the switches governs the power flow direction, hence bi-directional step up/down operation.

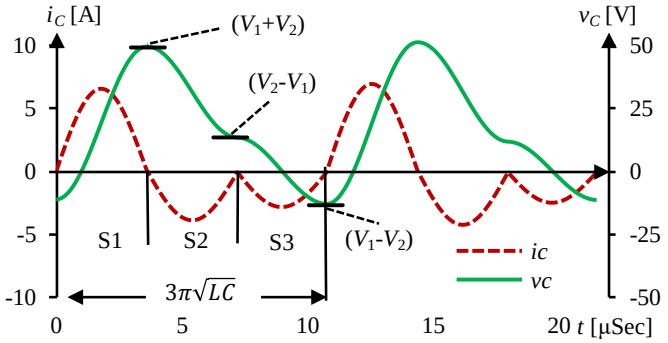


Fig. 13 Typical waveforms (obtained from simulation) of the flying capacitor voltage and current. The circuit parameters are: V_1=20V, V_2=31V, R_S=0.15Ω, L=5.2µH, C=0.25µF.

The operation of the converter shown in Fig. 12 is described for one steady-state charge/discharge/balance cycle, and is further illustrated by Fig. 13 that shows the capacitor voltage V_C and the resonant tank current I_C in the case of a non-unity step-up conversion. By turning Q_1 on, a charge state (S1) is commenced, which resonantly charges the flying capacitor from the source. At zero current, Q_1 is turned off and Q_2 is turned on (state S2). At this point, the flying capacitor resonantly discharges onto the output capacitor. Since V_1 and V_2 are of different values, only a portion of the charge is delivered to the output, and results in a V_C that is different in its magnitude compared to the starting point of S1. This voltage difference (neglecting parasitics) is equal to twice the residual voltage of the flying capacitor. By turning Q_3 on (S3), the resonant tank is short-circuited to create the required charge-balance by reversing the flying capacitor voltage polarity. The charge of C at the end of S3 is equal to equal its charge at the beginning of S1.

As will be explained in detail in the next section, the addition of a third, charge-balancing state to the switching sequence transforms the RSCC into a voltage-

dependent current sourcing converter. This leads to an optimal result, where the current that is output by the current source is injected into the load, thus adjusting the voltage at the output, while keeping the current independent of the conversion ratio. With the new topology, dependency is formed between V_1 and I_2 (rather than V_2). In this way, any desired conversion ratio may be obtained (i.e. the conversion ratio can become continuous), while maintaining high efficiency. It should be noted that under steady-state conditions, the order of the charge/discharge/balance sequence does not affect the operation of the converter for either step-up or step-down conversion. The order of the sequence will govern the power flow direction, i.e. from V_1 to V_2 or from V_2 to V_1. To deliver power from V_1 to V_2 the sequence will be (S1, S2, S3). That is, *charge* the flying capacitor from V_1, *discharge* the flying capacitor across V_2 and *reverse* the flying capacitor polarity. In the case of power to be delivered from V_2 to V_1 the sequence will be changed to (S1, S3, S2). The duration of each switching state is half the resonant period and hence the switches are turned on and off at ZCS. Voltage regulation may be applied by introducing a time delay between switching states, applying a delay between consecutive sequences, i.e. pulse density modulation (PDM), or by creating packets using on-off burst mode control [27], [34]. The resistors R_S in Fig. 12 represent the parasitic resistances in each loop and are assumed to be negligibly small in the analysis for the current and voltage conversion ratios.

2.3 Gyrator Mode Power Transfer

In each switching state, the *LC* tank connects to a voltage potential of either V_1,V_2 or 0. Assuming a high quality factor ($Q \gg 1$) of the resonant tank, the resonant current I_C and the flying capacitor voltage V_C are approximately sinusoidal, hence:

$$\begin{cases} V_C(t) \approx V_i - \left(V_i - V_C(0)\right)\cos\left(\dfrac{t}{\sqrt{LC}}\right) \\ I_C(t) \approx \dfrac{V_i - V_C(0)}{\sqrt{L/C}}\sin\left(\dfrac{t}{\sqrt{LC}}\right) \end{cases}, \tag{2}$$

where C is the value of the flying capacitor, and L is the series inductance. $t = 0$ represents the start of each switching state and V_i represents the imposed dc voltage, either V_1, or V_2, or 0V.

Following the principle of operation described earlier, assuming steady-state operation with transition between switching states at zero current, and by using (2), the voltages at the end of the charge, discharge and balance states can be expressed as:

$$\begin{cases} V_{C,1} \approx V_1 + \left(V_1 - V_{C,3}\right) = 2V_1 - V_{C,3} \\ V_{C,2} \approx V_2 + \left(V_2 - V_{C,1}\right) = 2V_2 - V_{C,1} \\ V_{C,3} \approx 0 + \left(0 - V_{C,2}\right) = -V_{C,2} \end{cases}, \tag{3}$$

where $V_{C,1}$ to $V_{C,3}$ represent V_C at the end of stages S1 to S3, respectively. After some manipulation, (3) can be rewritten as:

$$\begin{cases} V_{C,1} = V_1 + V_2 \\ V_{C,2} = V_2 - V_1 \\ V_{C,3} = V_1 - V_2 \end{cases}. \tag{4}$$

Substituting (2) into (4) yields the states' peak resonant currents ($I_{pk,S1}$, $I_{pk,S2}$, $I_{pk,S3}$):

$$\begin{cases} I_{pk,S1} = V_2 / Z \\ I_{pk,S2} = V_1 / Z \\ I_{pk,S3} = (V_1 - V_2) / Z \end{cases}, \quad Z = \sqrt{\frac{L}{C}}. \tag{5}$$

Assuming identical resonant characteristics for all states, that is, one third of the operation cycle for each state, the average input and output currents (I_1, I_2) can be obtained and a gyrator relationship between the currents (I_1, I_2) and voltages (V_1, V_2) is formed as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}, \quad g = g_n = \frac{2}{3\pi Z}. \tag{6}$$

Equation (6) implies that for a synchronously operated converter, the dependence of the average terminal currents (I_1, I_2) on the average terminal voltages (V_1, V_2) follows a gyrator relationship [35], [36] with a natural gyration gain of g_n. This expression is generic and holds for the case of power flow from V_1 to V_2 as well as for power flow from V_2 to V_1. However, as mentioned earlier, the direction of power flow is governed by the switching stage sequence, and the power flow direction reverses for the case of (S2, S1, S3). It should be further noted that due to the gyration action, the converter behaves as a voltage-dependent current source and there is virtually no restriction on the relative magnitudes of V_1 and V_2. That is, V_2 can be equal to, less than, or greater than V_1.

For the case where one of the terminals is connected to a resistive load, R_L, in parallel with a filter capacitor, C_L, the topology operates as a current sourcing dc-dc converter and the magnitude of the output voltage, V_2, depends on the load resistor as would be expected from a gyrator circuit:

$$V_2 = gR_L V_1. \tag{7}$$

The voltage gain, *A*, will be:

$$A=\frac{V_2}{V_1}=gR_L \ . \tag{8}$$

The natural operating frequency, f_n, is composed of three half-resonant sections, that are assumed identical. Therefore, f_n can be expressed as:

$$f_n=\frac{1}{3\pi\sqrt{LC}} \ . \tag{9}$$

2.4 Fundamental and Practical Characteristics

2.4.1 Regulation

The basic operation mechanism that follows charge, discharge and balance states creates a rigid gyration relationship as in (6). In the case that regulation is desired, *g* should be controlled. By introducing time delay between cycles, that is, effectively changing the operating frequency, *g* is made controllable and the gyration ratio *g* and operating frequency *f* can be re-defined as:

$$\begin{cases} g = Gg_n = \dfrac{2G}{3\pi Z} \\ f = Gf_n = \dfrac{G}{3\pi\sqrt{LC}} \end{cases}, \tag{10}$$

in which $G \in (0,1]$ is defined as the regulation factor. In this mode of operation, the output current will be determined by the input voltage and *g*.

2.4.2 Simplified efficiency analysis

Losses in the GRSCC are primarily generated by the resistive elements in the conduction paths of each sub-circuit. The resonant nature of the family facilitates ZCS and significantly reduces channel switching losses to either turn-on or turn-off (when using an element with a free-wheeling diode such as a MOSFET). At high voltage operation, where turn-on losses might be significant, channel switching loss can be minimized, ensuring zero-voltage switching at turn-on by offsetting the operating frequency slightly above or below resonance, as shown in [37]. However, this issue is common to the entire RSCC family and is beyond the scope of this research. It is assumed here that channel switching losses and the remaining switching losses are small.

For a full operation cycle at frequency f_s, the current of each sub-circuit is composed of one sinusoidal pulse (with a peak value as found in (5)) followed by zero current for the time duration of the delay plus the conduction time of the other two states. By maintaining the assumption of low losses, and following the previous equations, the relationship between the rms currents and the average output current, I_2, will be:

$$\begin{cases} I_{\text{rms,S1}} = \sqrt{\dfrac{G}{6}}\dfrac{R_L}{Z} I_2 \\ I_{\text{rms,S2}} = \dfrac{3\pi}{2}\dfrac{1}{\sqrt{6G}} I_2 \\ I_{\text{rms,S3}} = \left| \dfrac{3\pi}{2}\dfrac{1}{\sqrt{6G}} - \sqrt{\dfrac{G}{6}}\dfrac{R_L}{Z} \right| I_2 \end{cases} . \tag{11}$$

The total power dissipation can be calculated by summing the losses of the three sub-circuits. Given an identical parasitic resistance, R_S, for the three sub-circuits, the total dissipated power, P_{loss}, can be expressed as:

$$P_{loss} = I_2^2 \left(\frac{3\pi^2}{4G} + \frac{R_L^2 G}{3Z^2} - \frac{\pi R_L}{2Z} \right) R_S \ . \tag{12}$$

By substituting (6), (8) and (10) into (12) and after some manipulations, the equivalent resistance of the converter, R_e [19], [28] as a function of the load, voltage ratio and the circuit parameters is found to be:

$$R_e = R_L \frac{\pi}{2}\frac{R_S}{Z}\left(A + A^{-1} - 1 \right) . \tag{13}$$

The efficiency of the converter, η, can now be estimated by:

$$\eta = \frac{R_L}{R_L + R_e} = \frac{1}{1 + \dfrac{\pi R_S}{2Z}(A + A^{-1} - 1)} \ . \tag{14}$$

Fig. 14 shows typical curves that were obtained from (14) for the expected efficiency as a function of A, for various ratios of $Q = Z/R_S$. As can be observed, maximum efficiency is obtained at unity gain ($A = 1$), and it is a function of the ratio between the resistance and the resonant network characteristics. In Fig. 14, Z has been assumed as constant since it is determined by the natural gyration gain g_n. Equation (14) also implies that the efficiency is independent of G, resulting in a constant efficiency in a voltage regulation mode, when the current is controlled.

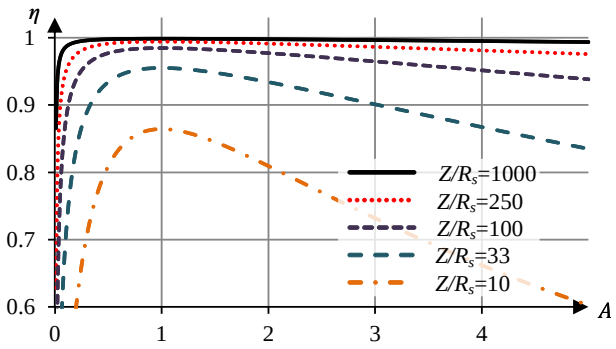


Fig. 14 Theoretical efficiency curves as a function of the voltage gain, A, with R_S normalized by Z as a parameter.

Equation (14) and Fig. 14 provide an insight into the operation of the new GRSCC as well as to the contributing factors of the efficiency. Ideally, assuming negligibly small parasitic resistances, the efficiency of the converter would be *100% for any finite conversion ratio*.

An extended analysis is provided in Chapter 5, where the low-loss assumption is revisited. The analyses are then compared to determine to what extent this simplified analysis holds and when it should be used.

2.4.3 Voltage ripple

Considering the above analysis, the operation of the GRSCC resembles the discontinuous-current-mode pulsed density modulation (PDM) operation of conventional switch-mode converters, which are predominantly found as voltage regulators. In this context, estimation of the input and output voltage ripple is essential for sizing considerations of filters. The analysis provided here addresses the output ripple, but can be similarly applied to the input ripple.

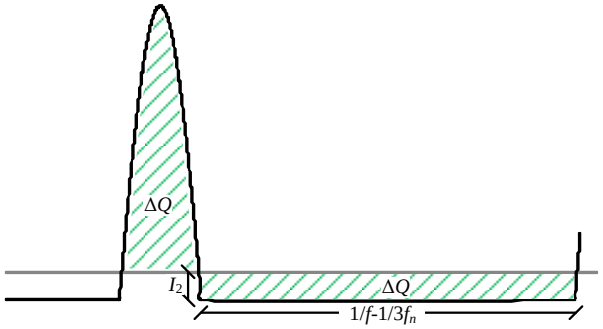


Fig. 15 The current on the output capacitor, C_L for one cycle. The confined area is symmetrical above and below zero, and represents the charge processed by C_L at each cycle.

By following the same design rules applied to switch-mode regulators [38], [39], that is, assuming constant output current, the current of the output capacitor (C_L) is similar in shape to the current of the discharge state, but without the average dc offset. A generic waveform of the output capacitor current is shown in Fig. 15. By approximating the negative part of the current shape, the per-cycle charge transfer, ΔQ_{C_L}, can be expressed as:

$$\Delta Q_{C_L} \approx I_2\left(\frac{1}{f}-\frac{1}{3f_n}\right) . \tag{15}$$

Substituting (7), (8) and (10) into (15) yields the expression for the normalized output ripple:

$$\frac{\Delta V_2}{V_2}=\frac{2}{A}\frac{C}{C_L}\left(1-\frac{G}{3}\right) , \tag{16}$$

where ΔV_2 is the peak-to-peak of the output ac ripple. The output ripple, as obtained by (16), is inverse linearly dependent on C_L and A. Furthermore, when voltage regulation is employed by varying G, the ripple is expected to deviate by about 30% for the entire operation range of $G \in (0,1]$.

2.4.4 Topology variation

The simplistic topology in Fig. 12 requires that it be implemented using four-quadrant (bi-directional) switches (Q_1, Q_2 and Q_3) that operate in synchronous/complementary action. This is required to maintain functionality by preventing reverse conduction by the FETs' body diodes. Using four-quadrant implementations for all three switches allows the converter to support bi-directional and non-inverting step-up/down operations in a single configuration. However, for more specific cases, such as unidirectional power flow and/or specific conversion types (up or down), the number of switches and the configuration complexity can be significantly reduced.

An attractive option to realize a GRSCC is by using a dual half-bridge configuration (Fig. 16). Possible applications for the bridge configuration can be as a balancer/equalizer of energy cells [25], [40] or photovoltaic arrays [31]-[33], as demonstrated by Fig. 16(a), or conventional step-down conversion, demonstrated by Fig. 16(b). It was found that for the dual half-bridge configuration, the four-quadrant switches can be replaced by conventional MOSFETs, while retaining the converter characteristics. As a consequence, the switch count required for the converter is a total

of four switches, comparable to conventional RSCC or non-inverting buck-boost configuration.

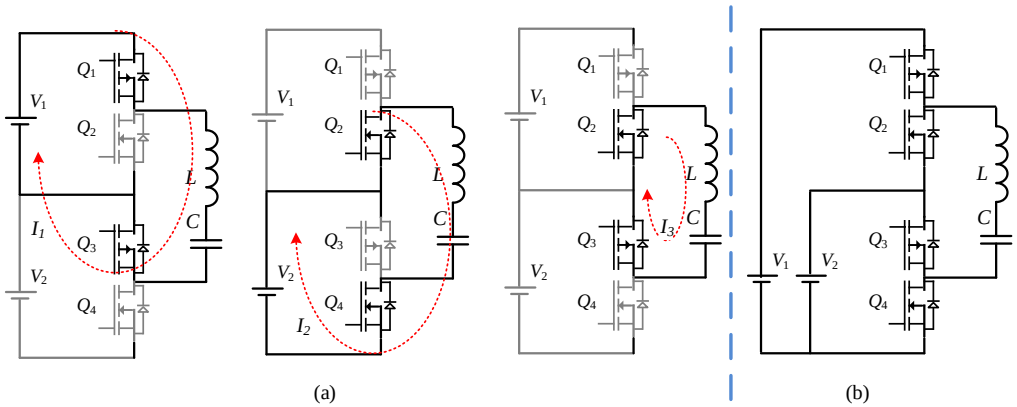


Fig. 16 GRSCC realized in full bridge configuration: (a) for stacked sources such as batteries and photovoltaic arrays, with the states depicted; (b) for regular source and loads.

It should be noted that for configurations that are implemented with two-quadrant switches, such as the bridge assembly (Fig. 16), the insertion of time delay between states for voltage regulation purposes has to be assigned to the proper state to avoid undesired circulating current. The delay should be located between states such that V_C is at the correct polarity to block the conduction of the MOSFET diodes. Taking the bridge configuration for example (Fig. 16), the proper sequence for this case would be: *discharge* (S2), *balance* (S3), *charge* (S1), *delay*. It should be noted that, as analyzed above, the order in which the sequence is applied does not affect the characteristics of the converter.

2.4.5 Operation with conventional PWM frontend

Regulation is facilitated by introducing a time delay between switching cycles and by doing so the gyration ratio g is made controllable (10). The resultant switching sequence per cycle therefore includes three virtually constant time intervals (neglecting parameters variations) for the charge, discharge and the balance phases (S1, S2, S3), and a fourth variable time frame for the PDM delay. One way to realize this pulse density modulated sequence is by synchronizing independent counters per interval, which is a relatively complex task for conventional off-shelf digital controllers. In this study, a simplified approach to implement PDM using readily available features of popular microcontrollers, without sacrificing the accuracy of the fixed intervals (to assure ZCS), has been realized. Here, similar to the control operation of resonant

converters, the total cycle period is the control variable rather than the residual time delay.

Conventional microcontrollers such as the Microchip dsPIC series feature a PWM peripheral with multiple channels capable of operating synchronously (i.e. sharing a master period setting) with independent ON time and phase delay. PDM realization based on these attributes is depicted in Fig. 17(a) for the basic configuration, and in Fig. 17(b) for the bridge version. As can be observed, each gate is linked to an independent PWM channel sharing the same period t ($1/f$). For each channel, the ON time, t_i, and the phase-shift (negative), φ_i, are assigned to create the desired sequence (i is the switch index). The specific time settings per channel are summarized in Table I. The time delay is the result of the time difference between the period (the control variable) and the switches' conduction time, that is:

$$t_d = t - 3t_0 \quad , \quad t_0 = \pi\sqrt{LC} \ . \tag{17}$$

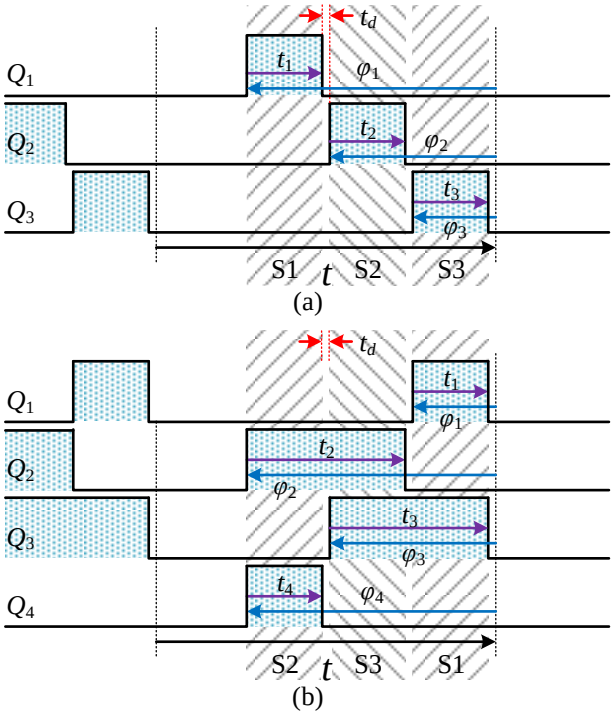


Fig. 17 Timing diagrams for the switching sequences of the GRSCC: (a) Basic configuration (Fig. 12), (b) Bridge realization (Fig. 16).

As can be seen in Fig. 17(b) for the special case of the bridge configuration, the switching sequence applies (S2, S3, S1) by overlapping the gate commands. Then, the required time delay is introduced. This is done to avoid reverse conduction paths due to negative potential of the flying capacitor that may result in undesired conduction of

the antiparallel diodes. Another benefit of this timing sequence is its compatibility to the conventional single on time setting of the PWM periphery.

TABLE I TIME SETTINGS FOR ON TIMES AND PHASE DELAYS OF FIG. 9

	t_1	t_2	t_3	t_4	φ_1	φ_2	φ_3	φ_4
Fig. 17a	t_0	t_0	t_0	-	$3t_0$	$2t_0$	t_0	-
Fig. 17b	t_0	$2t_0$	$2t_0$	t_0	t_0	$3t_0$	$2t_0$	$3t_0$

2.5 Comparison to Conventional Buck-Boost

2.5.1 Inductor

Similar to other resonant and DCM realizations, the inductor maintains a small value compared to the conventional CCM approach, however it has to sustain relatively high rms currents. In contrary to the magnetics design in switched-inductor converters operating in CCM, the per-cycle energy that is stored in the inductor is zero. As a result, the main factor affecting the inductor sizing stems from the core losses, rather than saturation limits. A convenient way to estimate the volume of the magnetic element is by the area product A_p, which can be expressed as:

$$A_p = \frac{L\Delta I I_{rms}}{JK\Delta B} \ , \tag{18}$$

where L is the desired inductance, ΔI is the maximum current variation through the inductor, ΔB is the maximum flux density variation due to ΔI, J is the current density that is allowed through the winding, and K is the fill factor.

For the particular case of the GRSCC, after some manipulations, (18) can be rewritten as:

$$A_p = \frac{\max(V_1, V_2) I_{rms}}{3\pi JK\hat{B}f_n} \ , \tag{19}$$

where $\hat{B}$ is the allowed peak flux density.

The area product of the inductor needed for the GRSCC described in the example above is relatively large since the DCM-like behavior of the GRSCC dictates high rms currents. If a ferrite is to be used, the resultant A_p would be comparable with an inductor for a buck-boost converter, designed according to the same specifications, operating in continuous conduction mode (CCM). However, since the inductance value that is required for the GRSCC is quite low (e.g. 0.5μH at 100kHz), a more compact rod configuration or a significantly smaller ferrite-less (i.e. air core) construction is feasible.

Consequently, higher $\hat{B}$ is allowed, resulting in a significantly smaller A_p. A normalized comparison between the required area products for various converter topologies and operation modes has been carried out and is summarized in Table II. A significant reduction of the inductor volume can be noticed for a GRSCC-based design by one-order of magnitude, when compared to a buck-boost of the same features. Table II also provides inductance estimation for operation at the specific frequency of 100kHz, Vo=20V, I_o=5A 20% ripple for the CCM modes of the buck and buck-boost.

TABLE II COMPARISON OF THE AREA PRODUCT, A_P BETWEEN VARIOUS CONVERTERS DESIGNED FOR VOLTAGE REGULATION

	Buck-boost		**Buck**	**GRSCC**		
	CCM	***BCM*** [a]	***BCM*** [a]	***Full core***	***Rod***	***Air***
$\tilde{A}_P$ [b]	50	10	10	40	10	1
$\hat{B}$ [T]	0.2	0.2	0.2	0.05	0.2	2
L [μH] for 100 kHz	35	5	10	0.5	0.5	0.5

a. Boundary Current Mode

b. Normalized to GRSCC with air core

2.5.2 Efficiency

To evaluate the efficiency features of the GRSCC, a comparative analysis versus a non-inverting buck-boost topology has been carried out. The basis for comparison took into account operation with identical target parameters (P_o=100W, V_o=20V), similar conduction losses (i.e. four switches in both topologies), and switching losses (when available). It should be noted that since the area product calculation of the magnetic element described above is based on equal losses, this factor has been removed from the efficiency estimation.

To establish a fair comparison for similar converters dimensions and reasonable losses, a synchronous buck-boost converter operating at BCM has been evaluated. The converter's efficiency considering conduction losses as well as switching losses (due to overlap) can be expressed as:

$$\eta_{BB} = \left[1 + 1.3 \frac{R_s}{R_L} \left(\frac{1+A}{A} \right)^2 + \frac{t_{tr}}{t} \frac{(1+A)^2}{3A} \right]^{-1}, \tag{20}$$

where the factor 1.3 is the rms to average current factor at BCM and t_{tr} is the on-off transition time of the switch.

Fig. 18 plots the efficiency of (20) compared with the efficiency estimation of the GRSCC derived in (14) as a function of the voltage gain A. The figure shows the results

for various loop resistances and operating frequencies. As can be observed, the main advantage of GRSCC is the ZCS operation that exhibits higher efficiency than the buck-boost at higher operating frequencies. This allows further enhancement of the power density of the GRSCC. For cases of higher conduction losses and lower switching frequency, utilization of a buck-boost converter is still preferred.

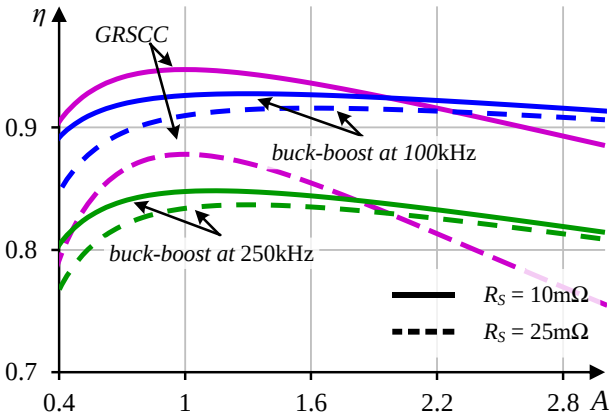


Fig. 18 efficiency curves of GRSCC and buck-boost converters operating with the target parameters: P_o=100W, V_o=20V (R_L=4Ω), t_{tr}×f_s=0.02,

2.6 Experimental Verification

TABLE III PARAMETERS OF THE EXPERIMENTAL PROTOTYPES

Parameter	Converter A		Converter B	
	Value	***Model***	***Value***	***Model***
C	0.26 µF	Polypropylene	10 ×0.1 µF	C4532C0G2A104J320KA
L	5.3 µH	ETD 34	0.5 µH	RM8/I-3F3
Q_1, Q_3	2×NMOS uni-directional	IRFP3077	PMOS	IXTP96P085T
Q_2, Q_4			NMOS	IXTP160N10T
C_L	1 mF	Electrolytic	5×10 µF	C5750X7SR1H106K
Drivers		MIC4427YN		MIC4427YN
MCU		dsPIC30F2020		dsPIC33F16GS502
R_S	130 mΩ		48 mΩ	
f_n	~100 kHz		~130kHz	
dead time	~180 ns		100 ns	
V_{in} (max)	55 V		30 V	
V_{out} (max)	70 V		30 V	
P_{out} (max)	200 W		100 W	

To demonstrate the operation of the GRSCC and to verify the theoretical analysis, two sets of experimental test-benches were constructed. In the first experiment, a Type-A converter that follows the generic topology of Fig. 12 was realized and examined for the fundamental characteristics of the gyrator converter and efficiency evaluation. In the second experiment, the converter was constructed as the bridge topology of Fig. 16 (Type-B) and its performance as voltage regulator was evaluated. Table III summarizes the parameters and lists the components of the two experimental prototypes.

In the Type-A topology, the bi-directional switches were realized by two power MOSFETs connected back to back. Floating switch drives were implemented by applying isolation transformers as shown in Fig. 19 [41]. The series resistance comprises the FET resistances, copper and core-losses. The system was tested under open-loop conditions, while the switching frequency and state switching periods were manually adjusted to obtain ZCS. Waveforms showing resonant, step-up and step-down, ZCS operation are given in Fig. 20. Validation of the converter's high efficiency along a continuous voltage conversion range is depicted in Fig. 21, and was carried out by varying the input voltage, and load resistance, while keeping the output power to be constant at around 10W.

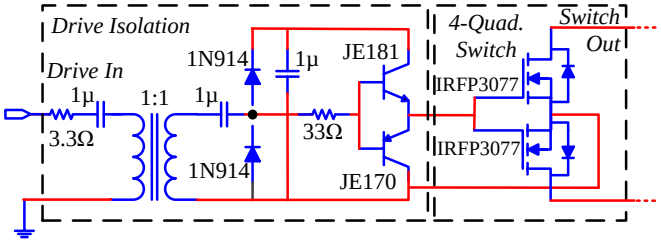


Fig. 19 Drive isolation for the switches in the type-A converter

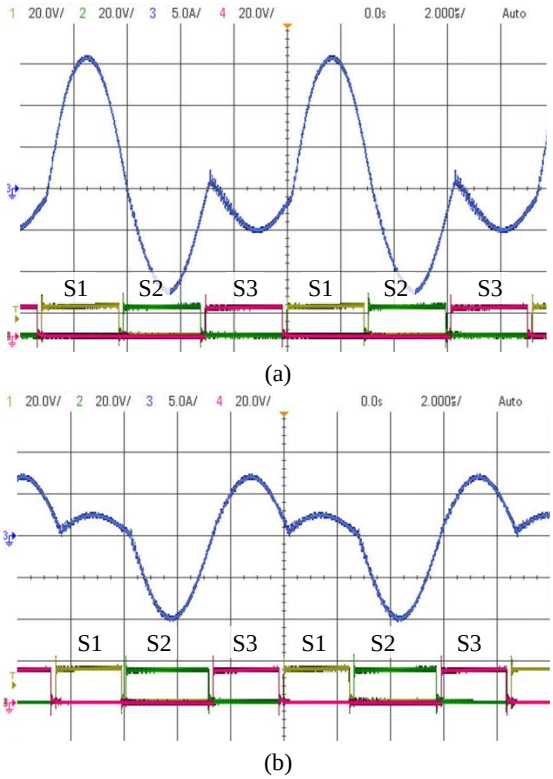


Fig. 20 Experimental waveforms: (a) In a step-up operation mode, (b) In a step down operation mode. Upper trace – inductor current (5A/Div.), Lower traces – S(1,2,3) gate signals. Horizontal scale 2µS/Div.

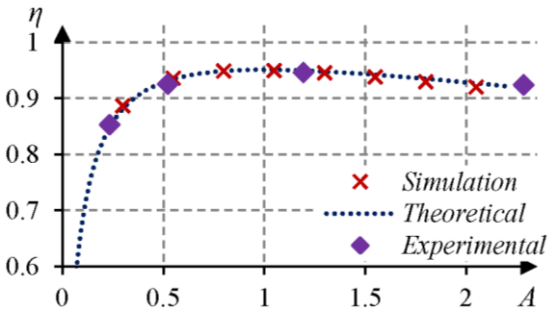


Fig. 21 Gyrator efficiency as a function of voltage gain, *A*.

As can be observed, the experimental results tightly follow theoretical calculations as well as the results of cycle-by-cycle simulation. The efficiency was measured to be well above 90% for wide operation range. The natural gyration ratio, g_n, of the converter as a function of voltage gain was evaluated by varying input voltage, while the output voltage was kept constant. This was done by varying R_L as V_1 changes. Theoretical calculations, simulations and experimental results for this evaluation are presented in Fig. 22.

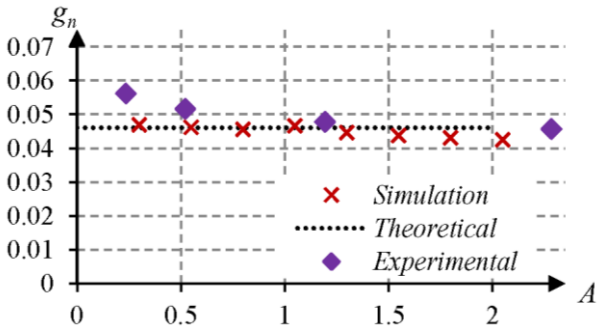


Fig. 22 Natural gyration ratio as a function of voltage gain, *A*.

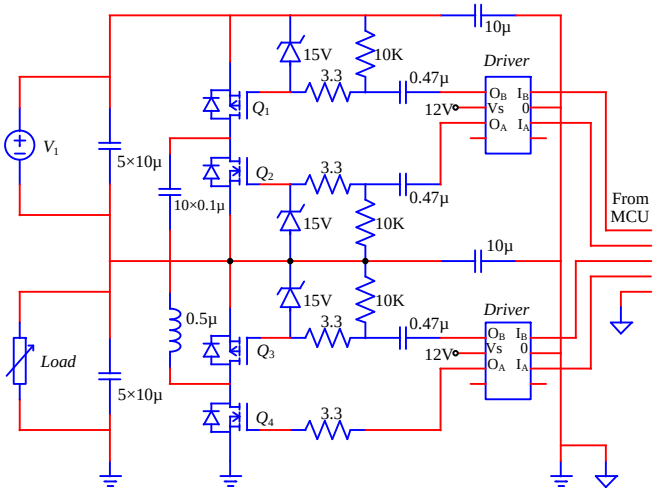


Fig. 23 Schematic of the type-B converter

The deviation of experimental results from the theoretical analysis at lower conversion ratios is primarily due to higher conduction losses, and consequently there are lower efficiencies at these ratios as can be seen from Fig. 21. Another reason for the deviation is that the resonant characteristics of the three states were not identical, and this was not accounted for in the derivations for g_n. In particular, as can be observed from Fig. 20b, the discharge period (S2) is significantly longer than other states and will have a growing effect on g_n for smaller values of A (larger step-down ratios).

In the Type-B topology of Fig. 16, the power MOSFETs Q_1 and Q_3 were implemented by PMOS and Q_2 and Q_4 by NMOS. As can be observed from Fig. 23, a capacitive coupled driver circuitry was used to pass the control signals from the microcontroller to the MOSFETs that were untied from ground potential [42], [43]. Fig. 24 shows a photograph of the PCB used for the experiment. Zero cross detection was done automatically by the microcontroller, while the frequency adjustment to maintain the desired regulation was obtained manually. It should be pointed out that unlike in the case of Converter A that operates in open-loop with constant frequency (f_n), Converter B was operated with manual frequency adjustments to achieve the desired output voltage. Fig. 25 shows the steady-state operation of the converter at f = 70kHz, V_{in} = 12V, V_{out} = 15V, P_{out} = 22W.

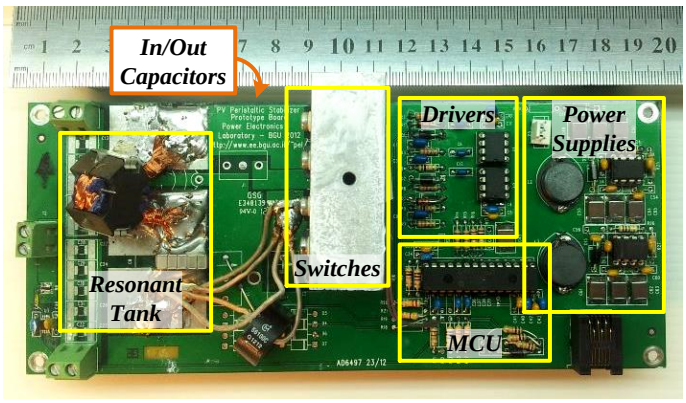


Fig. 24 Photograph of the PCB for the type-B converter

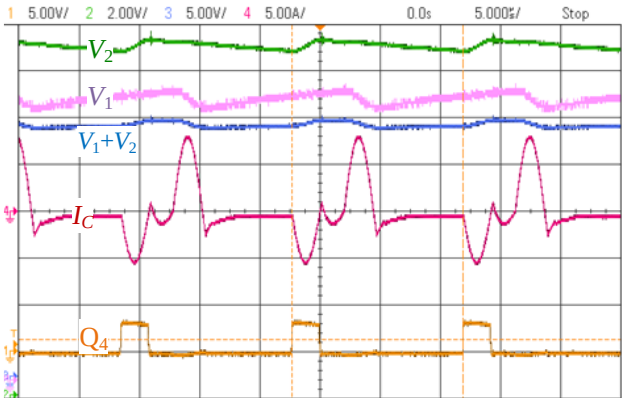


Fig. 25 Oscilloscope screenshot of a bridge gyrator converter, working at 70kHz with V_o = 15V, A = 1.25, $P_o \approx$ 22W, η = 90%. Traces from top to bottom: V_2, V_1(math funct. 5V/div), (V_1+V_2), I_C, $Q_{4,\mathrm{Gate}}$. The order of the states is S3-*discharge*, S1-*invert*, S2-*charge, delay*.

As one can see from the current waveform (second trace from the bottom), the converter is operated in a PDM mode; the switching frequency (f) is different from f_n, i.e. time-delay is introduced to facilitate regulation. Efficiency evaluation of the converter, for a range of voltage gains, was carried out by changing the input voltage and compensating via the total time such that the output power and output voltage, 22W and 12V respectively, were kept constant (Fig. 26). The theoretically calculated characteristics were found to be in close agreement with the experimental and simulation results.

Fig. 27 presents the efficiency of the Type-B converter as a function of the control parameter G. The theoretically predicted constant efficiency behavior is well validated by the simulation and experimental results for wide operation range. Some mismatches at lower G-s can be explained by the fact that at longer periods (lower G), the output voltage ripple increases as implied from (16), that is, larger voltage differences are present, and hence higher peak (and rms) currents are required to sustain the output voltage at the desired value, ultimately reducing the system efficiency. The deviation in the simulation points at low frequencies can originate from inaccuracies in the calculation method used, amplified by the low power at low frequencies. Fig. 28 summarizes the experimental traces of converter efficiency for different power levels as a function of control parameter G, for several conversion ratios (different traces), and supports the claim that the efficiency of the converter developed is primarily affected by the conduction losses.

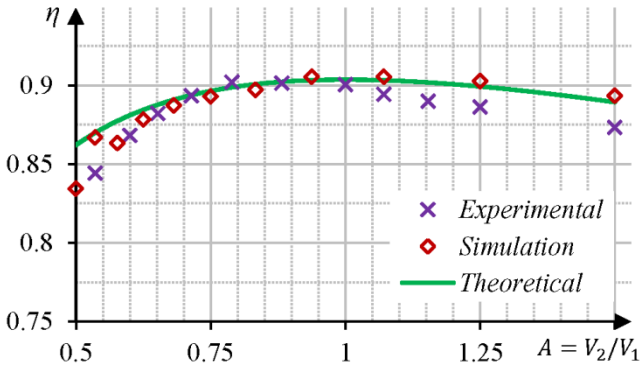


Fig. 26 Efficiency graph for the bridge gyrator as a function of *A*.

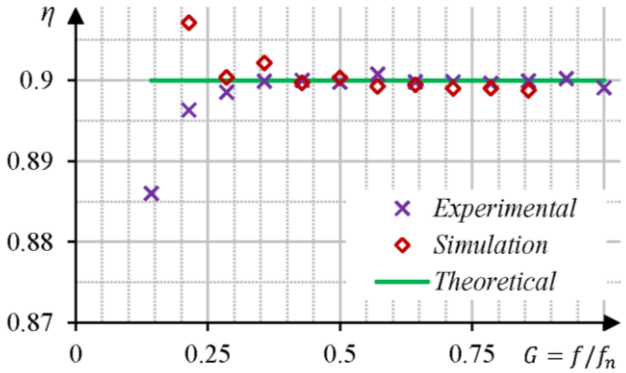


Fig. 27 Efficiency for the bridge gyrator as a function of the parameter, *G*.

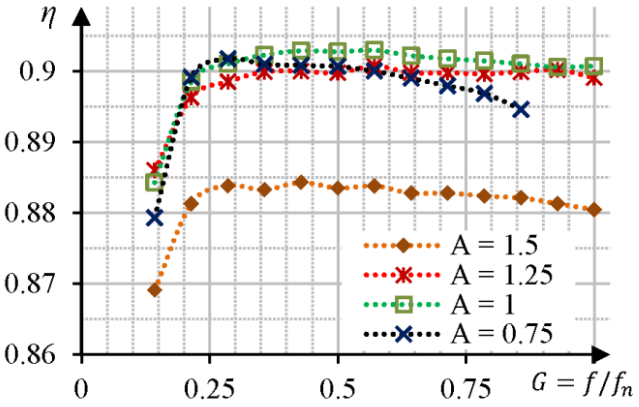


Fig. 28 Bridge Gyrator efficiency as a function of parameter G, voltage gain is a parameter.

CHAPTER 3:
Voltage Regulation by GRSCC

3.1 Introduction

State-of-the-art voltage regulators achieve minimal size and maximal power processing efficiency by combining switched-inductor converters with advanced nonlinear controllers [44]-[52]. The main limiting factor of this general concept is the presence of a relatively large inductor that prohibits, to a large extent, miniaturization and power-on-chip integration. Resonant-mode converters [53]-[58] allow volume reduction of the magnetic element by allowing higher frequency operation and lower energy storage requirements. Thanks to the soft-switching capabilities, the overall power conversion efficiency is not compromised due to the higher operating frequency [55], [56]. Another attractive feature that can be achieved by resonant converters, the capability to facilitate very high rejection ratio to variations in the line or in the load, has been demonstrated in [58], [59].

Conventional switched capacitor technology has become an attractive alternative for use in volume-sensitive applications, featuring high efficiency and economical implementation [60], [61]. However, as discussed in Chapter 1, it lacks the capability of achieving accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited. These limitations stem primarily from the fact that the efficiency of switched capacitor converters (SCCs) depends linearly on the voltage gain [19], [28], [30], [62].

The GRSCC (Chapter 2) has demonstrated unique potential for efficient voltage regulation over a wide range of conversion ratios and power levels, and can be used as the main building block of a voltage regulator.

This chapter explores the basic implementation of a small voltage regulator that is realized by the GRSCC and a simple pulse density modulation control scheme shown schematically in Fig. 29. The demonstrated voltage regulator exhibits an ideal response to load and line transients, i.e. with zero over/undershoot over the full operation range, as well as a constant efficiency profile across a wide range of voltage gain and power levels.

3.2 Voltage Regulation

The realization presented in Fig. 29 enables output voltage control by a comparator-based pulse density modulation (PDM). Discrete charge portions` transfer rate to the output is controlled such that a desired voltage level is maintained. The new voltage

regulator combines the virtues of both worlds: wide operation range having high efficiency at high frequencies (similarly to resonant switched-inductor converters), alongside reduced volume and potential chip-integration (similarly to SCC).

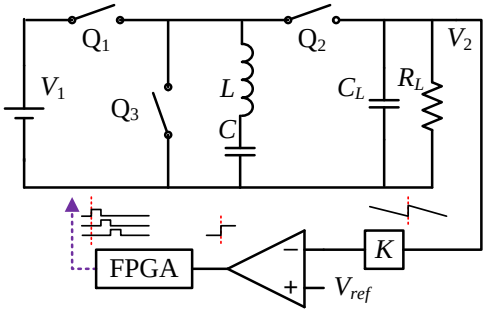


Fig. 29 The proposed voltage regulator: A new gyrator resonant switched capacitor converter and feedback loop.

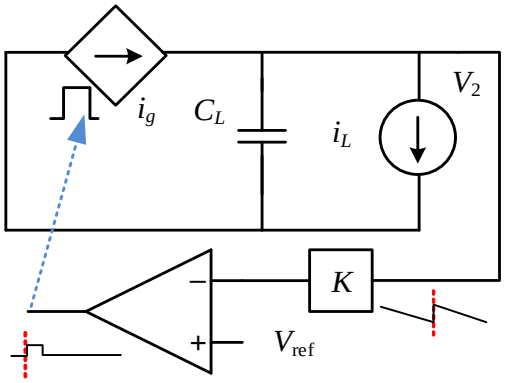


Fig. 30 An illustrative model of the GRSCC based regulator. The GRSCC is modeled as an ideal pulsed current source, I_g.

From (10) in Chapter 2, the gyration ratio g for the GRSCC can be rewritten as:

$$g = \frac{2f\sqrt{LC}}{Z} = 2fC \tag{21}$$

For a resistive load, R_L (7) can then be rewritten providing the output voltage as:

$$V_2 = I_2 R_L = 2R_L V_1 fC \ . \tag{22}$$

If f is made controllable, the system is able to react to and compensate for any changes in the input voltage, reference voltage or the load resistance such that the average output voltage is obtained without over/undershoot. This is due to the discontinuous-conduction mode (DCM)-like operation of the converter which naturally maintains per-cycle charge balance between the input and the output [63], which in the GRSCC case is facilitated with the addition of the third switching phase.

A more illustrative description of the voltage regulation concept using the GRSCC is shown in Fig. 30 and is complemented by the waveforms of Fig. 31. As described earlier in the previous section, and as can be observed from the experimental Fig. 25

(Chapter 2), the GRSCC operation is pulsed in its nature. Consequently, as a pulsed current source, i_g can be used to model its output characteristics. The current source, i_L, is used to model the current loading state. Voltage regulation is facilitated by triggering i_g to output a current pulse whenever the output voltage reaches the threshold level V_{ref}.

For a given load current I_L, and assuming that no current is injected from the source, the voltage across C_L drops virtually linearly (by first-order approximation). Once the output voltage reaches V_{ref}, a comparator event triggers the pulsed current source, restores the charge on C_L and resumes at the steady-state. This mechanism is maintained as long as the pulsed source contains sufficient energy to recover the voltage across C_L. Compensation for changes in the loading current is inherent due to differences in the discharge gradient of C_L, which vary the pulse rate of i_g.

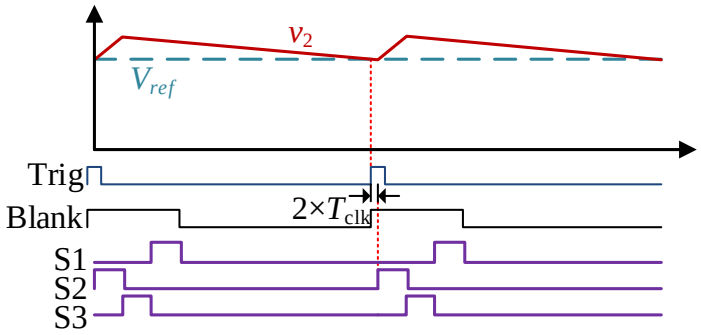


Fig. 31 Waveform relations between comparator inputs and the state signals for the proposed voltage regulator from Fig. 29. 'Trig' is the signal received from the external comparator, 'Blank' is an internal blanking signal to avoid overlapping if subseqent pulses are needed.

The PDM operation of the GRSCC, triggered by the comparator event, creates a switching sequence of (S2, S3, S1) and is then followed by a time-delay until the next comparator trigger. The order of the switching sequence is arranged such that after the time-delay, which allows the output voltage to drop down to V_{ref}, the discharge state (S2) is initiated to first charge the output capacitor back to $V_{\text{ref}} + \Delta V_2 / 2$, preventing further voltage drop. Then, the other two states (S3, S1) are commenced to *"arm"* the flying capacitor, having the converter ready for a new cycle. As mentioned earlier, the rate f in which the switching sequence is activated depends on the slope and the amplitude of the voltage ripple, that is, on the load current and C_L.

3.3 Practical Considerations

3.3.1 Offset

The deviation of the instantaneous output voltage from the desired value is within the margins of the peak-to-peak output voltage ripple, ΔV_2, which depends on the operating conditions and is inversely proportional to C_L as:

$$\Delta V_2 = 2V_1 \frac{C}{C_L}\left(1-\frac{f}{3f_n}\right) . \tag{23}$$

In case the output capacitor includes a significant series resistance, R_{CL}, the magnitude of the output voltage ripple can be approximated to (assuming in-phase effect of RCL [64]:

$$\Delta V_2 = 2V_1 \frac{C}{C_L}\left(1-\frac{f}{3f_n}\right) + R_{CL}\frac{V_1}{Z} . \tag{24}$$

The reference value is set to the lowest allowed voltage, taking into account the voltage ripple by:

$$V_{\text{ref}} = V_2 - \Delta V_2 / 2 . \tag{25}$$

Following the PDM method described herein, the average output voltage is constant (within the ripple margins), and is independent of R_L and V_{in}. As can be observed from (23), the voltage ripple primarily depends on V_1, while changes in the load (which vary f) are up to 17% of the ripple value. In most cases, this deviation is negligibly small, and ΔV_2 in (25) can be approximated to an averaged ripple amplitude. Since the average output voltage is maintained at all times, i.e. there is no transient time, the voltage regulator can be considered to constantly operate at steady-state, and the efficiency estimated in (14) is applicable. Furthermore, no-load protection is inherent since no triggering will occur.

3.3.2 Output filter and output voltage measurement

Similarly to other ripple-based voltage regulators, different types of output capacitors may affect the performance and the stability of the system [65]-[67]. This is a result of a more complex output impedance behavior than a single left-half-plane pole. Potential remedies to this problem have been widely covered in [66] by introducing a firm stability criterion to the structure of the output filter with respect to the on-time duration. In this study, the output filter design is limited to capacitors of the same type

and the selection of the output capacitance value is obtained by the target ripple value employing (24).

Another issue that needs to be resolved is the selection of the target output voltage ripple that will satisfy the load requirements and at the same time allow reliable measurement. A comparator-based measurement is inherently sensitive to noise, in particular due to the output capacitor's ESR in the presence of pulsating output current. From the comparator point of view, sufficiently high SNR is satisfied if the lower value of the target ripple exceeds the error measurement value of the comparator. A second measure of noise reduction can be obtained either by passive means using filter capacitors [66], [68], or by digital means employing a blanking period. This study adopts the latter approach, which in addition to enforcing the f_n limit, accounts for the stability considerations presented in [65], [69].

3.3.3 Startup

Soft start in this realization is inherent; upon startup the voltage across C_L is zero (i.e., $V_2 < V_{\text{ref}}$) and the controller operates at f_n to increase V_2. C_L is then charged under constant current until the desired voltage is obtained. To further limit inrush currents, V_{ref} can be made to slope up slowly. Due to the GRSCC's current sourcing nature, overload or short-circuit conditions would not damage the converter, however, voltage regulation is not guaranteed beyond the maximal output rate of f_n.

3.4 Behavioral Modelling

3.4.1 Average-behavioral model and stability analysis

Assuming that the GRSCC operates under ZCS, the behavior of the voltage regulator presented in this proof of stability for this type of regulators has been presented in [65], [66]. However, the details related to the behavior of the regulator in response to disturbances have not been widely covered. To evaluate the regulator's response and to analyze the stability, a generic average-behavioral model has been developed and verified by simulations. Without losing generality, the model is directly applied to the GRSCC as the power converter.

As described in Fig. 29, a ripple-based regulator comprises a switch-mode power stage and an output filter that is fed to the inverting terminal of a comparator. The

switching sequence to the power stage is triggered by the comparator event. This operation can be represented by the simplistic block diagram of Fig. 32.

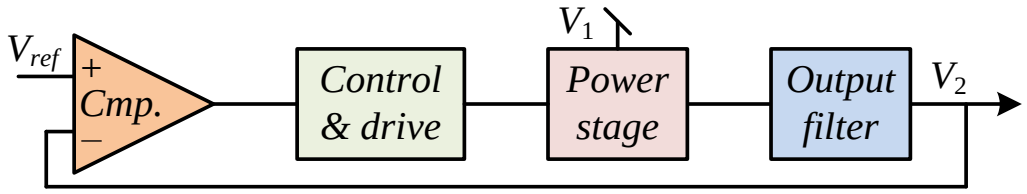


Fig. 32 A block diagram representing the closed-loop operation of a ripple-controlled regulator.

The output filter behaves according to the values of C_L and R_L. The output impedance can be expressed as:

$$Z_o = \frac{V_o}{I_2} = \frac{R_L}{1 + \mathrm{S} C_o R_L} \quad . \tag{26}$$

As mentioned in Section 3.2, the GRSCC power stage that is applied in this study outputs a current I_2 as a function of the input voltage V_1 and a large-signal control command F. Assuming ZCS operation, equation (22) is valid, resulting in a control-to-output transfer function of the form:

$$H_F = \frac{I_o}{F} = 2CV_1 \quad . \tag{27}$$

The comparator is modeled in this study by the resultant average behavior of the ripple regulator. In the context of the GRSCC, voltage comparison triggers the next charging cycle, effectively generating a frequency command. To analyze the behavior, a charge-based expression is derived as follows. The error between the output and the reference voltages, $V_e = V_{\mathrm{ref}} - V_{\mathrm{o}}$ corresponds to the missing charge at the output $Q_e = C_o V_e$. Subtracting this value from the charge obtained within a single pulse by the GRSCC, $Q_2 = 2CV_1$, yields the delivered charge from the regulator, Q_o as:

$$Q_o = Q_2 - Q_e = 2CV_1 - V_e / C_o \quad . \tag{28}$$

The equivalent frequency of the GRSCC is obtained by the information of the load current as:

$$F = \frac{I_o}{Q_o} = \frac{I_o}{2CV_1 - V_e / C_o} \quad . \tag{29}$$

To model the physical limitations of the switching sequence, the following constraints are added: F is limited to f_n at under voltage/overload, and forced to zero at overvoltage.

The resultant frequency can be re-written as:

$$F = \begin{cases} 0 & , \quad V_e < 0 \\ \dfrac{I_o}{2V_1 C - V_e / C_o} & , \quad \& \begin{matrix} Q_o > 0 \\ F < f_n \end{matrix} \\ f_n & , \quad \text{else} \end{cases} . \tag{30}$$

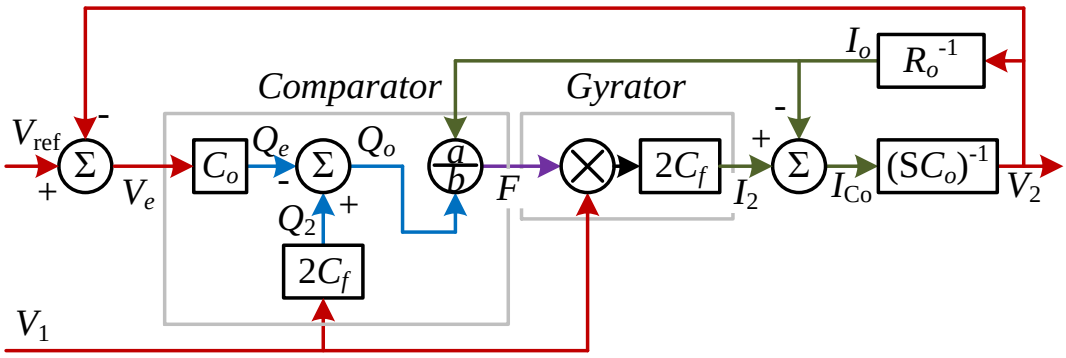


Fig. 33 An average-behavioral model for the GRSCC voltage regulator

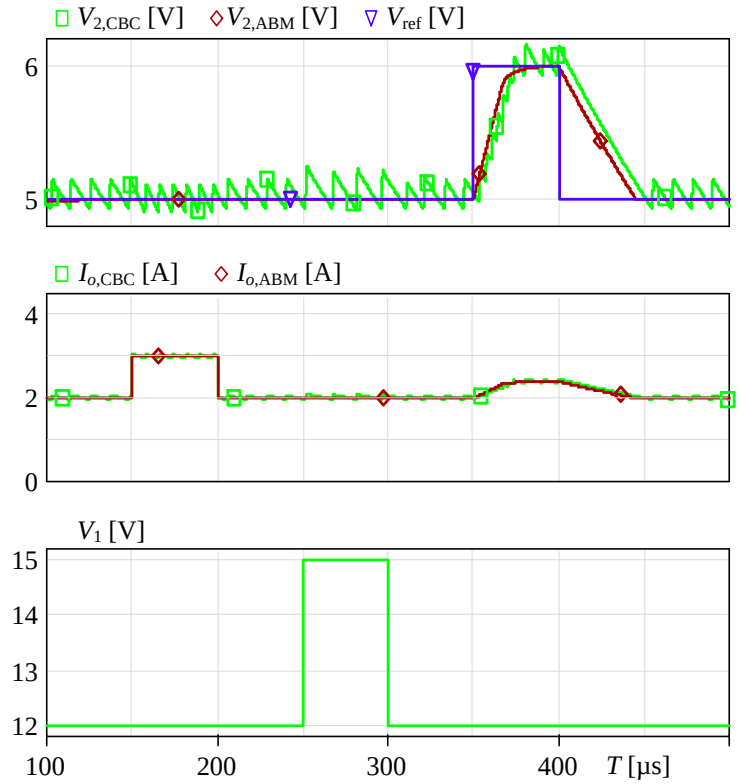


Fig. 34 A PSpice simulation that demonstrates the transient behavior of the presented ABM in comparison to a cycle-by-cycle model. Operating conditions and values match those of Table IV, with added 50 µs pulse disturbances of ΔI_o = 1A, ΔV_1 = 3V and ΔV_{ref} = 1V, distributed at 150µs, 250µs and 350µs accordingly.

Fig. 33 shows an average-behavioral model (ABM) of the GRSCC voltage regulator with the constraints of (30) omitted for clarity. This non-linear model is applicable to any modern circuit simulator for both large and small signal analysis. In addition, the

model is valid for examining disturbances in the reference voltage as well as in line or load conditions. To validate the model, it has been compared to a cycle-by-cycle simulation as depicted in Fig. 34, using PSpice (Cadence PSpice A/D V16.5). It can be seen that the response to line or load transients is immediate (within a single switching cycle), whereas the response to changes in V_{ref} is of first-order with slew-rate limitation due to the constraints on the large signal F. It should be noted that the slew-rate stems from to the ratio between the I_o, which depends on the load, and the maximum/minimum available I_2, which depends of F. Further insight to the design of the saturation current can be seen in section 4.2, where an envelope-tracking application is presented.

3.4.2 Small-signal analysis

To extract the small-signal transfer functions for each of the individual blocks, linearization around an operating point is applied and then followed by a small-signal analysis; the resulting block diagram is shown in Fig. 35. The expressions for each of the blocks are as follows:

$$
\begin{aligned}
B &= \left.\frac{f}{v_e}\right|_{\substack{i_o=0\\ v_1=0}} = \frac{C_o V_2}{\left(2CV_1\right)^2 R_L} \\
H_f &= \left.\frac{i_{Co}}{f}\right|_{v_1=0} = H_F = 2CV_1 \\
\frac{v_o}{i_{Co}} &= Z_o = \frac{R_L}{1+\mathrm{S}C_o R_L} \\
G_{v1} &= \left.\frac{i_{Co}}{v_1}\right|_{\substack{v_e=0\\ i_o=0}} = -\frac{2I_o CC_o}{\left(2V_1 C - V_e C_o\right)^2} V_e \\
H_{io} &= -\left.\frac{i_{Co}}{i_o}\right|_{\substack{v_e=0\\ v_1=0}} = -\frac{C_o}{2V_1 C - V_e C_o} V_e
\end{aligned}
\quad , \tag{31}
$$

where f, v_e, i_{Co}, v_o, v_1, and i_o are the small signal perturbations around the operating points of F, V_e, I_{Co}, V_o, V_1 and I_o, respectively. Based on Fig. 33 and (31), the small-signal closed-loop transfer function can be expressed as:

$$
v_o = \frac{BH_f Z_o}{1+BH_f Z_o} v_{\text{ref}} + \frac{H_{io} Z_o}{1+BH_f Z_o} i_o + \frac{G_{v1} Z_o}{1+BH_f Z_o} v_1 \ . \tag{32}
$$

Expression (32) is valid where the loop-gain is dominant, i.e. at frequencies where $BH_fZ_0 \gg 1$.

Fig. 36 shows the system frequency response to perturbations in the reference, input and the loading conditions. The information regarding the regulator's stability can be

directly obtained from (32). The system loop-gain, BH_fZ_o includes a single left-half-plane pole, which suggests the closed-loop response to changes in the reference is stable and of first-order. Since the characteristic equation is identical to all the perturbations, the system stability in response to changes in the input voltage or the load depends on H_{io} and G_{v1} alone [70]. As can be observed from (31), H_{io} and G_{v1} are constants, and therefore, stability is guaranteed. The response to changes in the line or load introduce relatively high rejection ratio (above 100dB) which implies that the system is, in fact, immune to these perturbations, confirming the initial objective of the ideal-response voltage regulator.

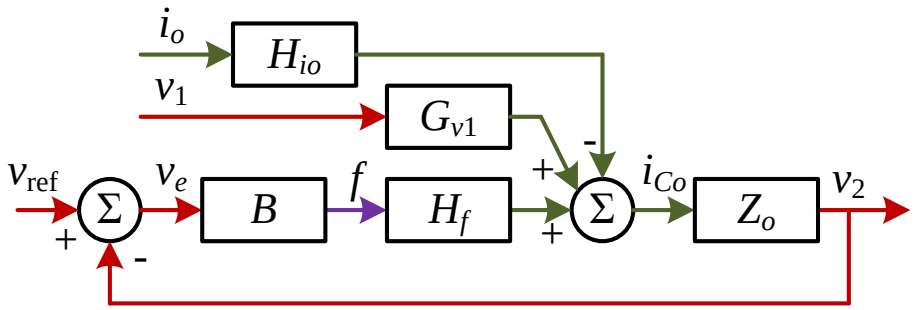


Fig. 35 A linear transfer diagram modelling the small-signal behavior of the GRSCC regulator.

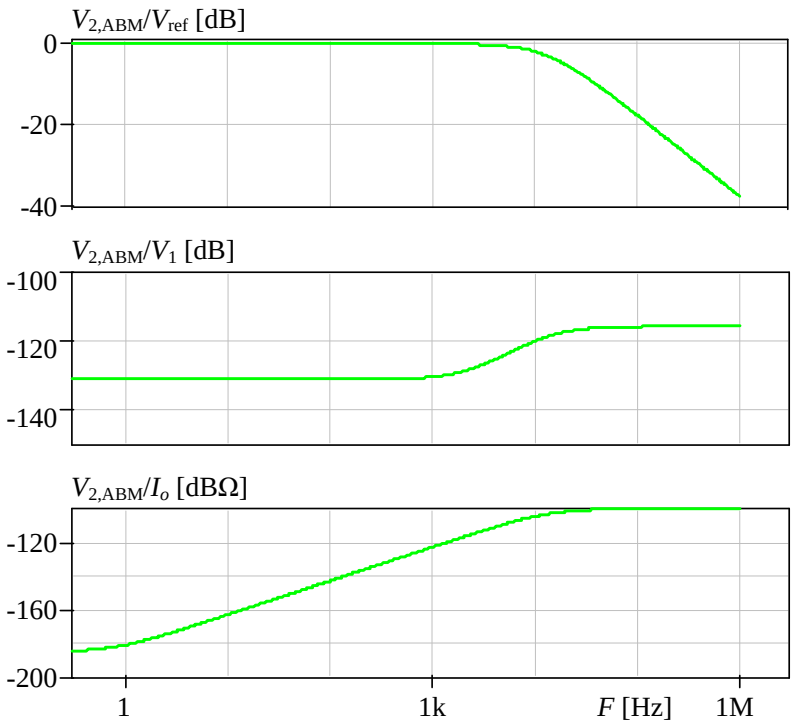


Fig. 36 PSpice frequency-response measurements of the presented ABM to small-signal perturbations at the reference, line and load.

3.4.3 Numeric validation of zero-order response

To verify the control-to-output (i_{Co}/f) zero-order response feature of the GRSCC, a frequency response simulation has been constructed in PSIM (Powersim inc.). The triggering algorithm has been implemented by a C-block generating a frequency modulated (FM) control command having carrier frequency of 90 kHz and modulating signal (magnitude) of 20 kHz. Then, the rate of the modulating signal has been swept while measuring the ratio between the output current and the magnitude of the modulating signal. Fig. 37 shows the resultant frequency response. It can be observed that the control-to-output response is virtually constant in magnitude with zero phase-lag over the entire operation range, i.e. up to half of the frequency of the lower sideband of the control command. This implies that the converter is capable of accommodating load transients with zero-order response up to the rate of $f_n/2$.

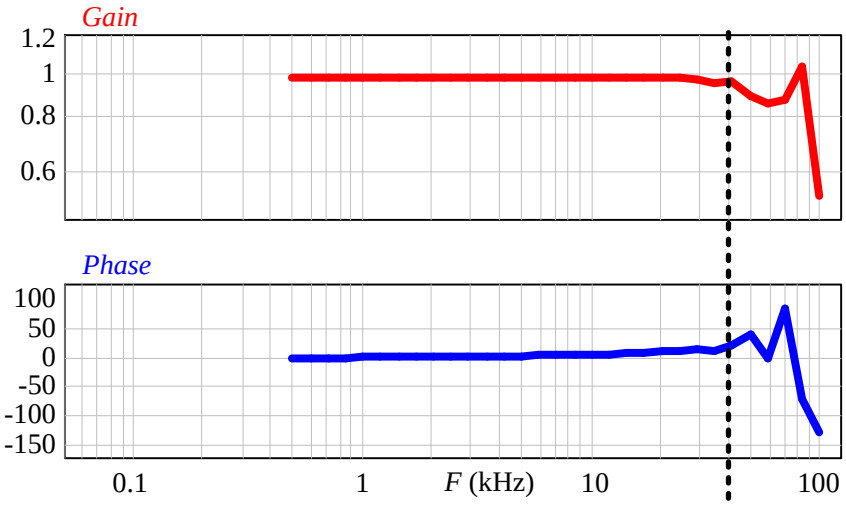


Fig. 37 Control-to-output frequency response. Top: output magnitude normalized to theoretical (ideal) output. Bottom: phase (degrees). The vertical line marks $f/2$=35 kHz

3.5 Design Example

The design procedure of a voltage regulator based on the GRSCC topology is described through an example of a 20W step down inverting voltage regulator with the target values of V_o = 5V, V_{in} = 8 to 15V, f_n < 500kHz.

First, the values of L and C are derived by combining f_n given by (9) and (22) with accounting for the worst-case of f_n, $V_{1,min}$ and $I_{2,max}$, as follows:

$$\begin{aligned} C &= \frac{I_{o,\max}}{2V_{1,\min} f_n} \\ L &= \left[\left(3\pi f_n\right)^2 C \right]^{-1} \end{aligned} \quad . \tag{33}$$

The second step is to estimate the values of the rms current that circulates in the resonant tank. This is done for proper selection of the switches as well as to determine the physical sizes of L and C. In a similar manner to the efficiency extracted in (14), the rms current can be expressed as:

$$I_{\text{rms}} = \sqrt{V_2 I_2 \frac{\pi}{2Z}\left(A + A^{-1} - 1\right)} \quad . \tag{34}$$

Finally, given a desired target voltage and defining the allowed voltage deviation, the output capacitor value and the reference voltage are calculated using (23) and (25) respectively.

Given the above parameters, the inductance and capacitance are calculated by (33) to be L = 100nH and C = 560nF. These were chosen such that 20W of power can be processed from the input range specified. Given a typical loop resistance of R_S = 20mΩ, the expected efficiency is in the range of 85% to 92%. Similarly to switched-inductor PDM converters, the rms currents are relatively higher than conventional converters that operate in continuous conduction mode (CCM). As opposed to other PDM converters, no additional losses are present thanks to the resonant current and the resultant soft-switching operation. In this particular design, the rms current is estimated to be 12A at maximum effort. The main problem with higher rms currents is the stress on the flying capacitor. This can be overcome by paralleling capacitors of smaller values.

3.6 Experimental Results

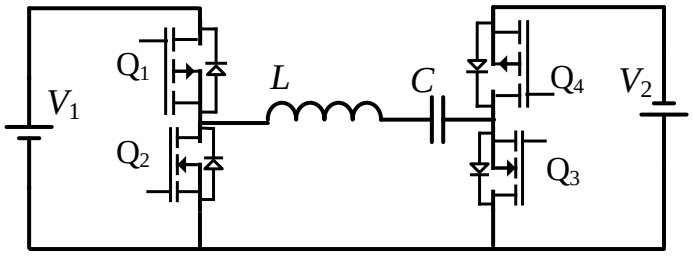


Fig. 38 The experimental inverting scheme, using four MOSFETs

TABLE IV EXPERIMENTAL SPECIFICATIONS

Parameter	*Value*	*Model*
C	10 ×100 nF	C4532C0G2A104J320KA
L	180 nH	Air-winding
Q_1, Q_3	PMOS	IXTP96P085T
Q_2, Q_4	NMOS	IXTP160N10T
C_L	5×10 μF	C5750X7SR1H106K
Drivers		MIC4427YN
R_S	48 mΩ	
f_n	~250kHz	
dead time	100 ns	
V_1	8 V - 15 V	
V_2	5 V	
Rated power	20 W	

To verify the operation of the converter as a voltage regulator and to demonstrate the ideal transient features of the system, a 20W experimental prototype was realized using an inverting bridge configuration (Fig. 38). The target parameters and the list of components used are summarized in Table IV. A digital PDM controller was implemented on a FPGA (Altera Cyclone IV). The ZCS operation of the gyrator RSCC is sensitive to input voltage variations, but since the input range is moderate, satisfactory results were achieved by pre-calibration.

The controller was programmed to execute a pulse sequence for the drivers whenever a trigger from a comparator was sensed for two or more consecutive clock-cycles, as illustrated in Fig. 31. An internal blanking signal was added to dictate $F_{\max}$ and prevent overlapping between sequences during startup or overloads.

Fig. 39 shows the current and voltage waveforms across the flying capacitor C, matching the theoretical waveforms as well as validating the operation under zero-current switching. The residual lagging current that follows the discharge phase is due to the discharge of drain-source capacitances. Fig. 40 demonstrates the ideal load transient response of the voltage regulator for both light-to-heavy and heavy-to-light modes for zero to nominal current (4A) load transients and for 1A to 3.5A.

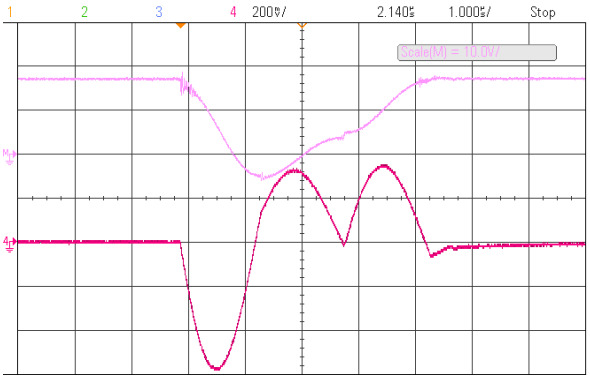


Fig. 39 Experimental waveforms of a discharge-invert-charge sequence, showing V_C (top, 10V/div) and I_C. (bottom, 9A/div)

The current waveforms in Fig. 40 (b) and (c) include some parasitic effects of the experimental load stepping setup; a load resistance with stray inductance was switched in and out using an open-drain sink. The turn-on rise-time shown in Fig. 40 (b) matches the load inductive time-constant value, while the frequency of the oscillations in the turn-off current in Fig. 40 (c) are well estimated by the load inductance-capacitance parasitics. The oscillations observed in V_2 are the result of relatively low common-mode rejection of the measurement.

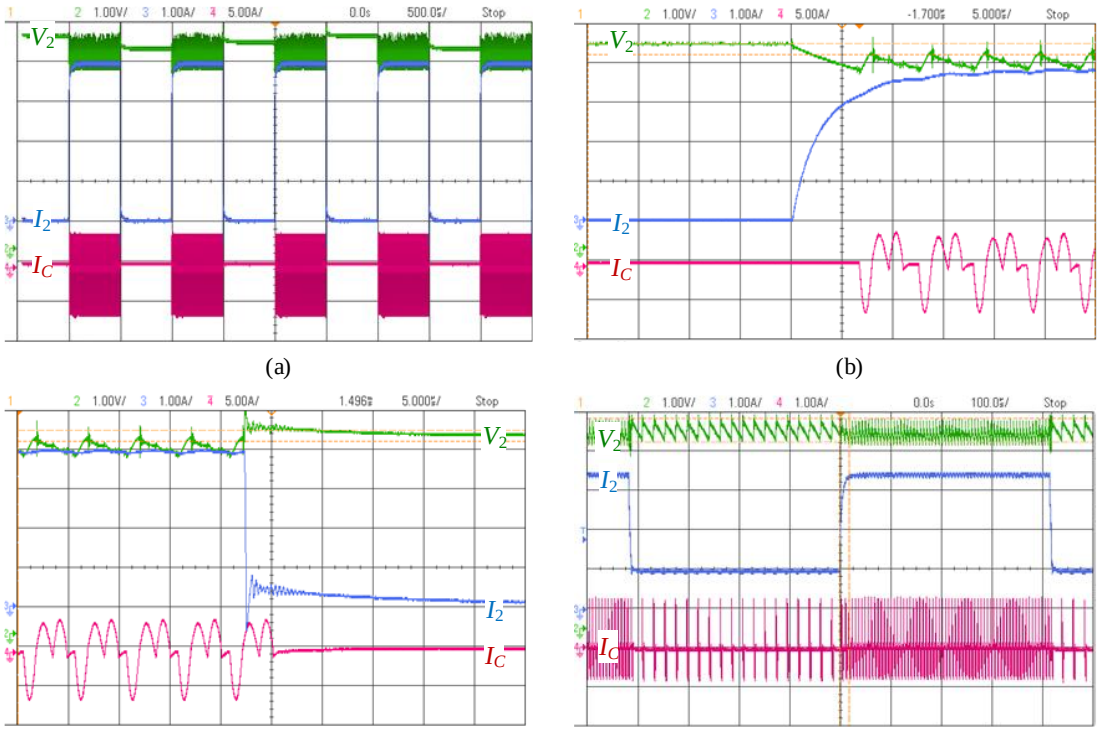


Fig. 40 Screenshots obtained from the experimental setup. V_1=12V, V_2=5V, I_2={0A,4A}. Signals are: CH2-V_2, CH3-I_2, CH4-I_C, (a) zoomed out view on voltage stabilization with full range of load step, I_2={0A,4A} switched repeatedly at 1kHz, (b) light-to-heavy load step, I_2={0A,4A}, (c) heavy-to-light load step, I_2={4A,0A} (d) mid-range load step variation, I_2={1A,3.5A} switched at 1kHz.

The deviation of the output voltage from its average value is measured to be around 100mV. A minor discrepancy is evident between the calculations of L and C for the effective operation range and is due to practical efficiency which is not taken into account in (33). This resulted in a slightly higher bound on the input voltage, around 9V (instead of the original 8V) used to deliver power of 20W to the output. The measured efficiency of the converter at 25% load ranged between η = 72% (V_1 = 15V) and η=83% (V_1= 9V), matching the calculated efficiency.

CHAPTER 4:
Regulation Applications

4.1 Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Connected GRSCC

4.1.1 Introduction

Advancement in hardware-efficient digital controllers [71]-[75] enables the implementation of advanced nonlinear control methods that improve the dynamic performance and, as a consequence, drastically reduce the size of the output capacitor of voltage-regulation modules (VRMs). Among them, time-optimal control (TOC) [45], [47], [48], [76]-[78] and minimum-deviation [79] controllers have demonstrated transient response having virtually the smallest possible voltage deviation, restricted only by the inductor current slew-rate. In VRM applications, this limitation has a major effect on the output voltage deviation in the case of an unloading transient event, primarily due to the high input-to-output conversion ratio. Another weakness of the classical time-optimal approach is the relatively higher current stress, beyond the steady-state value, that is required to restore the lost charge of the output capacitor during the recovery time [80]. As a result, the overall power processing efficiency is impacted by consecutive transients, when compared to steady-state [81].

State-of-the-art solutions that exceed the performance of the TOC method propose several circuit extensions to the original buck converter [82]. To deliver the current to the load with higher slew-rate, modifications that apply higher voltage on the inductor during load transients [83], [84] or to reduce the actual inductance of the main inductor [85], [86] have been proposed. Other extensions present an addition of a fast auxiliary converter having smaller inductance in parallel to the main converter [87]-[90], resonant circuit [91], switching resistors [92]-[94], or active region current injection circuit [95]-[98]. However, this comes at the cost of an increased input filter, since the load transient is reflected to the input, and the switches of the auxiliary stage must be rated to withstand the higher system voltage. This is partly resolved by compensating for only half of the current mismatch, which does not increase transient time [99]. Regulation of such auxiliary circuits requires additional sensors, which increase the realization, control and system complexity.

Studies have reported improved loading and unloading transient performance obtained using an auxiliary converter connected to the output side [100]. An independent energy bank is used, eliminating the impact on the input, and employs switches with lower voltage ratings, further reducing the power loss and the size of the

system. Although these solutions require additional sensors to regulate the auxiliary circuit's operation and are limited by switching frequency to mid-range output voltages, they provide a new concept for improving the performance of VRMs, and therefore are adopted in this study.

The GRSCC, developed as a regulator in the previous chapters, demonstrates an ultra-compact voltage regulator solution which obtains ideal transient response. However, a modest efficiency (around 85%) at steady-state is achieved due to high rms currents. Nonetheless, its main advantage is that due to low inductances needed, no ferromagnetic element is required, allowing on-chip integration.

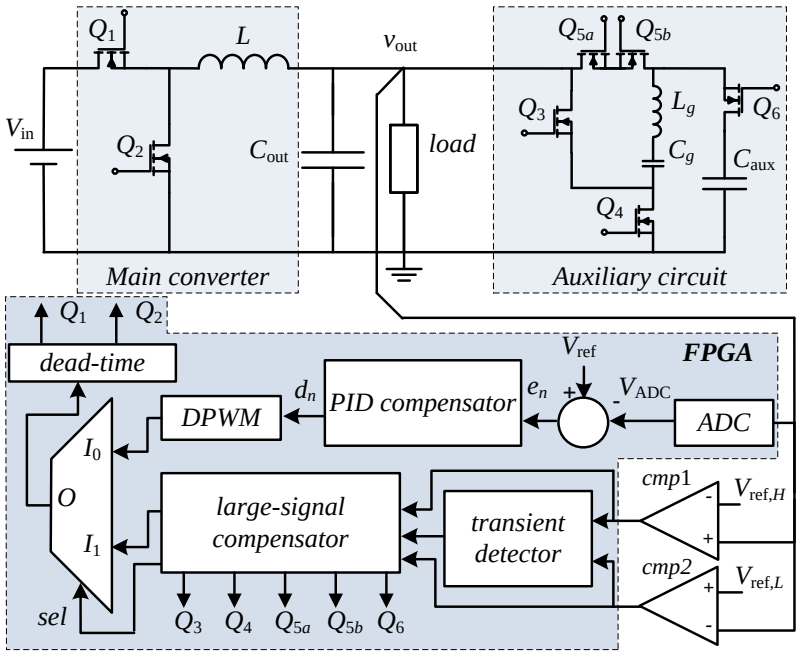


Fig. 41 Hybrid-VRM with load-side GRSCC auxiliary circuit. The area within the bottom box is implemented within an FPGA.

The objective here is to introduce a new compact VRM solution that merges a buck converter with a resonant switched-capacitor auxiliary circuit that is connected at the load side, as detailed in Fig. 41. By incorporating a new control concept, the auxiliary circuit effectively mimics increased capacitance during loading and unloading transient events, reducing the burden on both the input and output filters, and reduces the current stress. In addition, the hybrid-VRM presented in this study requires indication from the output voltage alone and is implemented using a simple state-machine based controller, making this solution simple and cost-effective.

4.1.2 Transient recovery by a load-side auxiliary circuit

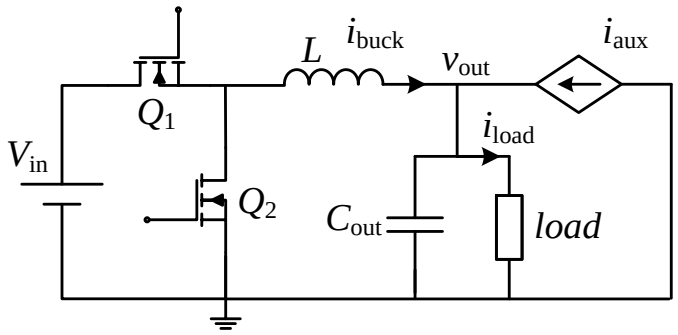


Fig. 42 Simplified circuit with the auxiliary circuit modelled as a controlled current source, demonstrating the current relationships towards the load.

A key factor for assisting the recovery of the main converter from a load transient is the capability of the auxiliary circuit to rapidly sink or source the current mismatch between the new load state and the main inductor current. To analyze the required behavior and control mechanism of the auxiliary unit, an idealized bi-directional current source that is connected to the output terminals of the voltage regulator can be assumed as depicted in Fig. 42.

The analysis is aided by Fig. 43 which shows average waveforms for different sinking patterns of the current source to a current unloading step of ΔI_{out}. It is further assumed that a time-optimal-like control is implemented for the main converter to maximally expedite the recovery phase.

To eliminate any deviations of v_{out} from the steady-state value, V_{out}, the auxiliary circuit is to mimic infinite capacitance, i.e. mirror the mismatch between i_{buck} and i_{load}. As shown in Fig. 43(a), the auxiliary current, i_{aux}, is triangular, ramping down from ΔI_{out} and reaching zero when i_{buck} equals i_{load}. In this case, the total transient time, T_{tr}, is governed by the main inductor current slew-rate and current mismatch, and can be expressed as:

$$T_{tr,\text{loading}} = \frac{L}{V_{in} - V_{out}} \Delta I_{out} \ , \ T_{tr,\text{unloading}} = \frac{L}{V_{out}} \Delta I_{out} \ , \tag{35}$$

where L is the main inductor value and V_{in} is the input voltage. This case produces a significantly shorter transient time than is obtained using classical TOC approach, since no additional discharging is required to drain excess charge from C_{out}.

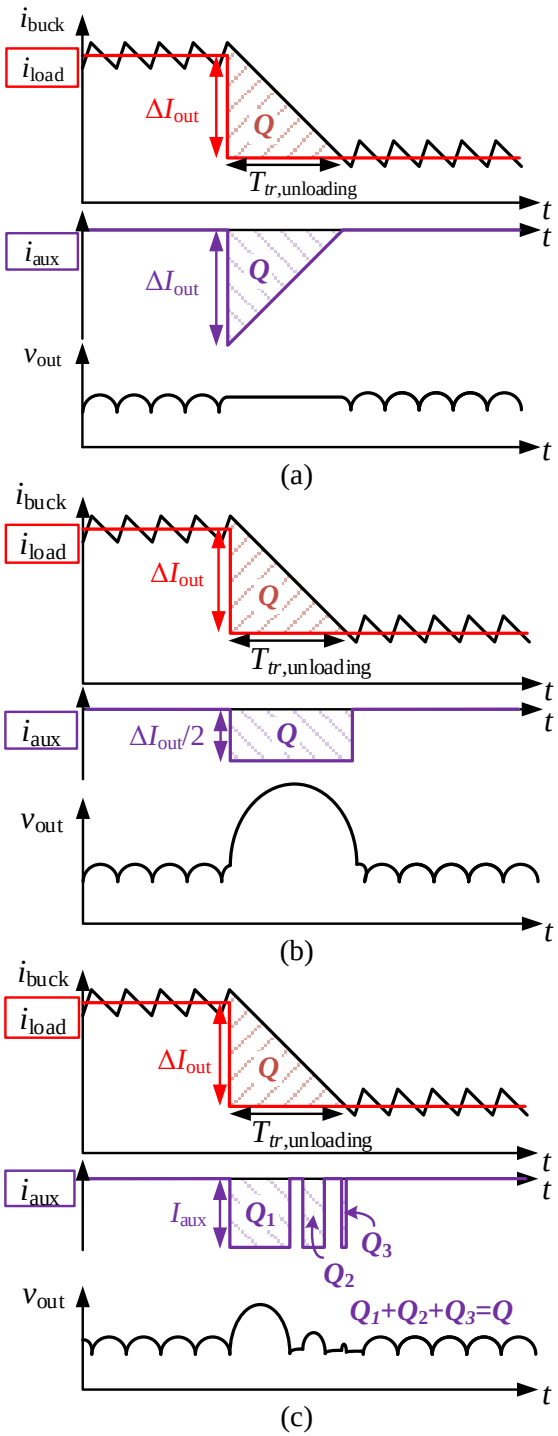


Fig. 43 Schematic response waveforms of the hybrid-VRM to an unloading step of ΔI_{out} for different auxiliary behaviour. (a) $i_{aux} \approx i_{load} - i_{buck}$, (b) $I_{aux} = \Delta I_{out}/2$, (c) $I_{aux} > \Delta I_{out}/2$, segmented to match the overall charge Q.

Realization of an auxiliary unit as described by Fig. 43(a), rated for the peak load current is, to some extent, over-designed. It requires higher stress-rated components to accommodate for stress that exists for only slight fractions of the transient time. Furthermore, an ideal response with zero voltage deviation is not an objective of a VRM. Even in tight VRM applications, some degree of voltage deviation is still

tolerable by standards [101], and therefore a more conservative approach can be taken. As shown in Fig. 43(b), improved unloading transient recovery, provided some allowed deviation margins, can be achieved by a constant current sinking profile of $I_{aux} = \Delta I_{out}/2$. It can be seen that although v_{out} initially deviates from V_{out}, it is fully restored at T_{tr}. In the aforementioned cases, the current source sinks an identical charge within T_{tr}, meaning that initial under-current is ultimately balanced by over-current during the second half of the transient. Considering a maximum allowed overshoot of ΔV_{out} and the greatest possible load change ΔI_{max}, C_{out} is sized as follows:

$$C_{out} = \frac{\Delta I_{max}^2 L}{8 \Delta V_{out} V_{out}} \ . \tag{36}$$

When compared to TOC, the shorter transient times and the smaller initial current mismatch are in favor of a hybrid-VRM, resulting in C_{out} which is four times smaller.

The method shown in Fig. 43(b) reduces the complexity of the auxiliary circuit compared to the method in Fig. 43(a), however, it requires a fairly accurate estimation of the load current. To overcome this obstacle, a recovery pattern as shown in Fig. 43(c) is suggested. In this method, the auxiliary current is set to $I_{aux} = \Delta I_{max}/2$ (by design) while the instantaneous ΔI_{out} is unknown. As long as $I_{aux} \geq \Delta I_{out}/2$, the resultant total transient time remains T_{tr}, governed by the main inductor current slew-rate.

The design of an auxiliary source that compensates for $\Delta I_{max}/2$ provides two main advantages: 1) the transient controller can be realized based purely on sensing the output voltage and without additional current sensing, and 2) the conditions for the end-of-transient are within the main inductor current slew-rate for any given transient, without the need for extra time to reestablish the steady-state voltage.

4.1.3 Power processing efficiency

Present-day efficiency estimations for dc-dc converters are performed under a general assumption of steady-state operation as the dominant working condition, defined here as static conversion efficiency. Neglecting switching losses and assuming steady-state operation, the main contributor to the conduction losses is the average inductor current, since the rms current of the ripple component is negligibly small [64].

These estimations for calculating the efficiency are relatively accurate in most applications in which the load is static or mostly-static. However, for modern applications having continuously varying loading conditions, the static conversion efficiency estimation might fail to predict the actual losses, and as a consequence, the

required thermal design of the system. Fig. 44 shows a typical static efficiency curve compared to a dynamic loading one, for a similar average output power. As can be observed, the deviation of the static efficiency estimation from the actual one significantly increases with the load repetition rate. It should also be noted that the situation worsens for applications having relatively high conversion ratios, such as the VRM case.

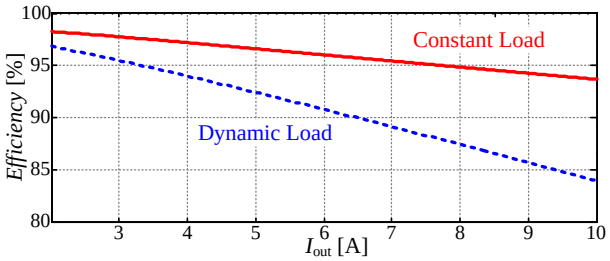


Fig. 44 Power processing efficiency of a buck converter connected to a constant load, versus a 50kHz dynamic load with the same average current, 50% load duty-ratio (see Fig. 45).

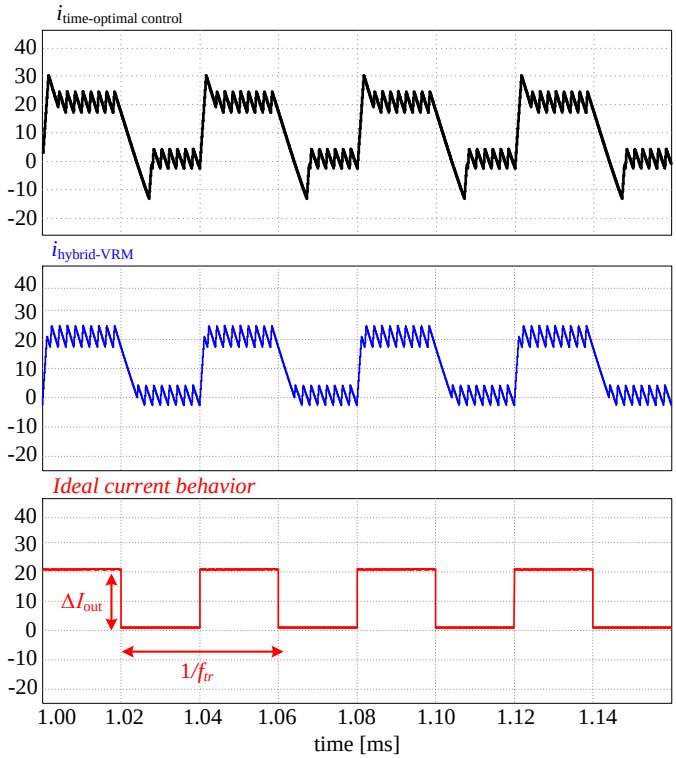


Fig. 45 Inductor current waveforms for TOC (top), hybrid-VRM (middle) and ideal inductor behavior (bottom).

To demonstrate the converter efficiency under varying load conditions, three cases are compared as shown in Fig. 45: an ideal inductor current behavior case, TOC [78] and a beyond time-optimal case [92] which is adopted in this study. To focus on the

difference between the controllers types, it is assumed that all methods are governed by an identical steady-state control law.

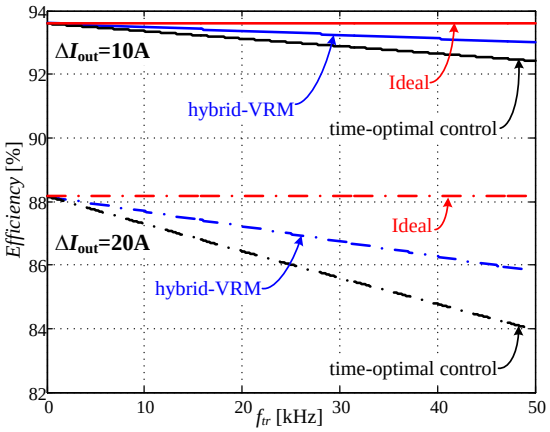


Fig. 46 VRM efficiency as a function of load transient rate for two load-step magnitudes. R_{buck}=10mΩ, R_n=2, switching losses are not considered.

Comparison of the resultant efficiency curves, and the ideal current waveform as a function of the load transients' rate, are shown in Fig. 46 (the expanded analysis is provided in [4]). As can be observed, elimination of the additional restoration current, i.e. peaks, reduces the overall rms current that in turn increases the power processing efficiency. In addition, another design concern is the inductor sizing. As derived in [80], TOC results in current overshoot of $\Delta I_{out}\sqrt{D}$ and undershoot of $\Delta I_{out}\sqrt{1-D}$ during loading and unloading transients of ΔI_{out}, respectively. Since these are eliminated by the hybrid-VRM approach, the sizing of the main inductor reduces as well.

4.1.4 GRSCC auxiliary circuit

Thanks to the soft-switching resonant nature of the GRSCC, it is applicable at high frequencies, and as a consequence, does not require a ferromagnetic core for its inductor. Furthermore, it has bi-directional current sourcing behavior and is able to react *immediately* to create a current step response having bandwidth of up to half its maximal switching frequency as detailed in Chapter 3.

A voltage bridge variation of the GRSCC has been implemented in this study and is shown as the auxiliary circuit of Fig. 41. It is structured relying on a voltage multiplying resonant switched capacitor converter topology, shifting the GRSCC's optimal efficiency point [15], as will later be described in Chapter 5. The main reason for the selection of this topology is to increase the energy density of the auxiliary storage capacitor C_{aux} by increasing its rated voltage and allowing larger ripple, but without adding voltage stress to the transistors. Another advantage of the bridge realization is

that the desired load-side current, i.e. $\Delta I_{max}/2$, can be obtained by designing the resonant network with higher characteristic impedance of the resonant tank. This implies that higher target efficiency of the GRSCC can be obtained for a given loop resistance.

The GRSCC is resonant in nature and can be completely halted at zero-current after each cycle. As a result, the nominal current can be resumed within one cycle. In the context of this study, this zero-order step capability enables the GRSCC to be used as the auxiliary current source unit. Moreover, there is no limitation to scalability, as the resonant tank values can be determined for any desired V_{out} and operating frequency with further option of interleaved operation. The bridge configuration also guarantees that the maximum stress on any given switch will be around V_{out}, which translates into small area requirements of the power switches.

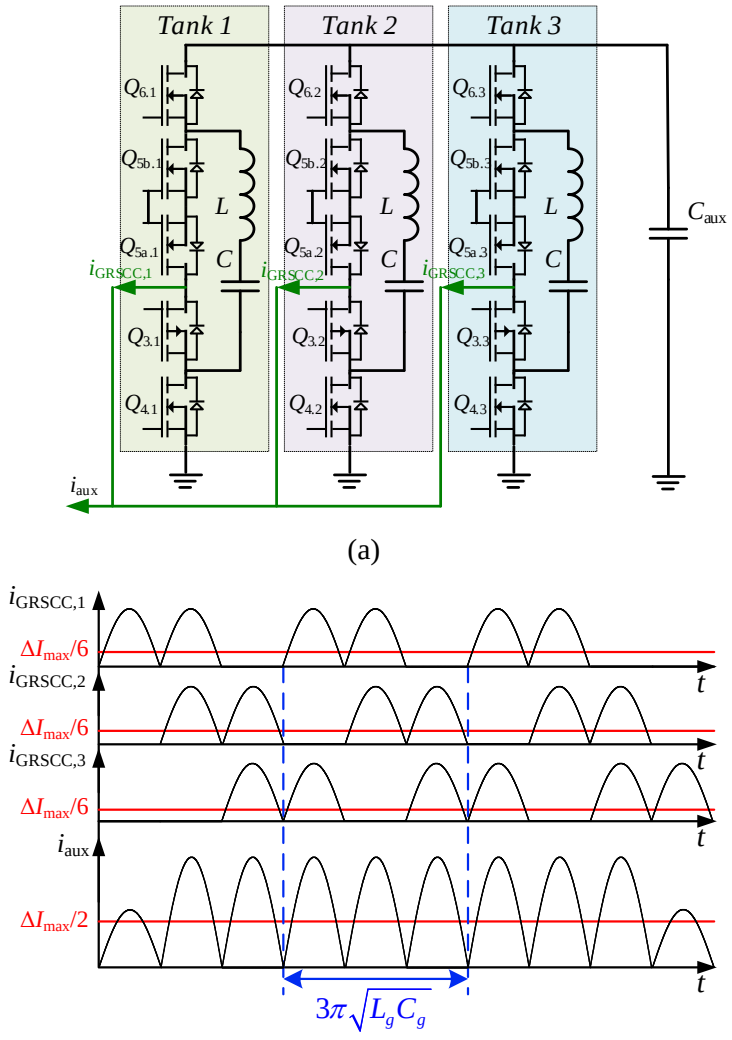


Fig. 47 (a) Three interleaved GRSCCs connected between the output and an auxiliary capacitor; (b) distribution of the auxiliary current between three interleaved GRSCCs operating at maximum frequency with half-resonance phase delay.

To further reduce the overall volume of system and to enhance the auxiliary circuit's efficiency, it is realized in this study using three small interleaved GRSCC modules, each designed to output $\Delta I_{max}/6$, operating with phase delay of half-resonance period, as demonstrated in Fig. 47. By doing so, the auxiliary circuit rms current is reduced by a factor of $(2/3)^{0.5}$ when compared to a single-converter equivalent, since there are more (and smaller) pulses that are evenly distributed over the transient phase, for the same average current. This configuration also increases the accuracy and resolution as a current source. Furthermore, lower current is required per module, allowing higher impedance of the resonant network.

The magnitude of the auxiliary current I_{aux} when using three GRSCC units for both loading and unloading transients follows the gyrator relationship with the auxiliary capacitor voltage V_{aux}, and is given by

$$I_{aux} = 6V_{aux} f_g C_g \ , \tag{37}$$

where f_g is the desired switching frequency of the GRSCCs, and C_g is the capacitance of the GRSCCs' resonant tank. The accuracy and resolution of the current source depends on f_g, and therefore f_g should be designed to be higher than the main converter's switching frequency f_s. For a selection of f_g, by setting $V_{aux} = 2V_{out}$ to obtain the optimal GRSCC efficiency and by using (37), the value of C_g can be extracted:

$$C_g = \frac{I_{aux}}{12V_{out} f_g} , \tag{38}$$

and the resonant characteristics of the GRSCCs yield the inductance L_g required to operate at the desired frequency:

$$L_g = \left[\left(3\pi f_g\right)^2 C_g \right]^{-1} . \tag{39}$$

4.1.5 Hybrid-VRM controller – principle of operation

The configuration of the hybrid-VRM controller is divided into two main units as shown in Fig. 41: a steady-state voltage-mode controller that is entirely implemented on FPGA [102], and a transient-mode controller.

Possible solutions for achieving high-performance transient response include measuring the output capacitor's di/dt value [95] or dv/dt value [72], [99]. However, these solutions usually require prior information or estimation regarding the converter's components, and high-bandwidth accurate sensors, which further increase the implementation complexity and cost of the system. In this study, in order to maintain

the hardware requirements at minimum, the transient-mode controller is assisted by two auxiliary comparators with two thresholds well below the maximum allowed voltage deviation, to facilitate fast transient detection and end-of-transient phase, as delineated in this section.

The description of the hybrid-VRM controller operation is assisted by Fig. 48 which illustrates, in-detail, the response for an unloading transient event:

- At $t < t_0$ the controller operates the buck converter with a voltage-mode steady-state compensator whereas the GRSCCs are idle.
- A load step at t_0 creates current mismatch between i_{buck} and i_{load}, resulting in a rise of v_{out}.
- At t_1, when v_{out} crosses $V_{ref,H}$, an unloading event is detected by *cmp*1 (Fig. 41) and a transient mode is initiated: Q_2 is turned on to ramp i_{buck} down with the highest slew-rate available. Simultaneously, the GRSCCs are activated to sink excess current and are set to $I_{aux} = \Delta I_{max}/2$.
- Since $\Delta I_{out} < \Delta I_{max}$, at instance t_2, v_{out} returns within the steady-state range below $V_{ref,H}$, the GRSCCs' operation is halted while Q_2 remains on, however, i_{buck} is still larger than i_{load}.
- This results in the output voltage rising over $V_{ref,H}$ at t_3, which re-triggers the GRSCCs.
- When v_{out} is within the steady-state range at t_4, i_{buck} approximately equals i_{load}. The end of the transient phase (t_5), in this case, is due to v_{out} crossing $V_{ref,L}$, detected by *cmp*2.

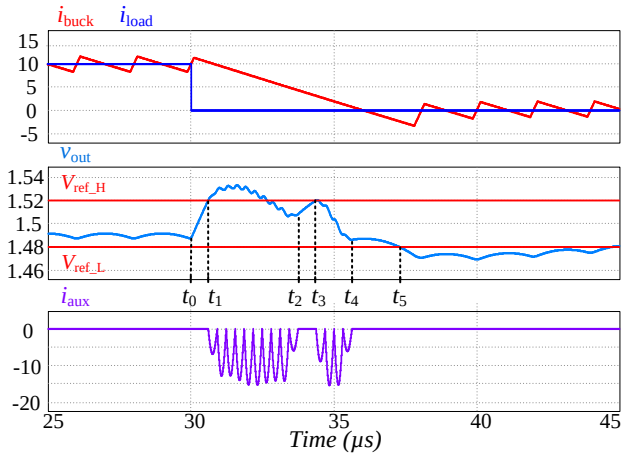


Fig. 48 Simulation results for the response of the hybrid-VRM to an unloading event. The auxiliary fires three sets of pulses at t_1 (as can be seen broken down in Fig. 47), followed by a single set at t_3

The information on the end-of-transient is derived, in this study, from the output voltage measurement by observing the comparator states. However, the information that is obtained from the output voltage indicates the current charge state of the output capacitor and not directly the current mismatch between i_{buck} and i_{load}. Given the example of Fig. 48 (t_2), it can be observed that the output voltage is momentarily restored to the steady-state value without reaching the point where i_{buck} equals i_{load}. The reason for this is that the charge balance has been achieved by the aid of the auxiliary circuit.

To overcome the problem of premature indication of the end-of-transient, without additional current sensors, a state-machine algorithm described by the flowchart of Fig. 49, has been developed. The controller monitors the output voltage by observing the comparator states. When v_{out} returns to within the steady-state thresholds, the GRSCCs are immediately halted, whereas the buck converter remains in transient mode. In case a current mismatch still exists, the output voltage is shifted back beyond the boundaries, and the auxiliary circuit is re-triggered.

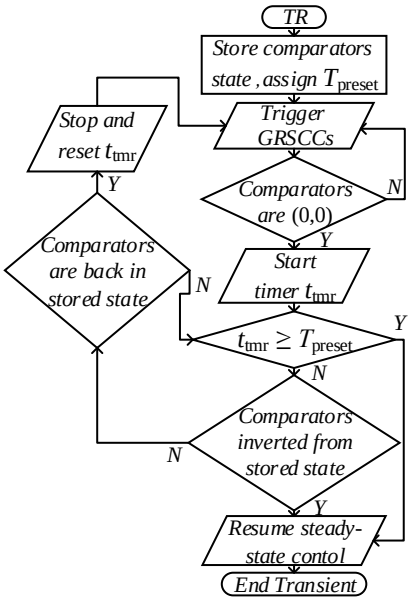


Fig. 49 Flowchart of the end-of-transient algorithm.

An end-of-transient indication (i.e., i_{buck} is in the vicinity of i_{load}) happens when the comparators' state has been inverted from the original transient-mode trigger. In the majority of cases, due to the use of v_{out} as a single indicator for the comparators, a small current mismatch may exist, as can be observed at t_5 in Fig. 48. To provide an additional layer of protection and to minimize any current mismatch, without additional current sensors, a time period limit has been added, the time starting when v_{out} has returned

within the comparators thresholds without change in the comparators' states. In case the preset time period has elapsed, an end-of-transient is detected and the steady-state voltage mode control is resumed.

More in-detail implementation details such as threshold settings, charge-reset of the auxiliary capacitor, and ensuring smooth resume to steady-state can be found in the original paper [4]. A different control method to implement a stand-alone "plug-and-play" auxiliary circuit has also been examined and is provided in [14].

4.1.6 Experimental verification

In order to validate the operation of the hybrid-VRM, a 20W 12V-to-1.5V prototype was built and tested, with a measured peak efficiency of 93%. The auxiliary circuit was realized by three interleaved GRSCCs, sharing the same input, output and control, as described in Section 4.1.4. A photograph of the experimental prototype is shown in Fig. 50. Table V lists the component values and parameters of the experimental prototype. A standalone efficiency measurement of the GRSCCs, i.e., without the main converter active, for various V_{aux} values is given in Fig. 51. The digital controller comprises steady-state voltage-mode control and transient-mode control, realized on an Altera Cyclone IV FPGA. Steady-state control is assisted by high-performance integrated ADC and DPWM on-FPGA realizations as described in [102]. The load transient signals were generated by an external signal generator, independently, without synchronization to the controller.

Fig. 50 Photograph of the hybrid-VRM power stage, including the buck converter and three interleaved GRSCCs.

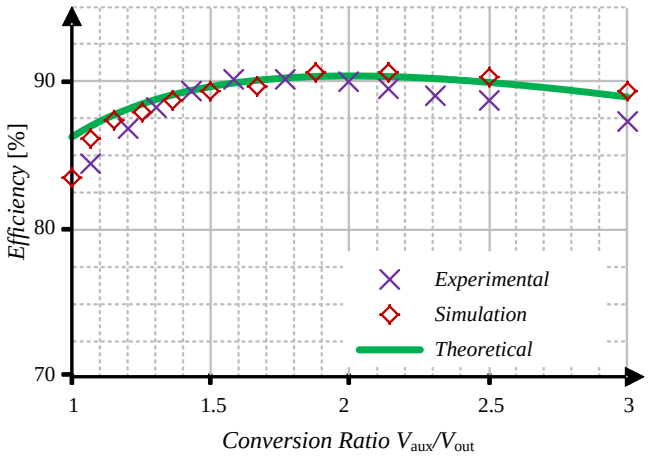


Fig. 51 Efficiency measurement of the GRSCCs.

TABLE V EXPERIMENTAL PROTOTYPE VALUES

Component	*Value*
Input voltage V_{in}	12 V
Output voltage V_{out}	1.5 V
Main inductor L	1.3 uH
Output capacitor C_{out}	150 uF
Buck converter switching freq. f_s	500 kHz
GRSCC maximal switching freq. f_g	~1.7 MHz
Auxiliary capacitor C_{aux}	20 uF
GRSCCs resonant tank capacitor C_q	0.3 uF
GRSCCs resonant tank inductor L_g	~10 nH (stray inductance)
Number of GRSCC stages	3

Fig. 52 presents the hybrid-VRM response to loading and unloading transient events of 10A in comparison to the buck converter operating under TOC, using the same

transient detection circuit. Fig. 52(a) and Fig. 52(b) show the response to a loading transient event of 10A (1.5A to 11.5A) for the hybrid-VRM and for TOC, respectively. The measured output voltage undershoot and total transient time for the hybrid-VRM are 60mV and 3µs, and for the TOC case they are 120mV and 9µs. An unloading transient of 10A (11.5A to 1.5A) is depicted in Fig. 52(c) and Fig. 52(d). In this case, the hybrid-VRM's response results in output voltage overshoot of 100mV with settling time of 12µs, and using TOC the voltage overshoot sums to be 390mV with 21µs settling time.

Fig. 53 presents the comparison between the hybrid-VRM and TOC for loading and unloading transients, smaller than the rated ΔI_{max} (4.5A to 11.5A). In the hybrid-VRM case of an unloading transient response (Fig. 53(c)), the GRSCCs are halted and then re-triggered in a similar manner to the analysis and simulation [4]. This occurs as the GRSCCs are set to sink current of more than half the load-step magnitude.

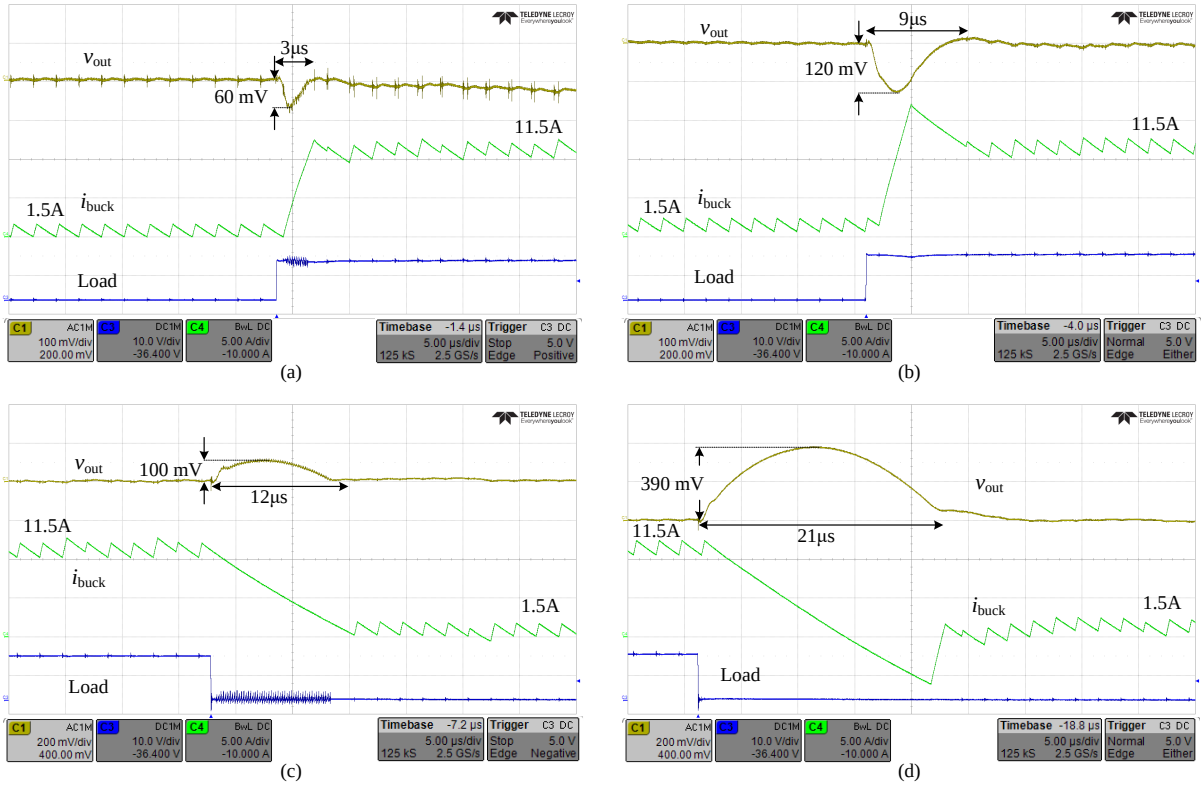


Fig. 52 Experimental results showing a 10A load transient response of the hybrid-VRM [(a), (c)] versus TOC [(b),(d)]. Signals from top to bottom: v_{out} [(a), (b) 100mV/div. (c), (d) 200mV/div, ac coupled], i_{buck} (5A/div), and load-step signal. Time scale is 5µs/div. (a), (b) 1.5A-11.5A loading event. (c), (d) 11.5-1.5A unloading event.

Fig. 54 shows the hybrid-VRM's response to a repetitive load transients of 7A (4.5A to 11.5A) at a frequency of 1 KHz with 50% load duty ratio. As can be observed, the

output voltage overshoots and undershoots remain the same as in Fig. 52, validating the capability of the system to handle consecutive transients.

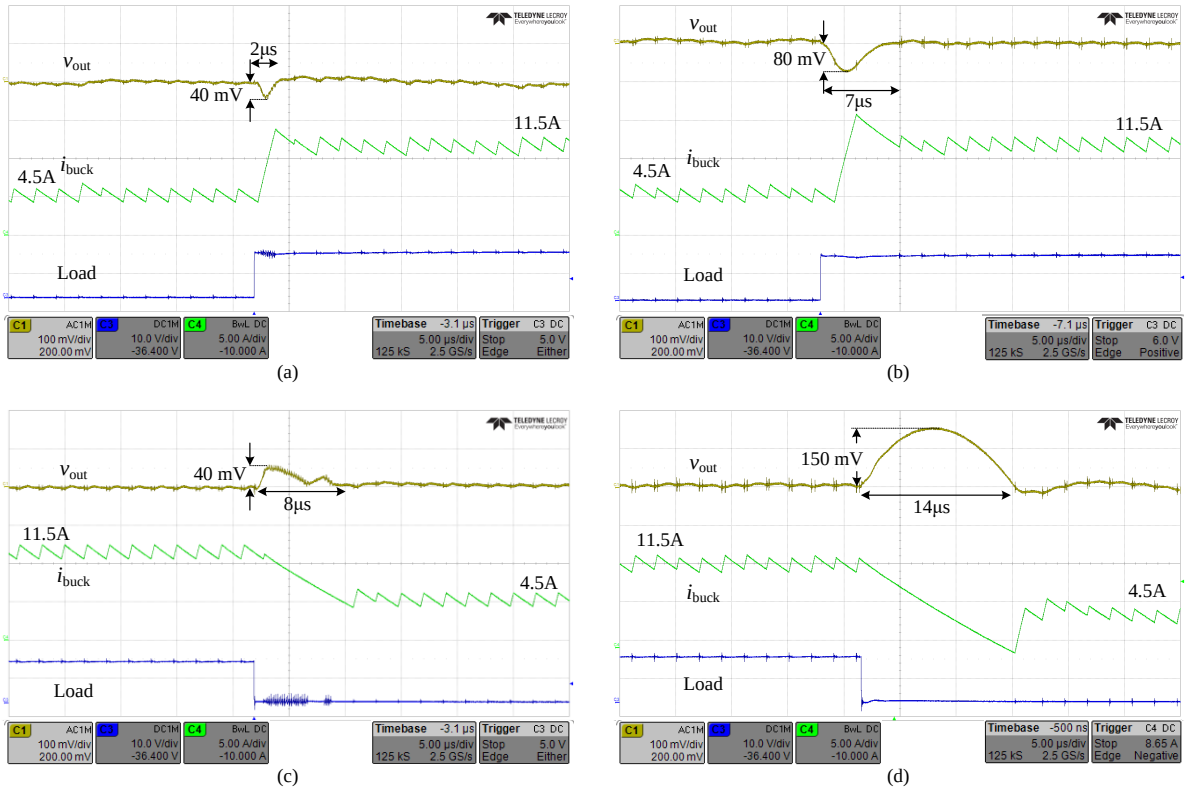


Fig. 53 Experimental results showing a 7A load transient response of the hybrid-VRM [(a),(c)] versus TOC [(b),(d)]. Signals from top to bottom: v_{out} (100mV/div, ac coupled), i_{buck} (5A/div), and load-step signal. Time scale is 5µs/div. (a),(b) 4.5A-11.5A loading event. (c),(d) 11.5-4.5A unloading event.

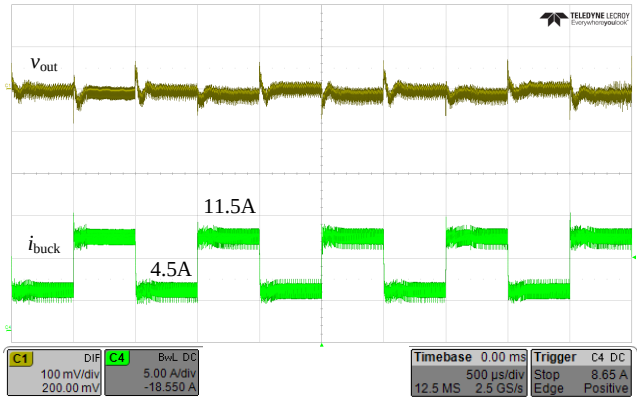


Fig. 54 Screenshot demonstrating the hybrid-VRM's response to a repetitive 1 KHz loading-unloading transients from 4.5A to 11.5A. Output capacitor voltage 100mV/div, inductor current 5A/div, time scale 500µs/div.

4.2 Envelope Tracking Power Supply for Volume-Sensitive Low-Power Applications Based on a GRSCC

4.2.1 Introduction

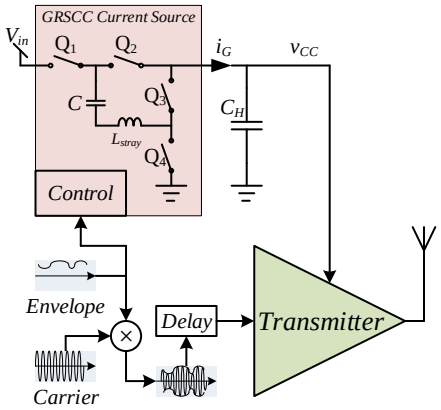


Fig. 55 GRSCC-based envelope tracker.

The issue of power management has become one of the primary factors important for achieving small and light equipment, and in particular prolonging the device operability (battery life) and maintaining satisfactory performance. The two main power consumers of a portable system are the processor and the communication (wireless) transmitter. The main objective of the processor's supply is to maintain a well-regulated constant output voltage under wide range of load changes. On the other hand, the main challenge in the design of the transmitter supply is for its voltage to be modulated at base-band signal rate (10MHz range), requiring extremely high control bandwidth [103]-[106]. Therefore, design efforts are not as much in efficiency but in size of passive components [103].

Envelope Elimination and Restoration (EER) or Envelope Tracking (ET) methods [104]-[118] realize envelope modulation of the power supply by either linear regulators, switch-mode regulators, or both. To achieve high efficiency of the switched-mode converter, switched-inductor converter topologies are prominent. Ideally, the efficiency characteristics can be maintained high for wide range of conversion ratios. However, to minimize the necessity of additional linear regulation to achieve the required bandwidth, ultra-fast switching converters are used [116], [119], [120] where their switching losses may affect the efficiency. In addition, the total size of these solutions is not necessarily reduced, since inductors are now required, which may also prohibit on-chip integration.

Switched-capacitor (SC) technology has a unique benefit of being a ‘perfect’ candidate for miniaturization and on-chip integration, as detailed in previous chapters as well as in [61]. In the context of ET, SC is a poor solution since it can produce high efficiency in singular conversion ratios [121], [122]. The presented GRSCC has a wider efficiency-curve and current sourcing capability and has been shown to respond without delay to line and load variations. These attributes make the GRSCC an attractive candidate for ET applications.

The objective of this section is to introduce a new rapid adaptive voltage scaling envelope tracking system that is realized by a GRSCC for volume-sensitive low-power applications. The solution, as detailed in Fig. 55, provides a high-efficiency, volume-saving alternative to the conventional switched-inductor approach. Combined with a newly developed non-linear controller, the ET power supply minimizes the tracking mismatch and significantly reduces losses related to the linear regulator shape adjuster.

4.2.2 Envelope tracking by current sourcing

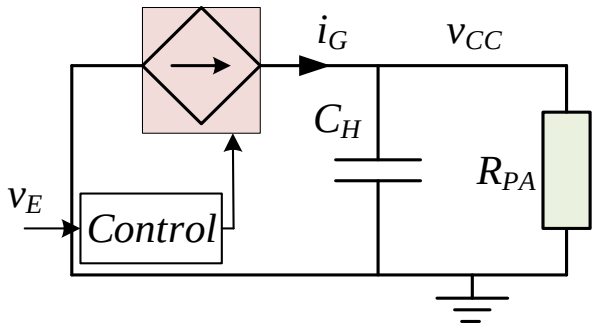


Fig. 56 An average model to illustrate the tracking concept. The GRSCC is modelled by a controlled current source with saturation.

A generic behavior of the circuit in Fig. 55 can be conceptually described by a controlled current-source that produces a variable current i_G and mimics the operation of the GRSCC, capacitance C_H and a load resistance R_{PA}, as illustrated in Fig. 56. As described in [104], [108], a constant resistor is used to emulate the effective loading by a transmitter. For a v_{CC} signal to perfectly match a desired envelope signal v_E, the current source is to output a signal, i_G with the linear dependency of the form:

$$i_G = \frac{v_E}{R_{PA}} + C_H \frac{dv_E}{dt} \quad . \tag{40}$$

A physical converter is limited by current boundaries of I_{min} and I_{max}. As a result, in some cases v_{CC} would be lower than the desired v_E, a prohibited scenario in ET applications. Derived from (40) and from the circuit in Fig. 56, the response of v_{CC} has

a first-order nature due to the current limitation of $I_{\max}$. In most ET applications, the information for the required voltage is available by pseudo-non-casual data (e.g. broadcast signal). Therefore, skewing the current injection sequence can be applied by a factor $\Delta T_{\max}$ which can be expressed as:

$$\Delta T_{\max} = -R_{\mathrm{PA}} C_H \ln\left(1 - \frac{V_{\mathrm{peak}}}{I_{\max} R_{\mathrm{PA}}}\right), \tag{41}$$

where V_{peak} is the maximum value for v_{CC}. A profile vector with length $\Delta T_{\max}$ of the desired target envelope is used as the reference signal to the tracking system.

To account for the current output limitations and to satisfy $v_{\mathrm{CC}} > v_E$ at all times, the reference vector is reconstructed based on the voltage ramp up or down capabilities of the current source. The resulting v_E^* deviates from v_E only when the desired envelope's slews are higher than the slews that can be obtained by the current source applied on C_{H}.

The procedure for generating v_E^* is carried out in three steps and is conceptually illustrated in Fig. 57 which describes an arbitrary portion of a given envelope signal v_E. A preliminary step based on the system parameters (i.e., the current ratings, output capacitance and the load), calculates the ramping up/down capabilities in the system as follows:

$$\begin{cases} v_{\text{ramp-up}} = I_{\max} R_{\mathrm{PA}} \left(1 - e^{-\frac{t}{R_{\mathrm{PA}} C_H}}\right) \\ v_{\text{ramp-down}} = -I_{\max} R_{\mathrm{PA}} \left(1 - 2e^{-\frac{t}{R_{\mathrm{PA}} C_H}}\right) \end{cases}. \tag{42}$$

In the second step (Fig. 57a), for a given vector length of $\Delta T_{\max}$, the possible ramp-up trajectories are compared with the slews of v_E and the reference vector is reconstructed by tangential trajectories to v_E (i.e., with equal slope) to assure that $v_{\mathrm{CC}} = v_E^* > v_E$ for any t. In the final step (Fig. 57b), the procedure is repeated with the ramp-down trajectories. The resulting reference vector v_E^* is depicted in Fig. 57c. For evaluation purposes, the current-limited injection sequence can be derived using (40) with v_E^*. Fig. 58 shows a wider view of the tracking operation, demonstrating generation of a continuous reference vector having severe current output limitations, as well as comparison with constant supply setting. It can be observed that in spite of the limited ramping capabilities, a significant portion of the losses is reduced thanks to the tracking method.

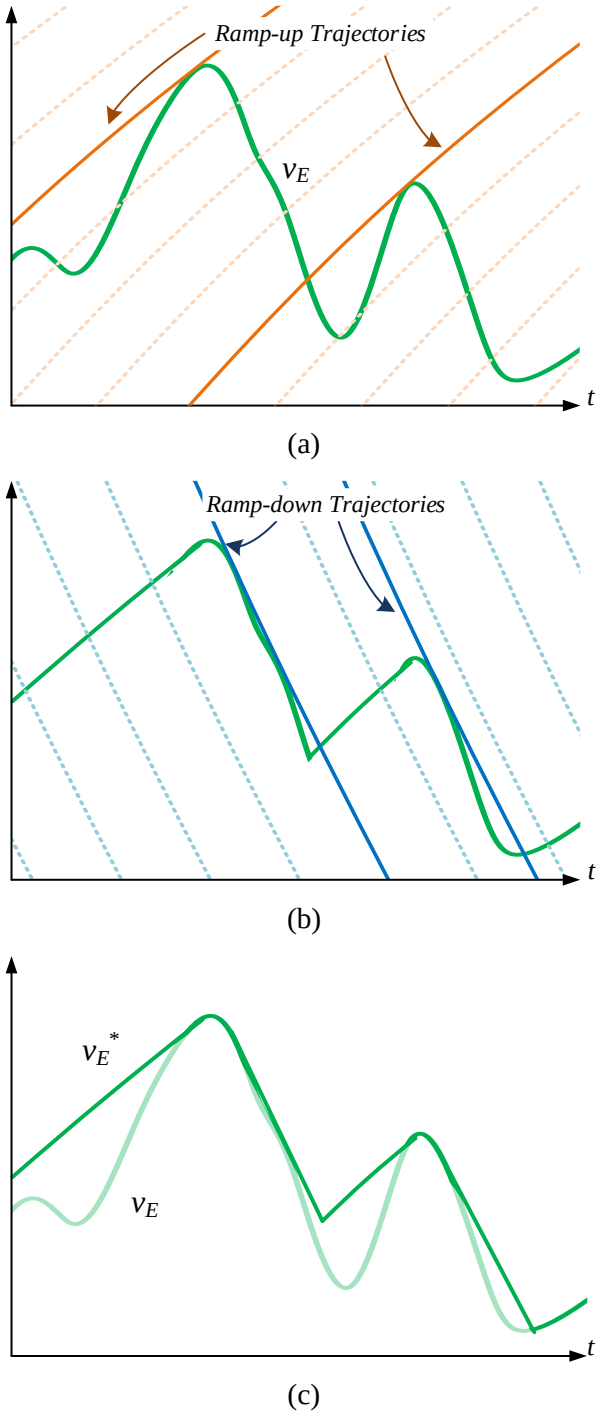


Fig. 57 Step-by-step tracking refernce vector generation procedure. (a) accommodating ramp-up limitations; (b) ramping down; (c) the resultant reference signal compared to the desired one.

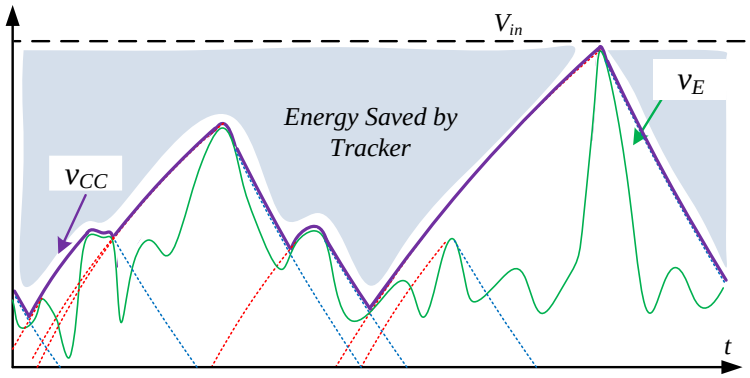


Fig. 58 Illustration describing the tracking operation and saved energy for an information segment in v_E under severe current limitation conditions.

4.2.3 Realization of a current source by a GRSCC

The GRSCC topology presented in the previous chapters of the thesis features near-ideal bi-directional pulsed current source behavior. The pulsed behavior can be expressed by average pulse current amplitude, I_{pulse}, of the converter (Fig. 59), given by:

$$I_{\text{pulse}} = \frac{2CV_{\text{in}}}{T_{\text{pulse}}} \quad , \quad T_{\text{pulse}} = \frac{1}{f_n} = 3\pi\sqrt{LC} \quad , \tag{43}$$

where C is the flying capacitor value, V_{in} is the supply voltage, and T_{pulse} is the pulse duration of the converter at its natural frequency set by the resonant network of L and C. Bi-directional operation is realized by reversing the three-state switching scheme, and is expressed in context of (43) by the expression having positive values for sourcing current and negative values for sinking current operation. As described in detail in Chapter 3, immediate response can be achieved with the GRSCC by pulse-density modulation (PDM).

Voltage regulation of a GRSCC using ripple-based PDM applies valley comparison to the output voltage, i.e., a comparator that triggers the pulsed source each time a reference value is met. Ideally, this method can be applied to envelope tracking by comparing v_{CC} to the synthesized v_E^*. Practically, in envelope tracking applications, the high-rate envelope variation and, in this study, the need to track a synthesized v_E^*, prohibits using a physical comparator due to the intrinsic delay between the valley detection to the pulse output. To remedy this, pre-calculation and comparison is conducted in advance as follows:

Assuming that the resultant output voltage deviation for a given pulse magnitude of I_{pulse} is relatively small, v_{CC} can be approximated by first order to (Fig. 60):

$$v_{CC}(t)=\begin{cases}\left(I_{\text{pulse}}-\dfrac{v_{CC}(t_0)}{R_{PA}}\right)\dfrac{(t-t_0)}{C_H} & , \quad t_0<t<t_1 \\ -\dfrac{v_{CC}(t_1)}{R_{PA}}\dfrac{(t-t_1)}{C_H} & , \quad t_1<t<t_2\end{cases} , \tag{44}$$

where t_0 is the time of an initiated pulse, $t_1 = t_0 + T_{\text{pulse}}$ is the pulse end, and t_2 is the trigger point for the next pulse, where $v_{CC} = v_E^*$ (see Fig. 60). v_{CC} is actively reduced when needed by sinking excess charge back to the source using indication from an upper threshold. This threshold is set to $v_{CC} = v_E^* + \Delta V_{CC}$, where ΔV_{CC} is the impact of a single pulse, expressed as:

$$\Delta V_{CC} = \frac{T_{\text{pulse}}\, I_{\text{pulse}}}{C_H} \ . \tag{45}$$

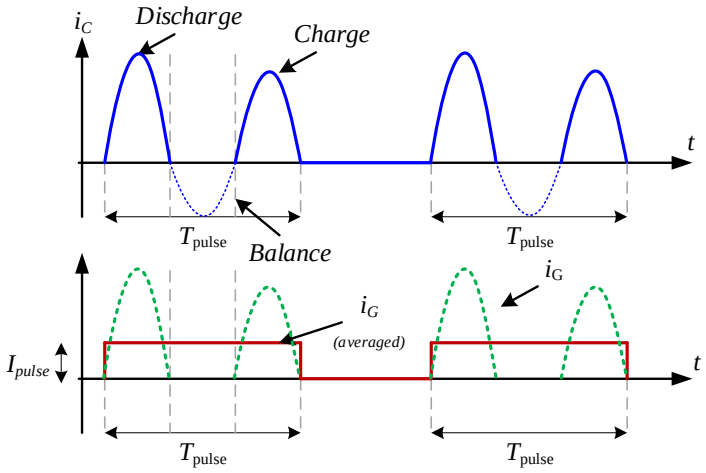


Fig. 59 Current wavforms on the GRSCC depicted in Fig. 55 for two pulses. The top graph displays the current on the resonant tank, i_c, bottom graph displays the resonant pulse as seen by the output, namely i_G and its' average representation. switch activity is as follows: discharge - Q_2,Q_4; balance - Q_2,Q_3; charge - Q_1,Q_3.

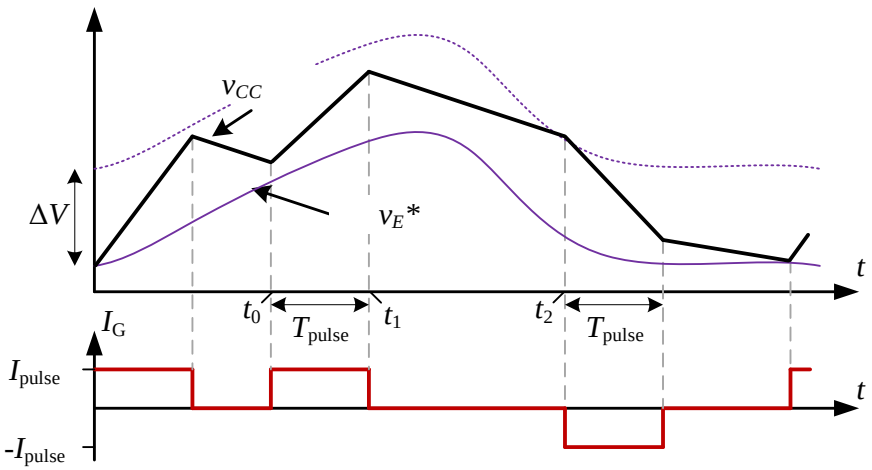


Fig. 60 The methodology for using a constant-pulse source for tracking v_E*

It should be noted that one potential drawback of this method is the lack of feedback, and as a result, sensitivity to parameter variations. This is resolved by either on-line parameter estimation, or worst-case based design with a minor effect on the tracking capability.

4.2.4 Simulation case study

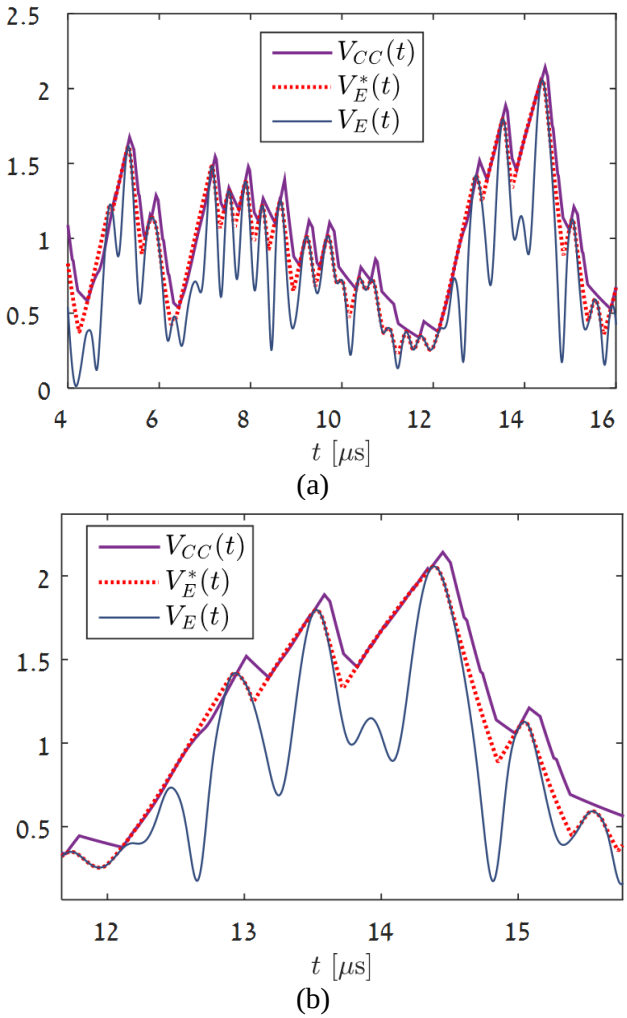


Fig. 61 Simulation results of the converter tracking a reconstructed envelope above v_E. (a) wide view, (b) zoom.

The target parameters for the envelope tracker are listed in Table VI. Given the output power and peak to average power ratio (PAPR), the peak current is $I_{\text{peak}} \approx 0.45$ A at $V_{\text{CC}} \approx 2.24$ V. Based on (43), the converter is designed to output current of $I_{\text{pulse}} = 1$ A to satisfy ramping capabilities of 2 V/µs. The maximum effective frequency is set at $f_{\text{max}} = 1/T_{\text{pulse}} = 10$ MHz. The resulting resonant network components' values are $C_f \approx 15$ nF, $L \approx 8$ nH. Choosing $C_H = 0.4$ µF results in $\Delta V_{\text{CC}} \approx 0.25$ V.

TABLE VI EXAMPLE DESIGN SPECIFICATIONS

Component	*Value*
Input voltage V_{in}	3.3 V
Minimum input voltage $V_{in,min}$	3 V
Average PA output power P_{out}	250 mW
Reflected load impedance R_{PA}	4.7 Ω
Peak average power ratio PAPR	4
Estimated envelope frequency	2.5 MHz

The tracking results have been produced using MATLAB and are shown in Fig. 61, which also shows the reference vector generated as described earlier. The design example results in 250% tracking efficiency improvement compared to a constant supply voltage ($\eta_{ET} = V_E / V_{CC} = 70\%$ versus 24%). It should be noted that the efficiency estimation included conservative design of the GRSCC with series loop resistances of $R_S = 50\text{m}\Omega$, and power-stage efficiency of $\eta = 85\%$.

4.2.5 Experimental verification

To verify the operation of the envelope tracker and to demonstrate the control scheme solution, a 250mW prototype was built and tested, and it is depicted in Fig. 62. Table VII lists the power-stage specifications and components' values. The converter was realized by a GRSCC with the resonant tank constructed using capacitors alone. To complete the resonant tank, air-core inductance of 10nH was added to reach the total of 20nH. The envelope reference signal was synthesized using MATLAB, based on generic OFDM symbols, and then translated to pulse timing and direction vectors. GRSCC control was implemented on an Altera Cyclone IV FPGA to create timed source/sink gate-signals for the transistor drivers. Soft-switching was achieved with pre-calibration of switching timings by hand.

Fig. 63 demonstrates the converter's output, recorded from oscilloscope (Teledyne LeCroy HD4016) and compared to the original envelope and the predicted trace through MATLAB. The tracking results are in very good agreement with the theoretical predictions, verifying the capabilities of the converter as well as the design procedure. The tracking efficiency is measured to be $\eta_{ET} \approx 65\%$ versus 20% in the linear mode approach, with $1/T_{pulse}$ just marginally above the envelope frequency, an improvement of more than 200%. Furthermore, the presented solution performs similarly to a switched-inductor approach. It should be noted that in some cases the current pulse is triggered before v_{CC} reaches v_E^*, and is due to a slight deviation of the resonant parameters and efficiency estimation in relation to the virtual boundaries discussed above.

TABLE VII EXPERIMENTAL SPECIFICATIONS

Component	*Value*
Input voltage V_{in}	3 V
Average PA output power P_{out}	250 mW
Load impedance R_{PA}	4.7 Ω
Tank capacitance C	60 nF
Estimated tank inductance L	20 nH
Output capacitance C_H	0.6 nF
Estimated loop resistance R_S	0.05 Ω
Maximum switching frequency f_{max}	3 MHz
Estimated envelope frequency	1 MHz
MOSFET type	SiA436DJ

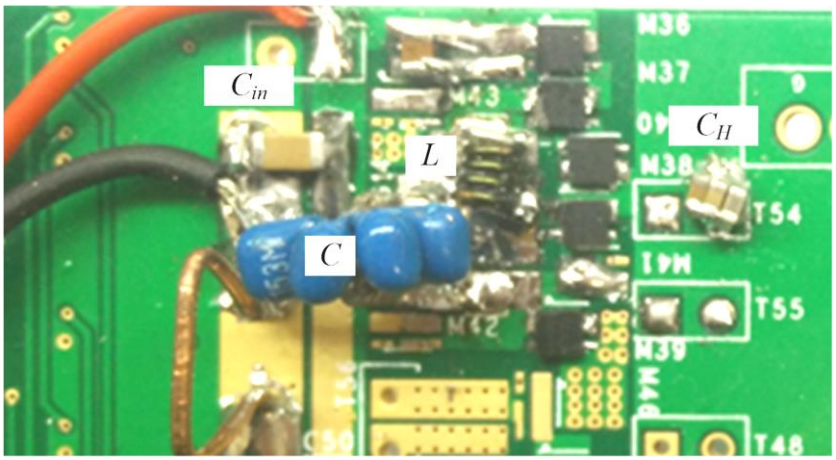


Fig. 62 250 mW 3MHz Experimental prototype. Zoomed in is the resonant tank.

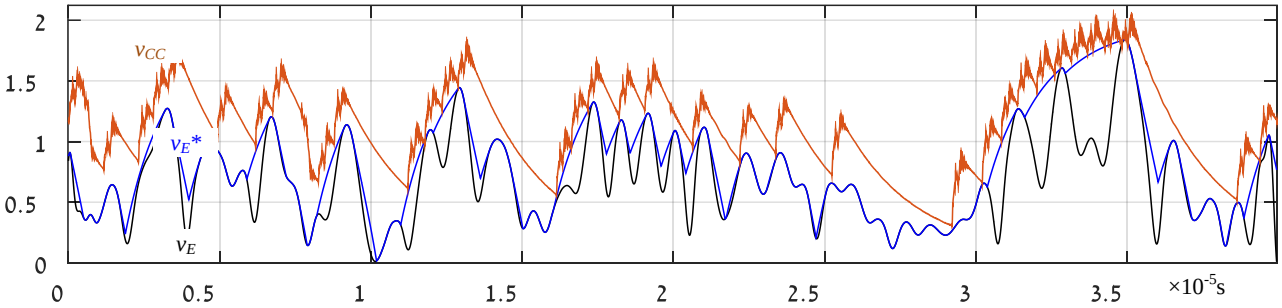


Fig. 63 Experimental results comparing a recorded signal to the original reconstructed envelope and v_E.

CHAPTER 5:
Advanced Analysis of Resonant Power Conversion

5.1 Introduction

In the previous chapters the GRSCC, was presented alongside some of its possible applications. The GRSCC was provided with one switch configuration and a control scheme as a 'default' enabler for gyrator operation. In this chapter, the theory of the gyrator operation of an SCC is expanded to a general case, with extended theoretical analysis of the operation and efficiency of the converter.

A new gyrator switched-resonant converter (GSwRC) is introduced. The GSwRC features enhanced current sourcing or sinking capabilities, high efficiency over a wide range of conversion ratios, and a unique methodology for shaping the efficiency characteristics of the converter by the switching scheme is presented. The primary advantage of this new converter is that a wide and continuous conversion ratio with high efficiency is achieved using a *single energy transfer cell* (i.e., one flying capacitor). This ultimately allows volume and complexity reduction when compared to other multi-target voltage converters that employ switched-capacitor [21], [23], [24] or switched-resonant approaches [41], [123], [124]. A variety of ten operation modes (switching schemes of the converter) applied to the presented family are demonstrated as a showcase of power-sourcing and efficiency capabilities of the new converter.

Then, a unified theory is developed for a generic switched-resonator converter including any number of ports. This is accomplished by expressing the average currents of the generic structure of the converter as a recursive equation which leads to a unified and topology-independent matrix that links the ports' currents to the voltages. Extensive and generalized behavioral loss-analysis models are developed for switched-resonator converters. These models address the impact of conduction losses on the converter's performance and efficiency, which were assumed to be negligible in the previously described analysis.

5.2 A family of switched-resonant converters with wide conversion ratio and controlled sourcing features for volume-sensitive applications

5.2.1 Generalized conversion characteristics of a switched-resonator network as a two-port network

The converter in its simplistic form, shown in Fig. 64, is a modification of a soft-switched resonant SCC with a switch assembly inspired by multi-target voltage converters such as the binary/Fibonacci SCC [21], [41] illustrated in Fig. 6, or the general transposed series-parallel (GTSP) SCC [23], [24]. As opposed to other configurations that employ multiple flying tanks, in this study, a single energy-transfer cell is used. The switches configuration allows the resonator to connect the input or the output ports directly or with reverse polarity, as well as a series-parallel connection to either port. Thus, multiple switching possibilities to achieve charge balance of the tank can be realized. As demonstrated previously throughout the thesis, this enables disengaging the rigid relationship between the efficiency and the voltage gain.

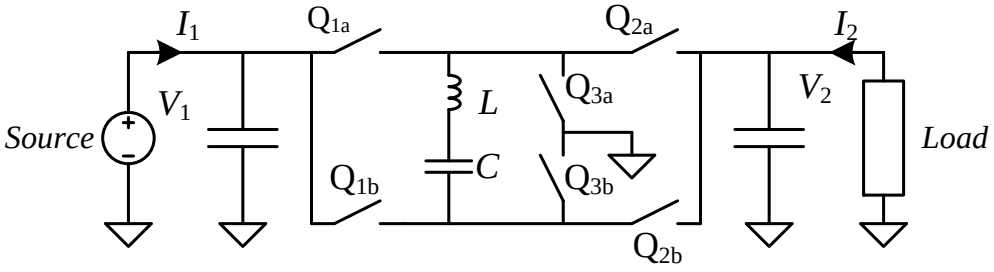


Fig. 64 The presented multi-mode switched-resonant converter.

A switch-mode converter can be described as a two-port network, as illustrated in Fig. 65, using average and dynamic behavioral modeling to define a relationship between the input and output port voltages V_1, V_2, and currents I_1, I_2. V_1, V_2 are considered known and independent of each other, while the dependency of the other parameters can be defined by the admittance, that is:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} . \tag{46}$$

The matrix parameters Y_{11} and Y_{22} represent the ports' self-admittance, i.e. dependence of each port's current on its own voltage, while Y_{12} and Y_{21} represent the cross-admittances. A matrix where $Y_{12} = G$, $Y_{21} = -G$ and $Y_{11} = Y_{22} = 0$, describes an ideal *gyrator* element [36].

A. Two-Port Admittance Modelling of a Switched-Resonator Network

Consider a generalized switched-resonant converter, illustrated in Fig. 66, having average port voltages V_1, V_2, and a switch assembly that applies N combinations of V_1 and V_2, i.e. *states*, on the resonator (i.e., series connection of L and C). A soft-switching mechanism is employed and assures transition between states at zero current after half-resonance period. Since the resonant behavior in each state is of a 2nd order, the converter can be analyzed in a discrete form by viewing the potential applied on the tank (resonator) during the state's interval and determining the values at the end of each state.

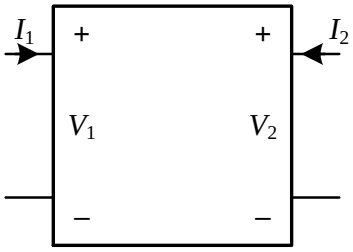


Fig. 65 Two-port

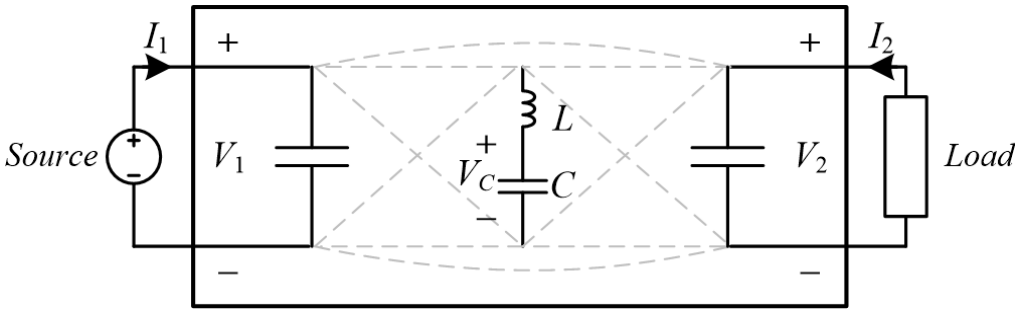


Fig. 66 A view of a switched-resonator network with dashed-lines representing possible connection alternatives to the input and output ports.

The tank's capacitor voltage at the end of state n, namely $V_{C,n}$, can be derived from its initial condition, $V_{C,n\text{-}1}$, and the voltage that is applied on the tank at the specific state, E_n. Assuming sufficiently high quality-factor, i.e. negligibly small losses, $V_{C,n}$ can be expressed at the half-resonance switching-point as

$$V_{C,n} \approx 2E_n - V_{C,n-1} \quad , \quad E_n = f\left(V_1, V_2\right) \ . \tag{47}$$

Populating the values for E_n into (47) for each of the states gives N equations with N unknowns $V_{C,1}$ to $V_{C,N}$. Assuming that all equations are independent, a unique solution exists for all the unknowns as a function of V_1 and V_2, i.e. the steady-state values for $V_{C,1}$ to $V_{C,N}$ are fixed and known. It should be noted that some switching combinations may result in dependent equations which still converge to a solution when symmetrical voltages are applied on the resonator, that is:

$$\sum_{n=1}^{N} E_n \left(-1\right)^{n-1} = 0 \tag{48}$$

The average current value in each state, $I_{C,n}$, is derived from the total charge difference from the previous state, that is:

$$I_{C,n} \approx \frac{2C}{T_{state}}\left(V_{C,n} - V_{C,n-1}\right) \quad , \quad T_{state} = \frac{1}{3 f_n} = \pi\sqrt{LC} \tag{49}$$

Where f_n is the natural frequency of the converter, L and C are the inductance and capacitance of the resonator, respectively. Once $I_{C,n}$ is obtained for the complete sequence, I_2 can be derived by averaging all of the state currents throughout the cycle in which the resonator connects to the output node. I_1 is derived in a similar manner. This yields:

$$\begin{aligned} I_1 &= f\, T_{state} \sum_{n=1}^{N} x_n I_{C,n} \quad , \quad x_n \in \{-1,0,1\} \\ I_2 &= f\, T_{state} \sum_{n=1}^{N} y_n I_{C,n} \quad , \quad y_n \in \{-1,0,1\} \end{aligned} \quad , \tag{50}$$

where F is limited by the repetition rate of the cycle, i.e. the frequency for the sum of switching states that compose one cycle $f \le f_n = (N\, T_{state})^{-1}$, and x_n, y_n are constants which indicate whether the tank is connected to the input and/or output at state n as well as the connection polarity. Current regulation can be obtained by modifying f using pulse-density modulation techniques described in Chapter 3, affecting the result of (50).

For example, at $n = 1$ a GRSCC connects to V_1, on $n = 2$ to V_2 and on $n = N = 3$ it connects shorts to itself; there is no polarity reversal so a connection will be treated as '1'. If the GRSCC operates at F_{max}

$$\begin{aligned} I_1 &= \frac{1}{3}\left(1 \times I_{C,1} + 0 \times I_{C,2} + 0 \times I_{C,3}\right) \\ I_2 &= \frac{1}{3}\left(0 \times I_{C,1} + 1 \times I_{C,2} + 0 \times I_{C,3}\right) \end{aligned} \tag{51}$$

Since (47)-(50) can be rewritten as a function of V_1 , V_2, after some manipulation (50) can be expressed as a function of the admittances as:

$$I_1 = Y_{11} V_1 + Y_{12} V_2 \quad , \quad I_2 = Y_{21} V_1 + Y_{22} V_2 \ . \tag{52}$$

B. Efficiency Modelling

The efficiency of the converter, dominated by conduction losses, can be obtained by evaluating the losses P_{loss} and the output power P_{load}, which form:

$$\eta = \left[1 + P_{loss} / P_{load}\right]^{-1} \ . \tag{53}$$

P_{loss} is obtained by summing the individual losses created in each state. Assuming no other significant losses (thanks to the ZCS), the losses are due to the rms currents

$I_{C,n,rms}$, through the conduction path resistance R. The total power dissipation can then be obtained using (49), with the average-to-rms ratio for a sine wave as:

$$P_{loss} = R\sum_{n=1}^{N} {I_{C,n,rms}}^2 \approx fT_{state}R\frac{\pi^2}{8}\sum_{n=1}^{N} {I_{C,n}}^2 \ , \tag{54}$$

where R is assumed here identical for all states, without loss of generality. The expression of (54) can be rewritten in a general form, represented by basic parameters from (47) and (49) as:

$$P_{loss} = \frac{fRC^2}{T_{state}}\left(\alpha {V_1}^2 + \beta {V_2}^2 - \gamma V_1 V_2\right) \ , \tag{55}$$

where the constants α, β, γ are weighting-factors of V_1, V_2 based on the mode of operation.

The output power can also be directly expressed by V_1 and V_2 and the parameters of the converter's admittance (52). This yields:

$$P_{load} = -P_2 = -\left(Y_{21}V_2V_1 + Y_{22}{V_2}^2\right). \tag{56}$$

In cases where the loss contribution of Y_{22} is relatively small, (55) and (87) can be substituted into (53) to form an efficiency expression that depends directly on the conversion ratio, A:

$$\eta = \left[1 + B\left(\alpha A^{-1} + \beta A - \gamma\right)\right]^{-1}, \ A = \frac{V_2}{V_1} \ , \tag{57}$$

where B combines the independent parameters from (55) and (87). It can be seen from (89) that, as described in Chapter 2, the efficiency variation of the switched-resonator network described herein depends on the conversion ratio alone.

Taking the derivative of (89) and equating to zero yields the conversion ratio in which the peak efficiency can be achieved, that is:

$$A_{optimal} = A\big|_{\max(\eta)} = \sqrt{\frac{\alpha}{\beta}} \ . \tag{58}$$

This implies that, assuming operation under ZCS and that the resonator is switched periodically after half-resonance, the location of the peak efficiency point is a weighted-function of the ports' voltages and can be adjusted by the applied voltages on the resonator, i.e. by choosing switching sequence that maximizes α/β. This provides a new design direction and guideline for SCCs and their derivatives, as will be shown next, enabling shifting the rigid optimal target voltage by manipulating the applied voltage on the energy-transfer cell.

5.2.2 Wide-conversion ratio operation modes

The switched-resonant topology presented in Fig. 64 provides seven possible switching states delineated in Fig. 67 as S_A through S_G, in which the resonator may be subjected to the following potentials:

$$\begin{array}{llll} E_A = V_1 & E_C = -V_1 & E_E = V_1 - V_2 & \\ E_B = V_2 & E_D = -V_2 & E_F = V_2 - V_1 & E_G = 0 \end{array} \tag{59}$$

Ten modes of operation are presented next, to showcase the flexibility to adjust the current sourcing capabilities of the converter and to shift the peak efficiency point to target specific operating conditions. A key factor in defining a switching sequence is assuring that charge balance of the flying capacitor is maintained within a cycle. The operation modes, i.e. the voltages that are applied on the resonator per state, are chosen such that the capacitor voltage at the end of a switching sequence retains its initial values. This condition is satisfied if a solution to (47) exists. The new operation modes used in this study are defined with respect to the method in which the voltage is applied on the resonator, and compared to the originally presented basic GRSCC with an optimal conversion ratio of A = 1 (Chapter 2) as a benchmark. Typical waveforms of the operation modes are depicted in Fig. 68, and the calculated conversion and efficiency characteristics of the operation modes are summarized in 0.

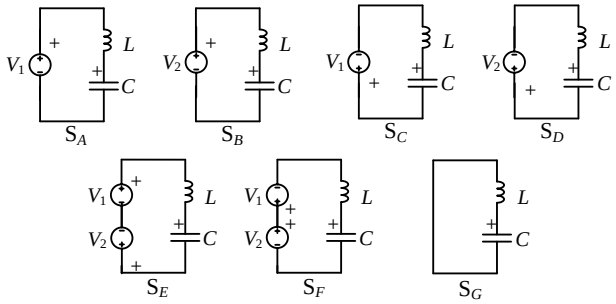


Fig. 67 Possible connection states for the converter presented in Fig. 64. Active switches for the various states. . S_A: Q_{1a}, Q_{3b}; S_B: Q_{2a}, Q_{3b}; S_C: Q_{3a}, Q_{1b}; S_D: Q_{3a}, Q_{2b}; S_E: Q_{1a}, Q_{2b}; S_F: Q_{2a}, Q_{1b}; S_G: Q_{2a}, Q_{2b}

It should be noted that per the selection of target range of conversion ratio and output power, the generalized converter of Fig. 64 can be simplified for the number of operating switches and controller. It should be further noted that in case the generalized converter is realized, then it is possible (demonstrated in the experimental section) to continuously and smoothly shift between the various operation modes as well as generate any desired combination of them. This is enabled since charge-balance of the

resonator (and its flying capacitor) is guaranteed per mode and as a result, cycle-by-cycle transition between the modes is allowed without any deviation of the variables or delay.

A benchmark operation mode is the case of a three-state basic GRSCC configuration described in Chapter 2. In this mode (sequence: S_A, S_B, S_G), namely **mode-3**, was originally implemented in Chapter 2 by a three-switch configuration. The resonator connects to the input through configuration S_A (Fig. 67) to charge, then by S_B to the output voltage and discharges. In order to achieve charge balance, the resonator is then short-circuited through S_G to circulate excess charge.

Five-state operation – In a variation from mode-3, the input and output potentials are applied twice on the resonator before a charge balance state is commenced. The operation is: charge the resonator by S_A, discharge by S_B, charge and discharge again by S_A and S_B, and then end the sequence by S_G to circulate excess charge. By effectively reducing circulation time, the overall time allocated for charge and discharge is increased. This intuitively implies (and validated later in this subsection) that higher current can be outputted since a larger portion of the cycle is devoted to process energy compared to the portion dedicated to balance the charge (in which energy is recycled but not transferred). This method of operation is denoted as **mode-5**, and used as the basis for more modes discussed next.

Bridge variation – An alternative method from mode-3a to process energy by the converter is to subject the resonator to the voltage difference between the input and the output [i.e. S_E, see Fig. 67], providing a lower voltage potential than in the unit mode. The charge state S_E is, like in mode-3, followed by S_B that applies the output voltage on the resonator and charge balance is achieved by a short-circuit [S_G, Fig. 67]. This provides the operation sequence for **mode-3b** (b for bridge), and the basis for more modes, e.g. the bridge variation can also be used for five-state operation, presented here as **mode-5b**.

Semi-complementary operation – In another variation of the switching sequence, charge balance can be facilitated through a different switching state, replacing the resonant short-circuit (S_G) by a complementary connection to V_2, providing new semi-complementary operation. In the charge state S_A the resonator is subjected to V_1. Then, by applying S_B, the network connects to V_2 and charge is transferred to the output. Charge balance is achieved in these modes through state S_D which applies a negative voltage ($-V_2$). This variation is presented here as **mode-3c** (c for complementary),

however it can be combined with any of the variations mentioned earlier, forming **mode-5c**, **mode-3bc** and **mode-5bc**, as summarized in Table VIII.

Complementary operation – This variation provides symmetric operation of the converter, as positive voltages are applied on the resonator, followed by their negative counterparts to achieve charge balance. By initiating S_A, the resonator is subjected to V_1 and charges, then it is subjected to V_2 to discharge by applying state S_B. To maintain charge balance the resonator is then inversely charged by S_C that subjects it to the negative potential $-V_1$, and then discharged by S_D which applies the negative voltage ($-V_2$). Complementary operation can be applied as described here to form **mode-4**, or combined with the bridge variation to form **mode-4b**.

The complete sequences and performance parameters for the ten possible modes formed by combining the above variations are summarized in Table IX, with characteristic resonator waveforms for each mode illustrated in Fig. 68. Comparison between the modes of operation reveals several differences in the properties of the new family. It can be observed that although identical conditions are applied in terms of the ports' voltages and components values, the resultant admittance matrices of the new modes are doubled, and sometimes quadrupled in value when compared to the benchmark mode-3. This directly translates to increased current sourcing capability of the converter. Using the five-state operation in mode-5 increases the power output by 1.2, as admittance is doubled but the effective frequency is lowered by 0.6. The semi-complementary mode-3c is capable of outputting twice the power than mode-3 for the same conditions (frequency and R, L, C values). Combining the two to form a five-state semi-complementary mode-5c increases the power output capability by a factor of 2.4. The output power capability of mode-4 is higher than the benchmark by a factor of 1.5, as admittance is doubled and frequency is lower by 0.75.

Seemingly, minor difference on the power delivery capabilities are observed between mode-3 or mode-3b. However, a major difference is found in the efficiency as a function of the conversion ratio A. As an example, when comparing the waveforms of mode-3 and mode-3b, it can be seen that the bridge variation induces significantly lower circulating current on the converter for a gain of A=0.75, implying difference in the efficiency characteristics when using the bridge variation.

TABLE VIII VARIANCES BETWEEN OPERATION MODES

Mode	*3*	*5*	*3b*	*5b*	*3c*	*5c*	*3bc*	*5bc*	*4*	*4b*
5-state operation		✓		✓		✓		✓		
Bridge			✓	✓			✓	✓		✓
Semi-complementary (inverted output)					✓	✓	✓	✓		
Complementary (symmetric operation)									✓	✓

TABLE IX PERFORMANCE CHARACTERISTICS

Mode	***3***	***5***	***3b***	***5b***	***3c***
Sequence	S_A, S_B, S_G	S_A, S_B, S_A, S_B, S_G	S_E, S_B, S_G	S_E, S_B, S_E, S_B, S_G	S_A, S_B, S_D
f_n	$\left(3\pi\sqrt{LC}\right)^{-1}$	$\left(5\pi\sqrt{LC}\right)^{-1}$	$\left(3\pi\sqrt{LC}\right)^{-1}$	$\left(5\pi\sqrt{LC}\right)^{-1}$	$\left(3\pi\sqrt{LC}\right)^{-1}$
$V_{C,n}$	$\begin{cases} V_{C,1}\approx V_1+V_2 \\ V_{C,2}\approx V_2-V_1 \\ V_{C,3}\approx V_1-V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx 2V_2 \\ V_{C,2}\approx 0 \\ V_{C,3}\approx 2V_1 \\ V_{C,4}\approx 2V_2-2V_1 \\ V_{C,5}\approx 2V_1-2V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx V_1 \\ V_{C,2}\approx 2V_2-V_1 \\ V_{C,3}\approx V_1-2V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx 2V_2 \\ V_{C,2}\approx 0 \\ V_{C,3}\approx 2V_1-2V_2 \\ V_{C,4}\approx 4V_2-2V_1 \\ V_{C,5}\approx 2V_1-4V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx V_1+2V_2 \\ V_{C,2}\approx -V_1 \\ V_{C,3}\approx V_1-2V_2 \end{cases}$
$Y_{m,n}$	$\begin{bmatrix} 0 & 2fC \\ -2fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 4fC \\ -4fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 2fC \\ -2fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 4fC \\ -4fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 4fC \\ -4fC & 0 \end{bmatrix}$
η	$\left[1+\frac{\pi}{2Q}\left(A^{-1}+A-1\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(2A^{-1}+5A-2\right)\right]^{-1}$	$\left[1+\frac{\pi}{2Q}\left(A^{-1}+3A-3\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(2A^{-1}+9A-6\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(A^{-1}+3A\right)\right]^{-1}$
$A_{opt.}$	1	0.63	0.58	0.47	0.58

PERFORMANCE CHARACTERISTICS (CONTINUED)

Mode	***5c***	***3bc***	***5bc***	***4***	***4b***
Sequence	S_A, S_B, S_A, S_B, S_D	S_E, S_B, S_D	S_E, S_B, S_E, S_B, S_D	S_A, S_B, S_C, S_D	S_E, S_B, S_F, S_D
F_{max}	$\left(5\pi\sqrt{LC}\right)^{-1}$	$\left(3\pi\sqrt{LC}\right)^{-1}$	$\left(5\pi\sqrt{LC}\right)^{-1}$	$\left(4\pi\sqrt{LC}\right)^{-1}$	$\left(4\pi\sqrt{LC}\right)^{-1}$
$V_{C,n}$	$\begin{cases} V_{C,1}\approx 3V_2 \\ V_{C,2}\approx -V_2 \\ V_{C,3}\approx 2V_1+V_2 \\ V_{C,4}\approx V_2-2V_1 \\ V_{C,5}\approx 2V_1-3V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx V_1+V_2 \\ V_{C,2}\approx V_2-V_1 \\ V_{C,3}\approx V_1-3V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx 3V_2 \\ V_{C,2}\approx -V_2 \\ V_{C,3}\approx 2V_1-V_2 \\ V_{C,4}\approx 3V_2-2V_1 \\ V_{C,5}\approx 2V_1-5V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx V_1+V_2 \\ V_{C,2}\approx V_2-V_1 \\ V_{C,3}\approx -\left(V_1+V_2\right) \\ V_{C,4}\approx V_1-V_2 \end{cases}$	$\begin{cases} V_{C,1}\approx V_1 \\ V_{C,2}\approx 2V_2-V_1 \\ V_{C,3}\approx -V_1 \\ V_{C,4}\approx V_1-2V_2 \end{cases}$
$Y_{m,n}$	$\begin{bmatrix} 0 & 8fC \\ -8fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 4fC \\ -4fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 8fC \\ -8fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 4fC \\ -4fC & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & 4fC \\ -4fC & 0 \end{bmatrix}$
η	$\left[1+\frac{\pi}{8Q}\left(5A^{-1}+9A-6\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(A^{-1}+4A-2\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(A^{-1}+10A-2\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(A^{-1}+A\right)\right]^{-1}$	$\left[1+\frac{\pi}{4Q}\left(A^{-1}+2A-2\right)\right]^{-1}$
A_{opimal}	0.74	0.5	0.58	1	0.71

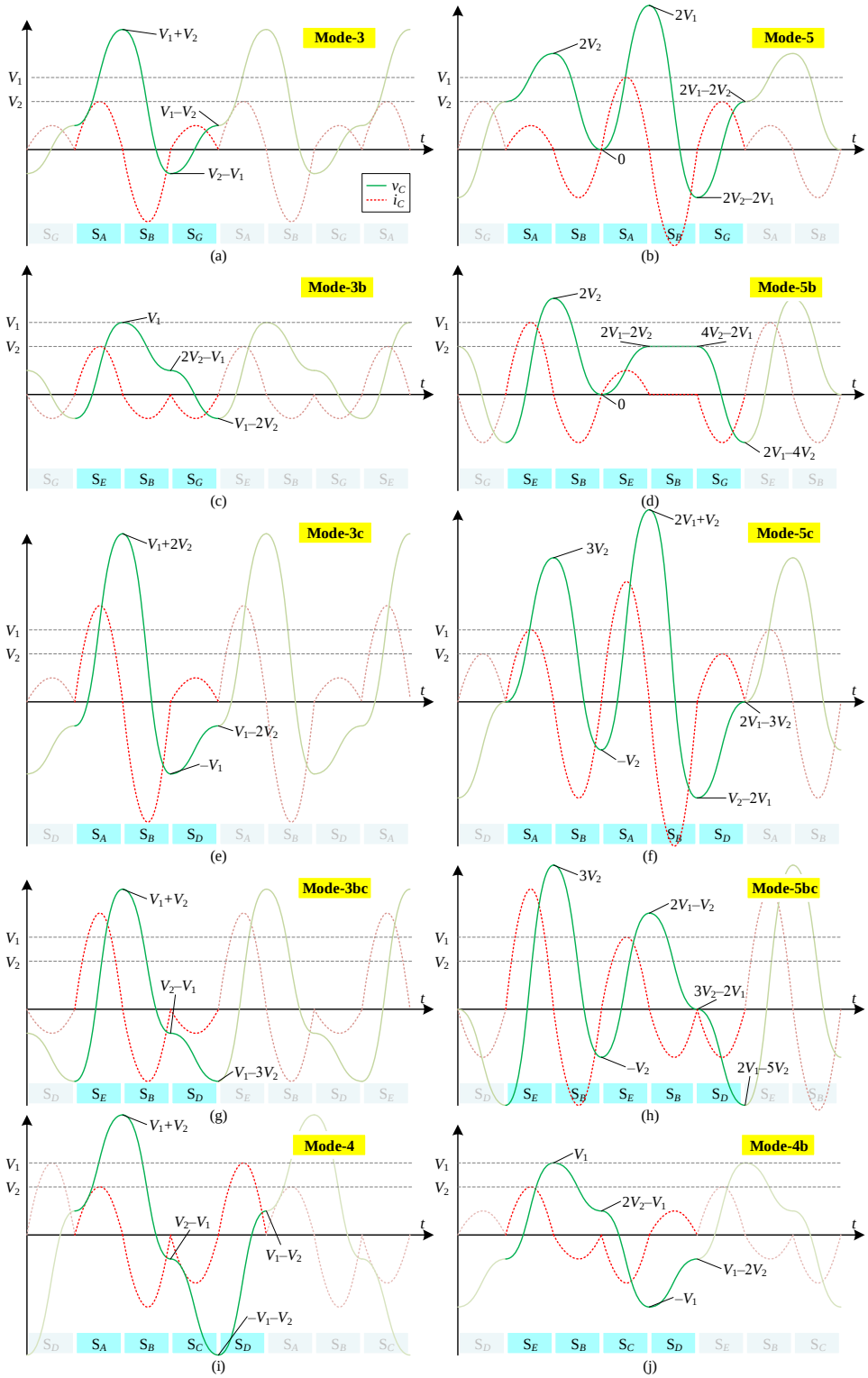


Fig. 68 Exemplary waveforms of the presented family for a case that $V_1 = 1.5V_2$ for all modes

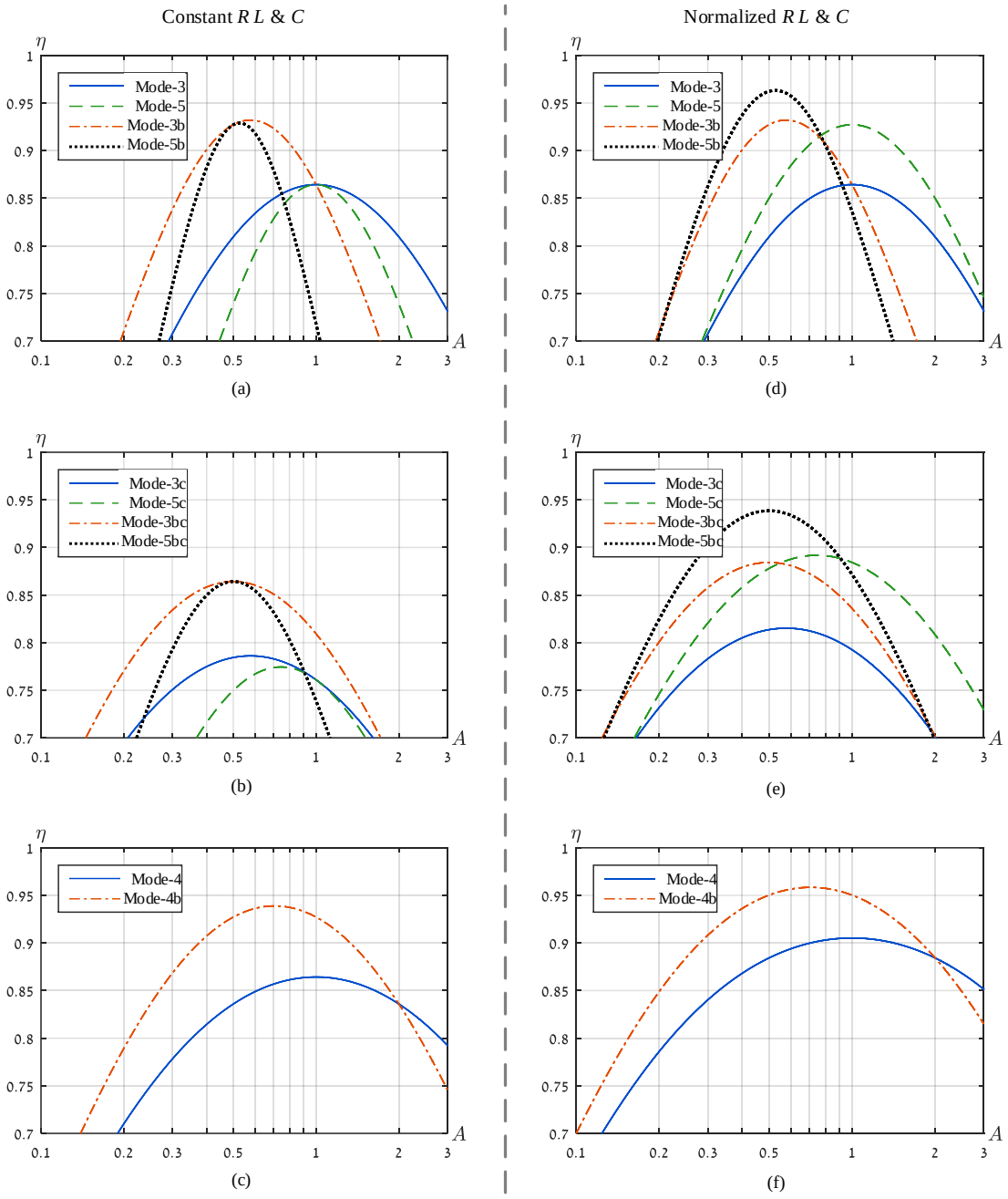


Fig. 69 Theoretically calculated efficiency plots of the presented converter as a function of conversion ratio for the ten presented operating modes when: Left (a)-(c) R,L,C are the same in all topologies providing a quality factor of $Q = 10$; (d)-(f) Resonator admittance is equal for all modes.

The efficiency expressions from Table IX have been plotted for better view and are presented in Fig. 69 for all modes. In Fig. 69(a-c) a case in which equal resonator parameters are used for all modes is depicted. It can be seen that for the majority of conversion ratios the converter is most efficient when using mode-4b, with peak efficiency at $A = 0.71$. Bridge variations do not change the power delivery capabilities but have a major impact on the efficiency: both in the peak location and value.

However, it can be seen that five-state sequences for example, increase the power output at the cost of a narrower applicable efficiency range. This can be explained by major increase in rms currents due to the large mismatch between the port voltages, as can be easily observed in the example of Fig. 68(f), which demonstrates high divergence in the current prior to the balance state (S_D).

Since the power delivery capabilities differ between the modes, an alternative comparison between modes has been performed by normalizing the operation to the same power delivery level. In 0Fig. 69(d-f), the resonator's parameters are adapted such that the total admittance matrix values (considering the maximum frequency) are the same for all modes, i.e. for the same power delivery capability. It can be seen that all modes are distinctively more efficient than the benchmark configuration. A highlighted example is that for the same power delivery capability, mode-4b provides higher efficiency of at least 7% for any gain. On selected range of conversion ratios, such as A=0.3, the semi-complementary mode-5bc allows for higher efficiency than mode-4b.

Further flexibility on the power delivery capabilities can be obtained by combining modes of operation. For instance, mixture of mode-5 and mode-5b can result in sequences such as S_A, S_B, S_E, S_B, S_G (namely mode-5d) or S_E, S_B, S_A, S_B, S_G (namely mode-5e). Mode-5e has a reduced output admittance of $Y_{21} = 2fC$, while mode-5d as an increased output admittance of $Y_{21} = 4fC$. The efficiency curves of these modes are shown non-normalized in Fig. 70.

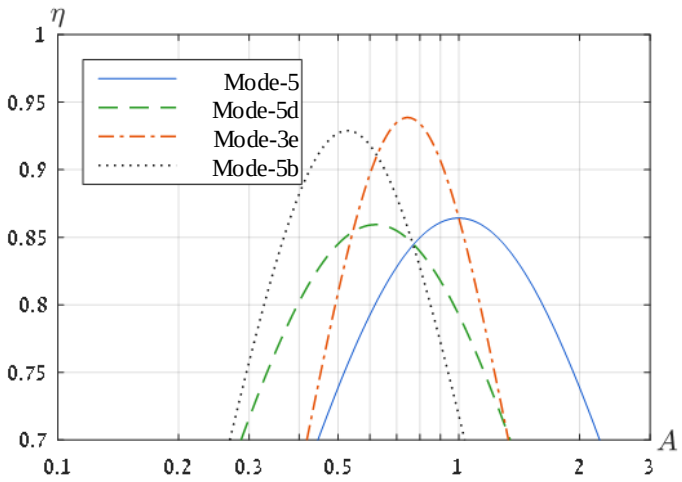


Fig. 70 Theoretically calculated efficiency plots of the presented converter as a function of conversion ratio for interleaved modes

5.2.3 Application

In similar way to the GRSCC and as described next, some switches of the GSwRC family can be implemented either by simple, single, transistor or by four-quadrant switches (reverse-blocking) such as a back-to-back configuration. For a case that a step-down is desired, then Q_{1a} and Q_{1b} need to be implemented as four-quadrant devices for proper operation. In this case the *resonator* is inherently clamped to V_1 without losing operability when the *capacitor* charges to higher voltage. In this case, the maximum voltage stress on switches $Q_{1a,b}$ and $Q_{3a,b}$ is the source value V_1.

An additional implementation variation is with Q_{2a} and Q_{2b} as four-quadrant switches. This provides higher flexibility of the converter, allowing step-up and step-down conversion. This comes at the cost of higher component count and losing the inherent resonator-clamp.

The presented GSwRC family extends the GRSCC family and provides true voltage regulation capabilities with the added value of immediate transient-response capabilities. These unique features allow the high power-density property of the SCC family to be utilized to further improve applications such as envelope-tracking, voltage-regulation in high-transient applications, both discussed in Chapter 4. Furthermore, recent studies which have presented high power-density regulation schemes using SCC technology [125], [126] still require a post-regulation at point-of-load. Table X provides a topology comparison for post-regulation schemes used today, compared to the proposed family. As will be demonstrated in the experimental section, the presented family facilitates efficient post-regulation using SCC technology.

TABLE X KEY ATTRIBUTES COMPARISON BETWEEN TOPOLOGIES

	SCC	***RSCC***	***Buck***	***GRSCC***	***GSwRC***
Efficiency characteristics	Singular	Singular	Wide	Narrow	Adjustable
Soft-switching capability	×	✓	×	✓	✓
Scalability	Limited by switching-loss	✓	Limited by switching-loss & large inductance	✓	✓
Component stress	Clamped to source voltages	Clamped to source voltages	Clamped to source voltages	Clamped to source voltages	Clamped to source voltages

5.2.4 Experimental verification

To demonstrate the operation of the various modes of the switched-resonant converter and to validate the theoretical analysis, a low output-voltage prototype was built and tested; $V_1 = 5$V to $V_2 = 1.2$V. The prototype was tested for three most promising modes for this conversion gain: mode-5, mode-3bc, mode-4. Experimental waveforms of the resonator's current and the capacitor's voltage operating in steady-state are shown in Fig. 71; the resonator's parameters were $C = 220$nF, $L \approx 40$nH ($T_{state} = 300$ns), the MOSFETs used where Siliconix SIA436EDJ, driven by MAX17601 drivers. The differences between the modes are apparent. The output power of the bridge-GRSCC was measured 2.75W, for the complementary mode 3.9W and for the semi-complementary 5.1W. These results are in excellent agreement with the theoretical prediction from 0Table IX.

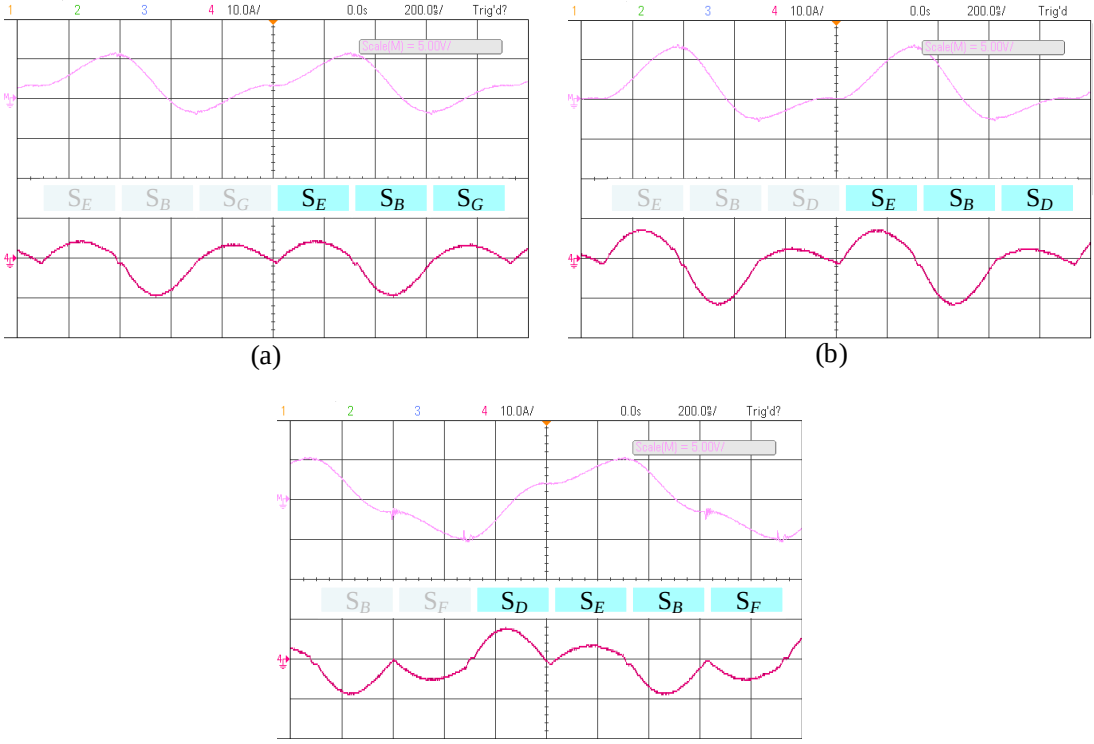
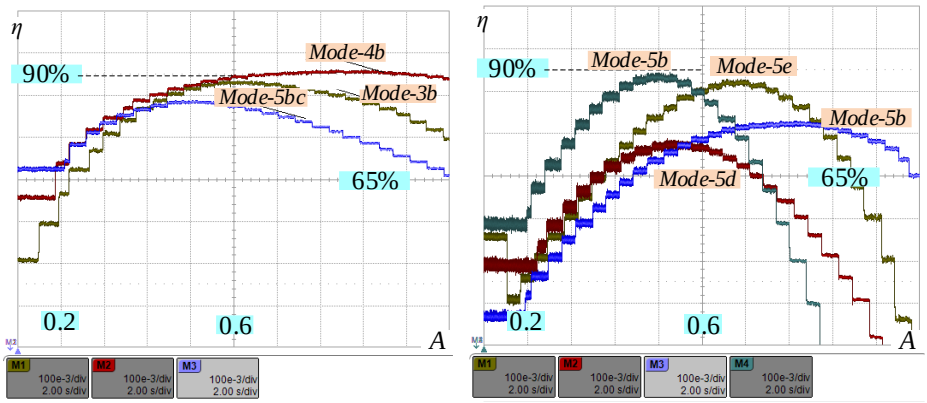


Fig. 71 Experimental waveforms of the presented converter for the following modes showing vC at the top and iC at the bottom of each screenshot: (a) mode-3b; (b) mode-3c; (c) mode-4b.



(a) (b)

Fig. 72 Experimental efficiency sweep as a function of output voltage gain. Vertical: 10%/Div. ; Horiz.: 0.1/Div. (a) comparison between modes 4b, 3b, and 5bc; (b) comparison of modes d, b, and their derivatives, modes 5b, 5c, 5d, 5e.

Fig. 72(a) shows the efficiency as a function of the conversion ratio comparing mode-3b, mode-5bc, and mode-4b. These measurements were carried out using an electronic load that was programmed to sweep V_2. The cycle frequency of the converters was set to maximum - f_n, i.e. maximizing the power output capability at each of the modes. As can be seen, a very good agreement is obtained with the theoretical curves of Fig. 69. Also demonstrated is the different conversion ratio for the peak efficiency at each of the modes. Fig. 72(b) shows an experimental efficiency plot demonstrating the hybrid combinations of mode-5d and mode-5e as in Fig. 70, validating the flexibility in choice of switching options to obtain different converter properties in terms of efficiency.

5.3 Performance Analysis of Gyrator Behavior in Multi-Port Resonant Switched Capacitor Converters

5.3.1 Motivation

Behavioral and loss modelling has been described for the GRSCC in Chapter 3 and Subsection 5.2. The basis for the analysis includes a simplification made by neglecting the exponential decay of the resonant current, i.e., assuming that the power-stage maintains high quality factor. This simplification relies on the assumption that to obtain efficient conversion, the loop resistance must be kept low. However, careful inspection, by non-ideal simulation as well as experiments, has shown that analysis based on a lumped resistance assumption results in an optimistic prediction, sometimes with significant differences from practical results, even for cases where the loop-resistances are low. It appears, then, that while high quality factor is a reasonable approximation for analysis of simplistic resonant-mode conversion with short time-periods, such as half-resonance period or a limited number of switching states, in modern RSCCs (i.e., power converters needing multiple switching modes to complete a cycle (e.g., resonant binary SCC [21] or GRSCC)), the exponential decay of the resonant current cannot be overlooked.

This section provides a general behavioral model for switched-resonator converters, which addresses the impact of conduction losses on the converter's performance and efficiency. A fully systematic analysis provides tools for comparing the performance of different converters and operation modes, for determining the optimal configuration given true operating conditions. For this, an analytical tool for behavioral modelling of converters with complex switching-schemes is introduced next. It is based on switching-state representation. The generic representation, which can be applied to a variety of converters, provides the basis for the behavioral model representing the switched-resonator converters.

5.3.2 Multiport – switching-state representation

Consider a generalized multiple port switch-mode converter illustrated in Fig. 73. The converter has K physical ports for connecting to dc sources and loads, a reactive element (illustrated in Fig. 73 as a resonator) as an energy transfer cell, and an arbitrary switch assembly.

Vectors **V** and **I** define the ports' voltages V_1 to V_k and currents I_1 to I_k, ($k = 1,\ldots,K$), that is:

$$\mathbf{V} = [V_1 \quad \cdots \quad V_K]^{\mathrm{T}} \quad , \quad \mathbf{I} = [I_1 \quad \cdots \quad I_K]^{\mathrm{T}} \; . \tag{60}$$

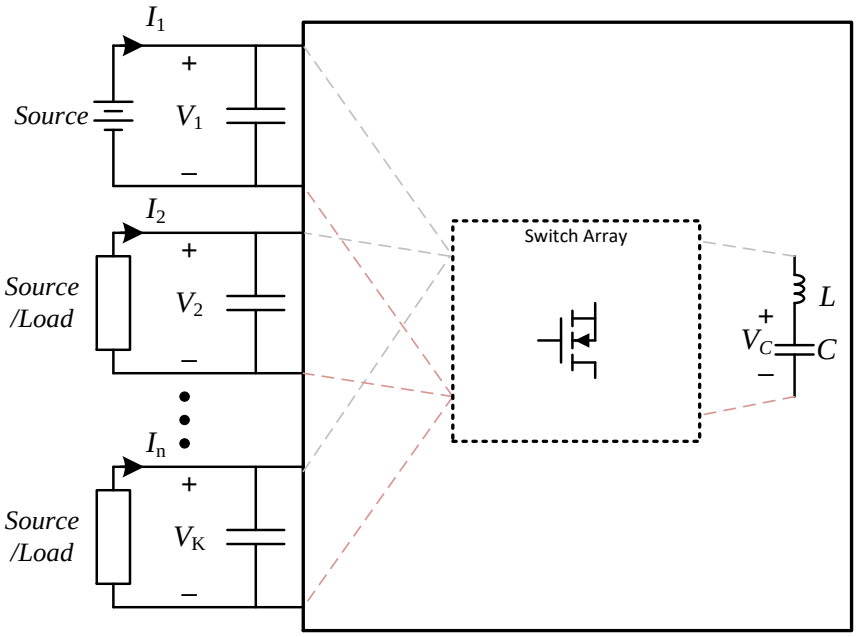


Fig. 73 A simplified diagram of a switched-resonator converter with an arbitrary switch-assembly to connect the resonator tank to *K* sources/loads

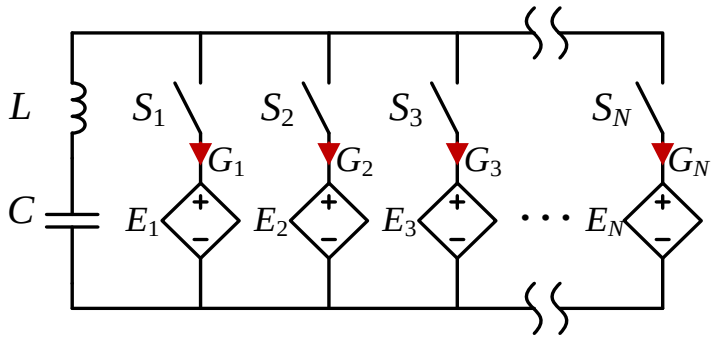


Fig. 74 An equivalent model of the switched-resonator converter, with *N* equivalent sources to represent each state.

The term *state* is used in this study to address the time period in which the converter's reactive element connects through a specific switch-configuration to one or more (or none) of the physical ports. A complete *cycle* of the switched-mode converter relates to a repeated sequence of *N* states.

An equivalent circuit for the switch-mode converter illustrated in Fig. 74 defines the converter's state-representation. It allows analysis of such a converter by considering the voltage potential applied to each state on the resonator as an individual source. The equivalent circuit comprises the reactive branch in parallel to *N* branches with a voltage

source E_n ($n = 1,\ldots,N$) and a switch S_n, which together represent the linear port combination applied during a single state. A set of parameters is defined to distinguish the physical ports parameters V_k and I_k, from the *state*-applied voltages on the resonator, namely E_n, and average state currents G_n, giving the state potentials vector **E** and average current vector **G**:

$$\mathbf{E} = \begin{bmatrix} E_1 & \cdots & E_N \end{bmatrix}^{\mathrm{T}} \quad , \quad \mathbf{G} = \begin{bmatrix} G_1 & \cdots & G_N \end{bmatrix}^{\mathrm{T}} \ . \tag{61}$$

Translation between **V** and **E** is done through a $N \times K$ transfer matrix $\boldsymbol{\Psi}$ which holds the data used to define the physical-port combination applied in each state:

$$\mathbf{E} = \boldsymbol{\Psi} \cdot \mathbf{V}, \qquad \boldsymbol{\Psi} = \begin{bmatrix} \psi_{11} & \cdots & \psi_{1K} \\ \vdots & \ddots & \vdots \\ \psi_{N1} & \cdots & \psi_{NK} \end{bmatrix}, \tag{62}$$

where ψ_{nk} defines the contribution of port $k \in \{1,\ldots,K\}$ to state $n \in \{1,\ldots,N\}$. The connection of a port can be described as positive polarity, negative polarity, or not connected, meaning that the values within $\boldsymbol{\Psi}$ are limited to $\psi_{nk} \in \{-1,0,1\}$. The average ports' currents back-translate from the state currents by the same transfer rules as the voltages. Translation between **G** and **I** is obtained by transposing $\boldsymbol{\Psi}$:

$$\mathbf{I} = \boldsymbol{\Psi}^{\mathrm{T}} \cdot \mathbf{G} \ . \tag{63}$$

By employing average and dynamic behavioral modeling and expanding the two-port theorem [127] used to describe the transfer-function of switch-mode converters, multiport analysis is used to eliminate the switches and to define a relationship between **E** and **G**. Here, **E** is considered known or having external dependence (e.g., a resistive load), while the dependency of **G** is defined by a $N \times N$ general admittance matrix **X** such that:

$$\mathbf{G} = \mathbf{X} \cdot \mathbf{E}, \qquad \mathbf{X} = \begin{bmatrix} X_{11} & \cdots & X_{1N} \\ \vdots & \ddots & \vdots \\ X_{N1} & \cdots & X_{NN} \end{bmatrix} . \tag{64}$$

The method to obtain **X** will be detailed in the following section. The relationship between **V** and **I** can then be formed from (64) by using the transfer matrices of (62) and (63), resulting a final $K \times K$ admittance matrix, **Y**:

$$\mathbf{I} = \mathbf{Y} \cdot \mathbf{V}, \qquad \mathbf{Y} = \boldsymbol{\Psi}^{\mathrm{T}} \cdot \mathbf{X} \cdot \boldsymbol{\Psi} = \begin{bmatrix} Y_{11} & \cdots & Y_{1K} \\ \vdots & \ddots & \vdots \\ Y_{K1} & \cdots & Y_{KK} \end{bmatrix} . \tag{65}$$

Multiport theorem can be used to simplify the analysis of a converter with a complex switching scheme, even if it maintains two physical ports. This is done by observing the state-domain through the equivalent circuit of Fig. 74.

5.3.3 Switched-resonator converters as multiport

Switched-resonator based converters containing a single reactive network, such as the GRSCC and the GSwRC, implement a complex switching scheme, in order to benefit from a wide-range for efficient conversion. In order to derive the behavior of the converter, the analysis is performed per-state. In each state, the resonator connects to the input or output ports in one out of several possibilities. The analysis utilizes the switching-state representation from Section 5.3.2 to reduce the complexity of the analysis and to derive a behavioral model which takes resistive losses into account, for improved accuracy. Low-loss simplification then provides lean expressions, completed by guidelines for the conditions under which the simplification may be used. The analysis is then followed by various application examples and performance analysis as a showcase for the advantages of the analysis.

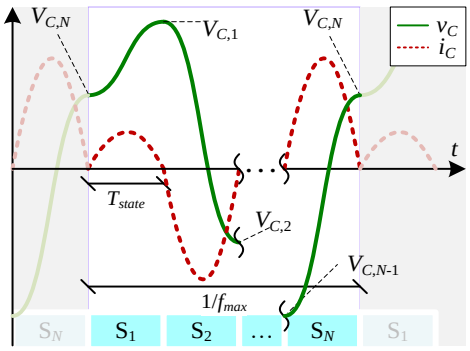


Fig. 75 Illustrative waveforms for the resonator current and capacitor voltage in a switched-resonator converter consisting N switching states

A. Behavioral Model

A single switched-resonator converter in its most general form can be described as shown in Fig. 73, where the reactive element is formed by a flying capacitor and an inductor connected in series. Each state duration is a time-period of T_{state}, defined by the resonator's half-resonance which is ideally:

$$T_{state} = \pi\sqrt{LC} \quad , \tag{66}$$

where L and C are the resonator's inductance and capacitance values. Exemplary resonator currents and flying-capacitor voltage waveforms are illustrated in Fig. 75,

demonstrating a switching-sequence composed of N states that sets an upper-frequency limit of the converter, f_n. The effective operating frequency, f, may be lower than f_n, since dead-time padding between the switching states is allowed, e.g. for control by pulse-density modulation (PDM) [66], which yields:

$$f \le \left(N\pi\sqrt{LC}\right)^{-1} \triangleq f_n \ . \tag{67}$$

The transition between states occurs at zero-current, and thereby energy is transferred between states by the energy stored at the capacitive element. The voltage carried by the resonator's capacitor during transition from state n to the next is defined here as $V_{C,n}$ (see Fig. 75). The value of $V_{C,n}$ serves as the link between states as it provides the initial condition for the following state $(n+1)$, and is derived by solving the series *R-L-C* circuit, based its own condition, $V_{C,n\text{-}1}$, and E_n:

$$V_{C,n} = E_n + a\left(E_n - V_{C,n-1}\right) \ , \tag{68}$$

where a expresses the attenuation of the *R-L-C* circuit as a result of the resonator's series losses during the state-period T_{state}, that is:

$$a = e^{-\frac{R}{2L}T_{state}} \ . \tag{69}$$

The cyclic operation in steady-state can be expressed by the following recursive set as:

$$\begin{cases} V_{C,1} = \left(1+a\right)E_1 - aV_{C,N} \\ V_{C,n} = \left(1+a\right)E_n - aV_{C,n-1} \end{cases} \quad , \quad n \in \left(1, N\right] \ . \tag{70}$$

Solving (70) for $V_{C,n}$ yields:

$$V_{C,n} = \frac{1+a}{1-\left(-a\right)^N}\left(\sum_{m=1}^{n}\left(-a\right)^{n-m}E_m + \sum_{m=n+1}^{N}\left(-a\right)^{N+n-m}E_m\right) \ . \tag{71}$$

The average current value of each state, G_n, is then derived from the total difference in charge across C from the previous state averaged over the complete duration of a sequence, that is:

$$G_n = f \cdot 2C\left(V_{C,n} - V_{C,n-1}\right) \ . \tag{72}$$

Substituting (71) into (72) and after some manipulation, the general admittance $\mathbf{X}$ of the multiport equivalent-circuit can be expressed as:

$$\mathbf{X} = fC\frac{1+a}{1-\left(-a\right)^N}\left(\frac{1+a}{a}\begin{bmatrix} 0 & \left(-a\right)^{N-1} & \left(-a\right)^{N-2} & & -a \\ -a & 0 & \left(-a\right)^{N-1} & \cdots & \left(-a\right)^{2} \\ \left(-a\right)^{2} & -a & 0 & & \left(-a\right)^{3} \\ & \vdots & & \ddots & \vdots \\ \left(-a\right)^{N-1} & \left(-a\right)^{N-2} & \left(-a\right)^{N-3} & \cdots & 0 \end{bmatrix} + \left(1-\left(-a\right)^{N-1}\right)\begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix}\right) \tag{73}$$

For a convenient solution, it is preferred to split the admittance matrix **X** into a cross-admittance matrix $\mathbf{X}_{\times}$, and a self-admittance matrix $\mathbf{X}_{\mathrm{I}}$, that is:

$$\mathbf{X} = \mathbf{X}_{\times} + \mathbf{X}_{\mathrm{I}} = \begin{bmatrix} 0 & X_{12} & \cdots & X_{1N} \\ X_{21} & 0 & & X_{2N} \\ \vdots & & \ddots & \vdots \\ X_{N1} & X_{N2} & \cdots & 0 \end{bmatrix} + \begin{bmatrix} X_{11} & 0 & \cdots & 0 \\ 0 & X_{22} & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & X_{NN} \end{bmatrix}. \tag{74}$$

A graphic representation of the admittance breakdown is shown in Fig. 76. It can be observed that the ports' equivalent parallel resistance is represented in $\mathbf{X}_{\mathrm{I}}$, whereas the power transfer characteristics are described through the values of $\mathbf{X}_{\times}$, i.e. the gyration relationship is formed by the representation of energy transferring sources and parallel port losses.

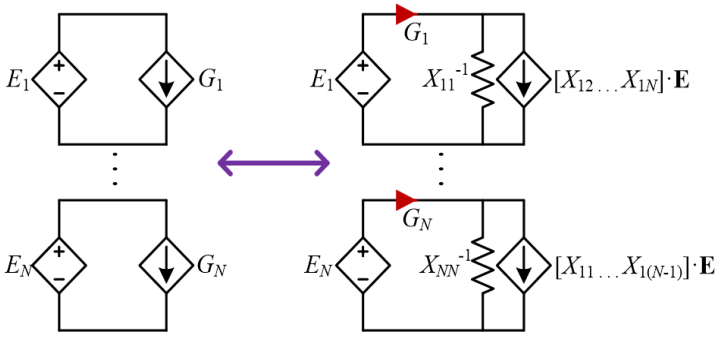


Fig. 76 Admittance representation of the branch currents G_n. Self-admittances $\mathbf{X}_{\mathrm{I}}$ provide parallel resistance while cross-admittances $\mathbf{X}_{\mathrm{X}}$ provide externally-dependent current.

Equation (74) can be rewritten as the following set, providing a practical analytical solution for **X**:

$$\mathbf{X} = fC\frac{1+a}{1-\left(-a^{N}\right)}\left(\frac{1+a}{a}\mathbf{X}_{\times}^{*} + \left(1-\left(-a\right)^{N-1}\right)\mathbf{X}_{\mathbf{I}}^{*}\right)$$

$$\begin{cases} \mathbf{X}_{\times}^{*} = \begin{bmatrix} 0 & (-a)^{N-1} & (-a)^{N-2} & & -a \\ -a & 0 & (-a)^{N-1} & \cdots & (-a)^{2} \\ (-a)^{2} & -a & 0 & & (-a)^{3} \\ & \vdots & & \ddots & \vdots \\ (-a)^{N-1} & (-a)^{N-2} & (-a)^{N-3} & \cdots & 0 \end{bmatrix} \\ \mathbf{X}_{\mathbf{I}}^{*} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix} \end{cases} \tag{75}$$

B. Low loss simplification

While (75) can be used to numerically compute the admittance of a converter alongside (65) to derive the ports' relationships, a low-loss simplification may provide

a compact, simplistic representation for behavioral analysis and for formula-derivation by inspection. Low losses approximation, in particular for resonant-type conversion, has a substantial track record and is used as an early-stage design tool by many practices. The functionality of the converter can be conveniently derived, and the losses' impact is later added. In converters that feature high rms currents, it is extremely beneficial to be able to clearly distinguish between the converter's native topological features and the features that result from the implementation. This becomes even more apparent for converters having complex and multiple switching states, such as the case of switched-resonator converters.

In this study, two cases of operation are distinguished from one another, for odd and even numbers of states. While an odd-state cycle intuitively formulates pure gyrator characteristics, certain additional conditions are needed for an even-state cycle to allow gyrator behavior.

i. Odd sequence

If N is odd and $a \to 1$, the self-admittance can be considered negligibly small since $(1-(-a)^{N-1}) \to 0$, therefore (75) can be simplified to an ideal multiport gyrator:

$$\mathbf{X}\big|_{\substack{N\,\text{is odd}\\ a\to 1}} \approx 2fC \begin{bmatrix} 0 & +1 & -1 & & -1 \\ -1 & 0 & +1 & \cdots & +1 \\ +1 & -1 & 0 & & -1 \\ & \vdots & & \ddots & \vdots \\ +1 & -1 & +1 & \cdots & 0 \end{bmatrix} . \tag{76}$$

Fully addressed in [3], this simplification is useful for manually analyzing the behavior of the GRSCC and most of the operation scenarios for the GSwRC. However, as detailed in the following examples, relatively high circulating currents in this converter quickly result in notable discrepancies between the results from (76) versus (75). Inaccuracies can be observed even for a case in which the resonator path quality-factor is considered high.

ii. Even sequence

If N is even, the attenuation cannot be fully ignored in (75), even in the case of $a \to 1$, where the simplification gives:

$$\mathbf{X}\big|_{\substack{N\,\text{is even}\\ a\to 1}} \approx \frac{4fC}{1-a^N}\left(\mathbf{X}_{\times}^{*}+\mathbf{X}_{\mathbf{I}}^{*}\right) . \tag{77}$$

It can be seen from (77) that for an even sequence, $\mathbf{X}$ does not converge to finite values, since the denominator approaches zero, i.e. an even sequence doesn't naturally provide charge balance for the resonator. However, when substituting $\mathbf{X}$ in (64) by (77) ,

dependency between branch voltages within **E** may allow converged values for the branch currents in **G**, if the numerator goes to zero in an exponential rate of $(1 - a^{n0})$, similar to the denominator in (77), where $n0$ may be of any value. This dependency naturally occurs if the values for **E** satisfy the following expression:

$$\sum_{n=1}^{N} E_n (-1)^n \le \left(1 - a^N\right), \tag{78}$$

which means that the sum of potentials seen by the resonator throughout a sequence is close to zero, and therefore charge-balance is forced by the applied potential on the resonator rather than by the native state of the converter. As detailed next, satisfactory parameter dependency in **E** can be obtained either by design (e.g. by creating a symmetric sequence), or naturally by I-V dependency of one or more branches (e.g. a resistive load).

5.3.4 Examples and comparison

The first example provides analysis for the 1:1 resonant switched-capacitor converter (RSCC), illustrated in Fig. 77(a). It consists of a two-state (even) sequence: charge from V_{in}, then discharge to V_{out}, and is described by a 2×2 identity transfer matrix $\boldsymbol{\Psi}$, i.e. $\mathbf{Y} = \mathbf{X}$. The value of **Y** is derived from (75) and (77) for the non-ideal and the ideal cases, respectively, and listed Table XI. Solving for the output current, i.e. $I_2 = f(\mathbf{V})$, gives:

$$I_2 = 4fC\frac{V_1 - V_2}{1 - a^2} \ . \tag{79}$$

This implies that for a converter with negligible attenuation, i.e. $a \to 1$, the current gain will be extreme. Further manipulation of (79) with the assumption of a filtered resistive load, namely R_L, provides the well-known voltage gain which converges to unity for $a \to 1$:

$$\frac{V_2}{V_1} = \frac{4fCR_L}{\left(1 - a^2\right) + 4fCR_L} \quad \xrightarrow[a \to 1]{} 1 \tag{80}$$

This result coincides with previous studies [19], [28], [29], [34], [122], [128]-[132] and provides an insight into the regulation capabilities of a conventional RSCC. It can be seen from (80) that although some (lossy) regulation can be obtained by manipulating f (through PDM), effective regulation isn't feasible without the presence of significant attenuation.

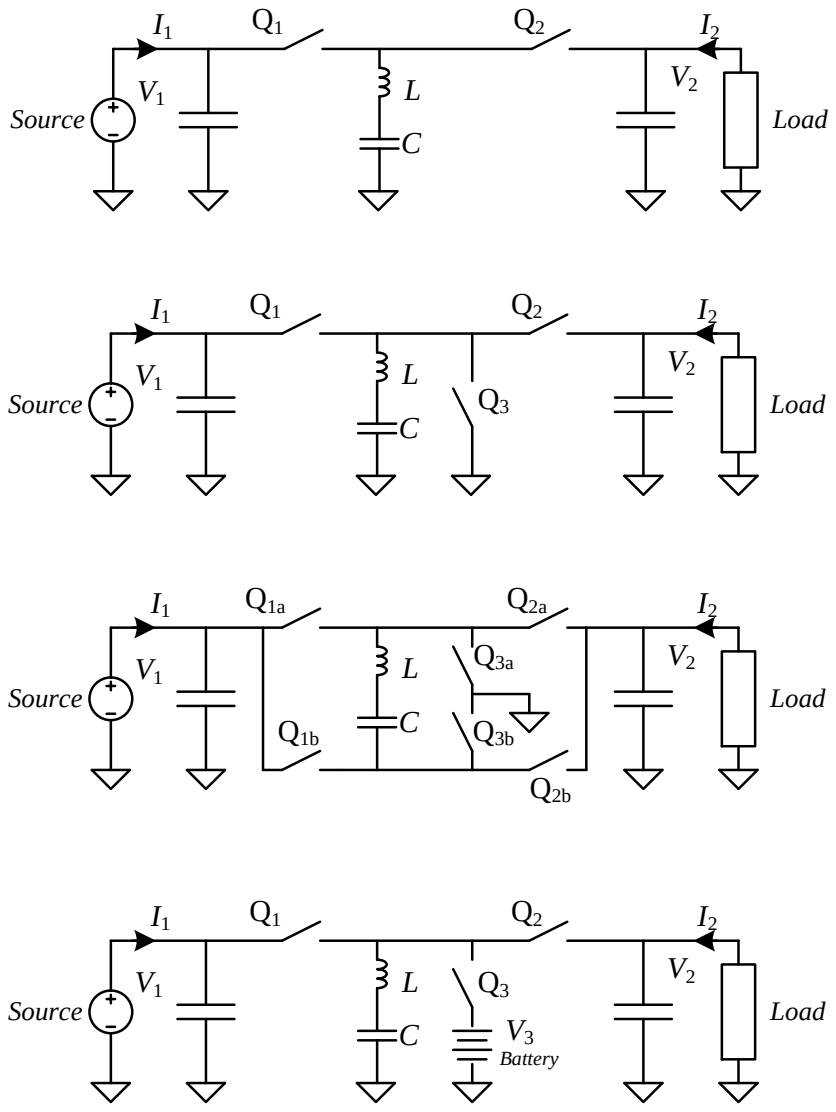


Fig. 77 Circuits for: (a) A 1:1 RSCC; (b) GRSCC, (c) GswRC; (d) DC UPS

Next, a basic GRSCC [Fig. 77(b)] is analyzed. The switching scheme for the GRSCC consists of a three-state (odd) sequence, using the same two states as the RSCC followed by an additional short-circuit state to replenish mismatched charge. The states are described by a 3×2 transfer matrix which has an additional null row compared to the RSCC, representing the shorted resonator at state 3, where no voltage is applied. The full solution to (75) and the simplified asymptotic solution given by (76) are both provided in Table XI.

Table XI also lists the solution for a longer, five-state sequence for the GRSCC. It is followed by solutions to selected operation modes of a more complex two-port switched-resonator converter presented in the beginning of this chapter [Fig. 77(c)], which allows linear combinations of V_1 and V_2 to be used for each state. Finally, a solution of a 3-port GRSCC as in [3] [Fig. 77(d)] is also listed.

TABLE XI PERFORMANCE CHARACTERISTICS

	K	N	$\boldsymbol{\Psi}$	$\mathbf{Y}$	$\mathbf{Y}(a\rightarrow 1)$	I_2^* $(a\rightarrow 1, f_{max})$
RSCC	2	2	$\begin{bmatrix}1 & 0\\ 0 & 1\end{bmatrix}$	$\frac{(1+a)^2}{1-a^2} fC\begin{bmatrix}1 & -1\\ -1 & 1\end{bmatrix}$	$\frac{4fC}{1-a^2}\begin{bmatrix}1 & -1\\ -1 & 1\end{bmatrix}$	
GRSCC	2	3	$\begin{bmatrix}1 & 0\\ 0 & 1\\ 0 & 0\end{bmatrix}$	$\frac{(1+a)^2}{1+a^3} fC\begin{bmatrix}1-a & a\\ -1 & 1-a\end{bmatrix}$	$2fC\begin{bmatrix}0 & 1\\ -1 & 0\end{bmatrix}$	1
GRSCC (5-state)	2	5	$\begin{bmatrix}1 & 0\\ 0 & 1\\ 1 & 0\\ 0 & 1\\ 0 & 0\end{bmatrix}$	$\frac{(1+a)^2}{1+a^5} fC\begin{bmatrix}(1-a)(2a^2+a+2) & 2a^3+a-1\\ -(2+a^3+a^2) & (1-a)(2a^2+a+2)\end{bmatrix}$	$4fC\begin{bmatrix}0 & 1\\ -1 & 0\end{bmatrix}$	1.2
GSwRC (mode 1)	2	3	$\begin{bmatrix}1 & -1\\ 0 & 1\\ 0 & -1\end{bmatrix}$	$\frac{(1+a)^2}{1+a^3}\frac{C}{T}\begin{bmatrix}1-a & 2a\\ -2 & a(1-a)\end{bmatrix}$	$4fC\begin{bmatrix}0 & 1\\ -1 & 0\end{bmatrix}$	2
GSwRC (mode 2)	2	4	$\begin{bmatrix}1 & -1\\ 0 & 1\\ -1 & 1\\ 0 & -1\end{bmatrix}$	$\frac{1-a^2}{1-a^4}2fC\begin{bmatrix}1-a^2 & 2a(1+a)\\ -2(1+a) & 2(1-a^2)\end{bmatrix}$	$4fC\begin{bmatrix}0 & 1\\ -1 & 0\end{bmatrix}$	1.5
GRSCC (3 ports)	3	3	$\begin{bmatrix}1 & 0 & 0\\ 0 & 1 & 0\\ 0 & 0 & 1\end{bmatrix}$	$\frac{(1+a)^2}{1+a^3} fC\begin{bmatrix}1-a & a & -1\\ -1 & 1-a & a\\ a & -1 & 1-a\end{bmatrix}$	$2fC\begin{bmatrix}0 & 1 & -1\\ -1 & 0 & 1\\ 1 & -1 & 0\end{bmatrix}$	

*Normalized by I_2 of the GRSCC

The different modes listed for the GRSCC and GSwRC are distinguished by the number of rows in $\boldsymbol{\Psi}$ and the populated values. As seen by Table XI, when $a \rightarrow 1$, the solution for $\mathbf{Y}$, and therefore the current handling capability of the converter differs only in magnitude, that is, a constant gain value (listed in the last column) describes the current handling capability of each mode at f_n when compared to the basic GRSCC (f_n depends on N for each mode). An overview of the non-ideal case of $\mathbf{Y}$ enables identifying the impact of a on performance: a converter performs better if the attenuation factor a has a significant positive contribution to the cross-admittances and a weak contribution to self-admittances.

For example, the current-handling capability of the GRSCC operating at a five-state mode is ideally 20% higher than a three-state mode for the same conditions, regardless of the output voltage. This, however, is not the case if losses are considered. In both cases, the output current is affected by all voltages through Y_{21} and Y_{22}, but for the five-state mode, Y_{22} is identified to be larger, at least by a factor of two. Fig. 78 shows the effect of V_2 on I_2 for switched-resonator converters having moderate attenuation of

$a = 0.85$ (equivalent to a quality-factor of $Q \approx 10$). It can be observed that in the presence of losses, the current-handling capability improves marginally. The minor improvement that is observed occurs at regions where the output voltage is low, therefore parallel output losses (represented by Y_{22}^{-1}) have less impact, and the improvement is due to a positive effect of a on Y_{21}. However, parallel losses linearly increase with the output voltage and have a severe impact on the output current. It is concluded from Fig. 78 that for a losses case of $a \leq 0.85$ (Q<10) there is no significant value in using a five-state mode for the GRSCC or mode-a in the GSwRC above unity-gain.

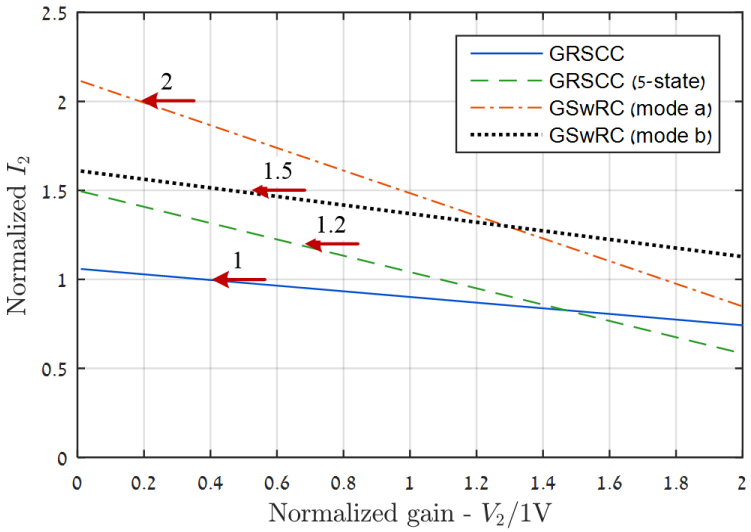


Fig. 78 The effect of the conversion ratio on I_2 on the GRSCC and GswRC. Normalized values for I_2, the arrows mark the currents' values for the ideal derivation.

5.3.5 Efficiency analysis

Following the model derived in the previous section, in which the average currents for each state have been extracted, it is now possible to formulate, in closed form, the expression for efficiency for any given multiport switched-resonator configuration. The model also enables identifying the contribution of losses in every state and quantifying the overall system efficiency. Without losing generality, it is assumed in this study that since a switched-resonator converter operates under zero current switching (ZCS), the primary contributor to the losses originates from the conduction path in every state. The general expression for the efficiency of the converter is expressed by the losses P_{loss} and the power at the output (load-side) ports P_{out}, that is:

$$\eta = \left(1 + \frac{P_{loss}}{P_{out}}\right)^{-1} \tag{81}$$

where P_{loss} is determined by summing the individual losses created in each state. These can be expressed as a function of the rms currents $I_{C,n,rms}$, through the conduction path resistance R in every state as:

$$P_{loss} = R\sum_{n=1}^{N} {I_{C,n,rms}}^2 \ , \tag{82}$$

where R is assumed here identical for all states for compact phrasing of the equations and without loss of generality. $I_{C,n,rms}$ can be analytically derived from the average state-current G_n by approximating to sine-wave current:

$${I_{C,n,rms}}^2 \approx \frac{\pi^2}{8\,fT_{state}} {G_n}^2 \ . \tag{83}$$

The total power dissipation can then be rewritten as:

$$P_{loss} \approx \frac{-\ln(a)}{4\,fC} \sum_{n=1}^{N} {G_n}^2 \tag{84}$$

In a multiport environment, P_{out} is determined by summing power *delivered* by the physical ports, that is:

$$P_{out} = - \sum_{k\in\{1,\ldots,\mathrm{K}\}\forall V_k I_k<0} V_k I_k \tag{85}$$

A. Two-port converter (K = 2)

In the most common case of a converter having a single-source and a single load ($K = 2$), the expression of (84) can be rewritten in a general form, extracting the basic parameters which from G_n (72):

$$P_{loss}\big|_{K=2} = BfCV_1V_2\left(\alpha A^{-1} + \beta A - \gamma\right), \quad A = \frac{V_2}{V_1}, \quad B = \frac{-\ln(a)}{4} \tag{86}$$

where the constants $\{\alpha, \beta, \gamma\} = f(a)$ are mode-dependent weighting-factors for V_1 and V_2 which are derived from $\sum_{n=1}^{N} {G_n}^2$ in (82), A represents the conversion ratio. Similarly for P_{out}:

$$P_{out}\big|_{K=2} = -P_2 = -fCV_1V_2\left(y_{21} + y_{22}A\right), \quad y_{21} = \frac{Y_{21}}{fC}, \ y_{22} = \frac{Y_{22}}{fC} \ . \tag{87}$$

Similarly to $\{\alpha, \beta, \gamma\}$, the constants $\{\ y_{21},\ y_{22}\} = f(a)$ are mode-dependent weighting-factors. It should be noted that $(y_{21} + y_{22}A) < 0$, since power exits the port. y_{21}, which represents delivered current, is negative, while y_{22}, which represents losses, is positive. Substituting (86) and (87) in (81) yields:

$$\eta\big|_{K=2} = \left[1 + B\frac{\left(\alpha A^{-1} + \beta A - \gamma\right)}{-\left(y_{21} + y_{22}A\right)}\right]^{-1} . \tag{88}$$

As demonstrated previously in Section 5.2 and further verified and categorized in the experiments in the next subsection, negligibly small losses can be assumed, so that idealized values of the currents are obtained in order to extract the factors of the admittance matrix **Y,** while losses are still considered for conduction loss derivation in (82). This allows (88) to be simplified to:

$$\eta\big|_{K=2,a\to 1} = \left[1 + \frac{\ln(a)}{-4y_{21}}\left(\alpha A^{-1} + \beta A - \gamma\right)\right]^{-1} . \tag{89}$$

It can be seen from (89) and (88) that regardless of the attenuation, *the efficiency of a switched-resonator converter depends on the conversion ratio alone,* which is in agreement with the findings in Chapter 2. This means that loading current does not impact the efficiency when the output voltage is regulated. This further verifies the model configuration of Fig. 76 which illustrates parallel losses, affected only by direct voltage.

Taking the derivative of (89) and equating to zero yields the conversion ratio at which the peak efficiency can be achieved, that is:

$$A_{optimal}\big|_{K=2,a\to 1} = A\big|_{\max(\eta)} = \sqrt{\frac{\alpha}{\beta}} . \tag{90}$$

A similar derivation can be conducted on (88), though the result is significantly more complex in terms of the number of coefficients. For simplification, in the case of step-down gains ($A<1$), by assuming that $\{\alpha, \beta, \gamma, y_{21,} 10{\cdot}y_{22}\}$ follow the same order of magnitude, (88) can be approximated to:

$$A_{optimal}\big|_{K=2,A<1} \sim \sqrt{\frac{\alpha}{\beta - y_{22}/y_{21}\gamma}} . \tag{91}$$

This implies that, assuming operation under ZCS, and assuming that the resonator is switched periodically at half-resonance, the location of the peak efficiency point is a weighted-function of the ports' voltages and can be adjusted by the applied voltage on the resonator, i.e. by modifying the switching sequence. This provides a new design direction and guideline for SCCs and their derivatives enabling to shift the rigid optimal target voltage by manipulating the applied voltage on the energy-transfer cell.

In order to determine the impact of using a simplified efficiency estimation of (89), efficiencies have been derived from (88) and compared to those derived from (89) for

the same conditions. Results in Fig. 79 have been obtained for the GRSCC and GSwRC examples listed in Table XI, considering moderate state attenuation of $a = 0.85$ ($Q \approx 10$). As can be seen in Fig. 79, for the area of interest, i.e. in the region of the optimal gain (peak efficiency) for lower gains, very good agreement is obtained between the full expression and the approximation. This means that the simplified efficiency expression of (89) which was used for the analysis in Chapter 3 provides a good efficiency estimate for this range. However, above the optimal conversion point, where parallel losses are more dominant, inclusion of the attenuation is essential for realistic efficiency modelling.

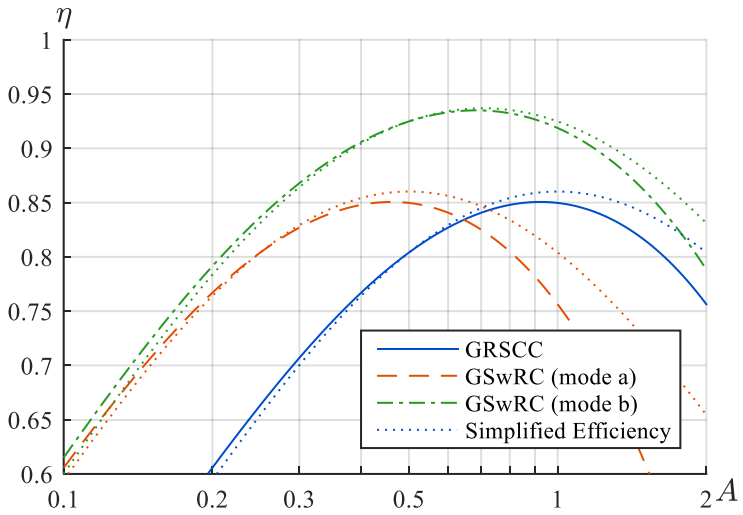


Fig. 79 Comparison between the full and simplified efficiency estimation for the GRSCC and GSwRC.

5.3.6 Experimental validation

To validate the theoretical analysis for switched-resonator converters and to demonstrate the contribution of loss inclusion to the accuracy of the theoretical model, a GSwRC prototype [see Fig. 77(c)] has been built and tested, designed with moderate peak efficiencies ranging between 80% and 90%, depending on the selected mode of operation. The prototype uses N-type MOSFETs (Siliconix SIA436DJ) driven by low-side drivers (Maxim MAX17601). Switches Q_{2a} and Q_{2b} are implemented by a back-to-back configuration consisting of two MOSFETs, to block the reverse-conducting diode. The drivers are supplied with 7V to allow all switches to conduct properly, since the transistors refer to different dc potentials ranging up to 5V for Q_{1a} and Q_{1b}. The measured resistance in the conduction path for all states ranges between 60-70 mΩ, creating an approximately 2% attenuation variance between all states, which allows *a*

to be considered constant. Further design parameters are provided in Table XII. The prototype has been tested for three modes of operation: a bridge variation of the GRSCC listed in Table XI (here $\psi_{12} = -1$ instead of 0), the two modes of the GSwRC are listed in Table XI as well.

TABLE XII EXPERIMENTAL DESIGN PARAMETERS

Parameter		*Value*
Loop resistance	R	65 mΩ
Resonator inductance	L	40 nH
Resonator capacitance	C	220 nF
State attenuation	a	0.79
Loop quality factor	Q	6.6
State period	T_{state}	295 ns
3-state frequency	$f_{n,(N=3)}$	1.13 MHz
4-state frequency	$f_{n,(N=4)}$	0.85 MHz
Peak efficiency	η_{max}	90%
Input voltage	V_1	5 V
Max. output current	$I_{2,max}$	5A

Fig. 80 and Fig. 81 compare the ideal, expected and measured output current and efficiency for the examined modes of operation. The results show excellent agreement with the theoretical prediction from Table XI. Measurements for I_2 in Fig. 80 validate the claim that the cross-admittance coefficient Y_{21} benefits from the presence of significant attenuation, as at low gains of A=0.2 it is observed that I_2 is higher than the ideal case. Current sourcing capability drops significantly at higher output levels, in correlation to the presence of parallel losses from Y_{22}. In Fig. 81, efficiency measurements for gains below the peak efficiency are in good agreement with the ideal and expected efficiency predictions, validating the claim that in that range the simplified efficiency estimation of (89) provides adequate prediction. At higher gains, the results follow the full efficiency estimation, deviating from the simplified curve.

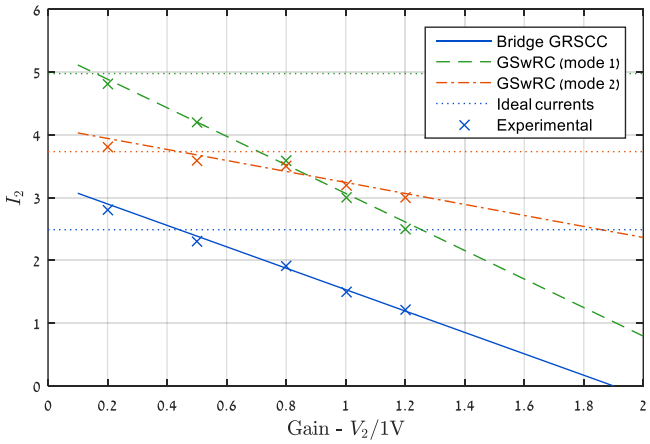


Fig. 80 Experimental verification for the predicted impact of the output voltage on I_2.

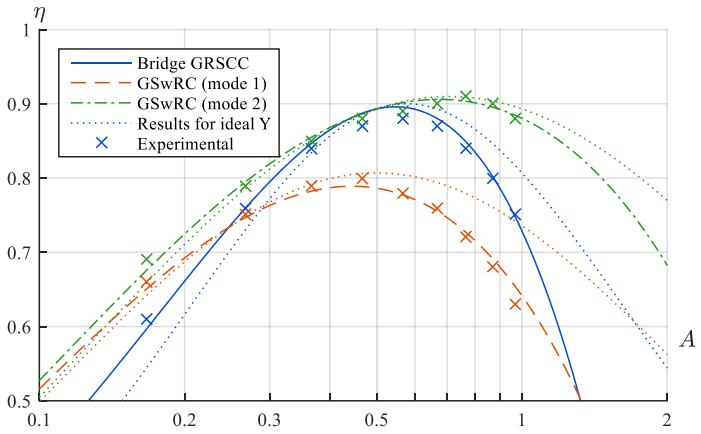


Fig. 81 Experimental verification of the accuracy of the efficiency prediction of the derived model

CHAPTER 6: Conclusion

Efficient voltage conversion over a wide and continuous range using SC technology alone – A new gyrator resonant switched capacitor converter (GRSCC) topology has been introduced. The converter demonstrates losses characteristics that are, to a large extent, independent of the voltage gain, which is a unique feature among the switched capacitor based converters. This attribute, resided thus far only in switched-inductor converters, has been fully realized by RSCC technology. The converter exhibits a gyrator-like behavior, which is an advantage in current sourcing applications.

Analysis of the converter's characteristics provides the fundamental static relationships for the gyration and conversion ratios and efficiency estimation. With the addition of control features, the converter operation resembles discontinuous-mode PDM of any switched-inductor converter, and may be treated as such. Efficiency comparison with buck-boost configuration demonstrates the GRSCC superiority when operating at higher switching frequencies within and beyond the target range. The unique advantage of the new GRSCC is that it merges the virtues of two worlds: wide operation range at high efficiency (from switched-inductor converters) and reduced volume (similarly to SCC).

Small and efficient voltage-regulator with ideal transient-response based on a GRSCC – A new, small and efficient voltage regulator based on resonant switched capacitor technology has been developed. Regulation is achieved via simple pulse density modulation control scheme. The demonstrated voltage regulator exhibits an ideal response to load and line transients, i.e. with zero over/undershoot over the full operation range, as well as a wide efficiency profile over a large range of voltage gain and power levels.

Power density analysis reveals that when considering a conservative design the required area product (volume) of the magnetic element is within the range of its comparable alternatives (e.g. a buck-boost converter). However due to the significantly lower inductance value that is required for the operation of the GRSCC, a ferrite-less design is feasible, which increases the power density of the voltage regulator by at least one-order of magnitude. Size estimation of the output capacitor reveals that the inherently continuous steady-state operation significantly reduces the required capacitance value and size.

Combining the benefits of the relatively simple converter design, the virtually no-effort approach for voltage regulation presented in the thesis, and the high power

density of the passive components, the GRSCC-based voltage regulator can be considered as an attractive candidate for voltage regulation applications that require a high response rate. Furthermore, the possibility of a ferrite-less magnetic design increases the power density of the converter, and allows the power supply to be fully integrated (omitting the output filter) on a chip. It should also be noted that in comparison to other switched-inductor ripple-based solutions, the presented approach is comparable in terms of efficiency and component count, in particular when step-up/down or bi-directional capabilities are required.

Increase high-frequency transient performance of voltage-regulation modules – A voltage regulator module with improved loading and unloading transient response has been presented. The improvement has been achieved by the addition of a load-side auxiliary circuit that comprises three interleaved GRSCCs. This VRM has the potential to be space conserving and cost-effective when implemented as an IC design. The output capacitance is significantly reduced (at the cost of small additional semiconductors) and does not require ferromagnetic elements beyond the main buck inductor.

The experimental results exemplify the performance of the design for both loading and unloading events, reducing output overshoots by up to 390% and transient time by up to 175% compared to TOC, without affecting the input side. In particular, for the relatively high conversion ratio case, significant improvement has been demonstrated in the response to an unloading event, compensating for the moderate current slew-rate of the buck inductor. The hybrid-VRM operates autonomously with reduced circuit complexity, i.e., no additional current-sense circuitry or pre-transient information is required.

Efficient rapid-adaptive voltage scaling system for volume-sensitive low-power envelope tracking applications – A new, rapid adaptive voltage scaling envelope tracking system based on the GRSCC has been presented. The GRSCC provides a natural current-source which facilitates tight tracking under limited design considerations. Combined with a newly developed non-linear controller, the system minimizes the tracking mismatch and significantly reduces losses related to further shape adjustments.

The envelope tracking methodology of this study improves the transmission-system efficiency by more than 200% , while using a switching frequency of less than 2.5 times higher than the envelope signal. Combined with the topology benefits, the volume-

saving simple GRSCC voltage regulation scheme presents an attractive alternative to the switch-inductor converters, in particular in area-sensitive applications, and establishes the foundations for better power delivery concepts for envelope tracking applications.

Extending the capabilities of efficient capacitor-based conversion beyond the GRSCC – A new switched-resonant converter with numerous modes of operation and demonstrated efficiency characteristics that exhibit a broad peak over an extended voltage gain-range, has been presented. The capability to shape the efficiency characteristics of the converter has been demonstrated through ten modes of operation. This attribute, present thus far only in multi-target voltage converters that employ several energy-transfer cells, is realized in this research by a single energy transfer cell.

A generalized procedure to describe switched-resonant or resonant-type switched-capacitor converters having multiple operation-modes as two-port networks has been described to evaluate and quantify the characteristics of such converters in various conditions. Combining the benefits of the relatively simple converter design and the need for a single energy-transfer cell to allow continuous high-efficiency conversion ratios, the GRSCC-based voltage regulator can be considered an attractive candidate for voltage regulation applications that require high response rate. Furthermore, the possibility of multiple operation modes allows flexibility in the converter design and further size reduction of the resonator.

Generalized behavioral model and efficiency analysis for switched-resonator converters - A new systematic method for accurately modelling the performance of switched-resonator converters, and which takes into consideration the full impact of conduction losses allows precise performance comparison between various types of switched-resonator converters given the operating conditions.

A multiport framework with switching-state representation is provided to assist development of behavioral models for converters with complex switching schemes. This fundamental theory is demonstrated with respect switched-resonator converters, but is not limited to them; it is applicable to any converter with multiple switching-states and/or multiple physical connections to be analyzed as multiport, facilitating behavioral modelling by conventional tools.

An accurate efficiency analysis has been conducted as well, revised from the simplified expression initially introduced. It is determined that at medium to large step-down conversion ratios, a simplified efficiency model provides similar results to the

full derivation, whereas at unity gain and above, the simplified model provides optimistic predictions, deviating from true values.

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תכנון ובקרה עבור ייצוב באמצעות ממירי קבלים מתמתגים תהודתיים המתנהגים כג'יראטור

מחקר לשם מילוי חלקי של הדרישות לקבלת תואר "דוקטור לפילוסופיה"

מאת

אלון סרברה

הוגש לסינאט אוניברסיטת בן גוריון בנגב

כ"ב בתשרי התשע"ט **14.10.2018**

באר-שבע

תכנון ובקרה עבור ייצוב באמצעות ממירי קבלים מתמתגים תהודתיים המתנהגים כג'יראטור

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אישור המנחה: פרופ' מור מרדכי פרץ Mor M. Peretz

אישור דיקן בית הספר ללימודי מחקר מתקדמים ע"ש קרייטמן: פרופ' דודי בר-צבי _____

כ"ב בתשרי התשע"ט **14.10.2018**

באר-שבע

העבודה נעשתה בהדרכת:

פרופ׳ מור מרדכי פרץ

המרכז לאלקטרוניקת הספק ומעגלים מוכללים – PEMIC

במחלקה להנדסת חשמל ומחשבים

הפקולטה להנדסה

הצהרת תלמיד המחקר עם הגשת עבודת הדוקטור לשיפוט

אני החתום מטה מצהיר/ה בזאת: (אנא סמן):

_✓_ חיברתי את חיבורי בעצמי, להוציא עזרת ההדרכה שקיבלתי מאת מנחה/ים.

_✓_ החומר המדעי הנכלל בעבודה זו הינו פרי מחקרי מתקופת היותי תלמיד/ת מחקר.

___ בעבודה נכלל חומר מחקרי שהוא פרי שיתוף עם אחרים, למעט עזרה טכנית הנהוגה בעבודה ניסיונית. לפי כך מצורפת בזאת הצהרה על תרומתי ותרומת שותפי למחקר, שאושרה על ידם ומוגשת בהסכמתם.

תאריך 14.10.18 שם התלמיד/ה אלון סרברה חתימה _____

תקציר

Abstract (Hebrew)

בעקבות פריחתם של מוצרי אלקטרוניקה ניידים, נעשים מאמצי מחקר ופיתוח ללא הרף על מנת להשיג מקורות הספק קלים יותר, ממוזערים יותר, וחסכוניים באנרגיה. מפתחיהם של ספקי כח מודרניים מצליחים כיום להגיע למימדים יחסית קטנים מבלי להתפשר משמעותית בנצילות האנרגטית, זאת על ידי שימוש ברכיבים משופרים ובשיטות תכנון המשלבות את הגמישות שמאפשרת בקרה דיגיטלית. אף על פי כן, ככל שהמגמה נמשכת הדרישות נעשות מאתגרות יותר: בקרת מוצא הדוקה יותר, זמני תגובה מהירים יותר בעבור שינויים בעומס ובכניסה, ונפח קטן יותר מהווים נדבך משמעותי בשיקולי התכנון של מערכות לניהול אנרגיה, ומהווים צוואר-בקבוק בהתקדמות התכנולוגיה הנוכחית.

עבור יישומים בהם יש חשיבות לנפח קטן, ממירי קבלים מתמתגים (SCC) מודרניים הפכו לאלטרנטיבה אטרקטיבית לפתרונות המבוססים על ממירי סלילים מתמתגים, כאשר ממירי SCC מאפשרים נצילות גבוהה וכלכליים למימוש. חסרון עיקרי הקיים במשפחת ממירי ה- SCC הוא שהנצילות שלהם קשורה באופן ישיר ליחס בין מתח המוצא של הממיר למתח המטרה המתוכנן (מתח המוצא ללא עומס, בחוג פתוח), ללא תלות ביישום של שיטת ייצוב המתח – וזאת בדומה למייצבים ליניאריים. התלות הליניארית של ה-SCC ביחס ההמרה נובעת מהיחס הקשיח בין סך המטען הנכנס והיוצא מהממיר.

קיימים מספר פתרונות אשר מפחיתים את הגזירה הזו על ידי יצירת מספר מתחי מטרה באמצעות שימוש במספר תאי קבלים-מתמתגים. ניתן בשיטה זו להגדיל את טווח הפעולה האפקטיבי של הממיר במחיר של הגדלת סיבוכיות שיטת החיבור של תאי הקבלים המתמתגים. גם במקרה זה, למרות השימוש במספר תאי קבלים-מתמתגים אופין הנצילות שומר על אופי בדיד.

ניתן ליישם ייצוב מתח מדויק במספר שיטות לשם השגת המוצא הדרוש: באמצעות שינוי פרמטרים ב-SCC, באמצעות הוספת דרגת ייצוב ייעודית, או באמצעות שילוב ממיר סלילים מתמתגים במערכת ויצירת טופולוגיה היברידית. לשיטת המרה חדשה יהיה ייתרון על השיטות הקיימות באם תצליח לנכס את המאפיינים והייתרונות של משפחת ה-SCC וגם לאפשר המרת הספק נצילה באופן רציף, בדומה לנצילות של פתרונות מבוססי סלילים מתמתגים.

מטרת מחקר זה היא להציג ולפרט שיטה רחבה לניהול אנרגיה עם שינוע נציל של הספק וייצוב רציף של מתח, באמצעות טכנולוגיית קבלים מתמתגים, למגוון רחב של יישומים. ההמרה היעילה מתבצעת ללא מגנטיקה או עם מגנטיקה מצומצמת משמעותית, וזאת באמצעות ניצול אלמנטים קיבוליים ככלי לשינוע האנרגיה. שיטה זו מאפשרת צפיפות הספק גבוהה ומהווה את המפתח לאינטגרציה של אלקטרוניקת הספק.

ממיר קבלים מתמתגים רזוננטי המתנהג כג'יראטור (GRSCC) מוצג לראשונה במחקר זה, עם פרופיל נצילות גבוהה המנותק מהתלות הליניארית המאפיינת את משפחת ה- SCC. מייצב מתח קומפקטי המבוסס על ה-GRSCC מוצג בעבודה זו, אשר מתאפיין בתגובה מסדר-אפס לשינויים מצד העומס ומאפשר מזעור משמעותי של האלמנט המגנטי כמו גם של קבלי הסינון בממיר. מודול מייצב מתח (VRM) מוצג בעבודה זו, אשר משלב ממיר סלילים מתמתגים נציל ביותר יחד עם GRSCC המחובר לצד העומס על מנת לסייע

בזמן אירועים של שינויי העמסה. ה VRM שנוצר מתאפיין בביצועים דינמיים משופרים באירועי העמסה כמו גם בארועי ירידת עומס, בעוד התכנון שומר על מבנה קומפקטי וקיבול מוצא מופחת.

ספק כח עוקב מעטפת מוצג בעבודה זו, אשר משפר את ביצועו של מודול משדר רדיו (RF), ומצמצם את נפחו הכללי. מימוש זה רותם את מאפייני הדו-כיווניות של ה- GRSCC, את התנהגותו כמקור זרם טבעי, ואת יכולת התגובה המיידית של הממיר, על מנת ליצור את המעטפת הדרושה להזנה לאספקת המגבר.

משפחה טופולוגית חדשה של GRSCC מוצגת לראשונה בעבודה זו ומנותחת בפירוט. הגרסא המורחבת של ה GRSCC מאפשרת מצבי פעולה מתקדמים, מה שמאפשר לעצב את מאפייני ההספק של הממיר כך ששיא הנצילות ימוקם ביחסי המרה שונים. מודל התנהגותי כוללני פותח בעבודה זו עבור ממירי קבלים במיתוג רך וממירים רזוננטיים בעלי יציאות וכניסות מרובות. המודל מגדיר מסגרת מערכתית לייצוג ממירים עם ריבוי מצבי-מיתוג כרשת אימפדנסים בתצורת Multiport. המודל כולל בפרט את השפעת ההפסדים על נצילות הממיר כמו גם על הביצועים והתכונות האופייניות שלו.

עבודת תיזה זו מסמלת קפיצת מדרגה ביכולות עיבוד הספק על-ידי טכנולוגיית קבלים מתמתגים, מכיוון שהיא מספקת לראשונה שיטה הבנתית למימוש ממירי קבלים מתמתגים עם נצילות גבוהה על גבי תחום רחב ורציף של טווחי מתח. ניתוח תיאורטי חדשני מספק יסודות חדשים ובוחן מחדש את הדרך בה ממירי קבלים מתמתגים מתוכננים ומנותחים. עבודת התיזה מספקת כר פורה ליישומים חדשים, מה שהודגם על ידי יישומי ייצוב מתח ומעקב מעטפת עם תכונות חסרות תקדים כגון droop-elimination, עיצוב עקומת הנצילות של ממיר, ועיצוב רציף של מעטפת אות.

תוצאות המחקר ל PHD מסכמות תרומה אקדמית של שישה מאמרי עיתון [6]-[1] אשר הוגשו ופורסמו ב- IEEE Transactions on Power Electronics (TPEL) וב- Journal of Emerging and Selected Topics in Power Electronics (JESTPE); שישה מאמרים נוספים בכנסים מובילים -[7] [12] – אשר כולם הוצגו ב- IEEE Applied Power Electronics Conference (APEC), וב- Energy Conversion Conference and exposition (ECCE). תוצאות המאמרים זכו פרסי ייחוד יוקרתיים הכוללים פרס "TPEL 2nd best paper award" לשנת 2017 [4], פרס המצגת הטובה ביותר ב APEC [11], ופרס וולף לתלמידי מחקר. תוצרי תכנית המחקר כבר תרמו למספר פרסומים נוספים בתחומים של בקרה דיגיטלית [14] ,[13] ובאינטגרציה לצ'יפ [16] ,[15], המתבססים על ה GRSCC כדרגת ההספק.

מילות מפתח – אלקטרוניקת הספק; מודול מייצב מתח; ממיר קבלים מתמתגים רזוננטי; ג'יראטור; בקרה דיגיטלית לאלקטרוניקת הספק;