Very High Conversion Ratio Power Management Systems

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE DEGREE OF "DOCTOR OF PHILOSOPHY"

By: Or Kirshenboim

Submitted to the Senate of Ben-Gurion University of the Negev

Date 12.09.19

Be'er Sheva

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Approved by the advisor: 

Approved by the Dean of the Kreitman School of Advanced Graduate Studies_____

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This work was carried out under the supervision of

Prof. Mor M. Peretz

Department: Electrical and Computers Engineering

Faculty: Engineering Sciences

September 2019

Research-Student's Affidavit when Submitting the Doctoral Thesis for Judgment

I, Or Kirshenboim, whose signature appears below, hereby declare that

(Please mark the appropriate statements):

V I have written this Thesis by myself, except for the help and guidance offered by my Thesis Advisors.

V The scientific materials included in this Thesis are products of my own research, culled from the period during which I was a research student.

V This Thesis incorporates research materials produced in cooperation with others, excluding the technical help commonly received during experimental work. Therefore, I am attaching another affidavit stating the contributions made by myself and the other participants in this research, which has been approved by them and submitted with their approval.

Date: 12.09.2019 Student's name: Or Kirshenboim Signature: 

מערכות ניהול הספק בעלות יחסי המרה גבוהים מאוד

מחקר לשם מילוי חלקי של הדרישות לקבלת תואר "דוקטור לפילוסופיה"

מאת:

אור קירשנבוים

הוגש לסינאט אוניברסיטת בן גוריון בנגב

תארי עברי: י"ב באלול תשע"ט **תאריך לועזי: 12.09.19**

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אישור המנחה: _____

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באר שבע

העבודה נעשתה בהדרכת:

פרופ' מור פרץ

במחלקה להנדסת חשמל ומחשבים

בפקולטה למדעי ההנדסה

September 2019

<u>הצהרת תלמיד המחקר עם הגשת עבודת הדוקטור לשיפוט</u>

אני החתום מטה מצהיר/ה בזאת: (אנא סמן):

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V **בעבודה נכלל חומר מחקרי שהוא פרי שיתוף עם אחרים, למעט עזרה טכנית הנהוגה בעבודה ניסיונית. לפי כך מצורפת בזאת הצהרה על תרומתי ותרומת שותפי למחקר, שאושרה על ידם ומוגשת בהסכמתם.**

תאריך: <u>12.09.2019</u> שם התלמיד/ה: <u>אור קירשנבוים</u> חתימה: 

∞

Dedicated to my wife, Michal, who encouraged me to aspire to heights and ignore any limitations that get in the way, since all limitations are simply waiting there for someone to break through them.

∞

September 2019

תקציר

עם התקדמות הטכנולוגיה של רכיבים לניהול הספק, ממירי הספק ביחס המרה גבוה מאוד מתחילים להיות אטרקטיביים כתחליף לממירים מרובי דרגות שהיו מובילים בעבר. הגישה של ממירים מרובי דרגות מבוססת על שרשור של מספר ממירים בודדים כאשר כל אחד מהם הוא בעל יחס המרה בינוני. בנוסף, לכל ממירי בשרשרת יש מטרות שונות הנעות בין עמידה בדרישות מקור ההספק, כמו למשל ביישומים של תיקום גורם הספק, ועד לעמידה בדרישות של העומס במובנים של אספקת זרם ושינויי מתח מוגבלים. בניגוד לכך, ישנם גם יישומים בהם המטרה היחידה היא להשיג את יחס ההמרה הגבוה מאוד, ללא דרישות מיוחדות נוספות. עם זאת, מטרה אחת שמשותפת לכלל הממירים בשרשרת היא לשמור על נצילות גבוהה שמתורגמת להפחתה של הפסדי הספק וכתוצאה מכך מערכות בעלות צפיפות הספק גבוהה. כאשר נעשה שימוש בגישה של ריבוי דרגות הנצילות נפגעת עקב ריבוי דרגות עיבוד ההספק, משום שלכל דרגת עיבוד הספק יש נצילות מוגבלת. עם עלייה מתמדת במספר היישומים הצורכים כמות אנרגיה גבוהה ואשר דורשים יחס המרה גבוה מאוד, למשל חוות שרתים גדולות, להשפעות של נצילות פחותה יש השלכות חמורות גם על עלויות וגם על השפעות סביבתיות כגון זיהום אויר בעקבות צריכת האנרגיה הגבוהה.

מטרת מחקר זה היא לחקור את האתגרים של ממירים ביחס המרה גבוה מאוד ולפתח שיטה חדשה לעיבוד הספק שמתאימה למערכות ניהול הספק בעלות יחס המרה גבוה מאוד. בנוסף, תתבצע השוואה של הגישות לפיתוח של מערכות מסוג זה ביחד עם חקר ביצועים. הצפי הוא כי שימוש בגישה החדשה יאפשר החלפה של שתי דרגות עיבוד הספק (או יותר) בדרגת עיבוד הספק בודדת אשר משפרת את הביצועים ואת הנצילות של הדרגות אותן היא מחליפה. עיבוד ההספק מתבצע ע"י שימוש בשיטת multi-level בדרגת עיבוד הספק משולבת אחת על מנת לקבל יכולות של יחס המרה גבוה מאוד. נוסף על כך, השיטה מאופיינת בנצילות גבוהה, תגובה דינאמית טובה וגודל קטן. מטרה נוספת היא לפתח את כל הכלים הנלווים לשימוש בממירים החדשים שיפותחו. אלו יכללו מידול ואנליזה של הממירים, פיתוח שיטות בקר ובקרים, פתרון בעיות מימוש וביצוע אנליזה להערכת הפסדי ההספק והנצילות. ידע זה יתורגם לקווים מנחים לתכנון ומימוש של ממירים בעלי בקרה חכמה בעתיד. התרומות הפוטנציאליות של מחקר זה טמונות באספקה של גישה נוחה וטבעית לתכנון ובקרה של מערכות עיבוד הספק בעלות יחס המרה גבוה מאוד.

עבודת התזה מוגשת כאסופת מאמרים אשר מורכבת בעיקרה מ-3 מאמרים אשר פורסמו בז'ורנל המקצועי IEEE Transactions on Power Electronics. שלושת המאמרים ביחד מציגים שתי טופולוגיות ממירים חדשות בעלות יחס המרה גבוה במיוחד ושיטת מידול ובקרה חדשנית עבור ממירים אלו ודומיהם. הבקרים החדשים שפותחו, ביחד עם תכונותיהן של הממירים, מציגים את הביצועים הגבוהים אליהם ניתן להגיע בעזרת שימוש בממירי דרגה אחת בעלי יחס המרה גבוה במיוחד.

Abstract

With the advancement of power components, very high conversion ratio power converters are now starting to become attractive as a replacement for multi-stage power converters that have been predominant in previous years. Typically, the multi-stage approach is based on cascading a number of power converters, each one with a moderate conversion ratio. In addition, each of the power converters has different objectives, ranging from satisfying the power source requirements, i.e. as in power factor correction applications, up to satisfying the load requirements in terms of load current and limited output voltage deviation. In contrast, there are applications where the objective is just to achieve a very high conversion ratio, without any special additional requirement. However, one objective that is common for all the converters in the chain is to maintain a high efficiency, which translates to lower power loss and, consequently, systems with higher power density. Using a multi-stage approach the efficiency is impacted due to the large number of stages that process the power, since each one has limited efficiency. With the rapidly increasing number of high power-consuming applications that require very high voltage conversion ratio, e.g. big datacenters, the effects of decreased efficiency have tremendous implications on cost of these systems as well as environmental pollution due to increased energy consumption.

The objective of this research is to explore the very high conversion ratio challenges and to develop a new approach for power processing that is suitable for very high conversion ratio power management systems. In addition, a comparison of the different approaches for developing this kind of systems is performed, along with a performance analysis. It is expected that, using the new approach, two (or more) power conversion stages can be replaced with a new single power conversion stage that will improve the efficiency and performance of the replaced stages. The power processing is performed by using the multi-level method in a single stage hybrid power conversion to achieve very high conversion ratio capabilities. It also has high efficiency, good dynamic performance and low volume. Another objective is to develop the surrounding tools for using the new converters are developed. These will include modeling and analysis, development of control methods and controllers, solving implementation issues and perform a power loss and efficiency analyses. This knowledge will then be translated into design guidelines for modules construction and realization of efficient control algorithms in the future. The potential

contributions of the study lie in providing a natural and streamlined approach for the design and control of very high conversion ratio power management systems.

This thesis is submitted as a paper collection and is comprised of 3 publications in the reputable journal IEEE Transactions on Power Electronics. The three papers together provide two new different converter topologies with very high conversion ratio and an innovative modeling and control strategy for these new converters and their derivatives. The custom controllers that have been developed, along with the new converters' characteristics, provide an excellent demonstration of the performance that can be achieved with the single stage converter with the very high conversion ratio approach.

List of Publications and Thesis Overview

[1] **O. Kirshenboim** and M. M. Peretz, "High efficiency non-isolated converter with very-high step-down conversion ratio," *IEEE Trans. on Power Electron.*, vol. 32, no. 5, pp. 3683-3690, May. 2017. (IF 7.151; JCR 13/260; Q1). Link

[2] **O. Kirshenboim**, T. Vekslender, and M. M. Peretz, "Closed-loop design and time-optimal control for a series-capacitor buck converter," *IEEE Trans. on Power Electron.* (IF 7.151; JCR 13/260; Q1). – Early Access - Accepted Apr. 2018. Link

[3] **O. Kirshenboim** and M. M. Peretz, "Combined multi-level and two-phase interleaved LLC converter with enhanced power processing characteristics and natural current sharing," *IEEE Trans. on Power Electron.* vol. 33, no. 7, pp. 5613-5620, Jul. 2018. (IF 7.151; JCR 13/260; Q1). Link

In **the first paper [1]**, a new non-isolated converter topology with very-high step-down conversion ratio and high efficiency for high current low voltage point-of-load voltage regulator modules is introduced. Compared to a conventional two-phase buck converter, the new converter triples the effective duty-ratio and lowers the voltage stress of the transistors, significantly reducing the overall volume of the converter while maintaining high efficiency. The new converter is capable of delivering a high current to the output by two interleaved phases and further features an inherent current sharing to balance the load between the phases.

The **second paper [2]** explores the large-signal and small-signal dynamics of a series-capacitor (SC) buck-type converter, which is a derivation of the converter presented in the first paper [1], and introduces an optimal closed-loop control scheme to accommodate both the steady-state and transient modes. As opposed to a conventional buck converter, where time-optimal control is realized by a single on-off cycle, in the SC-buck topology there is a need to distribute the switching phases to satisfy the charge-balance of the series-capacitor. The new control method merges a voltage-mode controller for steady-state operation and a non-linear, state-plane based transient-mode controller for load transients.

The **third paper [3]** introduces a new two-phase interleaved flying-capacitor LLC converter topology with high output current applications. It is an implementation of the concept of using a flying-capacitor as in the first [1] and second [2] papers in order to obtain its characteristics in a resonant converter as well as PWM converters. Compared to a conventional two-phase LLC converter, the new converter adds a single capacitor that contributes to lower voltage stress on the primary side's switches, automatically balances

the current distribution between the phases and enhances the power processing capabilities. All the attractive features of LLC converters are preserved, such as zero-voltage switching on the primary side's MOSFETs, zero-current switching on the secondary side's power devices, narrow switching frequency range and simple design.

Acknowledgments

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I must not forget all the students here at the Center for Power Electronics and Mixed-Signal IC whose support and friendship meant so much:, Mr. Timur Vekslender, Mr. Yevgeny Bezdenezhnykh, Mr. Bar Halivli, Mr. Nadav Dahan, Mr. Tom Urkin, Mr. Guy Sovik, Mr. Alexander Mindel, Ms. Hagit Peretz, Mr. Aviel Mazuz and anyone that I have forgotten to mention by name.

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With great appreciation I thank my dear wife Michal, for her tremendous loving support, patience and care. I want to thank my parents and brothers for their support and care, and for their contribution, each in his area of expertise.

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1. Introduction

1.1. Very High Conversion Ratio Challenges

Very high conversion ratio in power converters has been an issue for many years. The difficulty of achieving very high conversion ratio occurs due to physical limitations of converters, where the main limitations are a consequence of the inherent power loss in the system. It also affects the power conversion efficiency, cost of the systems, implementation difficulties, the requirement for special components and many more. When aiming towards using traditional converters' topologies with very high conversion ratio, the desired output voltage cannot be achieved since the power loss cannot be compensated by the control variable. This issue occurs since the change in the control variable also increases the power loss, and therefore a converter has a limit in its input-to-output conversion ratio [1].

This limit can be modeled as depicted in Fig. 1.1. The represented voltage source is the target output voltage, which is a function of the input voltage and the duty-ratio, R represents the inherent losses of the converter that are not duty-ratio dependent (e.g. due to inductor DCR resistance and switching), $R(D)$ is to represent the duty-ratio dependent power loss (e.g. rms power loss of switches and diodes' reverse recovery) and R_L represents the load. It means that $R+R(D)$ represents the output resistance of the converter. To compensate for the voltage drop on the R and $R(D)$ so that the load's voltage will be the desired V_{out}, the controlled voltage source can be increased by changing the control variable D. However, changing D also changes $R(D)$ and the voltage drop on $R(D)$ is increased, and therefore there is a limit on the achievable V_{out}. In addition, it is obvious that this additional power loss also affects the power conversion efficiency and power density, which are among the main objectives in the design of present day's power converters. It should be pointed out that in very high conversion ratio converters the effect of $R(D)$ is much more significant compared to the case of moderate conversion ratio converters. A possible solution for lowering $R(D)$ is to optimize the converter's components so that $R(D)$ will be at minimum for a specific operating point. This optimization can have a huge impact on the converter's achievable conversion ratio and efficiency.

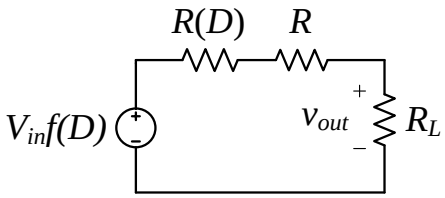

Fig. 1.1 Model of a converter's output resistance in terms of conversion ratio and duty-ratio dependent power loss.

Very high conversion ratio power conversion relates to many applications. Step-down applications with very high conversion ratios are very common, where the most common applications are low dc powered devices that are connected to the power grid. Here, the converter has to convert the 220V rectified ac voltage to a 1V~5V dc voltage. In addition, recently a new demand rose from the datacenters industry for converters that can efficiently convert a 48V dc input voltage to around 1V dc output voltage (a CPU supply voltage) in order to remove one power conversion stage in the power path of processors. The step-up applications relate to energy harvesting from low voltage renewable energy sources, e.g. photovoltaic panels [2], fuel cells [3] and thermoelectric generators [4]. Other examples for step-up applications that require very high conversion ratio with high voltage are x-ray [5], and plasma generators [6].

In some applications, if not all, the power conversion system must satisfy both the load and source demands: the load may change its current while its voltage must not deviate and the converter must satisfy electro-magnetic interference (EMI) standards for the source in order not to inject noise to back to the power source. For example, in a single panel photovoltaic energy harvesting the input voltage and current can deviate and while the voltage at the input of the inverter (the output of the power converter) should be high enough so that the inverter will operate with high efficiency. Therefore, the reason for the necessity of a high conversion ratio converter is to satisfy the efficiency requirement of the inverter. As a consequence, the converter must be efficient enough, otherwise the objective of the system will not be fulfilled.

Typically, to achieve a very high conversion ratio, two or more power conversion stages were connected in series, each with a moderate conversion ratio. The issue with this is that every stage affects the overall efficiency and complicating the whole power system design. In the context of power electronics, the issue of high conversion ratio converters starts to become a challenge as the number of loads and applications is constantly increasing. The

usage of modern power management platforms and point-of-load (PoL) is only at its beginning and expected to increase significantly over the next years.

1.1.1. Non-Isolated Topologies

1.1.1.1. Buck conveter

The most common topology for a converter is the buck converter. The buck converter, as any of the conventional topologies, is limited in its voltage conversion ratio due to the very short on-time of the MOSFETs required for high voltage conversion ratio. The short on-time presents limitations for both efficiency and controllers. Because of its simple structure and very low cost, the buck converter dominates the power supply market in the telecom and datacom fields [8].

The most serious problem of the synchronous buck converter operating with very small duty-ratio is its low efficiency, especially for high-frequency applications. During the very short time that the high-side MOSFET is on a large amount of energy is processed, which causes high power losses. In addition, the switching current of the MOSFETs equals the large output current, so the switching loss is significant. Also, high-voltage MOSFETs need to be used for the low-side MOSFET (the synchronous rectifier) in order to block the high input voltage, even though the output voltage is very low. Normally, high-voltage MOSFETs mean larger on-resistance and worse body-diode performance. Both the low-side MOSFET conduction loss and its body-diode reverse-recovery loss are dramatically increased.

The efficiency is severely impacted for several reasons. Due to the high current rms value of the high-side MOSFET it must have low on resistance, which increases its capacitances. In addition, the gate drive effort is higher due to the Miller plateau and there is a high voltage swing on the high-side MOSFET during turn on and turn off, which produces long overlap time of current and voltage and as a consequence higher power loss. The low-side MOSFET is problematic too since almost all the load current is flowing through it and therefore it must have extremely low on resistance – which is a problem in high voltage-rated MOSFETs due to large silicon area and high capacitances. Additional challenge that will be discussed later is the controller regulation.

1.1.1.1. Multilevel Converters

To reduce the volume of switch-mode converters, two-stage compact and power efficient solutions have been presented [9], [10]. In these solutions, a switched-capacitor fixed-ratio front-end stage performs a large portion of voltage conversion, and an inductor based downstream stage then provides final regulation. This solution reduces the voltage swing at the switching node of the inductor based stage, relaxing the requirement of the filter inductor, while improving the efficiency at the same time, due to lower input-to-output voltage conversion ratio [1], [11]. Typically, a multi-level converter is a converter that can output to a switching node more than just two voltages values (usually V_{in} and 0). Multilevel converters with flying capacitors, such as the three-level buck converter, have been proposed for high-voltage high-power applications [12]. It doubles the effective duty-ratio compared to a buck converter but is limited in its output current due to two MOSFETs in the power path. The drawback of this solution is that the power is processed two times due to the two stages structure, which impacts the efficiency. In addition, although it lowers the input-to-output voltage conversion ratio by a factor of 2, for very high conversion ratio converters this solution may not be efficient enough and may not able to satisfy the load requirement in term of delivering high current. Another issue is the regulation of the flying capacitor's voltage, as it can swing since it is not "naturally" regulated by the topology's operation.

1.1.1.2. Series-Capacitor Buck Converter

The series-capacitor buck converter, also known as a double step-down two-phase buck converter, originally presented in [13] and recently revised in [14]-[15], merges a two-phase interleaved buck converter with a switched-capacitor front-end and by doing so allows high frequency operation in the MHz range and better system dynamics with reduced components' stress. Additional attractive features of the series-capacitor buck converter are natural current sharing between the phases and effectively doubling the switches' on-time, which make it suitable for high conversion ratio applications, and natural regulation of the series capacitor's voltage that limits the voltage stress of the MOSFETs.

1.1.1.3. Voltage Multipliers

Voltage multipliers have been known for a long time [16], and typically realized by diode-capacitor stages. These circuits are widely used as transformerless high-voltage multipliers, as depicted in Fig. 1.2 in a ladder configuration (also known as the Cockcroft-

Walton voltage multiplier). Such circuits transform an ac voltage to a rectified dc voltage, which exceeds the amplitude of the input voltage by *n* times, where *n* is a number of capacitors in the circuit. The interest in these circuits has been increased recently with the advancement of integrated circuits and with the possibility of replacing the diodes by the high frequency switches [17]. It enables a building the low-power high voltage integrated sources, which do not include inductive elements or transformers [18]. There are many diode-capacitor based voltage multipliers, e.g. Dickson switched-capacitor converter [19], Cockcroft-Walton voltage multiplier [20], [21], and some other versions of voltage multipliers [22]-[24]. It should be noted that some of them can be realized in a step-down configuration. In theory, a diode-capacitor voltage multiplier can step-up an ac voltage source to any voltage, even extremely high voltage, by using large number of multiplying stages, but in practice there are limitations on the achievable voltage gain. The inherent limitation with the diode-capacitor voltage multipliers is that the output impedance increases rapidly with the number of multiplying stages, resulting in low efficiency and limited voltage gain. The reason for this is the fact that every multiplying stage processes the power, and therefore in this case there is a large number of power processing stages, each with limited efficiency.

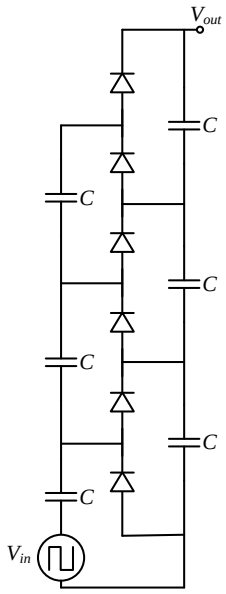

Fig. 1.2 Basic diode-capacitor voltage multiplier in ladder configuration.

1.1.2. Isolated Topologies

Another way of achieving high voltage gain in power converters is to use isolated topologies that incorporate transformers. These isolated topologies include forward,

flyback, half-bridge, full-bridge and their variations. For these cases, the voltage gain is determined not only by the duty-ratio, but also by the transformer's turns ratio *n*, i.e. it is a function of both *D* and *n*, as follows

$$\frac{V_{out}}{V_{in}} = f(D,n). \tag{1}$$

In theory, to achieve a very high voltage gain, *n* can be set very high (or low, depend if it is a step-up or step-down converter). However, in practice if the number of turns in a transformer is high, the primary and secondary windings are not physically close to each other, which results in high leakage inductance. The leakage inductance impacts the converter's efficiency and there is no simple lossless way to limit the voltage spike across the primary-side switch. In addition, large number of turns means higher resistance of the windings and higher output resistance, which limits the achievable voltage gain.

1.2. Control of High Conversion Ratio Converters

The control issue of very high conversion ratio converters appears in almost all the converters and for the sake of explanation will be described on a buck converter. In the ideal case of a buck converter at steady-state, the voltage conversion ratio is given by

$$\frac{V_{out}}{V_{in}} = D \ . \tag{2}$$

For high step-down dc–dc conversion, the duty-ratio becomes very small. Consequently, the regulation period is very short, which is much worse in high-frequency applications. However, all pulse-width modulation (PWM) controllers have the limitation of a minimum *controllable* on-time. It is difficult to maintain the circuit control with a duty-ratio of much less than 10% at high switching frequencies. Also, the gate drive is problematic in terms of turning the top switch off and on in such a short period [8]. In terms of controller design, due to the reasons presented in Section 1.1, the control-to-output transfer function varies as the duty-ratio is close to its limit (i.e. close to 1 or 0). This issue must be considered when designing a controller for very high conversion ratio converters, as it is quite a complicated issue.

In more complicated topologies, which that incorporate multiple switching devices, the controller’s design can be difficult, as some topologies require accurate timing and phase delay between switches. For example, in the series-capacitor buck converter the desired

delay between the two phases is exactly half a cycle (or 180^0 phase delay). This ensures that the duty-ratio range is maximized (up to 0.5) and the output voltage ripple contains only harmonics' frequencies that are twice and more of the switching frequency.

Another problem in advanced topologies that are attractive for a very high voltage conversion ratio is the high number of variables that need to be controlled. In multiphase converters the inductors' currents need to be controlled in order to have current sharing between the phases. In multilevel converters the flying capacitor's voltage must be controlled in order to limit the voltage stress of the power devices. This makes the control problem of such converters much more complicated due to the relatively high number of control variables.

This section overviews the control methods used to facilitate the required performance for various kinds of dc-dc converters. A special emphasis is given to modern nonlinear control methods for IET converters that are defined on the state-space.

1.2.1. Linear control methods

1.2.1.1. Voltage-mode control

Voltage-mode control (VMC) is a control technique used in many power systems where the duty cycle is adjusted to regulate the output voltage, based on the value of the error between the sensed output voltage and the reference voltage [1]. Steady-state is achieved when the actual output voltage equals the voltage reference.

A generalized structure of voltage-mode control loop contains three main stages and is depicted in Fig. 1.3. These three stages are the power stage, the modulator, and the voltage loop compensation network that ideally allows the highest possible bandwidth that maintains the stability. The voltage loop compensation includes calculating the voltage error v_e by comparing the voltage at the feedback to the reference voltage and then using an error amplifier to create a correction signal v_c. This signal enters a modulator and a PWM signal is generated with the compensated duty ratio. To properly understand each of the control loop stages, a voltage-mode controlled buck converter is depicted in Fig. 1.4.

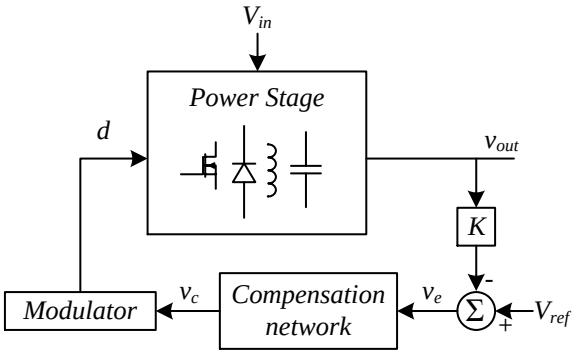

Fig. 1.3 Typical structure of voltage-mode controlled power stage.

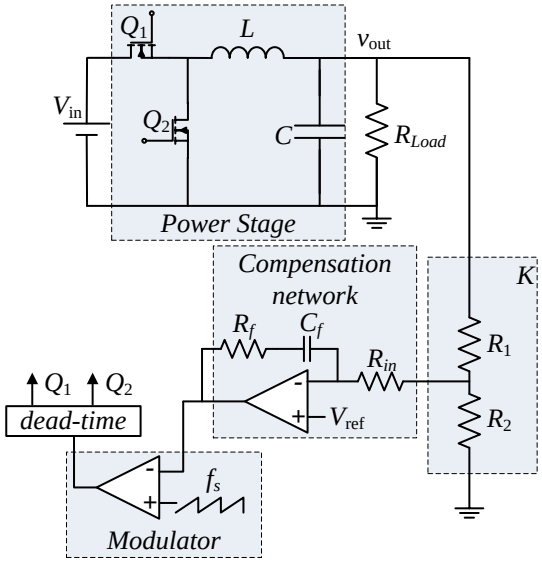

Fig. 1.4 Buck converter controlled by a voltage-mode controler with a PI compensation network.

Design of VMCs is based on the small-signal control-to-output transfer function of the converter so that the output voltage will track the reference voltage. The design aim is to produce the highest loop bandwidth possible, only limited by the switching frequency [1], where common compensators are proportional-integral (PI) and proportional-integral-derivative (PID). Although traditionally the design consideration is to track the reference voltage, in most applications the reference voltage is fixed, and the controller should handle changes in the load current or in the input voltage.

1.2.1.2. Current-mode control

Current-mode control (CMC) has been a popular and effective control technique for switched-mode converters [28]. It is based on sensing both the output voltage and the inductor current, where there are two control loops: inner loop for the inductor current and outer loop for the output voltage [29]. The current loop is a fast loop with a high bandwidth

that equals the switching frequency. The voltage loop is much slower than the current loop, and its output determines the reference v_e for the current loop, as depicted in Fig. 1.5.

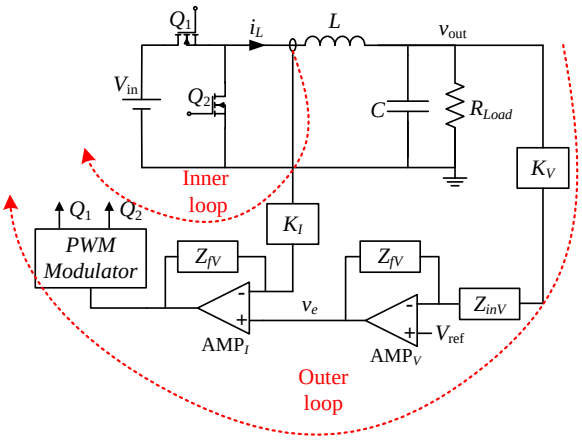

Fig. 1.5 Current-mode control schematic of a syncronous buck converter.

The current loop turns the inductor into a voltage-controlled current source, effectively removing the inductor from the outer voltage control loop transfer function at dc and low frequencies. The inner loop uses a PWM modulator which receives the sensed inductor current ramp, and a reference current obtained by the outer voltage loop to determine the switch control signal.

A significant difference between VMC and CMC is the PWM signal generation. For VMC a fixed external ramp is used, while for CMC the inductor current own ramp is used. CMC schemes have several advantages to offer over VMC. Since in CMC the inductor behaves as a current source, voltage variation at the input side doesn't go through to the output, what makes the CMC more immune to an input disturbances compared to a VMC [1]. Also, the CMC control-to-output transfer function can be simplified to a first order system, compared to second order for the case of VMC, and therefore converters with CMC have simpler dynamics and system stabilization is easier to obtain. CMC is implemented mostly with two approaches: 1) Peak current-mode control (PCMC), 2) Average current-mode control (ACMC).

PCMC is a very popular control method and will be presented in the following subsection.

1.2.1.3. Peak current-mode control

Among the different ways to implement CMC, peak current-mode control (PCMC) is probably the earliest and simplest approach. A block diagram of a PCMC power converter is presented in Fig. 1.6. The inner current loop senses the inductor current and directly compare it to the reference current i_{ref} using a comparator to monitor and maintain the peak inductor current equal to i_{ref}, as depicted in Fig. 1.7. The voltage loop compensator sets i_{ref} based on the voltage error between the output voltage and the reference voltage V_{ref}. It should be noted that for conversion ratio that requires a duty ratio higher than 0.5, sub harmonic oscillations occur [1]. These oscillations can be solved be the addition of slope compensation for i_{ref}. A big advantage of PCMC is that it provides inherent over-current protection due to the immediate current limit by the comparator.

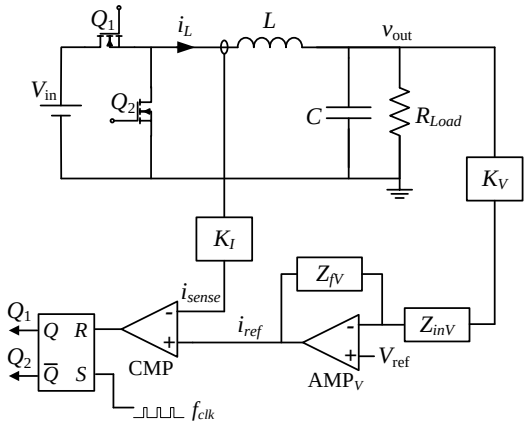

Fig. 1.6 Peak current-mode control of a syncronous buck converter.

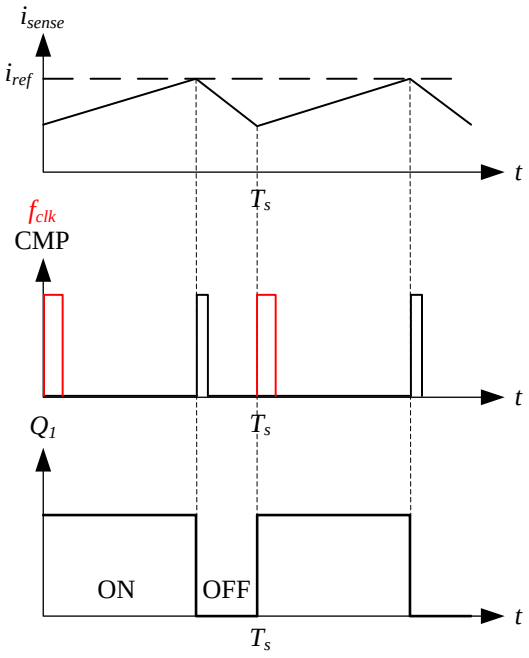

Fig. 1.7 Typical waveforms of peak current-mode controlled converter.

1.2.2. Digital control of switched-mode converters

In recent years, the interest in digital control for switched-mode converters has grown considerably [30]. The digital control approach potentially offers several advantages compared to the analog counterpart, such as the immunity to component variation, the ability to perform sophisticated control algorithm, self-calibrations, faster IC design using HDL synthesis and controller adaptation. In spite of these potential advantages, one of the limiting factors when using IC digital controller in high-frequency SMPS is the hard to achieve dynamic performance that is comparable to those of the analog controllers, especially in the presence of significant control delays and quantization effect. Thus, one of the major challenges in digital control for SMPS is the development of simple digital or mixed-signal control architectures with small additional silicon area required which ensures dynamic performances comparable to analog controllers. Such a controller usually requires high-resolution analog-to-digital converter (ADC) and digital-pulse-width modulator (DPWM), as shown in Fig. 1.8. The IC implementation of such a control is usually complex. It is also hampered by the undesirable quantization effect and limit cycle oscillations [31]-[32].

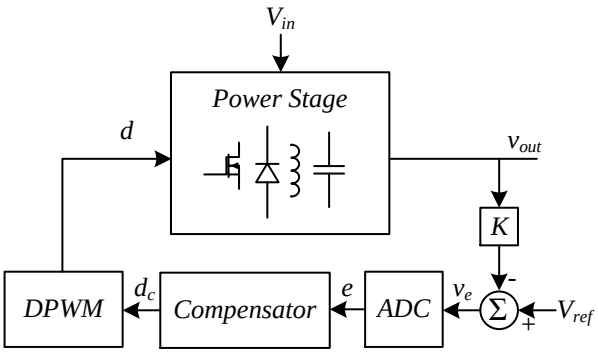

Fig. 1.8 Digitally controlled SMPS.

1.2.3. Nonlinear control methods

The switching action is an inherent property of switched-mode converter systems. In a mathematical sense such systems are discontinuous and thus nonlinear. Unfortunately it is this nonlinearity that, at the same time, represents both the main problem in circuit analysis as well as the bedrock for successful circuit design.

Conventional converter analysis approaches have therefore often tried to suppress the nonlinear characteristics. Techniques such as averaging and linearization have been widely

used [1]. The resulting loss in information is significant; not only does the issue of ripple get neglected in these approaches, but also most of the ensuing mathematical models solely apply to the converters' behavior.

This subsection will review two nonlinear control methods: sliding-mode control (SMC) and boundary control. These nonlinear control methods are suitable for switched-mode converters due to their inherent switching behavior.

1.2.3.1. Sliding-mode control

Most state of the art SMPS controllers are designed by using a state-space averaging method, which is essentially a small-signal approximation [1],[33]. Although this procedure works well for steady-state operation, it has mediocre performance while handling load transients. Most switched-mode converters operate in one of two structural modes: when the switch is on and when the switch is off. Due to the nonlinear nature of the switching operation used in the design of these regulators, they are classified as variable structure systems. SMC is a nonlinear control method that is suitable for variable structure systems and therefore it is a natural fit to utilize them in SMPSs [34].

Fundamental principle of the controller is to employ a certain sliding surface $\sigma(v_C,i_L)=0$ (typically defined in the state-space) as a reference path such that the controlled state variables can be directed toward a desired equilibrium point. Implementation of a sliding surface as a stabilizing reference path can be fully achieved by meeting the following three conditions [35]:

1. *Reachability condition*: the trajectories must reach the sliding surface for arbitrary initial conditions;
2. *Existence condition*: the state trajectories are directed toward the sliding surface when they are close to it;
3. *Stability condition*: the sliding surface will always direct the state trajectories toward a stable equilibrium point.

The principle of operation for SMC is to define a sliding (switching) surface that defines the control law for the converter, if the form of:

$$\begin{matrix} \sigma > 0, & \rightarrow off \\ \sigma < 0, & \rightarrow on \end{matrix} . \tag{1.3}$$

To avoid switching in an infinite frequency along the switching surface, a hysteresis band is added. The hysteresis band width is 2Δ, where Δ is a small parameter. Within this definition of the control law, the reachability and existence conditions can written as

$$\begin{aligned} \frac{d\sigma}{dt} &< 0 \quad for \quad \sigma > 0 \quad (off) \\ \frac{d\sigma}{dt} &> 0 \quad for \quad \sigma < 0 \quad (on) \end{aligned} \quad . \tag{1.4}$$

Fig. 1.9 shows typical SMC operation on the state-plane. As can be observed, the system starts at the initial condition (v_{C0},i_{L0}) and the control law determines that the state should now be the off state. The system state moves along the off state trajectory until it hits the switching surface σ where it changes to on state. From now on, the system state slides along the switching surface until it reaches the steady-state equilibrium point (V_{ref},I_{ref}).

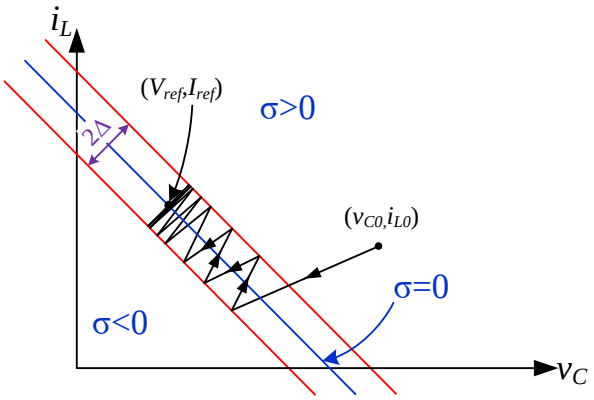

Fig. 1.9 Sliding-mode contoller operation and the resultant controlled trajectories on the state-plane.

The system's motion on the switching surface has an interesting geometric interpretation, as the "average" of the system's dynamics on both sides of the surface and close to it. To analyze the system dynamics along the switching surface, the equivalent control u_{eq} can be used [35].

1.2.3.2. Boundary control

Boundary control is a geometric-based control method which defines a curve of the form $\sigma = f(v_C, i_L) = 0$ on the state-plane called (switching) boundary. It is a generalization of well-known hysteretic type control methods such as voltage-mode hysteretic control and sliding-mode control. For converters with two possible switching states, a boundary defines when the converter is in on state and when it is in off state. Whenever the converter's states are located on one side of the boundary, i.e. $\sigma > 0$, the operation is governed by an on state, and whenever the states are located on the other side, i.e. $\sigma < 0$, the operation is governed

by an off state. Switching between the two states is made when the state trajectory crosses the boundary, thus, a boundary must pass through the desired steady-state operating point (V_{ref},I_{ref}) in order to be able to drive the converter to this point.

Points along the boundary can be classified to three types, according to how the on and off state trajectories behave when they cross the boundary, as depicted in Fig. 1.10:

a. Reflective: both on and off trajectories are directed toward the boundary.
b. Refractive: one state trajectory is directed toward the boundary and the other state trajectory is directed away from the boundary.
c. Rejective: both on and off state trajectories are directed away from the boundary.

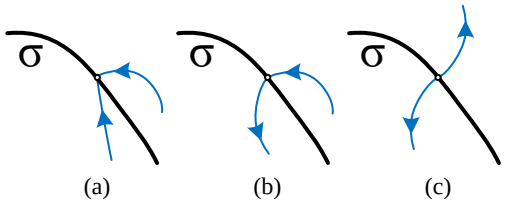

Fig. 1.10 Trajectories behavior at different boundary crossing points: (a) reflective point, (b) refractive point, (c) rejective point.

The state-plane of a switched-mode converter can be separated to the three different regions, i.e. reflective, refractive and rejective, according to the properties of every point and the on and off state trajectories passing through it [36]. The lines separating these three regions are the load-line and the steady-state on and off state trajectories. Consequently, the operation of a boundary controller can be classified to three modes as well, by the location of the boundary with respect to operation region. Operation in the reflective mode results in sliding-mode behavior, since the trajectories on both sides of the boundary are directed towards it. Once the state trajectory hits the boundary, the only movement possible is along the boundary. Operation in rejective mode results in movement away from the boundary, never crossing it again (all trajectories are pointed away from the boundary). Transitions between modes of operation are possible, but not all transitions exist if the system is large-signal stable. For example, operation in refractive mode can be followed be a reflective mode, but not the opposite.

A boundary controller is defined to be large-signal stable if it moves the converter's state variables to the steady-state operating point and keeps them there, resulting in a state-error (voltage and current error) approaching zero, limited by the converter switching frequency.

1.2.4. Load transient oriented control methods

To minimize the size of reactive components, the controllers for SMPSs are often designed to have fast response to load transients and other disturbances, especially in the case of modern VRMs, where high current and low voltage are required at the output of the SMPS. In low-to-medium power supplies, processing power from a fraction of watt to several hundreds of watts, where cost-effective implementation is of a key importance, analog controllers have been predominantly used [37]-[41]. There, a fast response is usually achieved by designing a wide bandwidth control loop. Recently emerged hardware-efficient digital controllers [42]-[48] enable the implementation of advanced nonlinear control methods for low-to-medium power systems, improving dynamic performance and, consequently, drastically reducing the size of the output capacitor. Among them, time-optimal [49]-[55], charge balance and minimum-deviation [56],[58] controllers have demonstrated transient response with virtually the smallest possible voltage deviation. These controllers are classified as hybrid controllers, due to their switching between multiple controllers depending on control objectives or operating conditions.

This subsection reviews the most recent load transient oriented controllers for SMPS.

1.2.4.1. Hybrid control

A Hybrid controller incorporates two or more control laws. The different control laws can be either different small-signal linear controllers, large-signal nonlinear controllers or a mixture of both. Switching between these control laws depends on the converter's states, where the objective of switching between the controllers can be either to achieve faster dynamic response, lower voltage or current overshoots and undershoots, improving efficiency or any other control objective. For example, a hybrid controller such as in [49] can operate as a small-signal linear controller (e.g. PI, PID) when the converter's states are within proximity of the steady-state operating point, and as time-optimal-like controller (see next subsection) for large-signal compensation when the converter's states are away from the new steady-state operating point, in order to achieve the fastest possible dynamic response.

In a hybrid controller that combines large-signal and small-signal linear controllers, it is not a necessary condition for large-signal stability that the large-signal controller will decrease the state-error toward zero and will maintain it in this point. This is since the small-signal linear controller is in charge of keeping the converter's states at the steady-state

operating point, maintaining a zero state-error. The only condition for stability in such a hybrid controller is that the large-signal controller will move the converter's states to the desired steady-state operating point. Thus, a hybrid controller large-signal stability exists if the large-signal compensator is capable of bringing the converter's states from any initial condition to the steady-state operating point.

1.2.4.2. Time-optimal control

Time-optimal control (TOC) has been widely studied in recent years [49]-[55]. It is a nonlinear control method that is designed to handle load transients with fastest possible response. The ideal TOC in the synchronous buck converter includes a single switch action, and its corresponding response including the state-plane trajectories are depicted in Fig. 1.11. The classical approaches for obtaining the ideal TOC based on Pontryagin's minimum principle [62] are not practical in switched-mode converters, since: 1) the solution needs the exact dynamics of the system, which is usually not available; 2) the computations involved may be very complicated; and 3) TOC is sensitive to operating conditions, parameter tolerances, and parasitics. As a consequence, the time-optimal controllers still have not been widely adopted in the industry.

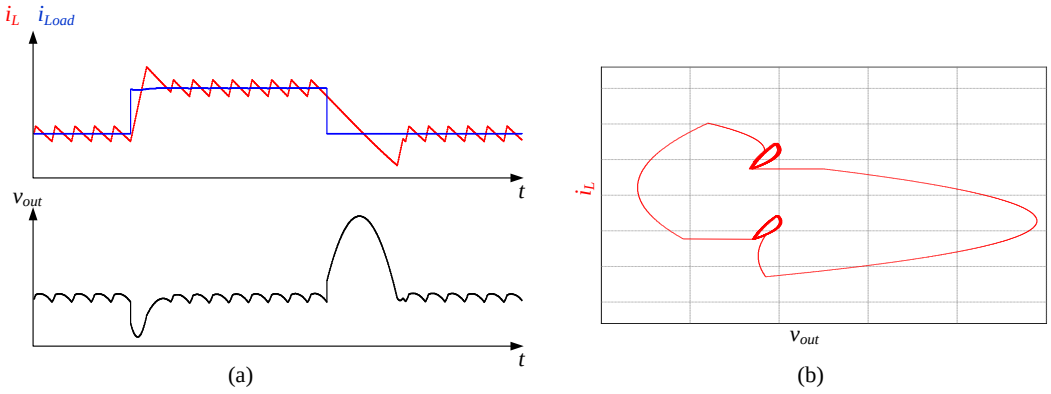

Fig. 1.11 Buck converter controlled by TOC response for a loading followed by an unloding transient. (a) Time response waveforms for inductor current and output voltage, (b) state-plane trajectories.

For direct energy transfer converters, the load transient response using TOC always results in the minimum possible output voltage deviation and, therefore, the minimum output capacitance value. However, for the IET converters such as boost that is not the case. There, the time-optimal response produces a larger than the minimum output voltage deviation and an extra stress of the components.

1.2.4.3. Minimum-deviation control

The minimum-deviation control method has been introduced for buck converters in [58]. This hybrid control method has a bit different control objective than TOC. The objective is to minimize the components' stress by reducing the peak inductor current and the output voltage deviation, while compromising the total transient time. For a loading transient, as in TOC, the inductor current is ramped up with the highest available slew rate. When the inductor current reaches the load current this is when the output voltage deviation is the highest, and from this point on the inductor peak current is limited and the output voltage slowly returns to its steady-state value, as shown in Fig. 1.12.

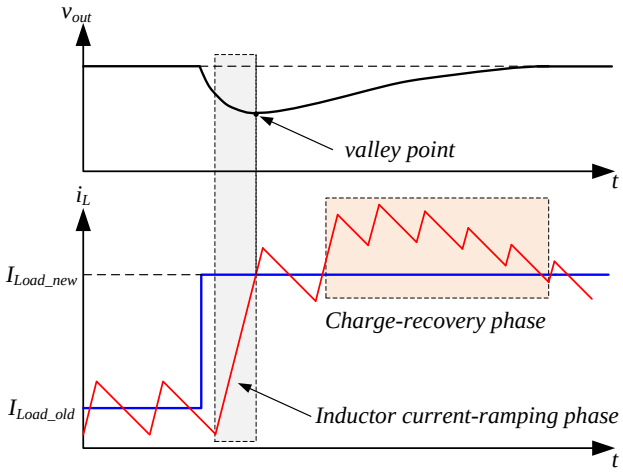

Fig. 1.12 Buck converter loading transeint response with minimum-deviation controller.

1.3. State-space representation of switched-mode converters

Analyzing a switched-mode converter in the state-space can be a powerful tool for power electronics engineers. The state-space reveals the state trajectories and, in many cases, shows properties that are hard or even impossible to notice when analyzing a converter in the time-domain. The state-space representation is mainly used for designing controllers and in particular nonlinear controllers, study the large-signal properties of the converter and to examine the stability of control methods.

Neglecting nonlinearities introduced by transformers or solid-state devices, in the case of a steady-state operation, a switched-mode converter's linear small-signal model can be used to analyze it behavior. Therefore, it is easy to examine the converter's characteristics by using any method related to the theory of linear circuits [59]. However, in transient operation, the linear small-signal model is no longer valid since a switched-mode converter becomes nonlinear, and analyzing it using linear methods becomes inaccurate. Transient

response can be better analyzed using the state-space representation, which refers to system's characterization and dynamic properties and can be applied to nonlinear systems. The analysis is aided by the state trajectories, described upon an appropriate state-space, which its coordinates are the system's state variables. Nowadays, more and more applications mostly operate in the transient operation, and consequently the state-space representation is extensively used and studied in "modern" control methods [56], [57].

Moreover, instead of the conventional representation in terms of frequency response and transfer functions, the state-space representation is an excellent alternative way to describe the system's model. There are several advantages for using the state-space representation when compared to the transfer function method, here are some of them:

1. State-space representation and analysis can be applied to nonlinear systems.
2. It can be applied to time invariant systems.
3. A more compact set of equations.
4. It is an effective option for the visualization of the system's characteristics.
5. It enables an examination of the system's behavior under different control strategies, including nonlinear control methods.
6. It can be easily applied to systems with multiple inputs and multiple outputs.
7. In contrast to a transfer function, which is defined only under zero state initial conditions, it is possible and easy to incorporate the effect of initial conditions in the solution.

The state-space is considered as a working region that describes the system and its operation, by states defined appropriately on the state-space. The state-space axes are defined as state variables, and the state of the system can be represented as a vector within that space. Most common dc-dc converters contains one inductor and one capacitor, and therefore for these cases the order of the system is 2. The state-space is now the state-plane, where its horizontal axis is the capacitor voltage and the vertical axis is the inductor current.

1.3.1. State variables

State variables shall only be those variables that cannot change their values instantaneously. Such variables are all those who appear in mathematical expressions for energy, for example current in the expression of the inductor's stored energy $Li_L^2/2$. Thus obvious candidates for state variables in a dc-dc converter are the inductor current and its

capacitor voltage. Very often they can be expressed in terms of differential equations of the state variables, namely, state equations.

1.3.2. State equations of switched-mode converters

A switched-mode converter is a system with two possible operation states: when the switch is on and when the switch is off. Therefore, the number of state equations would be two times the number of the state variables, i.e. one set of two equations for the on state and one set of two equations for the off state. By using this approach, the construction of the state equations is straightforward. The converter is analyzed as two different linear circuits and the state equations for each of the circuits can be easily derived [60], [61].

An example of deriving the state equations is given for a buck converter loaded by a constant current load. First, the buck is separated into two different linear circuits for the on state and for the off state, as presented in Fig. 1.13.

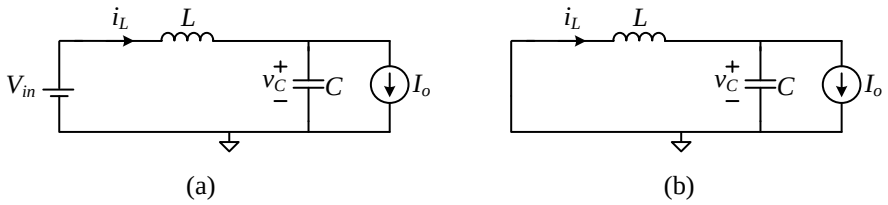

Fig. 1.13 Buck converter circuit for (a) on state (b) off state.

Then, the differential equations for the state variables are extracted by solving the two circuits, for the on state:

$$\text{on}: \frac{dv_C}{dt} = f_{1,on}\left(v_C, i_L\right) = \frac{i_L - I_o}{C}, \qquad \frac{di_L}{dt} = f_{2,on}\left(v_C, i_L\right) = \frac{V_{in} - v_C}{L}\ , \tag{1.5}$$

and for the off state:

$$\text{off}: \ \frac{dv_C}{dt} = f_{1,off}\left(v_C, i_L\right)\frac{i_L - I_o}{C}, \qquad \frac{di_L}{dt} = f_{2,off}\left(v_C, i_L\right) = \frac{-v_C}{L}\ . \tag{1.6}$$

1.3.3. State trajectories constraction

State trajectories are the natural state variables movement trajectories on the state-plane. Although the movement along the trajectories correlates to the change of the state variables with respect to time, the time parameter is implicit, i.e. the speed of movement cannot be determined from the trajectory itself.

The state trajectories construction is done by using the state equations for each of the two states. To write the trajectories expressions, it is first needed to find one state variable as a function of the other state variable, i.e.

$$g\left(v_C, i_L, v_{C_0}, i_{L_0}\right) = 0, \tag{1.7}$$

where v_{C0} and i_{L0} are different initial conditions for the capacitor voltage and inductor current, and then it can be drawn in the state-plane v_C - i_L. Since the time parameter is implicit in state-space representation, it is not mandatory to fully solve the differential equations and find the state variables with respect to time.

There are three main methods for drawing the state trajectories [35]:

1. Isoclines method - Finding the slope of the trajectories and substituting different points in the state-plane. The slope can be found by the expression

$$m\left(v_C, i_L\right) = \frac{di_L}{dv_C} = \frac{f_2\left(v_C, i_L\right)}{f_1\left(v_C, i_L\right)}\ , \tag{1.8}$$

   It should be noted that this method is always applicable and can be used for every system.
2. Finding the exact expression (1.7), this can be done by solving the integral

$$\int f_1\left(v_C, i_L\right) di_L = \int f_2\left(v_C, i_L\right) dv_C\ . \tag{1.9}$$

3. Finding each of the state variables expression with respect to time and then substitute the two equations to eliminate the time parameter.

A detailed example of deriving the state trajectories for buck and boost converters is given in the Appendix.

1.4.References

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2. High Efficiency Non-Isolated Converter with Very-High Step-Down Conversion Ratio

Abstract- This paper introduces a new non-isolated converter topology with very-high step-down conversion ratio and high efficiency for high current low voltage point-of-load voltage regulator modules. Compared to a conventional two-phase buck converter, the new converter triples the effective duty-ratio and lowers the voltage stress of the transistors, significantly reducing the overall volume of the converter while maintaining high efficiency. The new converter is capable of delivering high current to the output by two interleaved phases and further features an inherent current sharing to balance the load between the phases. The use of lower voltage stress transistors allows operation at high switching frequencies that translates into fast dynamic response to load perturbations. The operation of the topology is verified on a 30W, 48V-to-1V prototype, demonstrating peak efficiency of 91.5% and above 88% for most of the load range.

2.1. Introduction

In the recent years, with the proliferation of cloud computing, power consumption of datacenters has grown significantly [1]. Datacenters typically use a large number of CPUs, each requires a well-regulated dc voltage that is provided by a voltage regulator module (VRM) as the back-end converter. This is done to satisfy the power quality for the load and in particular to assure a tightly-regulated supply under rapid and consecutive load transients. In the majority of applications, since the power source is an unregulated 48V dc, the power processing chain in datacenters is constructed as a two-stage converter architecture. The first stage is a 48V-to-12V converter to provide the 12V bus and the second is a 12V-to-1.xV point-of-load (PoL) converter. The two-stage architecture has been widely used in the last 20 years, and due to the massive increase in power consumption of datacenters, improving the efficiency of the power delivery architectures has been assigned as a primary objective [2]-[4].

One of the popular solutions for a two-stage conversion from 48V-to-1.xV is by cascading two converters [5]. Since each of the stages has different objectives, they are designed accordingly. To achieve fast dynamic response required by the CPU and to shrink to components size, the 12V-to-1.xV PoL buck converter operates at relatively high switching frequency, whereas the objective of the 48V-to-12V converter is mainly to

maintain high efficiency. Typically, the 12V-to-1.xV converter comprises multiphase interleaved buck converters, to be able to deliver the high current (few tens of amps) to the CPU and to reduce the output filter volume while maintaining good efficiency over wide load range [6]-[7]. However, although each of the two-stages is over 90% efficient, the overall 48V-to-1.xV conversion efficiency is less than 85% [5], [8]. Aside of the power losses in each of the converters, one of the contributors that lowers the efficiency is the 12V power delivery bus that produces high conduction losses [8].

For some time now, due to both conservative reasons and implementation issues, a single-stage PoL solutions that apply direct 48V-to-1.xV conversion have been avoided. However, with the advancement in semiconductor power devices and control algorithms, some solutions have the potential of being more efficient overall when compared to the two-stage architecture. The main reason for this is the conduction losses on the 48V power bus are significantly lower (for the same power level), up to 16 times, than on a 12V one. As a result, the direct 48V-to-1.xV conversion has another advantage of further reducing the volume of the overall system by trimming down the conductors of the 12V bus.

Very high conversion ratio converters have been investigated in previous years [9]-[30], where in most solutions transformers are used to handle the high voltage conversion ratio. To accommodate the size and cost, these solutions are typically rated for higher power and designed to supply few processors cores. In addition, they typically lack the ability of producing the fast dynamic response to load changes, making them less attractive for VRM applications as a single-stage. The non-isolated high conversion ratio solutions that have been reported in recent years can be divided into two groups. The first group is of enhanced performance buck converter that has been enabled by the advancement of semiconductor technology and the introduction of Gallium Nitride (GaN) power devices [31]. There, the narrow on time that is required (1/48 T_s, neglecting losses) is achieved by fast switching transistors. However, the efficiency of the converter does not pass the mid-80%. Another problem is that an extremely high resolution duty-ratio generator is required to facilitate accurate regulation. The second group of the direct conversion solutions are topology extension of combined-merged converters that employ flying capacitors to lower the effective conversion ratio, enabling multilevel multiphase capabilities to the converter which translates to lower stresses, higher efficiency and wider dynamic range. Among them, multi-phase buck converters with extended duty-cycle and their derivations [13]-[23], which one of the derivations is also known as the series-capacitor buck converter [22], multilevel buck converters [24]-[28], 7-switch flying capacitor multilevel buck converter [29] and

variations of the Ćuk converter [30]. These converters perform better than a buck converter in terms of efficiency since their effective duty-ratio is extended and the transistors voltage stress is reduced [22]. Naturally, any of the variation can be further enhanced with GaN power devices. It should be noted that, to the authors' knowledge, thus far, none of the extended duty ratio converters has been detailed for a 48V-to-1.xV applications.

Within the wide variety of the non-isolated solutions, the series-capacitor buck converter stands out as an attractive solution due to various features. From the load side, it operates similarly to a two-phase interleaved buck converter that can produces extremely fast dynamic response to load changes [32], [33] and also has the same component count except for one capacitor, yet has half of the voltage stress on 3 out of the 4 transistors. It operates at a doubled duty-ratio compared to a buck converter and the series capacitor, along with the symmetrical operation, provides natural current sharing between the phases [34]. On the other hand, at high conversion ratios the low-side transistors still need to handle both high rms current and the voltage stress that is not negligible. In addition, the doubling feature of the duty-ratio may still be tight for regulation in very-high conversion ratio applications.

The objective of this study is to introduce a new non-isolated topology for very-high conversion ratio applications with high efficiency. The new topology, depicted in Fig. 2.1, *effectively triples the duty-ratio, lowers and better distributes the transistors' voltage stress, and features natural current sharing between the phases*. The new double series-capacitor buck converter (DSCBC) adds one series capacitor and one transistor to the component count of a series-capacitor buck converter. It is especially beneficial in terms of volume, cost and efficiency for VRM applications and as a 48V-to-1.xV single-stage converter solution.

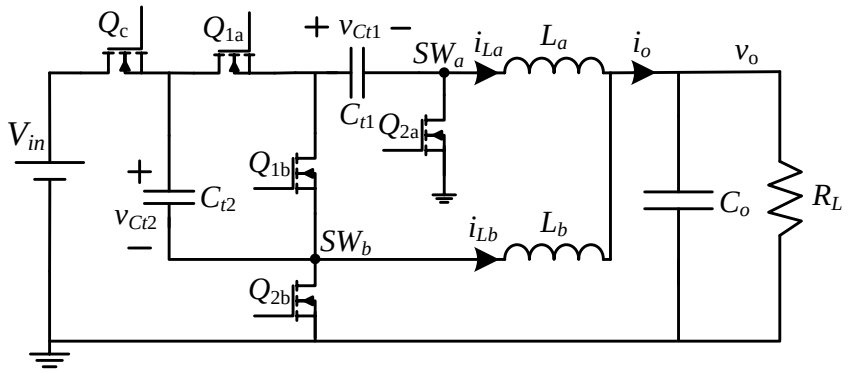

Fig. 2.1 The double series capacitor buck converter (DSCBC).

The rest of the paper is organized as follows: Section 2.2 presents the DSCBC principle of operation and provides typical key waveforms of the new converter. In Section 2.3 a full

steady-state analysis of the DSCBC is delineated and simulation results are presented. Experimental results and efficiency measurements are provided in Section 2.4, and Section 2.5 concludes the paper.

2.2. Double Series-Capacitor Buck Converter

The DSCBC topology, shown in Fig. 2.1, combines the benefits of a switched-capacitor circuit and a series-capacitor buck converter. This topology adds two series capacitors (C_{t1} and C_{t2}) and one transistor (Q_c) to the component count of a standard two-phase buck converter and has a total of 5 transistors, two power delivery capacitors and two inductors. The converter's configuration and waveforms resemble the ones of the series-capacitor buck converter and the two-phase interleaved buck converter, with the benefits of tripled duty-ratio, lower voltage stress transistors and inherent current balancing, making the topology an ideal candidate for high output current high conversion ratio applications.

The description of the DSCBC operation is aided by the idealized timing diagram in Fig. 2.2 and the sub circuits with their currents paths highlighted in Fig. 2.3. The switching period is divided into four time intervals with four states (I-IV), where states II and IV are, in fact, identical. During state I (phase B is on and phase A is off, see Fig. 2.3(a)) the transistors Q_{1b}, Q_{2a} and Q_c are on. The input voltage connects to L_b through the capacitor C_{t2} which reduces the applied voltage on the inductor, and the inductor current i_{Lb} is ramped up while charging C_{t2}. In parallel, the capacitor C_{t1} also connects to L_b and discharges. Since in this phase SW_a is at GND, the inductor L_a is connected between GND and the output capacitor C_o and delivers its stored energy to the output. In state II (see Fig. 2.3(b)) the transistors Q_{2a} and Q_{2b} are on, resulting in both nodes SW_a and SW_b to connect with GND, and both phases A and B are off. Both inductors are connected between GND and C_o and the inductors currents ramp down. State III (phase A is on and phase B is off, see Fig. 2.3(c)) start at half the switching period at $T_s/2$ and the transistors Q_{1a} and Q_{2b} are on. L_a is sourced by a series connection of C_{t2} and C_{t1}, where C_{t2} is discharges while C_{t1} is charged by i_{La}. Since SW_b is at GND, the stored energy in the inductor L_b is delivered to the output. By connecting the two capacitors in series with opposite polarities the applied voltage on L_a during this state is lowered, resulting in a lower current ripple that, in turn allows the extension of the duty-ratio. State IV is identical to state II, transistors Q_{2a} and Q_{2b} are on and the two phases are off.

As can be observed in Fig. 2.2, by setting a symmetrical duty-ratio command on both phases, the operation of the DSCBC is similar to a two-phase interleaved buck converter with an input voltage one-third V_{in} for each phase which translates to extended duty-ratio operation with respect to the input voltage. In addition, the average current is distributed $I_o/3$ and $2I_o/3$ ratio which also implies on the power that is processed by each phase. As will be analyzed and further detailed in the next section, while the basic features (extended duty ratio, lower voltage stress and current balancing) are maintained, the duty-ratio settings of each phase translates into power processed by it, a feature that adds another degree of freedom in optimizing the design of the converter.

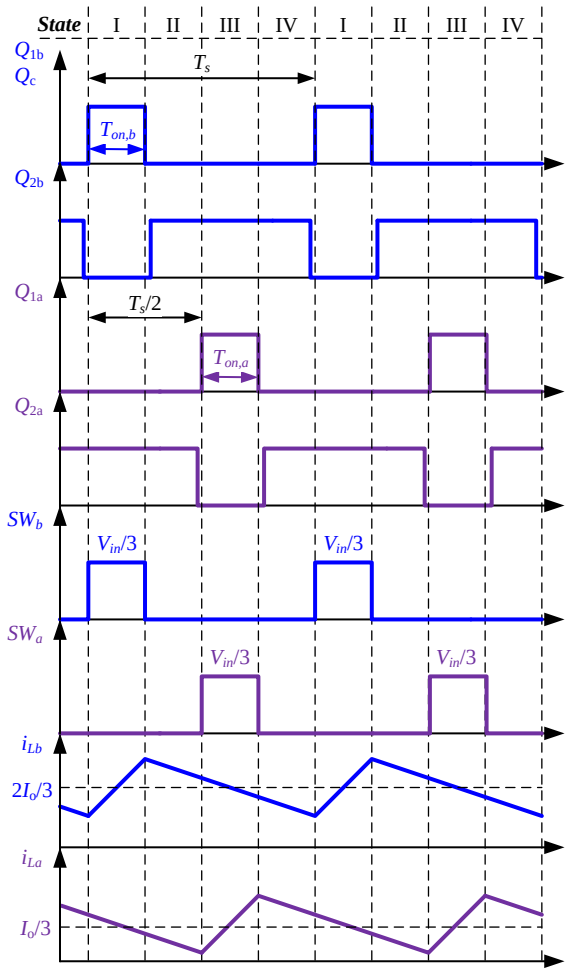

Fig. 2.2 Idealized waveforms of the DSCBC topology.

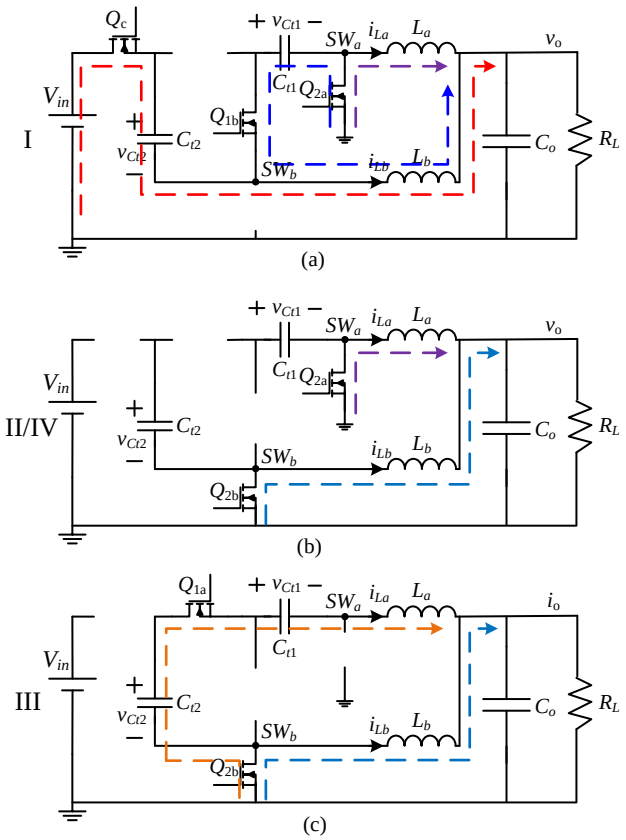

Fig. 2.3 Currents paths in the DSCBC topology: (a) State I: phase B is on and phase A is off, (b) States II and IV: both phases A and B are off, (c) State III: phase B is off and phase A is on.

2.3.Steady-State Analysis

The steady-state analysis of the DSCBC topology presented in this section is assisted by a steady-state simulation of a 30W 48V-to-1V converter, operating at 500KHz switching frequency per-phase, and is depicted in Fig. 2.4. The simulation shows the key waveforms of the new topology: inductors currents, output voltage, switching nodes voltages, series capacitors voltages and currents, and voltage stress of all the transistors.

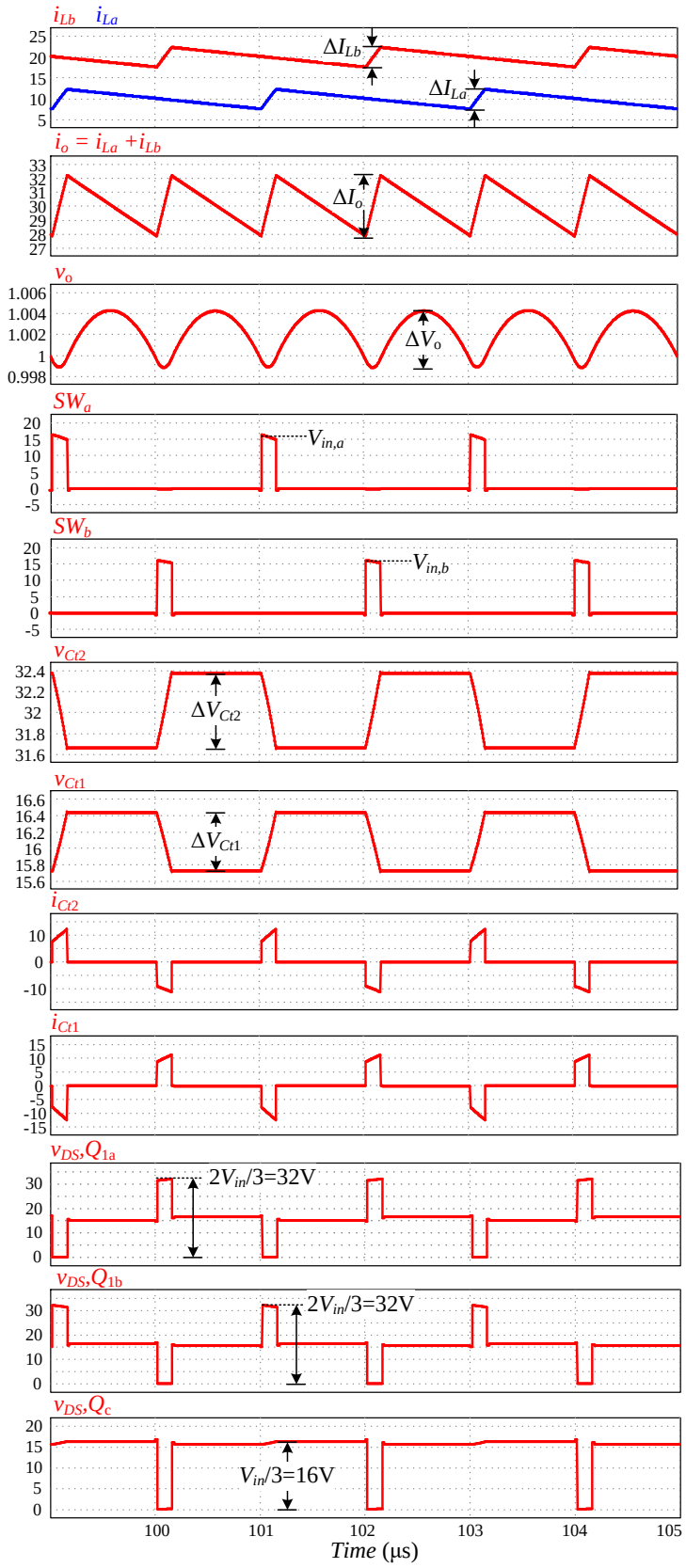

Fig. 2.4 Simulation waveforms of the DSCBC topology for equal duty-ratios.

2.3.1. Average Analysis and Voltage Gain

A key factor in the operation of the DSCBC is the capacitors voltages, which lower the transistors voltage stress and enable the operation with larger on-time of the transistors compared to both a buck converter and a series-capacitor buck converter. Since the average voltage applied on the inductors is zero, the average voltages at the switching nodes SW_b and SW_a equal V_o, the average output voltage can be expressed as

$$\begin{aligned} \left(V_{in}-V_{Ct2}\right)D_b &= V_o \\ \left(V_{Ct2}-V_{Ct1}\right)D_a &= V_o \end{aligned}, \tag{1}$$

where $D_a=T_{on,a}/T_s$ and $D_b=T_{on,b}/T_s$ are the duty-ratios for phase A and phase B, respectively. During state I the sum of the capacitors' voltages equals the input voltage, i.e.

$$V_{Ct1}+V_{Ct2}=V_{in}. \tag{2}$$

Using (1) and (2), and after some manipulations, yields the average capacitors voltages:

$$\begin{aligned} V_{Ct2} &= \frac{D_a+D_b}{2D_a+D_b}V_{in} \\ V_{Ct1} &= \frac{D_a}{2D_a+D_b}V_{in} \end{aligned}. \tag{3}$$

The voltage conversion ratio can be derived from (1) and (3), and can be expressed as:

$$M=\frac{V_o}{V_{in}}=\frac{D_aD_b}{2D_a+D_b}, \tag{4}$$

Therefore, (3) and (4) imply that setting equal duty-ratios, i.e. $D_a=D_b=D$, for the two phases, results in average capacitors voltages of $V_{Ct2}=2V_{in}/3$ and $V_{Ct1}=V_{in}/3$, where the expression for voltage conversion ratio is reduced to

$$M=\frac{V_o}{V_{in}}=\frac{D}{3}, \tag{5}$$

which is 3 times higher compared to the duty-ratio of a buck converter.

2.3.2. Steady-State Inductors Currents and Output Voltage Ripple

As mentioned in Section 2.2, the operation of the DSCBC is similar to a two-phase interleaved buck converter, but with different input voltage for each phase. The input voltage for each of the phases is calculated by the voltage during the on-time of each phase

at the nodes SW_a and SW_b for phase A and B, respectively. Using (3), the input voltage of phase A can be expressed as:

$$V_{in,a} = V_{Ct2} - V_{Ct1} = \frac{D_b}{2D_a + D_b} V_{in} \quad , \tag{6}$$

and in a similar manner, the input voltage of phase B is

$$V_{in,\mathrm{b}} = V_{in} - V_{Ct2} = \frac{D_a}{2D_a + D_b} V_{in} \quad . \tag{7}$$

As a result, two effective voltage conversion ratios for each of the phases are considered, $V_o/V_{in,a}$ for phase A and $V_o/V_{in,b}$ for phase B.

The slew rates of the inductors currents i_{La} and i_{Lb} during the on-time of each of the phase are:

$$\left.\frac{di_{La}}{dt}\right|_{on,a} = \frac{V_{Ct2} - V_{Ct1} - V_o}{L_a}, \quad \left.\frac{di_{Lb}}{dt}\right|_{on,b} = \frac{V_{in} - V_{Ct2} - V_o}{L_b} \quad , \tag{8}$$

where for the rest of the period the slew rates are:

$$\left.\frac{di_{La}}{dt}\right|_{off,a} = -\frac{V_o}{L_a} \qquad \left.\frac{di_{Lb}}{dt}\right|_{off,b} = -\frac{V_o}{L_b} \quad . \tag{9}$$

The inductors currents' ripples ΔI_{La} and ΔI_{Lb} can be calculated using (8) and are given by

$$\Delta I_{La} = \frac{V_{Ct2} - V_{Ct1} - V_o}{L_a f_s} D_a, \quad \Delta I_{Lb} = \frac{V_{in} - V_{Ct2} - V_o}{L_b f_s} D_b \tag{10}$$

where f_s is the switching frequency. For the private case of equal duty-ratios D_a=D_b=D the inductors currents ripples can be expressed as

$$\Delta I_{La} = \frac{V_{in}/3 - V_o}{L_a f_s} D, \qquad \Delta I_{Lb} = \frac{V_{in}/3 - V_o}{L_b f_s} D \quad . \tag{11}$$

Assuming equal duty ratios, the output voltage ripple can be calculated using the charge delivered and consumed from the output capacitor during a switching period and can be expressed as:

$$\Delta V_o = \frac{\Delta I_o}{8 C_o f_s} \tag{12}$$

where ΔI_o is the total current ripple at the output, obtained by summing the inductors currents, i.e. the ac component magnitude of $i_{La}(t)$+$i_{Lb}(t)$. Using (8), (9), and after some manipulation ΔI_o is given by

$$\Delta I_o = \frac{(V_{in}/3 - V_o) L_b - V_o L_a}{L_a L_b f_s} D \quad , \tag{13}$$

and assuming $L_a \approx L_b \approx L$ the output voltage ripple is calculated by substitution of (13) into (12):

$$\Delta V_o = \frac{V_{in} - 6V_o}{24LC_o f_s^2} D \quad . \tag{14}$$

2.3.3. Current Balancing and Power Distribution

The load current I_o is delivered from both phases A and B and equals to the sum of the average inductors currents:

$$I_o = I_{La} + I_{Lb} \, . \tag{15}$$

The average value of each of the inductors currents can be calculated using the fact that charge balance is achieved for each of the capacitors C_{t1} and C_{t2}. For example, the charge delivered to C_{t2} during state I must equal the charge consumed from C_{t2} during state III. This yields

$$\text{state I}: \quad Q_{Ct2} = \frac{1}{2} I_{Lb} \frac{D_b}{f_s} \, , \tag{16}$$

$$\text{state III}: \quad Q_{Ct2} = I_{La} \frac{D_a}{f_s} \, . \tag{17}$$

Substituting (15) into (16) and equating it to (17), yields the average inductors currents that are given by

$$I_{La} = \frac{D_b}{2D_a + D_b} I_o \, , \tag{18}$$

and

$$I_{Lb} = \frac{2D_a}{2D_a + D_b} I_o \, . \tag{19}$$

As can be seen in (18) and (19), the average inductors currents depend on the duty-ratio settings. This provides an additional degree of freedom to distribute the load current between the phases by changing the ratio between D_a and D_b. For example, by setting the duty-ratios to be equal, the average inductors currents are

$$\begin{aligned} I_{La} &= \frac{1}{3} I_o \\ I_{Lb} &= \frac{2}{3} I_o \end{aligned} \, , \tag{20}$$

and by setting D_b=2D_a the average inductors currents will be equal, i.e.

$$I_{La} = I_{Lb} = \frac{I_o}{2} . \tag{21}$$

2.3.4. Series Capacitors Voltage Ripple

The simplified analysis of the converter's behavior in steady-state operation, and in particular for the average behavior the capacitors voltages V_{Ct1} and V_{Ct2} can be considered constant. However, in practice their voltage ripple, caused by charging and discharging them each switching cycle, can play a crucial role in the final design and size of the converter. It is therefore essential to quantify the voltage ripple for each of the series capacitors.

During the charging and discharging states the capacitors' currents are determined by the inductor current that is connected to them during the on-time, i.e. by I_{Lb} during state I and by I_{La} during state III. The voltage ripple of the capacitors can be easily calculated during state III, when phase A is on and both the capacitors are connected in series with L_a:

$$\Delta V_{Ct1} = \frac{I_{La} D_a}{C_{t1} f_s}, \quad \Delta V_{Ct2} = \frac{I_{La} D_a}{C_{t2} f_s} , \tag{22}$$

and for equal duty-ratios the capacitors voltage ripple can be calculated using (5) and (20), which yields:

$$\Delta V_{Ct1} = \frac{I_o V_o}{C_{t1} V_{in} f_s}, \quad \Delta V_{Ct2} = \frac{I_o V_o}{C_{t2} V_{in} f_s} . \tag{23}$$

It should be noted that the charging and discharging actions of the capacitors are so-called *soft-charged* [35], i.e. connected through an inductance that dictates the charging or discharging current and as a result does not involve emulated resistance losses [36], [37] that are a function of the switching frequency.

2.3.5. Summary of the Topology Highlights

The DSCBC topology features natural current sharing between phase A and phase B, as can be seen from expressions (18) and (19). The current sharing attribute is the result of the charge balance on the capacitors C_{t1} and C_{t2}, and it is independent on their capacitance values. The feature of duty-ratios dependent current sharing allows to control the power distribution per phase and enables the proper design of each of the phases. For example, if equal currents between the two phases is desired, setting D_a=2D_b satisfies the requirement,

but comes at the cost of different effective voltage conversion ratios of each of the phases. In this case, phase B voltage conversion ratio will be $V_{in}/4V_o$ whereas phase A voltage conversion ratio will be $V_{in}/2V_o$. By setting $D_a=D_b$ phase B current will be twice higher than the current in phase A, according to (20). However, since the current sharing is an inherent feature and it is parameter-independent, the two phases can be designed according to the load (average current) that is being processed by each phase, i.e. with different transistors and inductors for each phase, to optimize the converter's operation, efficiency and power density.

In addition to the above characteristics of the DSCBC, the topology also lowers the voltage stress of the transistors compared to a two-phase buck converter. As opposed to the voltage stress of the transistors in a buck converter, which is V_{in} for both of the transistors, the voltage stress of the transistors in the DSCBC is divided with an opposite ratio to the current handling per transistor, and fortunately, in favor of higher efficiency design. Here, the voltage stress of the transistors Q_c, Q_{2a} and Q_{2b} equals V_{Ct1} and the stress of Q_{1a} and Q_{1b} equals V_{Ct2}; all are given in (3). This feature allows for a better and more compact design of the converter, especially in high voltage conversion ratio applications, since the transistors Q_{2a} and Q_{2b} that have much higher rms currents (since they conduct most of the switching cycle at high conversion ratios) also have significantly lower voltage stress which allows the use of transistors with lower $R_{DS(on)}$ per silicon area. Moreover, for these kind of applications with short on-time, the low rms current through the transistors Q_c, Q_{1a} and Q_{1b} allows to consider transistors with higher $R_{DS(on)}$ but with much lower capacitances, which expedites the switching transitions and lowers both switching losses and the gate drivers requirements, especially in high input voltage applications

2.4.Experimental Results

To validate the operation of the DSCBC at high voltage conversion ratio, a 30W 48V-to-1V prototype that operates at 500KHz switching frequency per phase was built and tested. Table I lists the components values and parameters of the experimental prototype. The converter was digitally controlled using an Altera FPGA [38] using fully digital high performance ADC and DPWM peripherals as detailed in [39].

TABLE I. EXPERIMENTAL PROTOTYPE VALUES

Component	*Value / Type*
Input voltage V_{in}	48 V
Output voltage V_o	1 V
Switching frequency f_s	500 kHz per phase (1MHz effective)
Output capacitor C_{out}	100 µF
Inductors L_a and L_b	0.44 µH, 0.21 mΩ DCR
Capacitors C_{t1} and C_{t2}	3.3 µF, 100V, 3 mΩ ESR,1206 case
Q_c MOSFET	SiA466EDJ, 20 V, 9.5 mΩ
Q_{1a} and Q_{1b} MOSFETs	Si4288DY, 40 V, 20 mΩ, Dual
Q_{2a} MOSFET	SiRA12DP, 30 V, 4.3 mΩ
Q_{2b} MOSFET	SiRA04DP, 30 V, 2.2 mΩ

Figs. 5 to 8 show the converter's waveforms for output current of 18A with equal duty-ratios. Fig. 2.5 shows the input voltage, the output voltage and the sum of the inductor currents. Due to the two-phase interleaved operation of the converter, the effective switching frequency at the output of the converter doubles, from 500KHz to 1MHz. The inductors currents and series capacitors voltages are depicted in Fig. 2.6. As can be observed, natural current sharing between phases A and B is obtained and with a ratio of 2:1, and the capacitors voltage are $V_{in}/3$ and $2V_{in}/3$ for C_{t1} and C_{t2}, respectively. Fig. 2.7 shows the voltages at the switching nodes SW_a and SW_b. The duty-ratio of the switching nodes is slightly higher than 1/16 (due to losses), validating the ability of the converter to effectively and practically triple the duty-ratio compared to a buck converter. Loading and unloading transients of 5A are depicted in Fig. 2.8, demonstrating the fast dynamic response of the converter to load change. Efficiency measurement of the converter with 48V input and various output voltages are provided in Fig. 2.9, demonstrating a peak efficiency of 91.5% and above 88% for most of the load range at 1V output and even higher efficiency for higher output voltages. Fig. 2.10 shows the efficiency measurement for 1V output and various input voltages to examine the DSCBC efficiency in case the input voltage is unregulated.

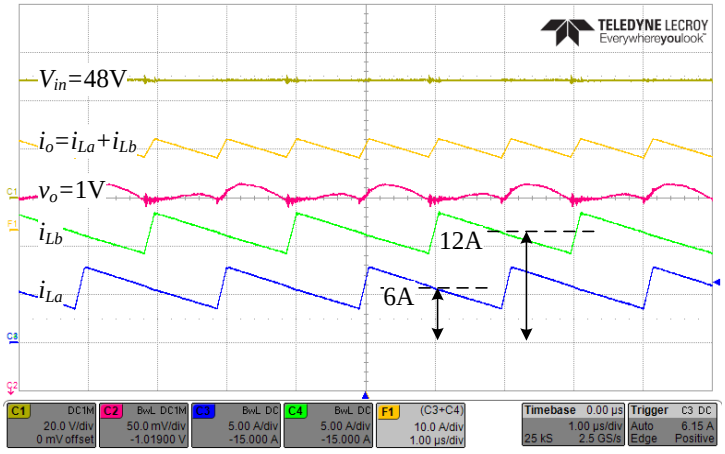

Fig. 2.5 Experimental results: C1 - input voltage (20V/div), C2 - output voltage (50mV/div), C3 - phase A inductor current (5A/div), C4 - phase B inductor current (5A/div), F1 - output current (sum of the inductors currents, 5A/div). Time scale is 1µs/div.

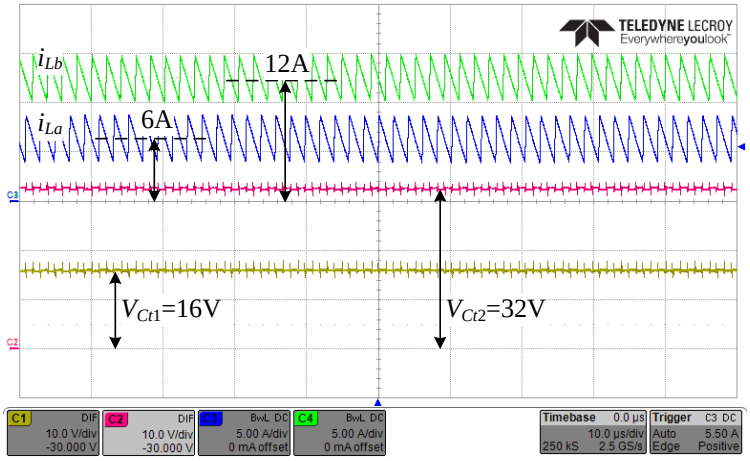

Fig. 2.6 Experimental results: C1 and C2 - Series capacitors voltages (10V/div), C3 and C4 - inductors currents (5A/div). Time scale is 10µs/div.

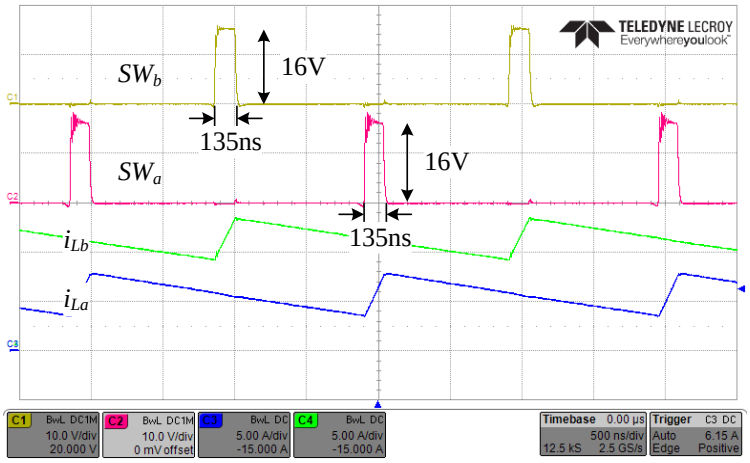

Fig. 2.7 Experimental results: C1 - switching node SW_b (10V/div), C2 - switching node SW_a (10V/div), C3 and C4 - inductors currents (5A/div). Time scale is 500ns/div.

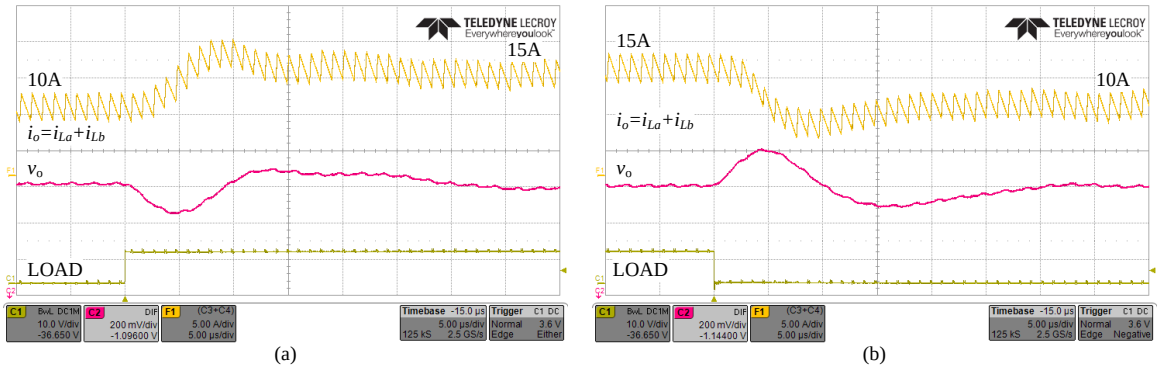

Fig. 2.8 Experimental results of 5A load transients: (a) 10A to 15A loading transient, (b) 15A to 10A unloading transient. C1 - load step signal, C2 - output voltage (200mV/div), F1 - output current (sum of the inductors currents, 5A/div). Time scale is 5µs/div.

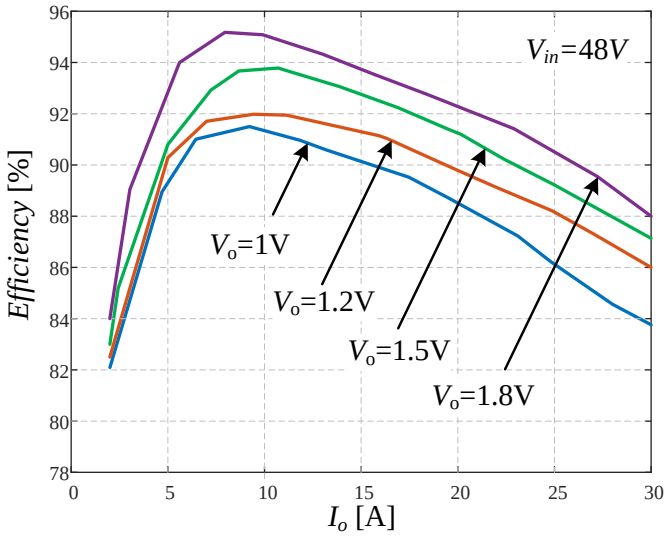

Fig. 2.9 Experimental efficiency measurements of the DSCBC for different output voltages.

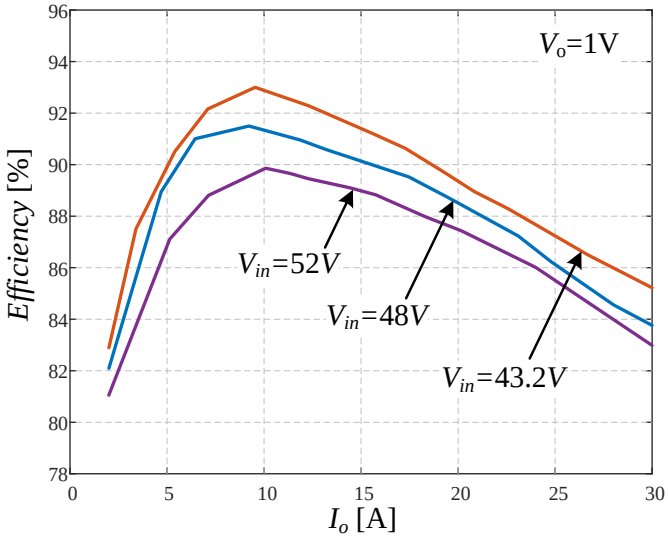

Fig. 2.10 Experimental efficiency measurements of the DSCBC for different input voltages.

2.5. Conclusion

A new very-high step-down conversion ratio with high efficiency and non-isolated converter topology has been presented. The topology comprises two-phases for high current delivery and uses two series capacitors, operating with soft-charging characteristic. The energy processing by the capacitors significantly lowers the voltage stress of the transistors, triples the duty-ratio and provides an inherent current sharing feature between the two phases. These properties reduce the VRM's volume while increasing the efficiency in 48V-to-1.xV conversion that is common and highly desired in datacenters and other cutting-edge applications.

The experimental results validated the theoretical analysis and demonstrated the superior performance of the topology for a 48V-to-1V operation, achieving 91.5% peak efficiency and above 88% for most of the load range. The high efficiency of the converter has been obtained while the solution hasn't compromised other important specifications such as fast dynamic response. These make the new converter topology a very attractive candidate for 48V input, single-stage PoL converters for datacenters and other VRM applications.

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3. Closed-Loop Design and Transient-Mode Control for a Series-Capacitor Buck Converter

Abstract - This paper explores the large-signal and small-signal dynamics of a series-capacitor (SC) buck-type converter and introduces an optimal closed-loop control scheme to accommodate both the steady-state and transient modes. As opposed to a conventional buck converter, where time-optimal control is realized by a single on-off cycle, in the SC-buck topology there is a need to distribute the switching phases to satisfy the charge-balance of the series-capacitor. The new control method merges a voltage-mode controller for steady-state operation and a non-linear, state-plane based transient-mode controller for load transients. A detailed principle of operation of the SC-buck converter is provided and explained through an average behavioral model and state-plane analysis. The operation of the controller is experimentally verified on a 20W 12V-to-1V converter, demonstrating voltage-mode control operation as well as minimum-deviation and time-optimal responses for load transients.

Keywords— Time-optimal control, state-space control, dc-dc converters, voltage regulation.

3.1. Introduction

In recent years, a significant effort is made to enhance the performance of voltage regulator modules (VRMs) for high-performance integrated circuits that operate with low supply voltage and high current. Tight output voltage regulation, high efficiency, and accommodating load transients are key factors in the design of the switch-mode power supplies (SMPS), in particular for high step-down conversion ratio applications. Several converter topologies and circuit extensions have been discussed in the literature to minimize the size of passive components and improve the dynamics of the VRM. One direction of VRM implementation is based on multi-phase interleaved converters, allowing high frequency operation and size reduction at the cost of complex control for current sharing [2]-[3]. Another approach is by multi-level converters where the lower component stress allows better sizing of the components and efficiency improvement [4], [24].

The series-capacitor (SC) buck converter, also known as a double step-down two-phase buck converter, originally presented in [6] and revised in [13]-[11], merges a two-phase interleaved buck converter with a switched-capacitor front-end and by doing so allows high

frequency operation in the MHz range and better system dynamics with reduced components' stress. Additional attractive features of the SC-buck converter are natural current sharing between the phases and effectively doubling the switches' on-time, which make it suitable for high conversion ratio applications.

Recent studies have quantified the attributes of the SC-buck topology at high frequency [12], [13] and demonstrated improved light load efficiency when operating in DCM [14]. Further extensions presented a two-phase, four-inductor, converter which emphasizes its current sharing feature when the power is distributed between multiple phases [15]. Although the converter's topology has been widely and thoroughly investigated [15], dynamic analysis and digital controller design for the topology and its derivatives have not been systematically explored. It would be a further value to examine the converter suitability for time-optimal controller assignment in order to be considered attractive for VRM applications.

The objective of this study is therefore to investigate the dynamic features of a SC-buck converter and to introduce an optimal closed-loop digital controller that merges a voltage-mode compensation for steady-state operation and a non-linear control law for load transients, as detailed in Fig. 3.1. In this study, two modeling approaches are presented, the first is by an average-behavioral model to examine the small-signal control-to-output response and design a discrete-time voltage-mode controller. The second method is to obtain a state-space representation which will be the basis for the design of a non-linear minimum-deviation and time-optimal controllers for load transients. The design and definition of the non-linear controllers are significantly more challenging in the context of the SC-buck converter since they involve four state-variables compared to two state-variables in the case of a conventional buck converter.

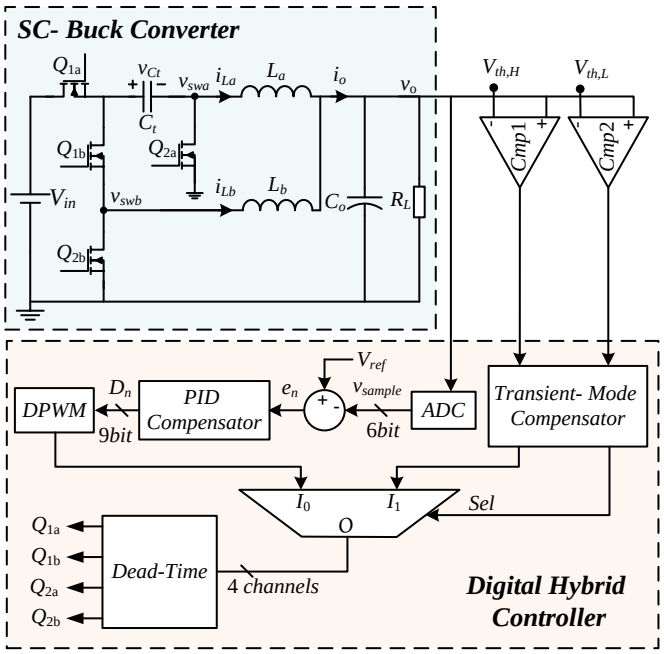


Fig. 3.1 SC-buck converter and a hybrid controller

The rest of the paper is organized as follows: Section 3.2 describes the steady-state operation of the converter, extracts an average-behavioral model representation, and provides a design procedure of a discrete-time voltage-mode compensation scheme, with survey and discussion on the effects of sampling and compensation on multi-phase type buck converters. Section 3.3 provides a large-signal analysis and state-space modeling, minimum-deviation control algorithm, effect of the series-capacitor on the transient performance and potential remedies using a time-optimal control algorithms of the SC-buck converter and detailed simulation results. Fully detailed and demonstrated experimental setup of the all the key novelties are presented in Section 3.4. Section 3.5 concludes the paper

3.2.Steady-State Operation and Voltage-Mode Controller

The description of the SC-buck converter is assisted by the topology structure and typical waveforms, as shown in Fig. 3.2 and Fig. 3.3, respectively. The steady-state operation is similar to that of an interleaved, two-phase buck converter with a slight difference that the back-end converter is fed by a series-capacitor C_t that is charged to approximately $V_{in}/2$. The duty-ratio for both phases (*a* and *b*) is identical and each phase is time-interleaved with a 180^o phase delay. As a result, four switching-states are identified. In state-1, Q_{1a} and Q_{2b} are on, resulting in v_{swa} that equals $V_{in}/2$ and the inductor current i_{La} ramps up with a slew-rate of $(V_{in}/2\text{-}V_o)/L_a$ and i_{Lb} ramps down with a slew-rate of $-V_o/L_b$. In state-2, Q_{1a} is turned

off, Q_{2a}, Q_{2b} are on, and the operation resembles a conventional buck converter in off state. In state-3 Q_{2a} and Q_{1b} are on, C_t acts as the source for phase *b*, and the inductor current i_{Lb} ramps up with a slew-rate of $(V_{\text{in}}/2\text{-}V_o)/L_b$ while i_{La} ramps down with a slew-rate of $-V_o/L_a$. State-4 is identical to state-2. Charge balance of C_t is naturally maintained by this operation allowing both charge and discharge action per cycle [13], and for equal on-times of phase *a* and *b*, this naturally stabilizes v_{Ct} to half the input voltage.

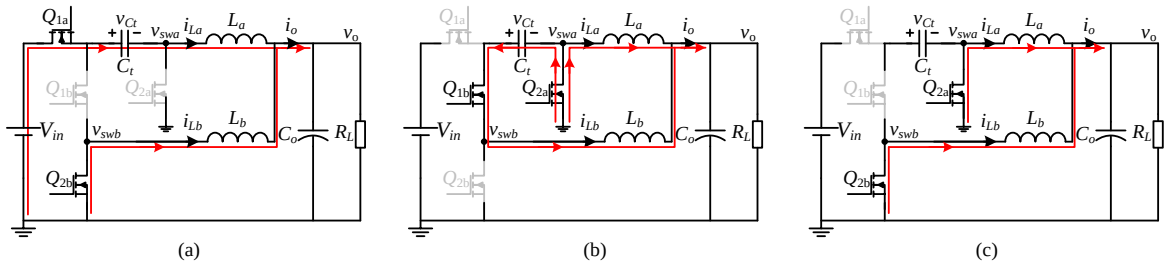


Fig. 3.2 Current paths in switching-states of the SC-buck converter: (a) State-1, (b) State-3, (c) State-2 and State-4.

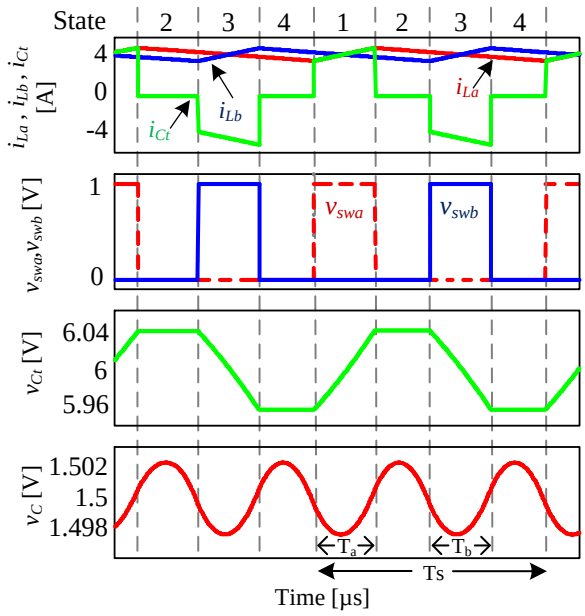


Fig. 3.3 Typical waveforms of a SC-buck converter.

Following the switching sequence and assuming CCM operation, the behavioral operation of the converter is obtained by averaging [16]-[17]. The average voltage across the inductors, $\langle v_{La} \rangle$, $\langle v_{Lb} \rangle$ and the average capacitor current $\langle i_{Ct} \rangle$ can be expressed as:

$$\langle i_{Ct} \rangle = D_a i_{La} - D_b i_{Lb} \tag{1}$$

$$\langle v_{La} \rangle = D_a (V_{\text{in}} - V_{Ct}) - V_{\text{o}} \tag{2}$$

$$\langle v_{Lb} \rangle = D_b V_{Ct} - V_{\text{o}} \ , \tag{3}$$

where $D_a=T_a/T_s$ and $D_b=T_b/T_s$ are the duty-ratios related to the conduction time of Q_{1a} and Q_{2a}, respectively. V_o is the output voltage and T_s is the switching period.

Fig. 3.4 shows a graphical representation for an average-behavioral model as described by (1)-(3). As mentioned earlier, the duty-ratios for both phases are equal, i.e. $D_a=D_b=D$. By applying small-signal linearization, the full control-to-output transfer function can be obtained. To simplify the expressions, V_{Ct} is assumed constant by small-ripple approximation [18], resulting in a control-to-output expression of the form:

$$\frac{v_o}{d}(s)=\frac{\frac{V_{in}}{2}\left(sC_oR_c+1\right)}{s^2\frac{C_o\left(L_a\parallel L_b\right)}{R_L}\left(R_L+R_c\right)+s\left(C_oR_c+\frac{L_a\parallel L_b}{R_L}\right)+1} \tag{4}$$

As can be observed from (4), this expression is similar to the control-to-output response of a classical two-phase buck converter with half the input voltage. A typical frequency response of (4) is depicted in Fig. 3.5 along with the required compensator that its design is detailed in the next sub-section.

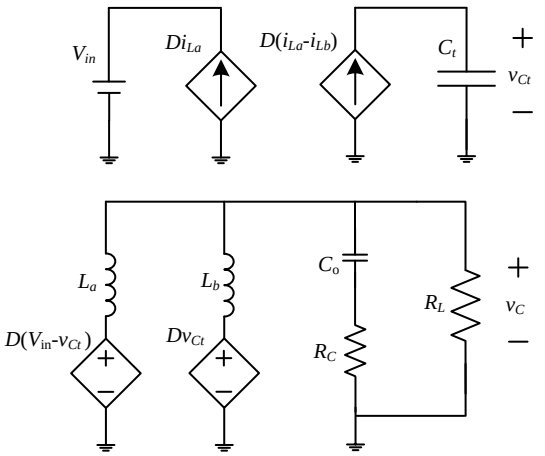


Fig. 3.4 Average-behavioral model of the SC-buck converter.

3.2.1. Closed-Loop Discrete-Time Compensator Design

To satisfy the requirements for loop-gain stability and high bandwidth, the crossover frequency f_c of the closed-loop system is chosen to be one tenth of the switching frequency while the target phase margin is set to be above 50°. Based on the control-to-output transfer function behavior, the setting of the target parameters in this way guarantees suitability for PID compensation scheme [19]. The extraction of the PID coefficients (a,b,c) is based on

the methodology that has been presented in [20] with minor adjustments to a frequency-domain design. The design procedure is as follows:

- Specify the crossover frequency fc and the phase margin of the desired closed-loop A_{CL}(s) frequency response based on a knowledge of the control-to-output response A_{OL}(z).
- Obtain the denominator of A_{CL}(z) by a pole-zero matching s-to-z transformation.
- Derive the numerator of A_{CL}(z) such that the closed-loop response is of second order system [20].
- Derive the transfer function of an ideal compensator B_{ideal}(z) that yields the desired closed-loop response.
- Obtain the response of a template PID compensator B_{PID}(z) from the first three samples of the ideal compensator B_{ideal}(z) by evaluation of difference equations.

The designed PID compensator has been validated through Matlab simulations as a full closed-loop system with a 12V-to-1V SC-buck converter, operating at 800 KHz (L_a=L_b=0.5 μH; C_t=10 μF; C_o=200 μF). The target closed-loop parameters are crossover frequency of 80 KHz and phase margin of 50º. Fig. 3.5 shows the frequency response of the converter (blue), the 1/B_{PID} of the PID compensator (red) and the loop-gain (green), where the expressions for these discrete transfer functions are given in (5). It should be noted that the time delay due to the discrete implementation is taken into account and causes an additional phase shift at high frequencies close to f_s/2 [20].

$$
\begin{aligned}
A_{OL}(z) &= \frac{0.0416z + 0.0007382}{z^2 - 1.959z + 0.9661} \\
B_{PID}(z) &= \frac{15.34z^2 - 27.77z + 12.59}{z^2 - z} \\
LG(z) &= \frac{0.6381z^3 - 1.144z^2 + 0.5032z + 0.009292}{z^4 - 2.959z^3 + 2.925z^2 - 0.9661z}
\end{aligned}
\tag{5}
$$

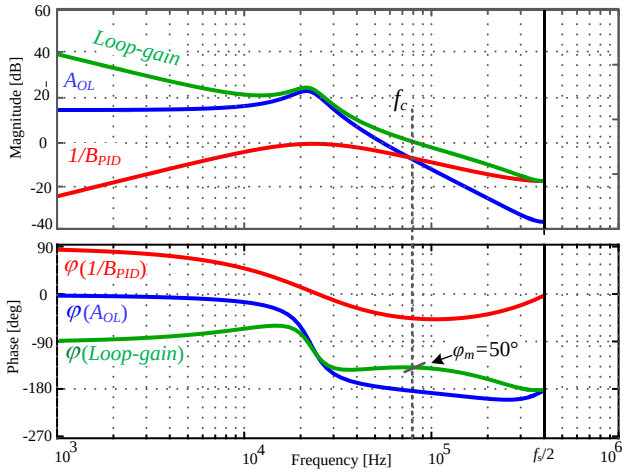


Fig. 3.5 Frequency responses of: control-to-output A_{OL} (blue), inverse compensator $1/B_{\mathrm{PID}}$ (red), and the Loop-Gain (green). Crossover frequency is marked f_c.

3.2.2. Sampling and Compensation

In conventional operation of switch-mode converters, the correction command (which can be the duty-ratio, on-time, off-time or frequency) is obtained once every switching cycle. As a result, in the context of control and modeling their dynamic behavior, such converters can be viewed as sample-data systems [21], [22]. This attribute fundamentally relates to the synchronized operation of the converter and therefore, variations within the switching cycle are so-called transparent to a linearized compensation scheme. In single-phase converters, it is considered superfluous to obtain information of the state-variable (e.g. the output voltage) more than once per switching cycle [23], [24]. On the other hand, in multiphase and interleaved converters, the correction rate of the control command can be expedited by a factor of the number of units that are employed, effectively improving the control bandwidth [25], [26]. That is, while each of the units operates at the base frequency, the effective frequency at which the system can be updated is multiplied by the number of units that are affecting the state-variable under regulation.

As opposed to a conventional single-phase converter, the operation of the SC-buck converter and the effect on the output voltage resembles more an interleaved one. The duty-ratio command can be updated twice per switching cycle since each of the phases is shifted by 180°, effectively doubles the rate that the output voltage can be regulated. The observer, i.e. in the case of digital realization the ADC, samples the output voltage at its ripple frequency of $2f_s$, and therefore the design of the controller can be fully optimized to achieve a loop-gain with higher bandwidth. The effect on the control-to-output frequency response

can be viewed by comparing Figs. 5 and 6, which demonstrate double bandwidth of the loop-gain from 80 KHz (Fig. 3.5) to 160 KHz as shown in Fig. 3.6 because of sampling and compensation at $2f_s$.

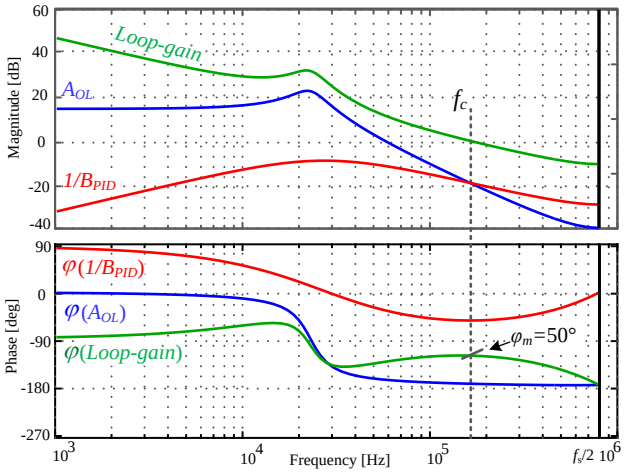


Fig. 3.6 The frequency responses for sampling the output at $2f_s$: control-to-output A_{OL} (blue), inverse compensator $1/B_{PID}$ (red), and the Loop-gain (green). Crossover frequency is marked f_c.

To verify the results that have been predicted theoretically and plotted using Matlab, a small-signal frequency response of the SC-buck has been extracted through a cycle-by-cycle simulation using PSIM. The simulation circuit setup is depicted in Fig. 3.7, where V_{sweep} is the excitation for the ac-sweep, the open-loop is given by $A_{OL}=V_{o\_sampled}/V_1$, the controller is given by $B_{PID}=V_2/V_{o\_sampled}$ and the loop-gain is given by $LG=V_2/V_1$. The resultant frequency responses for sampling and compensating at f_s and $2f_s$ are shown in Fig. 3.8(a) and Fig. 3.8(b), respectively. As can be observed, the results are in excellent agreement with the theoretical analysis.

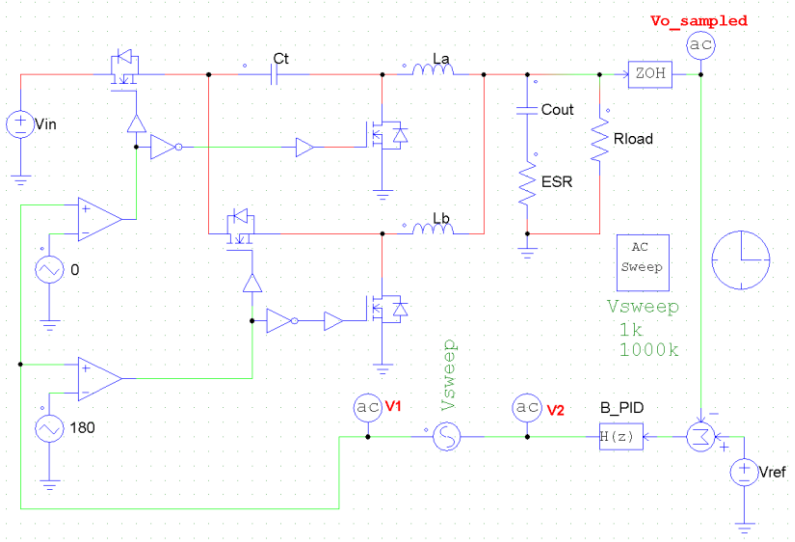


Fig. 3.7 PSIM simulation circuit setup for obtaining the small-signal frequency response using a cycle-by-cycle simulation.

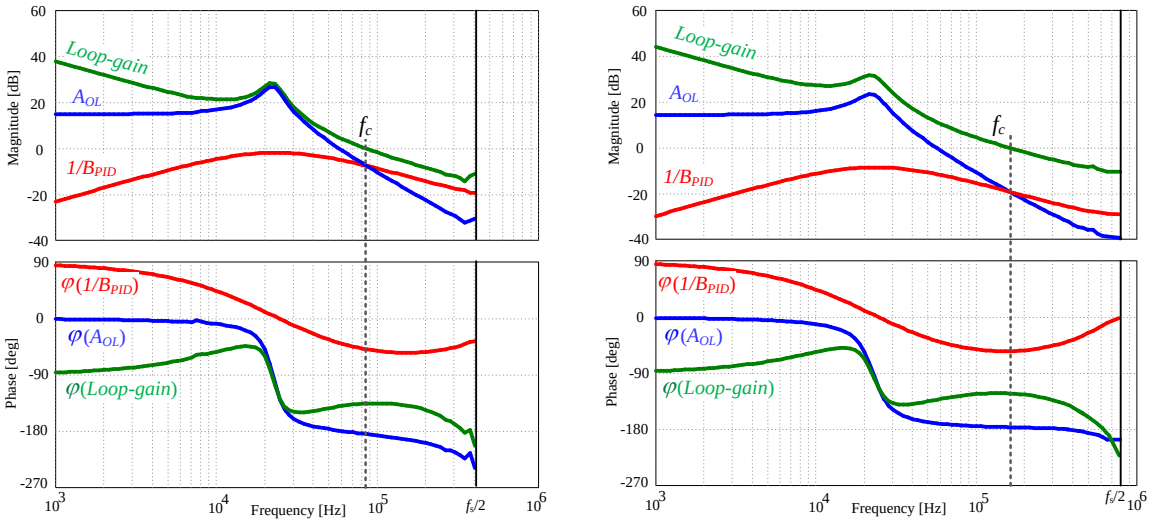


Fig. 3.8 Small-signal frequency response obtained by a cycle-by-cycle simulation for: (a) sampling and compensation at f_s, (b) sampling and compensation at $2f_s$.

Fig. 3.9 shows the different timing diagrams for the compensator operation for the case where the output voltage is sampled and the duty-ratio command is updated at the base frequency (Fig. 3.9(a)), and the case where the output voltage is sampled and the duty-ratio command is updated twice in every switching cycle (Fig. 3.9(b)). It can be seen that the higher sampling frequency reduces the time delay response of the controller from a maximum of T_s to a maximum of $T_s/2$, since in every instance there is a phase that can respond to a change in the duty-ratio command from the controller. It is important to note that this modification can be applied on the compensator of the SC-Buck converter without major hardware changes in the digital controller.

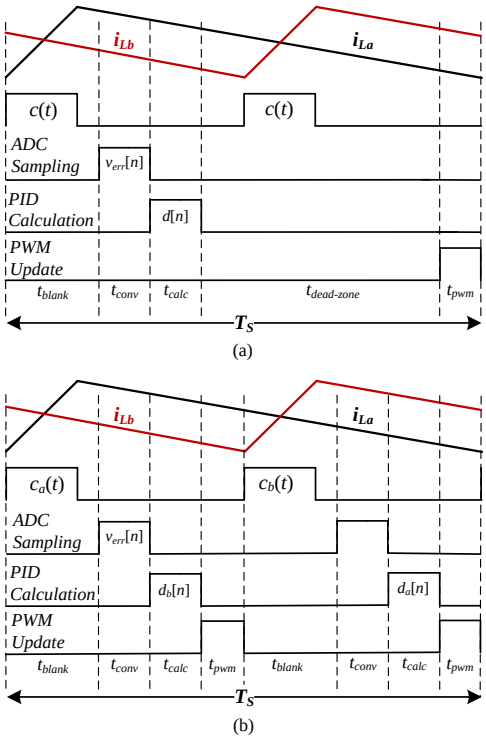


Fig. 3.9 Comparison of timing sequence: (a) one sample per switching period, (b) two samples per switching period.

To evaluate the difference between sampling once every cycle and twice every cycle, a simulation case study of an 800 KHz SC-buck converter response to a 10A loading transient has been conducted and its results are shown in Fig. 3.10. It can be observed that, due to the higher loop-gain bandwidth, the output voltage undershoot is reduced from 100mV to 60mV, and the settling time has been trimmed from 25μs down to 12μs when sampling at $2f_s$.

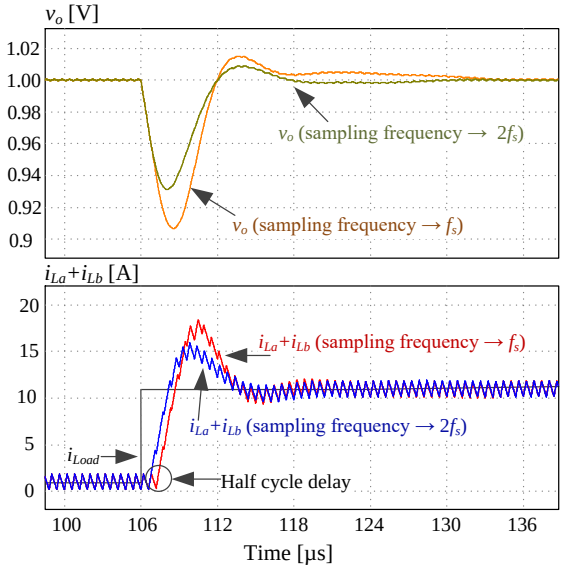


Fig. 3.10 Simulation results showing the differences in a 10A loading transient response between the cases of using a sampling frequency of f_s and $2f_s$.

3.3. State-Space Representation, Minimum-Deviation Control and Time-Optimal Control

To further enhance the performance of the SC-buck converter when dealing with load transients, it is essential to obtain the information of the possible state-trajectories of the converter in order to recover to the new steady-state operating point from a load transient. To facilitate the desired rapid recovery of the converter, a transient-mode controller is used in addition to the steady-state controller. In this study, a voltage-mode controller is assumed for steady-state operation and therefore the objective of the transient-mode controller is to minimize the output voltage deviation and/or recovery time of the converter in load transients, i.e. to generate a minimum-deviation [27], [28] or time-optimal responses [29]-[37]. This approach of using a dedicated transient-mode controller to handle load transients significantly reduces the burden and design requirements from the steady-state controller since it does not handle any load transients by itself. This way, the design of the steady-state controller can be loosen since it only has to maintain a zero voltage error at steady-state and handle the small mismatch between the inductors currents and load current that may occur at the end-of-transient instance. Unlike a conventional two-phase buck converter, in the SC-buck converter case, charge balance of the series-capacitor must be satisfied during the transient time to allow smooth transition back to the steady-state operation. This implies that the 'simple' on-off time-optimal cycle as carried out by many applications would not hold in this case and, as a matter of fact, would worsen the overall performance.

To realize the required switching sequence, the first task is to map the behavior of the state-variables with respect to the new load conditions [38]-[41], then the required switching sequence can be derived from the trajectories' map of the state-variables on the state-plane. It should be noted that for simplicity of the following analysis, parasitic components, e.g. ESR and ESL, are neglected since it is found that they have relatively minor effect [42].

The state equations for state-1 can be expressed as:

$$\frac{dv_C}{dt} = \frac{1}{C_o}\left(i_{L_a} + i_{L_b} - \frac{v_C}{R_L}\right), \tag{6}$$

$$\frac{di_{L_a}}{dt} = \frac{V_{in} - v_{Ct} - v_C}{L_a}, \qquad \frac{di_{L_b}}{dt} = \frac{-v_C}{L_b}, \tag{7}$$

Substituting (6) into (7) and after some manipulations, the expression for i_{La} can be expressed as:

$$i_{L_a} = i_{L_a}(0) - \frac{L_a}{L_b}\frac{V_{in}/2 - v_C}{v_C}\left(i_{L_b} - i_{L_b}(0)\right), \tag{8}$$

where $i_{La}(0)$ and $i_{Lb}(0)$ are the inductors' currents at the beginning of state-1. As can be seen in (8), the current difference of i_{La} - $i_{La}(0)$ depends on the current difference of i_{Lb} - $i_{Lb}(0)$. It should be noted that since the same on-time is used for both states 1 and 3, the series-capacitor voltage automatically converge to $V_{in}/2$ [11], which is a typically the desired design. Therefore, substituting (8) and (7) into (6) and assuming $v_{Ct}=V_{in}/2$ yields:

$$\frac{C_o}{3}v_C^{\,3} - L_b\frac{i_{L_b}}{R_L}v_C^{\,2} + \left(i_{L_b}^{\,2}L_b + i_{L_b}L_b i_{L_a}(0) - i_{L_b}L_b i_{L_b}(0)\right)v_C + L_b V_{in}\left(\frac{i_{L_b}i_{L_b}(0)}{2} - \frac{i_{L_b}^{\,2}}{4}\right) + const_b = 0 \tag{9}$$

where $const_b$ is defined by the initial values of i_{Lb} and v_C at the beginning of state-1 The first solution of this function yields the state-1 trajectories of the converter in the form of $v_C=f(i_{Lb})$ with three initial conditions: $i_{La}(0)$, $i_{Lb}(0)$ and $v_C(0)$.

By symmetry in the operation of state-3 to state-1 and proper variable assignment, the state-trajectories for state-3 are derived from (9). The variables are assigned as: $v_{Ct}=V_{in}/2$, i_{La} swaps with i_{Lb}, and L_a swaps with L_b. This results in:

$$\frac{C_o}{3}v_C^{\,3} - L_a\frac{i_{L_a}}{R_L}v_C^{\,2} + \left(i_{L_a}^{\,2}L_a + i_{L_a}L_a i_{L_b}(0) - i_{L_a}L_a i_{L_a}(0)\right)v_C + L_a V_{in}\left(\frac{i_{L_a}i_{L_a}(0)}{2} - \frac{i_{L_a}^{\,2}}{4}\right) + const_a = 0 \tag{10}$$

where $const_a$ is defined by the initial values of i_{La} and v_C at the beginning of state-3

States 2 and 4, which are the off states, are identical and the state equations can be expressed as:

$$\frac{dv_C}{dt} = \frac{1}{C_o}\left(i_{L_a} + i_{L_b} - \frac{v_C}{R_L}\right), \tag{11}$$

$$\frac{di_{La}}{dt} = -\frac{v_C}{L_a}\ ,\ \frac{di_{Lb}}{dt} = -\frac{v_C}{L_b}, \tag{12}$$

Using (11) and (12), the expression of i_{La} can be derived:

$$i_{L_a} = i_{L_a}(0) + \frac{L_a}{L_b}\left(i_{L_b} - i_{L_b}(0)\right), \tag{13}$$

and the state trajectories for each state are obtained by the variable assignment as described earlier.

Substituting (13) and (12) into (11) yields

$$v_C{}^2 \frac{C_o}{2} - v_C \frac{L_a}{R_\mathrm{L}} + L_a \left(i_{L_a}{}^2 + \left(i_{L_b}(0) - i_{L_a}(0) \right) i_{L_a} \right) + const = 0 \quad , \tag{14}$$

where *const* is defined by the initial values of the inductors' currents and output voltage at the beginning of the state-2 or state-4. Solving (14) yields the trajectories of the converter $v_C = f(i_{La})$ for states 2 and 4.

Following the above derivations, the state trajectories for the SC-buck converter are defined as a conventional buck converter with two expansions. First, the converter includes two on-states (state-1 and state-3) and two identical off states (state-2 and state-4). The second expansion is that there are three initials conditions instead of two. As a result, the procedure to obtain the graphical state-space map as presented in Fig. 3.11 is as follows:

- Horizontal axis variable for all states is the output capacitor voltage v_C.
- For states 1 and 2, the vertical axis variable is i_{Lb}; for states 3 and 4 i_{La} is used as the vertical axis. i.e., the state-variable is the inductor current that is currently in off state (with direction down toward the horizontal axis) is used as the vertical axis.
- The progress direction of all the trajectories is down along the vertical axis.
- Transition on the map between states 1 to 3 is not continuous, but depends on the actual value of the inductors currents. Because of this so-called singularity, it is possible to view the climb-up of the inductor current from a lower point to a higher one, as depicted in Fig. 3.12.

The procedure enables to draw a state-space map with two trajectories instead of four, where states 1 and 3 share one trajectory (on) and states 2 and 4 share the other (off), and as a consequence two-dimensional state-plane instead of three-dimensional state-space can be used. This is facilitated by duplication of the vertical axis such that it represents both i_{La} and i_{Lb} as shown in Fig. 3.11. The blue (solid) trajectories represent an on state; state-1 is monitored by i_{Lb} and state-3 is supervised by i_{La}. The red (dotted) trajectories represent an off state; state-2 is monitored by i_{Lb} and state-4 is supervised by i_{La}. For an easier view, a single trajectory is depicted in Fig. 3.12 for a case of a loading transient (full movement along the trajectory is detailed in the next sub-section).

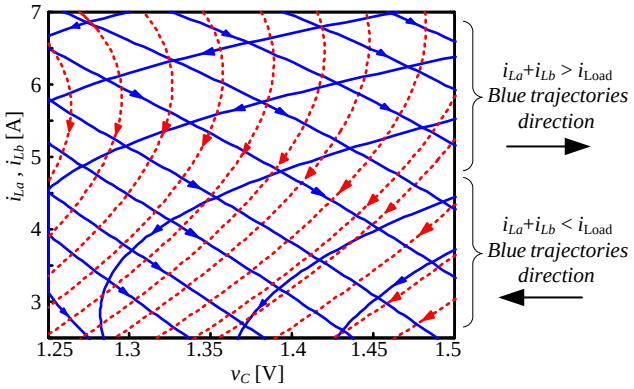


Fig. 3.11 State-space map for the SC-buck converter. On (states 1 and 3-solid-blue) and off (states 2 and 4 - doted red) trajectories.

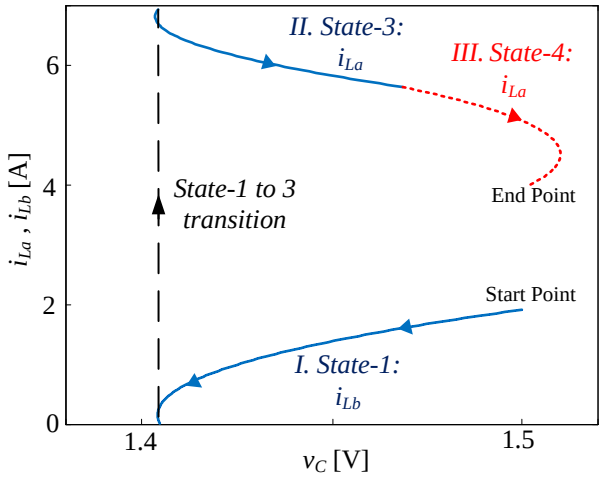


Fig. 3.12 Optimal trajectories for loading transient: I. On period of phase *a* (state-1). II. On period of phase *b* (state-3). III. Off period of both phases (state 2 or 4). Note the singular transition point – monitoring different currents using the same plot.

The state trajectories derived in (9), (10) and (14), and depicted in Fig. 3.11 are quite complex and it is hard to decipher the dynamic properties of the converter and to define a control law based on them. To overcome this challenge, a new state-variable is defined as the sum of inductors currents $i_{sum} = i_{La} + i_{Lb}$. The output capacitor voltage is maintained as the second state-variable that is used. Using this set of state-variables, the state-equations for state 1 are given by:

$$\frac{di_{sum}}{dt} = \frac{\left(V_{in} - v_{Ct}\right)\dfrac{L_b}{L_a + L_b} - v_C}{L_a \parallel L_b}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \dfrac{v_C}{R_L}}{C_o}, \tag{15}$$

for state 3 given by:

$$\frac{di_{sum}}{dt} = \frac{v_{Ct}\dfrac{L_a}{L_a + L_b} - v_C}{L_a \parallel L_b}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \dfrac{v_C}{R_L}}{C_o}, \tag{16}$$

and for states 2 and 4 given by:

$$\frac{di_{sum}}{dt} = -\frac{v_C}{L_a \parallel L_b}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}. \tag{17}$$

Under the assumptions of identical on-times for states 1 and 3 and the same inductance used in both phases, i.e. $v_{Ct}=V_{in}/2$ and $L_a=L_b=L$, expressions (15) and (16) of the on states are identical and given by:

$$\frac{di_{sum}}{dt} = \frac{V_{in}/4 - v_C}{L/2}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}, \tag{18}$$

and (17) for the off states can now be re-written as:

$$\frac{di_{sum}}{dt} = -\frac{v_C}{L/2}, \qquad \frac{dv_C}{dt} = \frac{i_{sum} - \frac{v_C}{R_L}}{C_o}. \tag{19}$$

The resultant set of state equations [(18) for the on states and (19) for the off states] exactly match the state equations of a conventional buck converter with an input voltage of $V_{in}/4$ and inductor of $L/2$. This also implies that the state trajectories of the SC-buck are the same as a conventional buck converter. The state trajectory for the on states is given by:

$$C_o\left(v_C - \frac{V_{in}}{4}\right)^2 + \frac{L}{2}\left(i_{sum} - I_{Load}\right)^2 = C_o\left(v_C(0) - \frac{V_{in}}{4}\right)^2 + \frac{L}{2}\left(i_{sum}(0) - I_{Load}\right)^2, \tag{20}$$

And for the off states the state trajectories are

$$C_o v_C^2 + \frac{L}{2}\left(i_{sum} - I_{Load}\right)^2 = C_o v_C^2(0) + \frac{L}{2}\left(i_{sum}(0) - I_{Load}\right)^2, \tag{21}$$

where I_{Load} is the load current and equals V_o/R_L, $i_{sum}(0)$ is the initial value of the sum of inductor currents, i.e. $i_{La}(0)$ and $i_{Lb}(0)$, and $v_C(0)$ is the initial value of the output capacitor voltage. Plotting these trajectories on the state plane (v_C, i_{sum}) result in two ellipses with centers at ($V_{in}/4$, I_{Load}) for the on states and (0, I_{Load}) for the off states, as depicted in Fig. 3.13.

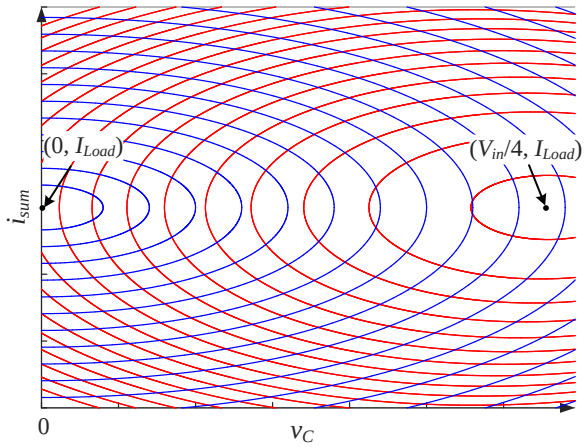


Fig. 3.13 State-plane of the SC-buck with v_C and i_{sum} as the state-variables.

By observing the above trajectories and based on previous studies [36], a time-optimal control law can be derived by following the trajectory depicted in Fig. 3.14 for a loading transient. However, such movement might be deceptive since it is not guaranteed that all the four state-variables of the SC-buck (i_{La}, i_{Lb}, v_{Ct}, v_C) converter reach their new steady-state operating point. One reason is that there is a degree of freedom in i_{sum}, i.e. there is no guarantee the each of the inductors currents are in their new steady-state operating point if their sum reach its steady-state operating point. A simple example is that one inductor carries the load current by itself while the other inductor current is zero. A second reason is that the series-capacitor voltage is not described on this state-plane and therefore its voltage is not controlled. Therefore, a necessary (and not sufficient) condition for time-optimal response is a movement on the state-plane as depicted in Fig. 3.14. To overcome these issues, two controllers have been developed and are detailed in the following subsections.

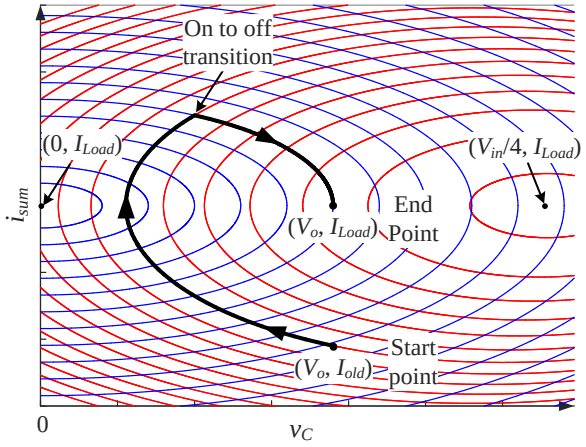


Fig. 3.14 Time-optimal movement on the state-plane for a loading transient.

3.3.1. Minimum-Deviation Transient-Mode Controller

Observation of the resultant state-space map for the SC-buck converter reveals one of the main differences of this converter topology with respect to a multi-phase buck. As exemplified by Fig. 3.15(a), during an on state while one of the inductors currents ramps up and may satisfy the required charge balance to the output, the other phase's inductor current ramps down and may result in unstable convergence around the new steady-state point. In addition, since only one phase carries the load, the minimum possible deviation is not obtained. It should be noted that for demonstration purposes, the load transient convergence in Fig. 3.15(a) has been obtained using an extremely overly-sized series-capacitor (1 mF) to hold the charge during the exceedingly long on time. The situation worsens when C_t is sized to the steady-state requirements (50 µF in the simulated case) as depicted in Fig. 3.15(b), which results in divergence from the new steady-state operating point.

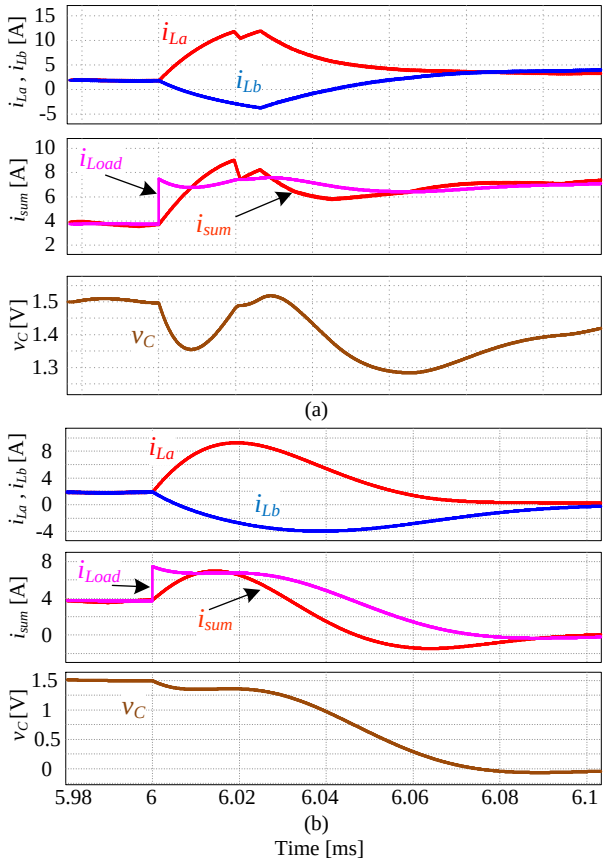


Fig. 3.15 Attempts of time-optimal recovery from loading transient with uneven distribution of the on phases: (a) large series-capacitor (1 mF) and (b) steady-state sized series-capacitor (50µF).

Based on the behavior of the converter and by observing the trajectories' map, better results are obtained by distribution of the on periods between the phases. As presented in

Fig. 3.12, switching between one on sequence to another, and then applying the off phase, results in a smaller voltage drop, down to the minimum-deviation of v_C.

To facilitate fast transient detection and end-of-transient phase, the first is assisted by two auxiliary comparators with thresholds very close to the reference output voltage ($V_{th,H}$ and $V_{th,L}$, see Fig. 3.1). The comparators assist in the detection of both loading and unloading transients to initiate the operation of the transient-mode controllers.

A minimum-deviation switching sequence for the SC-buck converter is as follows (described for loading transient):

- At the detection of a load change by comparator *cmp2*, the controller switches to one of the on states (1 or 3).
- A second on period of the alternating phase is initiated when sum of the currents equals to the new load current. This point is detected by the event of the output voltage reaching its minimum point [27].
- Third, an off state (state 2 or 4) can be initiated based on the charge balance of the output capacitor, which can be achieved by transient time calculation. Q_{charge} and $Q_{\text{discharge}}$, which represents the value of the output capacitor charge and discharge, must be equal, as shown in Fig. 3.17. By assuming that the sum of the inductors current $i_{La}+i_{Lb}$ ramps up with a slope of $(V_{\text{in}}/2-2V_o)/L$, and ramps down with a slope of $-2V_o/L$, the second on state ends when $T_3=T_1D_o^{0.5}$ [31], where D_o is the duty-ratio seen by the output capacitor (due to summing of the two inductors currents), and is given by

$$D_o = 4\frac{V_o}{V_{in}}. \tag{22}$$

This assures the desired equilibrium and can be implemented using counters.

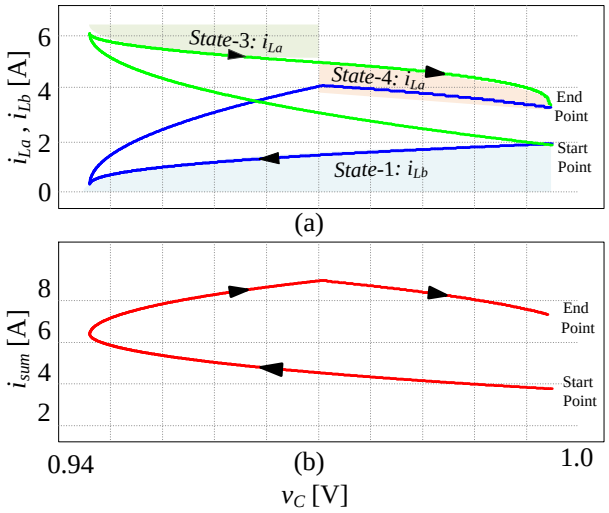


Fig. 3.16 Simulation results of a loading transient on the state-plane: vertical axis is (a) the inductor currents, (b) the sum of the inductors currents.

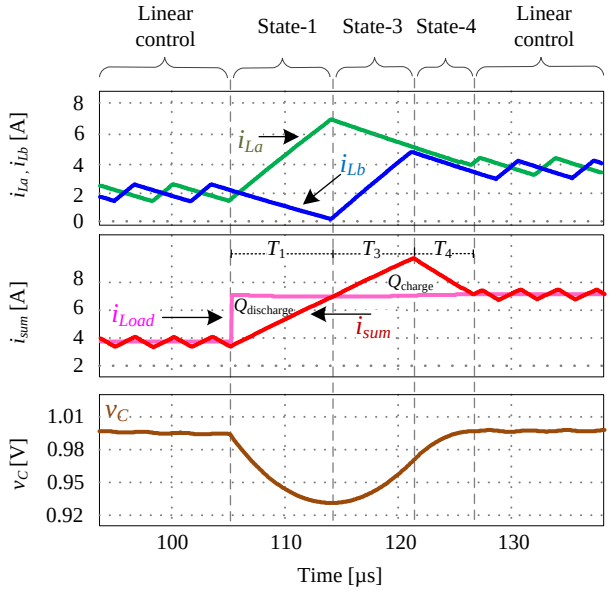


Fig. 3.17 Minimum-deviation recovery sequence for a loading transient.

The method of detecting the point where the sum of inductors current equal the new load current is by detection of the peak\valley of the output voltage. However, it should be noted that the voltage value of the peak\valley is not important. Only the event of reaching a peak\valley is important, and that is the reason for searching the point where the slope of the output voltage is zero. The method for detection of the voltage valley point (or the current cross-over point) in the presented SC-buck converter is the same as in any other time-optimal algorithm for buck converters that requires this kind of detection, and therefore it is not considered as a main contribution in the paper. These methods include sensing of the output voltage (either with ADC or analog sensing), sensing the output capacitor current

or estimating the output capacitor current [27], [30]-[32], [43]. It should be noted that direct sensing of the inductor current for this purpose is possible only in single phase converters. In the SC-buck converter the currents of both phases need to be sensed in order to detect the instance when their sum equals the load current. For this reason, we have shown and used one method out of several that have been presented in previous studies. The detection method has been implemented by observing the derivative of the output voltage and detecting its zero-crossing, in a similar approach as detailed in [27].

Fig. 3.16 and Fig. 3.17 demonstrate the full sequence procedure for a loading transient, showing the individual inductors currents, sum of the currents, and the output capacitor voltage for both the time-domain and the state-plane. As can be seen, the resulting recovery trajectory of the sum of currents exactly matches a time-optimal behavior for a loading transient of single-phase buck converter. However, as will be discussed in the following subsection, although the response may seem like a time-optimal one, it is only a minimum-deviation response. This is since the series-capacitor is being over-charged or discharged during the transient period, which results in oscillations after the end of transient. In fact, to obtain a true time-optimal response, all the four state-variables (v_C, v_{Ct}, i_{La}, i_{Lb}) must reach the new steady-state operation point at the minimum possible time. In the above case, three out of the four state-variables reach the new steady-state point, but the fourth one which is v_{Ct} is now at the correct point at the end of transient. Therefore, although the output voltage deviation is minimal, additional time is needed to move v_{Ct} to the new steady-state operation point and fully recover from the load transient, which implies that this is not a true time-optimal response.

In addition to loading transients, the transient-mode controller is also capable of handling unloading transients. For this case there is more similarity to a conventional buck converter since the off state (2 or 4) is quite similar and differs in the slew-rate of the output current ($-V_o/L$ for buck and $-2V_o/L$ for SC-buck). Fig. 3.18 and Fig. 3.19 demonstrate the full sequence procedure for an unloading transient, showing the individual inductors currents, sum of the currents, and the output capacitor voltage for both the time-domain and the state-plane.

For unloading transients, the switching procedure is as follows:

- At the detection of an unloading transient by comparator *cmp1*, the controller switches to one of the off states (2 or 4).

- Second, an on state (distributing between the two phases) is initiated based on the charge balance of the output capacitor, which achieved by transient time calculation. By assuming that the sum of the inductors currents i_{La}+i_{Lb} ramps down with constant slope of -2V_o/L, and ramps up with a slope of (V_{in}/2-2V_o)/L, the off state ends when T_{4b}=T_{4a}(1-D_o)$^{0.5}$ [31] (see Fig. 3.19), where D_o is given by (22).

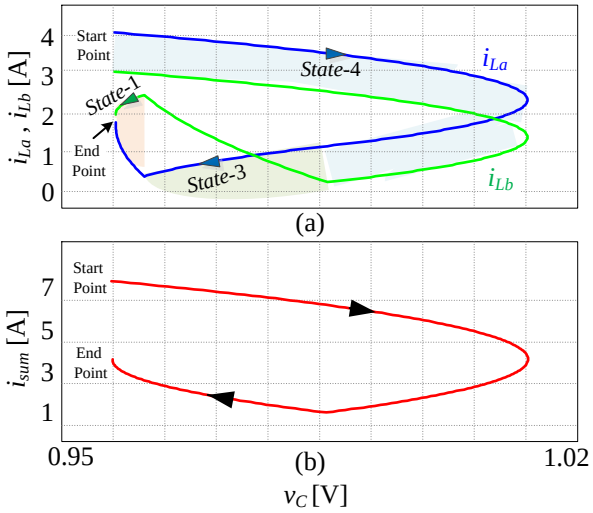


Fig. 3.18 Simulation results of unloading transient on the state-plane: vertical axis is (a) the inductor currents, (b) the sum of the inductors currents.

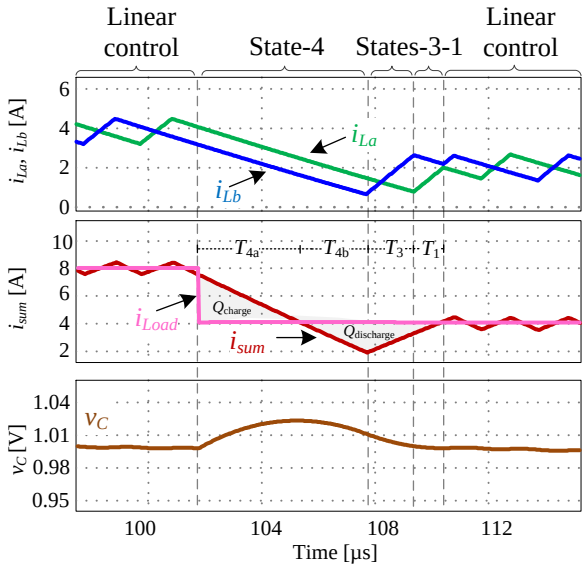


Fig. 3.19 Minimum-deviation recovery sequence for unloading transient event.

3.3.2. Synchronized Time-Optimal Controller by Duty-Ratio Saturation

As can be observed in Fig. 3.20, the first on time during the transient is significantly prolonged compared to the on time in steady-state operation, which may result in over-charge (or discharge) of the series-capacitor. Since the distribution of the on time between the phases is not equal, i.e. $T_1 \neq T_3$, the series-capacitor voltage v_{Ct} can no longer be assumed as a constant that equals $V_{in}/2$. As a result, the inductors currents at the end of transient are not equal. At this point, although the output voltage is not affected by it, oscillations of the currents occur since $V_{Ct} \neq V_{in}/2$ and $T_a = T_b$. The reason for these oscillations is the fact that the design of the controller assumes that v_{Ct} is constant and the input voltages of the two phases are equal. To overcome this issue, an improved transient-mode controller that produces a time-optimal response, i.e. moving all the four state-variables to the new steady-state operation point in the minimum possible time, has been developed. One possibility to solve this issue is to increase the series-capacitor's size to reduce the magnitude of the oscillations; however, as seen in the previous section, this requires an overly sized capacitor, which is prohibitive in volume-sensitive applications. An alternative solution that has been adopted here is to distribute the task of the on state between the two phases. This is shown in Fig. 3.22 and facilitated by assignment of even on times between the two phases while limiting the switching frequency. An equivalent approach to the minimum-deviation method presented earlier is achieved by saturation of the duty-ratio to its maximum value for the SC-buck converter, i.e. to D=0.5, for ramping up the inductors currents. Using this approach, v_{Ct} remains virtually constant and equals $V_{in}/2$ throughout the duration of the load transient, and as a result the inductors currents are equal at the end of transient (within the current ripple) and oscillations of them after the transient are prevented. In fact, to completely avoid any change in v_{Ct}, the switching frequency during the transient must be infinite. Since voltage ripple of the series-capacitor is allowed and exists also in steady-state operation, there is no need to reduce it to zero for the transient period. In a properly designed converter, typical voltage ripple of the series-capacitor is 5-10% of the nominal voltage under every load conditions, and using the synchronized time-optimal controller the maximum voltage ripple can be estimated since the duty-ratio (and on-time) of the phases is known. Therefore, the switching frequency for the transient period remains the steady-state switching frequency, and although a small error of the series-capacitor voltage may appear at the end of transient, it is small and within the voltage ripple magnitude and can be handled by the steady-state controller without causing an addition transient. Although more switching

actions are used during the transient and as a consequence the switching losses may increase, they are negligibly small as the switching frequency remains the same as in steady-state operation. It should be noted that switch commutation times may impact the transient time due to an effective duty ratio that is lower than 0.5, but since they are small compared to the on times of a switches and their effect is very small. In addition, switch commutation times do not impact the series-capacitor voltage since there is current flowing through the series-capacitor only during the two on states.

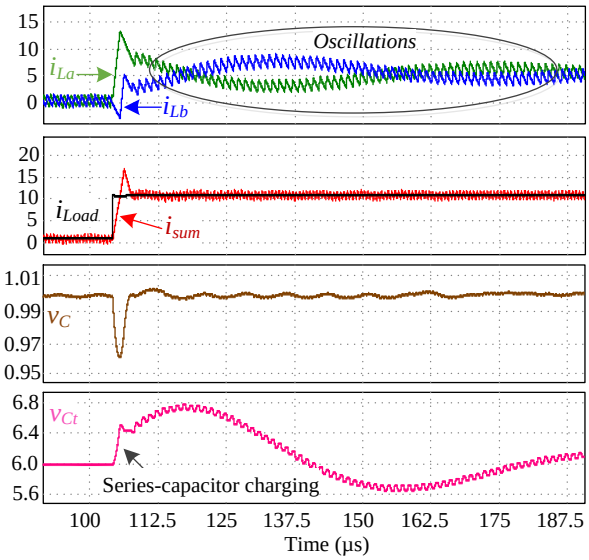


Fig. 3.20 Oscillations of i_{La} and i_{Lb} after the transient due to charging of the series-capacitor during the transient period when using the minimum-deviation controller.

Fig. 3.22 and Fig. 3.21 demonstrate the full switching sequence of the duty-ratio saturation approach for a loading transient in both time-domain and in the state-planes. At the detection of a loading event, the controller saturate the duty-ratio to D=0.5 and the on time is equally shared between the phases. Next, an off state (state 2 or 4) is initiated based on the charge balance of the output capacitor as described for the minimum-deviation controller in the previous subsection. It can be seen in Fig. 3.22 that, although the switching frequency is finite and there are small errors in the inductors currents, the difference between the inductors currents remains within the current ripple during as well as after the transition period, the voltage of the series-capacitor is virtually constant and the oscillations are avoided. It should be noted that in order to avoid any mismatches in the inductors currents and series-capacitor voltage at the end of transient, the switching frequency during the transient period should be infinite. The infinite switching frequency is required in order to overcome any situation where one of the phases has more on states than the other and charge balance of C_t is not fully maintained. However, in a properly designed converter where C_t

is designed to have small ripple, excellent charge balance can be obtained when operating at the steady-state switching frequency for the transient period. Another significant advantage of this approach is the fast that the DPWM is not bypassed for the transient period and synchronization in the system is maintained. This feature enables a smoother transition between the steady-state and transient-mode controllers.

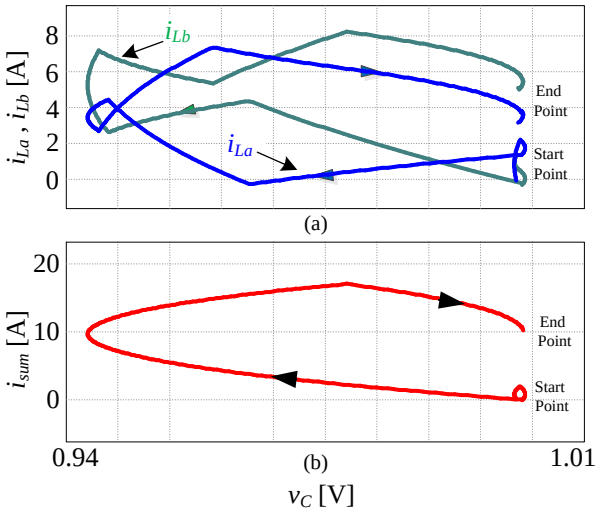


Fig. 3.21 Simulated loading transient response of the synchronized time-optimal controller using duty-ratio saturation on the state-plane. Vertical axis is (a) the inductors currents, (b) the sum of the inductors currents.

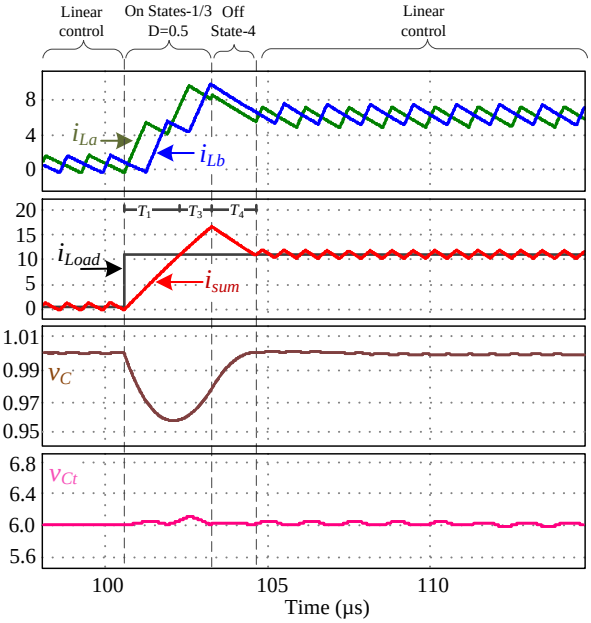


Fig. 3.22 Simulated time-domain response of a loading transient of the synchronized time-optimal controller using duty-ratio saturation.

To verify that time-optimal response is facilitated, the movement of the state-variables along the trajectories is examined for both approaches by observation of the output voltage and the sum of the inductors currents. Consequently, the resultant state-plane maps (see

Figs. 15, 17 and 20) resembles one of a conventional buck converter. It can be observed from Figs. 15 through 21 that, the resultant optimal trajectory is the one where the minimum output voltage deviation is obtained, i.e. as in conventional time-optimal control [43].

The unloading response when using the time-optimal controller is very similar to an unloading transient using the minimum-deviation controller, as shown in Fig. 3.23. The difference between the two is only in the distribution of the on times between the two phases. While the time-optimal controller distributes the on-time evenly between the phases by setting the duty-ratio to 0.5 in states 1 and 3, the minimum-deviation controller don't necessarily do so. Since the on-time in high conversion ratio is very short and the switching frequency in finite, there is a negligibly small difference between the responses of the controllers. The reason is that for this case the on-time just before the end of transient is very short since D_o is small. For this reason, the response shown in Fig. 3.23 is very similar to the one shown in Fig. 18. The state-space response is not presented here due to very high similarity to the one shown in Fig. 3.18. Nevertheless, in the following experimental section all the transient responses are shown.

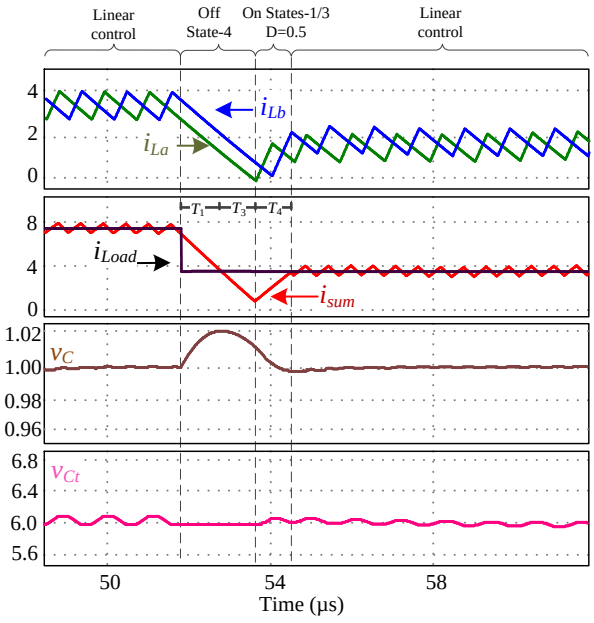


Fig. 3.23 Simulated time-domain response of an unloading transient of the synchronized time-optimal controller using duty-ratio saturation.

3.4. Experimental Results

To validate the operation of the voltage-mode controller that is based on the average-behavioral small-signal model and the transient-mode controller, a 12-to-1V SC-buck

converter prototype that operates at 800 KHz has been built and tested. The main components of the prototype are listed in TABLE I. The digital controller comprises the steady-state voltage-mode compensator and the transient-mode controller as shown in Fig. 3.1. The controller has been entirely realized on Altera Cyclone IV FPGA [44], including custom design of all related peripherals with an all-digital delay-line window-ADC and DPWM as described in [45], [46] and the total number of logic elements that were used is 1214 for the entire controller. Load transient signals were also generated by the FPGA, independently, without synchronization to the controller.

In this study Delay-line based window-ADC has been used for sampling the output voltage during steady-state operation. This architecture of ADC provides accurate measurement with modest hardware, and its full details and principle of operation are given in [46]. In the presented experimental setup, a 6-bit window-ADC is used. The ADC's sampling rate is set to be twice the switching frequency, i.e. $f_{sampling}$=1.6 MHz, with resolution of 5mV/bit.

The comparator's thresholds have been designed to be close enough to the nominal voltage for accurate transient detection and operation but also far enough from it to avoid false triggering of the transient-mode controller, as detailed in [27], [47], [48]. Therefore, for the presented experimental setup the thresholds were designed to be 1V±20mV. The comparators' voltages thresholds generating circuit is described in Fig. 3.24.

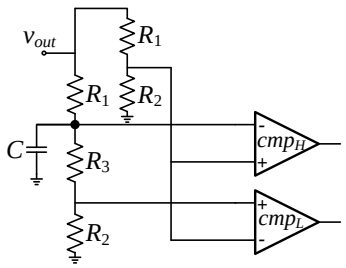
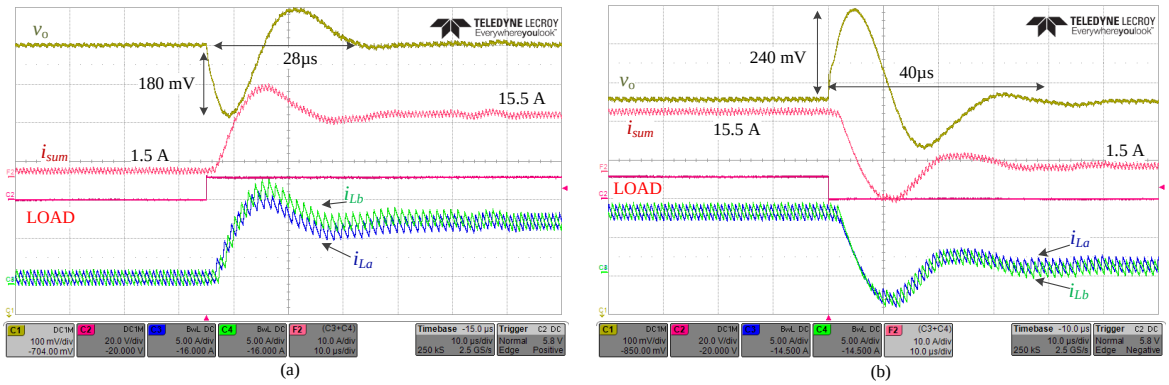


Fig. 3.24 Comparators references voltages generating circuit.

TABLE I. EXPERIMENTAL PROTOTYPE PARAMETERS

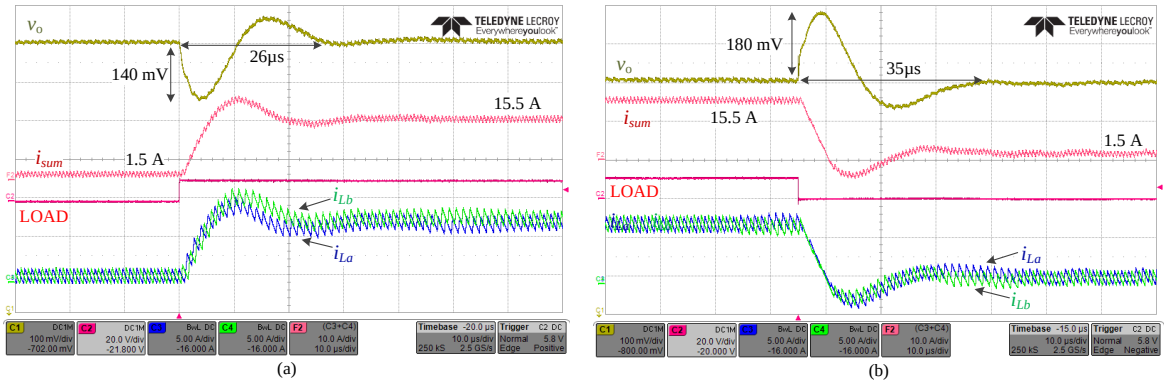
Parameter	***Value***
Inductors L_a, L_b	0.5 µH
Series-capacitor C_t	10 µF
Output capacitor C_o	200 µF
Output capacitor ESR R_c	1.5 mΩ
Switching frequency f_s	800 KHz
Comparator Voltage Reference $V_{ref,H}$	V_o + 20mV
Comparator Voltage Reference $V_{ref,L}$	V_o - 20mV

Fig. 3.25 and Fig. 3.26 show the operation of the digital voltage-mode controlled SC-buck converter with the transient-mode controller disabled, handling loading and unloading transients to compare the difference between a sampling frequency of f_s and $2f_s$, respectively. For a 14A loading transient, sampling at f_s - the output voltage undershoot and settling time are 180mV and 28µs, respectively. Sampling at $2f_s$ - the output voltage undershoot is reduced to 140mV and the settling time to 26µs. For an unloading transient of 14A the output voltage overshoot is 240mV and the settling time is 40µs with sampling at f_s, compared to 180mV overshoot and 35µs settling time with sampling at $2f_s$. It can be observed that there is a significant delay when sampling at f_s at the beginning of the transients due to the delay of $T_s/2$, as predicted by the evaluation in Section II.



(a) (b)

Fig. 3.25 Voltage-mode controller response for sampling at f_s to a (a) 1.5A → 15.5A loading transient (b) 15.5A → 1.5A unloading transient. C1 – v_o output voltage (100mV/div), C2 – Load step signal, C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div.



(a) (b)

Fig. 3.26 Voltage-mode controller response for sampling at $2f_s$ to a (a) 1.5A → 15.5A loading transient (b) 15.5A → 1.5A unloading transient. C1 – v_o output voltage (100mV/div), C2 – Load step signal, C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div.

Fig. 3.27 depicts the minimum-deviation transient-mode controller response to 14A loading and unloading transients. As can be seen, with this control law the output voltage deviations and settling times are significantly reduced compared to the voltage-mode

controller. For a 14A loading transient, the output voltage undershoot is 80mV and transient time is 6µs, and for a 14A unloading transient the output voltage overshoot is 120mV and the transient time is only 8µs. However, as predicted by the analysis and simulations in Section III, it can be observed that oscillations of the inductors current occur due to over-charge of the series-capacitor, which implies that this is not a time-optimal response as one of the four state-variables is not at the correct operating point at the end of transient and result in increased settling times of 43µs for loading and 26µs for unloading.

Fig. 3.28 shows time-domain and state-plane representation for 14A load transient response of the synchronized time-optimal transient-mode controller. As can be seen, the output voltage deviations are the same as in the case of the minimum-deviation controller in Fig. 3.27, but the settling times are significantly reduced since the oscillations of the inductors currents are avoided. This is since v_{Ct} remains approximately constant (within ripple margins) for the transient period, despite of the fact that the two phases has unevenly distributed on-times, i.e. phase *a* has 4 on-times and phase *b* has only 3 on-times during the transient (See Fig. 3.28(a)). In addition, the state-plane representation validates the analysis of the time-optimal trajectories from Section III. It should be noted that there is noticeable regulation process after the end of transient, in a similar manner as allowed by VRM applications [49]. However, this regulation is required due to small errors in the inductors currents at the end of transient that happen due to finite switching frequency. Since these errors are small, the steady-state controller can handle them without any significant output voltage overshoot or undershoot.

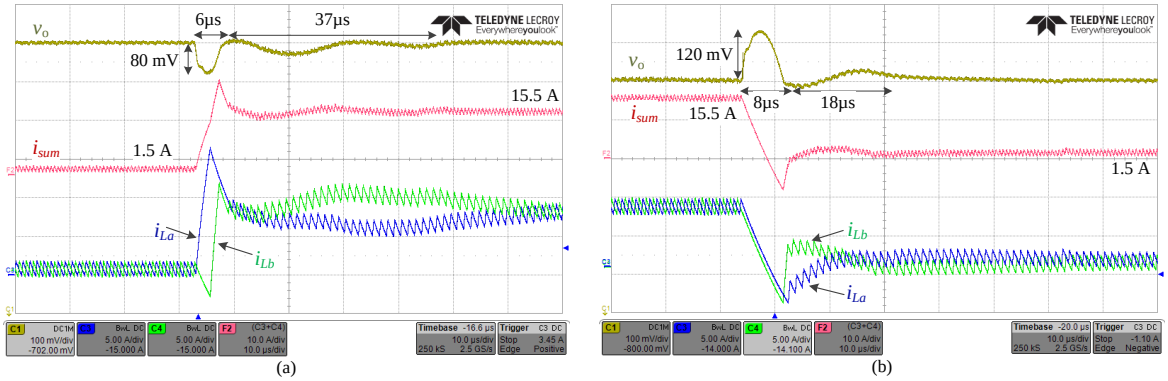


Fig. 3.27 Minimum-deviation controller response to a (a) 1.5A → 15.5A loading transient (b) 15.5A → 1.5A unloading transient. C1 – v_o output voltage (100mV/div), C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div.

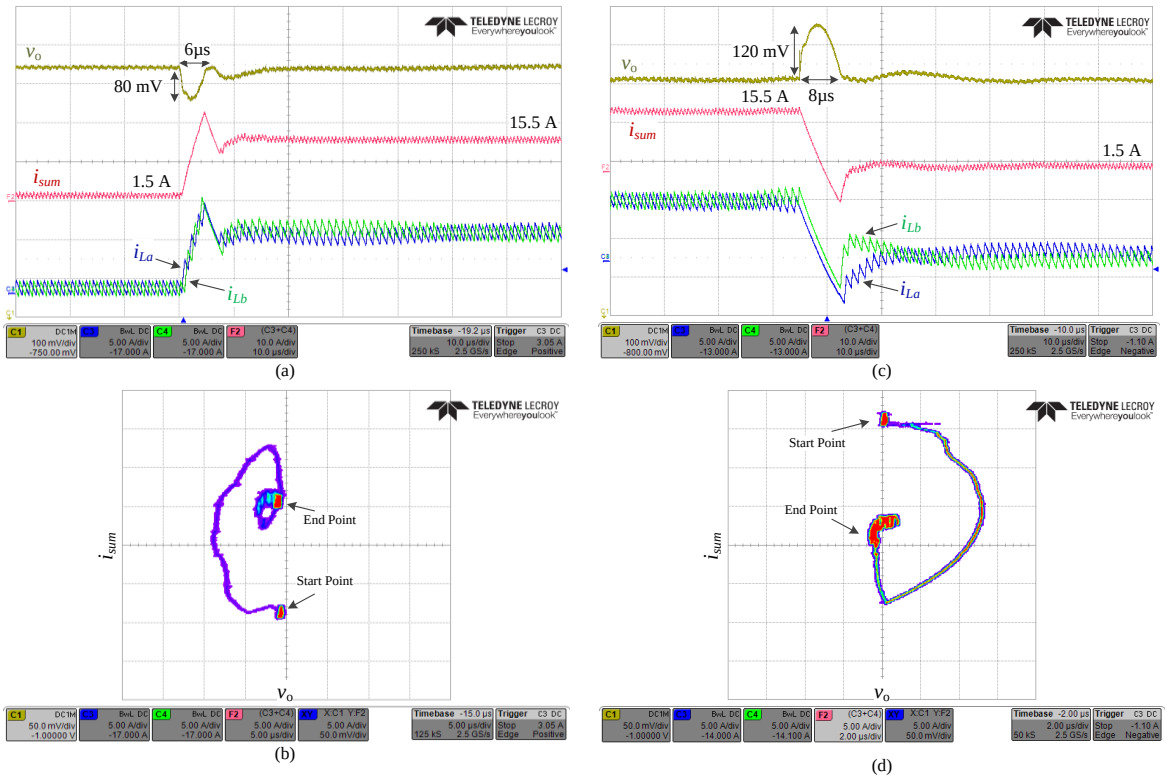


Fig. 3.28 Time-domain and state-plane representation response of the synchronized time-optimal controller to a 1.5A → 15.5A loading transient [(a), (b)] and 15.5A →1.5A unloading transient [(c), (d)]. For (a) and (c): C1 – v_o output voltage (100mV/div), C3 - i_{La} (5A/div), C4 - i_{Lb} (5A/div), F2 – Sum of inductors currents i_{sum} (10A/div). Time scale is 10µs/div. for (b) and (d): horizontal axis is v_o (50mV/div), vertical axis is sum of inductors currents i_{sum} (5A/div).

3.5. Conclusion

In this study, an optimal closed-loop control scheme for a series-capacitor buck converter has been presented. The controller, which has been realized on a digital platform, merges a voltage-mode controller for steady-state operation and a transient-mode time-optimal controller for load transients. In the theoretical analysis, an average-behavioral model as well as state-space representation of the converter have been derived, then two transient-mode controllers have been developed. The analysis revealed that a key factor for recovery of the converter from load transients is the capability of the controller to satisfy the charge-balance of the series-capacitor at all times (including during load transients). The transient-mode controllers that have been developed distribute the on-time period between the phases and by doing so, an expedited yet smooth, transient recovery is achieved. The experimental validation of the controller operations has been found to be in very good agreement with the theoretical predictions. Also shown are the differences between small-signal voltage-mode and time-optimal control alternatives, demonstrating the superiority of the state-variables based approach.

3.6. References

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4. Combined Multi-Level and Two-phase Interleaved LLC Converter with Enhanced Power Processing Characteristics and Natural Current Sharing

Abstract- This paper introduces a new two-phase interleaved flying-capacitor LLC converter topology with high output current applications. Compared to a conventional two-phase LLC converter, the new converter adds a single capacitor that contributes to lower voltage stress on the primary side's switches, automatically balances the current distribution between the phases and enhances the power processing capabilities. All the attractive features of LLC converters are preserved, such as zero-voltage switching on the primary side's MOSFETs, zero-current switching on the secondary side's power devices, narrow switching frequency range and simple design. Full principle of operation and analysis of the converter are described, as well as the converter's primary characteristics and the impact of non-ideal components on the current sharing behavior. A 600W, 400V-to-12V experimental prototype is used as a showcase of the attractive features of the new converter, demonstrating excellent current sharing, simple implementation and high efficiency of up to 97.3%.

4.1. Introduction

Today's power converters are required to deliver more power and achieve high efficiency over a wide load range. The LLC resonant converter topology is able to address such challenges and is advantageous in front-end DC-DC conversion applications as a result of the zero-voltage switching (ZVS) for the primary side's MOSFETs and zero-current switching (ZCS) for the secondary side's power devices [1]-[5]. In addition, it features narrow switching frequency range to facilitate regulation, fast transient response and relatively low cost mainly due to incorporation of the transformer's leakage inductance as the resonant inductor. In particular in its half-bridge implementation, the topology has been widely and successfully applied to flat panel TVs, 80+ ATX and small form factor PCs, where the requirements on efficiency and power density of their switching mode power supplies (SMPSs) are getting more and more stringent.

In high power applications where the current stress in a converter becomes high, paralleling of two (or more) converters, namely multi-phase operation, is a good solution

for distribution of the current stress and it has been broadly investigated for both PWM [6]-[23] and resonant converters [11]-[13]. It has been found that multi-phase operation of LLC converters introduces implementation challenges that are typically related to the load current sharing between the converter's phases [11]-[24]. Current sharing is required to increase the power processing capability, maintain high efficiency and improve the reliability since the thermal stress is better distributed. Therefore, current sharing is considered mandatory in multi-phase LLC converters operation.

The main reason for an unbalanced load sharing between converter's phases lays in the difference between the components of the resonant networks. When interleaving phases, since the operation hinges on equivalent switching frequency of the different phases, mismatches in the resonant tank components impact the current distribution between the phases [13]. This is since only one phase operates at the frequency where the required voltage gain is achieved. Even small differences, within the resonant components values' tolerances, can have a severe effect on the current sharing and one phase will deliver most of the load current when other phases deliver a significantly smaller portion of it [19]. Several solutions have been proposed to achieve current sharing [12]-[24]. These solutions are used to match the resonant tanks components' values and can be classified as active or passive. In the active solutions, additional circuitry is added in order to control the resonant tank capacitance [13], [14] or inductance [15], to control the switching frequency [16] or to control the phase shift between the phases in case of three-phase structure [17]. However, these solutions suffer from complex control and implementation issues, high component count and high cost. The passive solutions use a common capacitor [18] or common inductor [19], [20] for impedance matching of the phases [21]. Another passive solution that achieves good current sharing is based on series-input connected capacitors [22], [23].

To further improve the power processing capability of LLC resonant converters, multi-level operation has been investigated [25]. This approach provides lower voltage stress on the primary side's power devices and allows for the use of lower voltage rated MOSFETs with lower $R_{DS(on)}$ per silicon area. The use of lower voltage rated MOSFETs reduces the conduction losses for a given area while maintaining very low switching losses due to ZVS. Another important feature of the multi-level operation is that the required dead-time and magnetizing inductance current to achieve ZVS can be decreased since lower energy is stored in the parasitic capacitances of the MOSFETs, which further improves the efficiency of the converter.

The objective of this study is to introduce a new two-phase interleaved flying-capacitor LLC (TIFLLC) resonant converter topology that combines multi-phase and multi-level operations. The new topology, shown in Fig. 4.1, incorporates a flying-capacitor that lowers the voltage stress on the primary side's MOSFETs, balances the currents delivered by the two phases and enhances the power processing characteristics. A significant advantage of the TIFLLC converter topology is that it preserves the benefits of conventional LLC converters such as soft-switching on all power devices, wide load range, narrow switching frequency range as well as excels with high efficiency. These advantages make the topology an attractive candidate for high output current applications.

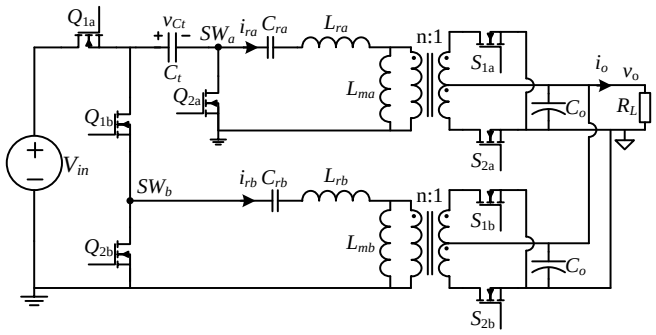

Fig. 4.1 Two-phase interleaved flying-capacitor LLC (TIFLLC) converter topology.

The rest of the paper is organized as follows: Section 4.2 presents the TIFLLC converter topology principle of operation and provides typical key waveforms of the new converter. Design considerations and details regarding the flying-capacitor are provided in Section 4.3. Next, the current sharing and enhanced power processing characteristics are described and analyzed in Section 4.4. Implementation of the TIFLLC prototype and experimental results are provided in Section 4.5. Section 4.6 concludes the paper.

4.2. Principle of Operation

The TIFLLC converter, shown in Fig. 4.1, combines the benefits of a switched-capacitor circuit and a series-resonant LLC converter. This topology adds a single capacitor C_t to the component count of a conventional two-phase LLC converter, depicted in Fig. 4.2. The converter's configuration and waveforms resemble the ones of the two-phase interleaved LLC converter, with the benefits of lower voltage stress transistors.

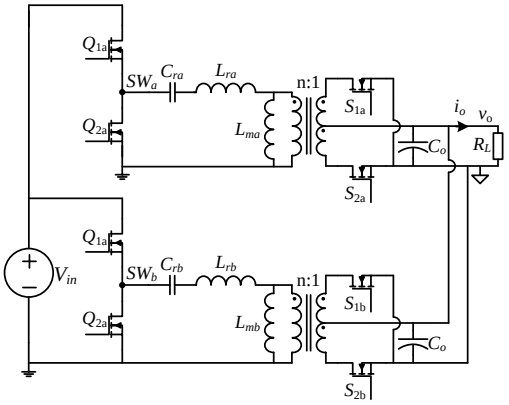

Fig. 4.2 Conventional two-phase LLC converter.

The operation of the TIFLLC converter is similar to the one of a conventional two-phase interleaved LLC converter with 180^0 phase delay, i.e., when the switching node (SW_a or SW_b) of one phase is high, then the switching node of the other phase is low. However, it should be noted that while in conventional two-phase interleaved LLC converter the phase delay between the phases can be arbitrarily selected (typically selected to be 90^0 to reduce the output voltage ripple) the 180^0 phase delay in the TIFLLC converter cannot be changed and therefore it doesn't contribute to output voltage ripple reduction. Therefore, two switching states are recognized as shown in Fig. 4.3 with the corresponding waveforms (obtained by a PSIM simulation) shown in Fig. 4.4: State I: phase *a* is on and phase *b* is off; State II: phase *a* is off and phase *b* is on.

In state I, depicted in Fig. 4.3(a), switches Q_{1a} and Q_{2b} are on, the input voltage connects to phase *a* through the flying-capacitor C_t and the applied voltage on its resonant tank is V_{in}-V_{Ct}, while the resonant tank of phase *b* connects to ground via Q_{2b}. At the secondary side, switches S_{2a} and S_{1b} are on for synchronous rectification operation. State II is shown in Fig. 4.3(b). Here, switches Q_{1b} and Q_{2a} are on and the flying-capacitor acts as the source for phase *b*, imposing a voltage of V_{Ct} on its resonant tank, while the resonant tank of phase *a* connects to ground; switches S_{1a} and S_{2b} are on for synchronous rectification of the output current. As in conventional LLC resonant converters, dead-time between the two switching states is added to facilitate ZVS for the primary side's MOSFETs, and ZCS is obtained for the secondary side's power devices. It should be noted that C_t is designed to be significantly larger than the resonant capacitors and therefore it acts as a voltage source that has minor effect or none on the resonant behavior of the converter's phases. Further design details regarding the flying-capacitor are provided in Section III.

As can be observed from Fig. 4.3 and Fig. 4.4, the operation of the TIFLLC converter topology resembles a two-phase interleaved LLC converter with two input voltages for each phase that sum to V_{in}. As will be detailed in the next section, these input voltages adapt their value based on the voltage gain per phase and as a result, high immunity is achieved to mismatches between the phases' resonant components. In addition, the use of a flying-capacitor naturally equalizes the current distribution the current between the phases, which in turn, enhances the power processing characteristics of the converter.

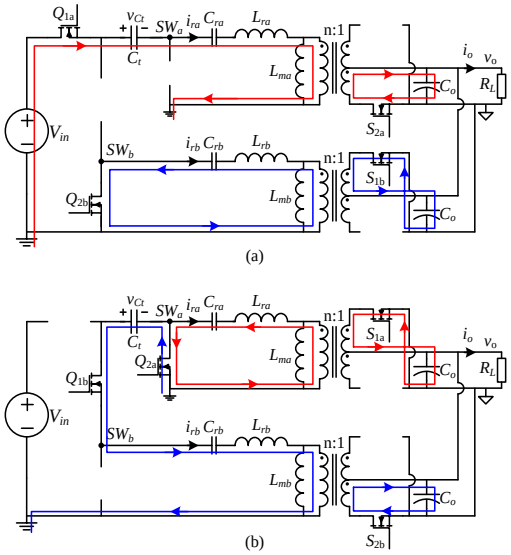

Fig. 4.3 Current paths in the TIFLLC converter: (a) State I: phase *a* is on and phase *b* is off, (b) State II: phase *a* is off and phase *b* is on.

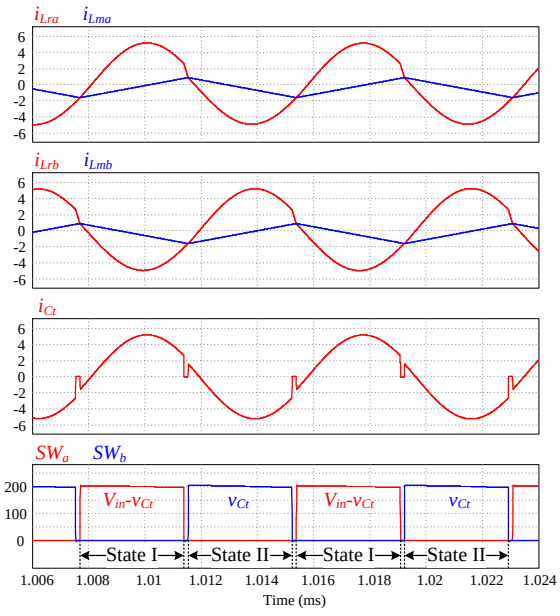

Fig. 4.4 Typical waveforms of the TIFLLC converter.

4.3.Analysis of Primary Characteristics for the TIFLLC Converter Topology

The flying-capacitor used in the TIFLLC converter introduces several interesting characteristics. The applied voltage on the switching nodes SW_a and SW_b is half of the input voltage which lowers the voltage stress on three out of the four primary side's MOSFETs by half. It also allows for lenient conditions to achieve ZVS on all the primary side's MOSFETs, since the voltage swing on these transistors during the commutation period is only half the input voltage. Moreover, the applied voltage on the resonant tank is also lowered by half and allows a design of a resonant network with lower impedance, i.e. lower inductance for the same switching frequency. Another very important property that will be detailed in the next section is the charge-balance on the flying-capacitor that provides current distribution between the converter's phases.

The voltage of the flying-capacitor v_{Ct} is assumed constant V_{Ct} for a duration of a switching cycle due to its low voltage ripple. The flying-capacitor's voltage ripple Δv_{Ct} depends primarily on the load current and it is designed to be small, i.e. no more than 5% of the nominal value of V_{Ct} that typically equals $V_{\text{in}}/2$. This selection of a sufficiently high flying-capacitor value also guarantees that the tanks' resonant frequency is not affected by this capacitor. The expression for Δv_{Ct} is calculated by the charge being transferred in each state, and can be expressed as

$$\Delta v_{Ct} = \frac{I_{out}}{4nf_s C_t} \quad , \tag{1}$$

where I_{out} is the load current, f_s is the switching frequency and n is the transformer's turns ratio.

The DC voltage of the flying-capacitor in the ideal case, i.e. the case of identical resonant components for both phases, equals $V_{in}/2$. For any other case, there may be a drift of V_{Ct} which is a result of the gain difference between the phases. Under first harmonic approximation (FHA) the normalized voltage gains G_a and G_b (for phases a and b, respectively) are expressed as (obtained by the equivalent circuit shown in Fig. 4.5):

$$G_a\left(f_s\right) = \frac{nV_{out,ac}}{V_{ina,ac}} = \frac{1}{\left(1+\frac{L_{ra}}{L_{ma}}-\frac{L_{ra}}{L_{ma}}\frac{1}{f_{na}^2}\right)+j\frac{\sqrt{L_{ra}/C_{ra}}}{n^2 R_{ac,a}}\left(f_{na}-\frac{1}{f_{na}}\right)} \tag{2}$$

$$G_b(f_s)=\frac{nV_{out,ac}}{V_{inb,ac}}=\frac{1}{\left(1+\frac{L_{rb}}{L_{mb}}-\frac{L_{rb}}{L_{mb}}\frac{1}{f_{nb}^2}\right)+j\frac{\sqrt{L_{rb}/C_{rb}}}{n^2R_{ac,b}}\left(f_{nb}-\frac{1}{f_{nb}}\right)} \quad (3)$$

where $V_{ina,ac}$ and $V_{inb,ac}$ are the ac input voltages of the phases *a* and *b*, respectively, given by:

$$V_{ina,ac}=\frac{V_{in}-V_{Ct}}{2}, \qquad V_{inb,ac}=\frac{V_{Ct}}{2}, \quad (4)$$

and f_{na}, f_{nb} are the normalized switching frequencies of phases *a* and *b*, defined as:

$$f_{na}=\frac{f_s}{f_{ra}}=\frac{f_s}{1/2\pi\sqrt{L_{ra}C_{ra}}}, \qquad f_{nb}=\frac{f_s}{f_{rb}}=\frac{f_s}{1/2\pi\sqrt{L_{rb}C_{rb}}}. \quad (5)$$

Using (2)-(4) and after some manipulations, the flying-capacitor voltage can be extracted and expressed as:

$$V_{Ct}(f_s)=\frac{V_{in}}{1+\frac{|G_b(f_s)|}{|G_a(f_s)|}}. \quad (6)$$

This implies that in case that the voltage gains of the phases are not equal, e.g. due to components' tolerances, the voltage deviates from the $V_{in}/2$ value and also depends on the switching frequency. Fig. 4.6 shows the variance in flying-capacitor voltage as a result of components' difference between the phases as a function of the normalized switching frequency, where in each case a different component has been changed and the case study parameters are detailed in Table I. It can observed that for higher output power the voltage deviation from 200V is smaller compared to lower output power. It can also be observed that the overall deviation, even for the lower power case, is relatively small for the switching frequency's area of interest (marked with arrow on Fig. 4.6) where ZVS on the primary-side's MOSFETs is achieved and the voltage gain is not highly dependent on the load, i.e. above $0.6f_r$. Lower frequencies than $0.6f_r$ may enter the capacitive region for some load conditions which may result in high switching losses and reduced efficiency. It should be noted that the value of $0.6f_r$ is only relevant for the presented case study and it different for every converter's design. Fig. 4.7 presents the variance in the flying-capacitor voltage for the worst case scenario where all the resonant tank's components of one phase have 20%

variation compared to the other phase. As can be observed, even for such extreme conditions the voltage deviation is small and therefore has minor effect on the converter's operation.

As in any capacitor based multi-level converter, there is an issue during start-up operation when the flying-capacitor is discharged of voltage stress on some of the MOSFETs. A possible solution to solve this problem and avoid any high inrush current to charge the flying-capacitor has been presented in [26], where an additional switch and a resistor have been connected in parallel with a low voltage MOSFET to limit any inrush current during start-up. Since the required capacitance of the flying-capacitor in the TIFLLC converter is relatively small, its charging time can be much shorter than an overall start-up procedure that includes soft-start.

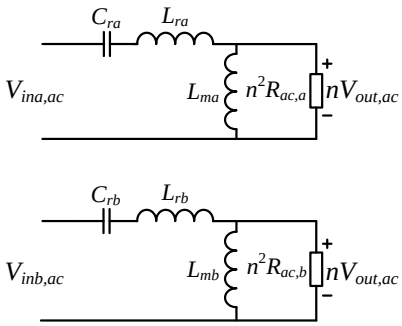

Fig. 4.5 Equivalent model of the TIFLLC converter using first harmonic approximation.

TABLE I. CASE STUDY PARAMETERS VALUES

Component	***Value / Type***
Input voltage V_{in}	400 V
Output voltage V_o	12 V
Transformers' turns ratio n	8
Phase a resonant frequency f_r	~150 KHz
Phase a resonant capacitor C_{ra}	44 nF
Phase a resonant inductor L_{ra}	25 μH
Phase a magnetizing inductor L_{ma}	150 μH

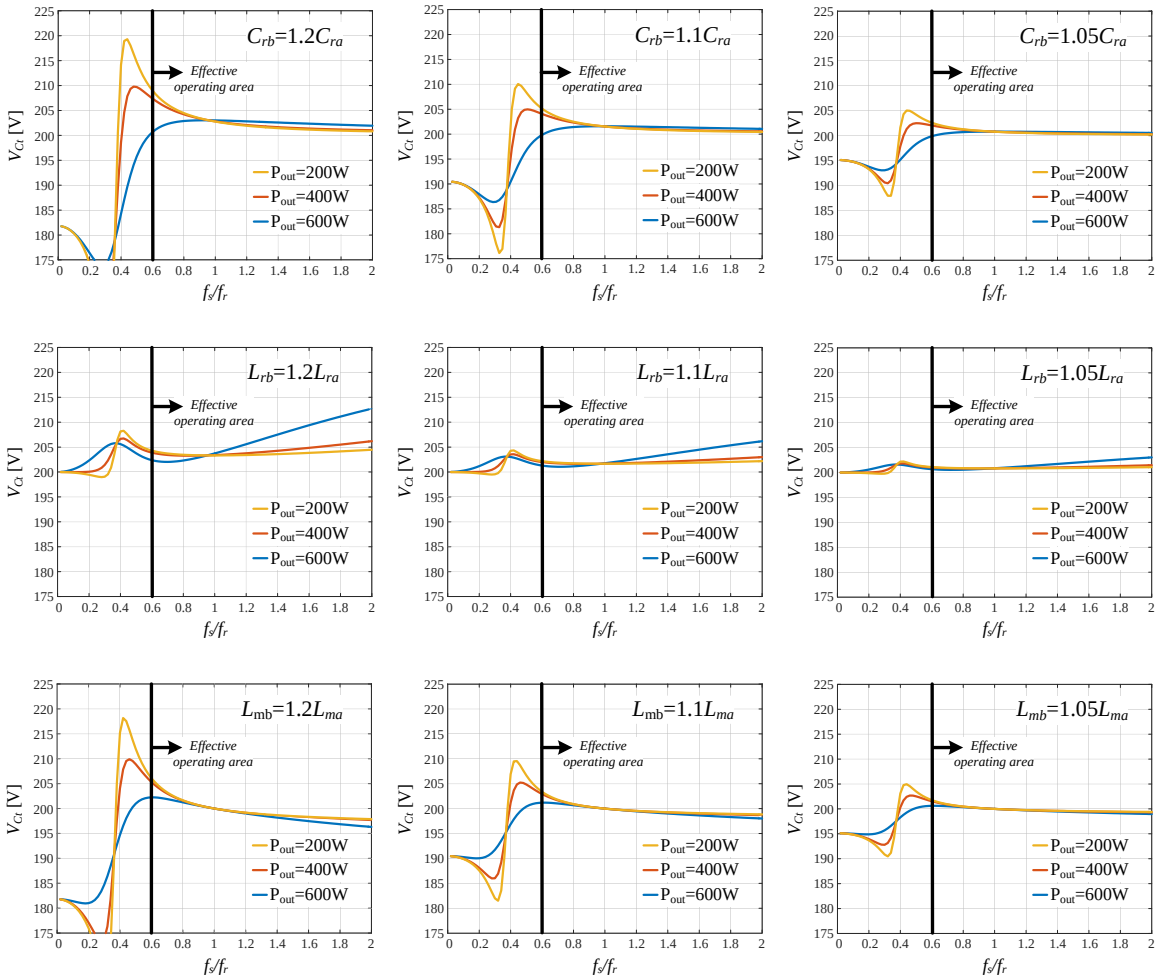

Fig. 4.6 Flying-capacitor voltage as a function of the switching frequency for phases with different resonant tank's parameters.

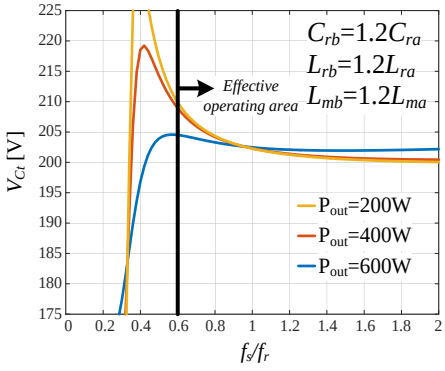

Fig. 4.7 Flying-capacitor voltage as a function of the switching frequency for worst-case resonant tank component's variation between the phases.

4.4. Current Sharing under Parameter variations

In Current sharing of multi-phase LLC converters has been widely investigated in [12]-[24]. In the TIFLLC converter topology, the charge-balance of the flying-capacitor assists in passive current sharing between the phases. Two MOSFETs conduct the current of the flying-capacitor: these are Q_{1a} during state I and Q_{1b} during state II, i.e.

$$i_{Ct} = \begin{cases} i_{Q1a} & @\,state\,I \\ -i_{Q1b} & @\,state\,II \end{cases} . \tag{7}$$

Since charge-balance on this capacitor exists, the average current through it must be zero, and the average currents through these two MOSFETs in every switching cycle are equal, i.e.

$$\left\langle i_{Q1a} \right\rangle = \left\langle i_{Q1b} \right\rangle . \tag{8}$$

Neglecting power loss in the system and assuming that the efficiency is high, the following holds

$$\begin{aligned} P_{in,a} &= P_{out,a} \\ P_{in,b} &= P_{out,b} \end{aligned} , \tag{9}$$

where P_{in} and P_{out} are the average input and output powers of each phase. The equality of (9) can be rewritten as

$$\begin{aligned} P_{in,a} &= \left\langle v_{in,a} \right\rangle \left\langle i_{in,a} \right\rangle = \frac{V_{in} - V_{Ct}}{2} \left\langle i_{Q1a} \right\rangle = I_{out,a}^2 R_{ac,a} = V_{out} I_{out,a} \\ P_{in,b} &= \left\langle v_{in,b} \right\rangle \left\langle i_{in,b} \right\rangle = \frac{V_{Ct}}{2} \left\langle i_{Q1b} \right\rangle = I_{out,b}^2 R_{ac,b} = V_{out} I_{out,b} \end{aligned} , \tag{10}$$

where $I_{out,a}$ and $I_{out,b}$ are the average output currents of the phases. From (8)-(10) it can be derived that the ratio between the two phases' output currents equals the ratio between the input voltages of the two phases, i.e.:

$$\frac{I_{out,a}}{I_{out,b}} = \frac{V_{in,a}}{V_{in,b}} = \frac{V_{in} - V_{Ct}}{V_{Ct}} . \tag{11}$$

The expression in (11) provides an insight to the current sharing mechanism that is achieved with the usage of the flying-capacitor. The voltage V_{Ct}, as opposed to V_{in}, can dynamically change and as a result both $V_{in,a}$ and $V_{in,b}$ would vary accordingly. In the case

that both the input and output voltages are common for the two phases, a mismatch of the resonant components results in voltage gains G_a and G_b that differ from the effective input-to-output ratio. The operation of the flying-capacitor automatically corrects the effective phase's input voltage (and as a result the input-to-output ratio) to comply with the variation in the voltage gain. It should be noted that this balancing action of the input voltages of the phases exceeds beyond the simplistic property of components variations for other parameters of the system such as the turn ratios of the phases' transformers.

Using the expression given in (6) and after some manipulations, the ratio between the phases' output currents can be expressed as

$$\frac{I_{out,a}}{I_{out,b}} = \frac{G_b}{G_a}, \tag{12}$$

where G_a and G_b are given in (2) and (3). The current error between the two phases (the ratio between the difference and sum of the output currents, as defined in [19]), can be now expressed as

$$\sigma_{error} = \left| \frac{G_a - G_b}{G_a + G_b} \right|. \tag{13}$$

Fig. 4.8 shows the value of (13) as a function of the switching frequency and the output power for a case of a converter with parameters that are as given in TABLE I, and the variation in the resonant capacitor of phase *b* is by 20% compared to the resonant capacitor of phase *a*, and for the worst case scenario where all the resonant tank' components have 20% variation. It can be observed that for a switching frequency higher than $0.6f_r$ the current error is less than 5% for both cases, which is an attractive attribute for passive current sharing even at such an extreme case of components' difference.

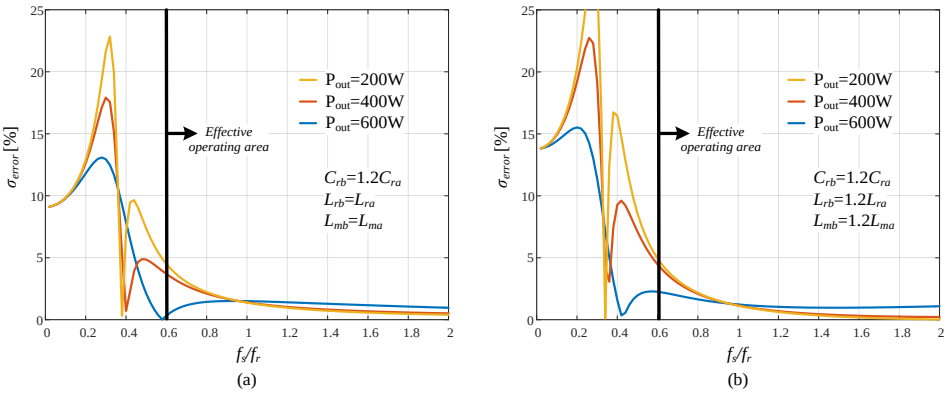

Fig. 4.8 Current error between the phases as a function of the switching frequency for: (a) C_{rb}=1.2C_{ra}, (b) worst case component's mismatch: C_{rb}=1.2C_{ra}, L_{rb}=1.2L_{ra}, L_{mb}=1.2L_{ma}.

The very good current distribution in the TIFLLC converter topology also contributes to enhanced power processing characteristics. The 180^0 phase delay between the converter phases provides an interesting feature when Q_{2a} is on. During the period of state II Q_{2a} has two main purposes, one is applying a low potential path for the resonant current of phase *a*, i.e. zero voltage on the resonant tank. The second is connecting the negative port of the flying-capacitor to ground in order to apply V_{Ct} on the resonant tank of phase *b*. Therefore, Q_{2a} participates in the operation of both phases and during state II it passes resonant currents of the two phases simultaneously. Since at this state the resonant currents are in opposite direction (the current in phase *a* is negative whereas the current in phase *b* is positive), the net current flowing through Q_{2a} is zero, as shown in Fig. 4.9. The main contribution to the current rms value of Q_{2a} is its current during the dead-time, where the current magnitude equals to the resonant current magnitude, which is not zero. This translates into a more relaxed selection of this switch and implies that a higher on-resistance MOSFET with lower capacitances is sufficient for the tasks required by Q_{2a}. This selection does not compromise on the efficiency of the converter, which in fact, improves and benefit from a lower required magnetizing inductance circulating current and gate driving requirements.

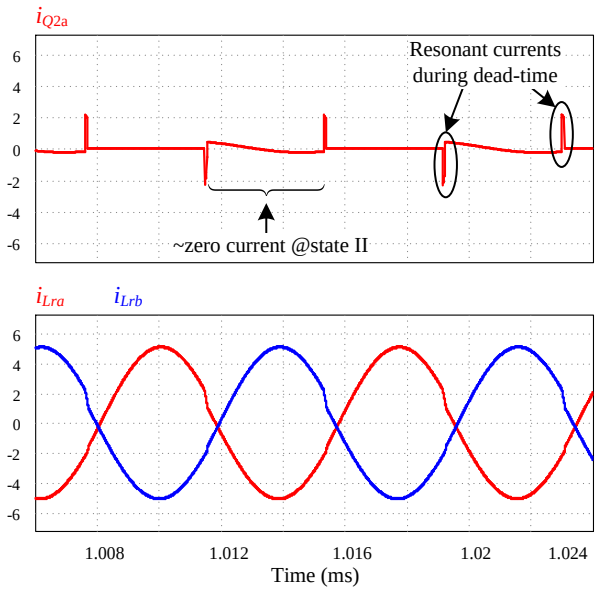

Fig. 4.9 Zero current characteristic of Q_{2a}.

4.5. Experimental Results

To validate the operation of the TIFLLC converter operation, a 600W, 400V-to-12V prototype was built and tested. The transformers of both phases were hand made to create a difference between the resonant components of the phases and their measured leakage and

magnetizing inductance are detailed in TABLE II. In addition, to further create a difference between the phases' parameters, the turn ratios of the transformers were designed to be not equal. The rest of components values and parameters of the TIFLLC experimental prototype are given in TABLE II. The converter is digitally controlled using an Altera FPGA [38] using fully digital high performance ADC and DPWM peripherals as detailed in [39] and [29].

The control scheme that was used in this study is described by the simplified block diagram of the TIFLLC controller, depicted in Fig. 4.10. A window-ADC samples the output voltage and compares it with a reference value V_{ref} to create an error signal $v_e[n]$ that is the input of a digital PID compensator. A PID compensation scheme is used to obtain high loop-gain bandwidth and its output is the frequency of the DPWM $f_s[n]$. The output of the DPWM is a square wave with frequency f_s and 0.5 duty-ratio. The square wave is then inverted to create two square waves with 180^0 phase delay. At last, two dead-time units are used to create sufficient dead-time between the high and low side gate signals of each phase in order to obtain ZVS on the primary-side's MOSFETs.

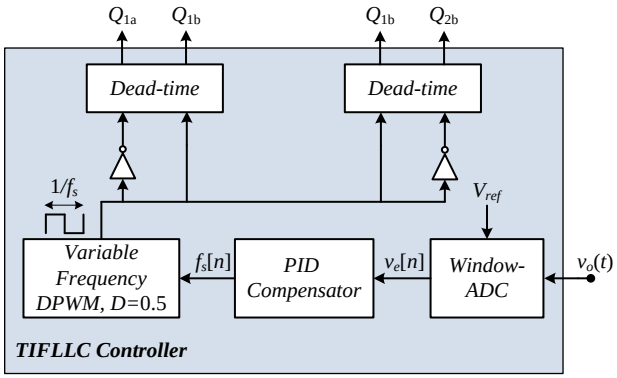

Fig. 4.10 Simplified block diagram of the TIFLLC controller.

TABLE II. EXPERIMENTAL PROTOTYPE'S PARAMETERS VALUES

Component	***Value / Type***
Input voltage V_{in}	400 V
Output voltage V_o	12 V
Flying capacitor C_t	3 µF
Output capacitance C_{out}	1 mF
Phase *a* transformer's turns ratio n_a	9
Phase *b* transformer's turns ratio n_b	9.3
Phase *a* resonant frequency f_{ra}	~138 KHz
Phase *b* resonant frequency f_{rb}	~130 KHz
Phase *a* resonant capacitor C_{ra}	66 nF ±10%
Phase *b* resonant capacitor C_{rb}	66 nF ±10%
Phase *a* resonant inductor L_{ra}	20 µH
Phase *b* resonant inductor L_{rb}	23 µH
Phase *a* magnetizing inductance L_{ma}	150 µH
Phase *a* magnetizing inductance L_{mb}	155 µH

Primary-side gate drivers	UCC27714

4.5.1. Implementation of the Primary-Side's MOSFETs Gate Drivers

Although the two phases of the TIFLLC converter are not conventional half bridges, its gate drive circuitry is similar to the gate drive circuitry of a two conventional half bridges transistors assemblies, except for a slight modification in the charging path of the boot capacitor of phase *a*. A simple bootstrap driver cannot be employed for this case since its source (SW_a) does not meet ground at any time and its bootstrap capacitor would not charge by a drive voltage referenced to ground. To overcome this obstacle, instead of connecting the bootstrap diode of phase *a*'s driver ($D_{boot,a}$) to a ground referenced drive voltage, it connects the bootstrap capacitor of phase *b*'s driver $C_{boot,b}$, as shown in Fig. 4.11. This way when Q_{1b} is on, $C_{boot,a}$ is charged by $C_{boot,b}$ through $D_{boot,a}$ in a similar operation to the one of diode-capacitor charge pump. The other MOSFETs driving is simple: Q_{1b} and Q_{2b} are standard high-side and low-side MOSFETs driven by a dual bootstrap driver configuration and Q_{2a} is driven by the low-side driver of the dual bootstrap driver that also drives Q_{1a}. The component count of the driving configuration remains the same as the component count of conventional two-phase LLC converter.

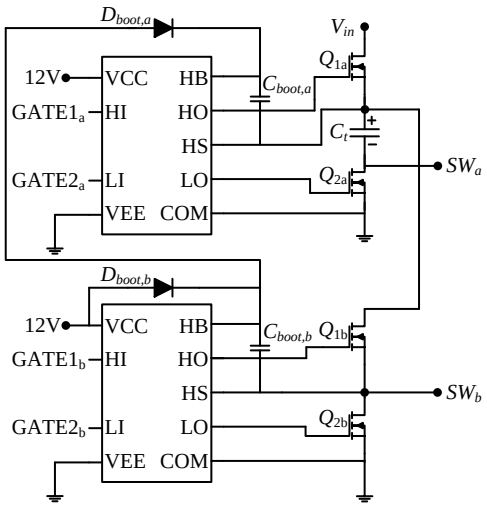

Fig. 4.11 Gates drivers' realization in the TIFLLC converter.

4.5.2. Experimental Results

Figs. 12 to 14 show the converter's waveforms for output current of 50A (full load). Fig. 4.12 shows the flying-capacitor voltage, output voltage and the primary-side's currents of the two phases. As can be observed, in spite of the difference between the parameters of the

phases, the phases' currents are almost equal with a very small difference between them, with a measured current error of 0.4%. In addition, the flying-capacitor voltage is 204V which is very close to $V_{in}/2$, as expected by the theoretical analysis from Section III. It should be noted that the output voltage ripple is measured at around 1V, which is the worst case voltage ripple due to operation in full load and a result of relatively small output capacitance used in the experimental prototype. Depicted in Fig. 4.13 is the voltage ripple of the flying-capacitor Δv_{Ct} with a magnitude of around 5V, which is approximately 2.5% of V_{Ct}. Fig. 4.14 depicts the switching nodes SW_a and SW_b. As can be observed, ZVS of the primary-side's MOSFETs is obtained and the voltage of the switching nodes is around 200V (half of V_{in}) when they are high. Fig. 4.15 presents the measured current error for the full load range of the converter when the resonant capacitors have equal values (as in TABLE II) and when one of the resonant capacitors (C_{ra}) has been replaced with significantly small capacitor (55nF instead of 66nF) which represents a 20% difference between the phases' capacitors . The results are in very good agreement with the analysis from Section IV, verifying the natural current sharing between the phases and the small current error even at large components mismatch. Efficiency measurements of the converter for the two setups are provided in Fig. 4.16, demonstrating a peak efficiency of 97.3% and above 96% for most of the load range. It can also be observed that the variation of the resonant capacitor has negligibly small effect on efficiency, and its effect is only noticeable at high output currents which is reasonable due to the fact that the conduction losses are dominant and the current sharing error is slightly higher, resulting in one phase that is less efficient than the other.

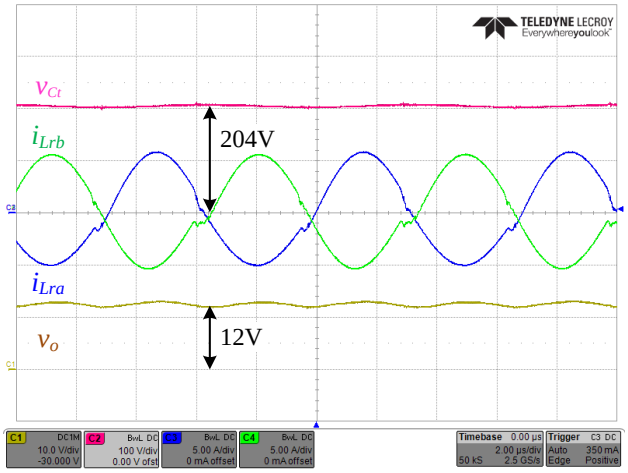

Fig. 4.12 Experimental waveforms of the TIFLLC converter. C1 – output voltage v_o (5V/div), C2 – flying-capacitor voltage v_{Ct} (100V/div), C3 – phase *a* primary-side resonant tank current i_{Lra} (5A/div), C4 – phase *b* primary-side resonant tank current i_{Lrb} (5A/div). Time scale is 2µs/div.

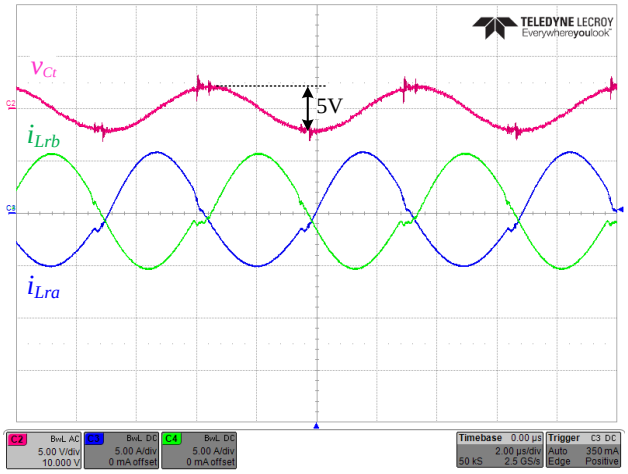

Fig. 4.13 Experimental waveforms of the TIFLLC converter. C2 – flying-capacitor voltage v_{Ct} (5V/div, ac coupled), C3 – phase *a* primary-side resonant tank current i_{Lra} (5A/div), C4 – phase *b* primary-side resonant tank current i_{Lrb} (5A/div). Time scale is 2µs/div.

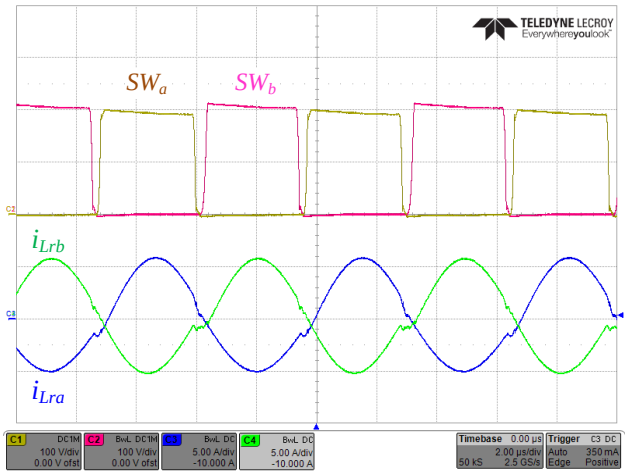

Fig. 4.14 Experimental waveforms of the TIFLLC converter. C1 – switching node voltage of phase *a* SW_a (100V/div), C2 – switching node voltage of phase *b* SW_b (100V/div), C3 – phase *a* primary-side resonant tank current i_{Lra} (5A/div), C4 – phase *b* primary-side resonant tank current i_{Lrb} (5A/div). Time scale is 2µs/div.

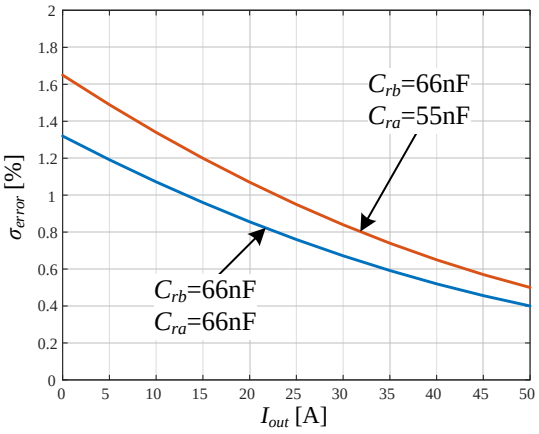

Fig. 4.15 Measured current error between the phases of the experimental prototype.

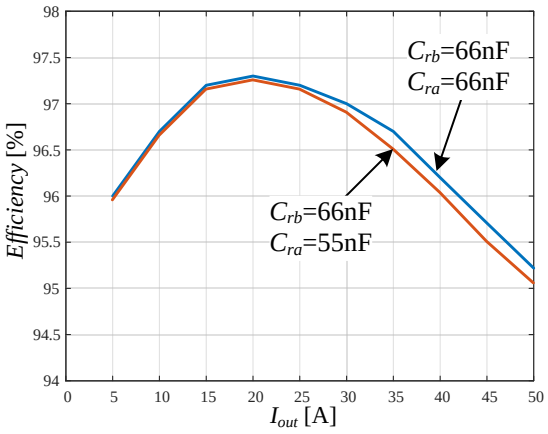

Fig. 4.16 Efficiency measurements of the experimental prototype.

4.6. Conclusion

A new two-phase interleaved flying capacitor LLC converter topology has been presented in this study. The topology comprises two-phases for high current delivery and uses a flying-capacitor to lower the voltage stress on the switches, naturally balance the current distribution between the phases and enhance the power processing capabilities. The converter preserves all the benefits of conventional LLC converters while maintaining low sensitivity to resonant tank parameters' mismatches and conventional driving circuitry with no extra components. Full principle of operation has been described, as well as the converter's primary characteristics and the impact of non-ideal components on the current sharing behavior. The experimental results of the new converter are in excellent agreement with the theoretical analysis, showing promising power processing characteristics and making the converter an attractive candidate as front-end converter for high output current applications.

4.7. References

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5. Discussion

5.1. Contribution of the Research

Very High Conversion Ratio Converter Topologies – Two new converters topologies have been introduced in both PWM and resonant converters, specially designed for applications that requires very high DC-DC voltage conversion ratio. Since both present and future applications require very high voltage conversion, the development of "tailored" converter topologies improves the efficiency, and therefore significantly improves the power loss and size of the converters, creating a significant cost reduction without using high-end materials that are specially designed for high-voltage and/or high-current with increases cost, allowing the advancement in technology and miniaturization of the power stages in applications.

Modelling of Very High Conversion Ratio Converters – This allows for controllers' design and implementation in both analog and digital manners. It reveals some characteristics and similarities to exiting converters models, allowing for faster and more efficient implementation of the controllers.

Advanced Non-Linear Controllers – Time Optimal Controller and Minimum Deviation Controller – Development of these control methods for advanced converter topologies supports the implementation of such converters in commercial applications, due to the additional volume reduction by reducing the reactive components' stress while maintaining extremely fast load transient response.

5.2. Suggestions for Future Research

Some suggestions for future lines of investigation that can be developed as a result of this thesis are outlined below:

Efficiency optimization guidelines for the new converters – Better understanding the tradeoff between the number of series capacitors and its effect on efficiency, with a restriction on the components' selection.

Controller development and hardware-efficient implementation for the new converters – Digital implementation of the non-linear controllers with as low as possible hardware requirements, to allow faster and cost-efficient adoption by the industry.

Addressing hardware implementation challenges – Such as soft start and pre-charging of the flying capacitors to avoid above-rating voltage stress on the semiconductor devices during start-up. Also to have a simple adaptive controller to compensate for variances between the phases in order to keep the flying-capacitor voltage within the allowed range.

6. Conclusion

In this research, new very-high conversion ratio converter topologies and control methods have been presented. The topologies comprise two-phases for high current delivery and use series capacitors, operating with soft-charging characteristic. The energy processing by the capacitors significantly lowers the voltage stress of the transistors and provides an inherent current sharing feature between the two phases, and enhances the power processing capabilities. The very-high conversion ratio approach has been demonstrated on two converter topologies, both hard-switched PWM converter and soft-switched resonant converter, showing its benefits in different popular applications, e.g. 400V-to-12V power supply and a 48V-to-1.xV voltage regulator module.

The control methods developed in this research are optimal closed-loop control scheme for a series-capacitor buck converter has been presented. The controller merges a voltage-mode controller for steady-state operation and a transient-mode time-optimal controller for load transients. In the theoretical analysis, an average-behavioral model as well as state-space representation of the converter have been derived, then two transient-mode controllers have been developed. The transient-mode controllers that have been developed distribute the on-time period between the phases and by doing so, an expedited yet smooth, transient recovery is achieved.

The results of this research open the path for engineers to design the next-generation converters for future applications that become more and more significant in the power electronics industry.

7. Appendix

7.1. Power Loss Analysis of the Double Series Capacitor Buck Converter Topology

7.1.1. Switching Losses

Switching losses in the DSCBC include all the losses that directly depend on the switching frequency. These losses include: overlap of current and voltage during turn and turn off of the MOSFETs, the power loss due to both input and output parasitic capacitances of the MOSFETs, dead-time losses and body diode's reverse recovery losses.

7.1.1.1. Overlap Switching Losses

The losses due to overlap are calculated using the expression

$$P_{overlap} = \frac{I_D V_{DS}}{6}\left(t_r + t_f\right) f_{sw} \ , \tag{1}$$

where I_D is the current at the time of switching, V_{DS} is the drain-source voltage, f_{sw} is the switching frequency and t_r and t_f are the rise and fall times. Using (1) the losses of the DSCBC's MOSFETs are:

$$\begin{aligned} P_{overlap,Q_c,Q_{1a},Q_{1b}} &= \frac{D I_{out} V_{in}}{54}\left(t_r + t_f\right) f_{sw} \\ P_{overlap,Q2a} &= \frac{(1-D) I_{out} V_{SD}}{18}\left(t_r + t_f\right) f_{sw} \\ P_{overlap,Q2b} &= \frac{2(1-D) I_{out} V_{SD}}{18}\left(t_r + t_f\right) f_{sw} \end{aligned} \ , \tag{2}$$

where V_{in} is the input voltage, I_{out} is the load current, D is the steady-state duty-ratio and V_{SD} is the source-drain voltage of $Q_{2\text{a}}$ and $Q_{2\text{b}}$ due to conduction of the body diode.

7.1.1.2. Parasitic Capacitances Switching Losses

The losses due to parasitic capacitance occur since these capacitances are charged and discharged with energy every switching cycle. Two capacitances are considered: output capacitance C_{oss} and input capacitance C_{iss}. The C_{oss} capacitance is discharged on the MOSFET's $R_{\text{DS(on)}}$ during turn on of the MOSFET. The C_{iss} capacitance is charged with the gate driver supply voltage V_{DRV} and discharged on the driver. The losses due to C_{iss} are also known as drive losses. The power loss due to each capacitance is calculated using

$$P_{\text{capacitance}} = C V^2 f_{sw} \tag{3}$$

where C is the capacitance value and V is the voltage of the capacitance when charged.

For the DSCBC, the losses due to C_{oss} are:

$$\begin{aligned} P_{\text{capacitance},Q_c,Q_{2a},Q_{2b}} &= C_{oss}\left(\frac{V_{in}}{3}\right)^2 f_{sw} \\ P_{\text{capacitance},Q_{1a},Q_{1b}} &= C_{oss}\left(\frac{2V_{in}}{3}\right)^2 f_{sw} \end{aligned}, \tag{4}$$

and the drive losses for each of the MOSFETs are given by

$$P_{\text{drive}} = C_{iss} V_{DRV}^2 f_{sw} . \tag{5}$$

7.1.1.3. Dead-Time and Reverse Recovery Losses

Dead-time losses are considered as the power dissipated by the body diodes of the MOSFETs when they are off. These losses depend on the current magnitude flowing through the diode, the diode forward voltage and the time of this period. These losses appear only in the low-side MOSFETs Q_{2a} and Q_{2b}, and given by

$$\begin{aligned} P_{dead-time,Q_{2a}} &= (1-D)\frac{I_{out}}{3} V_{SD} f_{sw} t_{dead} \\ P_{dead-time,Q_{2b}} &= (1-D)\frac{2I_{out}}{3} V_{SD} f_{sw} t_{dead} \end{aligned} . \tag{6}$$

where V_{SD} is the diode forward voltage, I_{out} is the output current and t_{dead} is the dead-time.

Reverse recovery losses occur when the high-side MOSFETs are turned on and the body-diodes of the low-side MOSFETs stops conducting. As in conventional converters, the power loss due to the reverse recovery effect is dissipated on the high-side MOSFETs, and the power loss due to each of the low-side MOSFETs is given by:

$$P_{RR} = Q_{RR} V_{DS} f_{sw} \tag{7}$$

where Q_{RR} is the reverse recovery charge and V_{DS} is the voltage on the high-side MOSFET.

7.1.2. Conduction Losses

Switching losses in the DSCBC include all the losses that appear due to resistance of the power devices and their rms current. These losses include the MOSFETs' conduction losses, the inductors' conduction losses and the series-capacitors' conduction losses, and are calculated using the expression

$$P_{conduction} = I_{RMS}^2 R . \tag{8}$$

7.1.2.1. MOSFETs Conduction Losses

In the DSCBC the three high-side MOSFETs (Q_c, Q_{1a} and Q_{1b}) all have the same rms current, and it is given by

$$I_{rms,Q_c} = I_{rms,Q_{1a}} = I_{rms,Q_{1b}} = \sqrt{\frac{3V_{out}}{V_{in}}}\sqrt{\left(\frac{I_{out}}{3}\right)^2 + \frac{\Delta I_L^2}{12}} \tag{9}$$

where ΔI_L is the inductors current ripple. The conduction power loss of these MOSFETs is calculated by multiplying (9) by the MOSFETs' on resistance $R_{DS(on)}$:

$$P_{cond,,Q_c,Q_{1a},Q_{1b}} = \frac{3V_{out}}{V_{in}}\left(\left(\frac{I_{out}}{3}\right)^2 + \frac{\Delta I_L^2}{12}\right)R_{DS,on} \ . \tag{10}$$

For the low-side MOSFETs Q_{2a} and Q_{2b} the conduction power loss is given by

$$\begin{aligned} P_{cond,Q_{2a}} &= \left(1-\frac{3V_{out}}{V_{in}}\right)\left(\left(\frac{I_{out}}{3}\right)^2 + \frac{\Delta I_L^2}{12}\right)R_{DS,on,Q_{2a}} \\ P_{cond,Q_{2b}} &= \left(1-\frac{3V_{out}}{V_{in}}\right)\left(\left(\frac{2}{3}I_{out}\right)^2 + \frac{\Delta I_L^2}{12}\right)R_{DS,on,Q_{2b}} \end{aligned} \ . \tag{11}$$

7.1.2.2. Inductors and Capacitors Conduction Losses

The inductors conduction losses differ from each other due to the different average currents flowing through each of them, and the power loss is calculated by

$$\begin{aligned} P_{cond,La} &= \left(\left(\frac{I_{out}}{3}\right)^2 + \frac{\Delta I_L^2}{12}\right)R_{La} \\ P_{cond,Lb} &= \left(\left(\frac{2}{3}I_{out}\right)^2 + \frac{\Delta I_L^2}{12}\right)R_{Lb} \end{aligned} \tag{12}$$

where R_{La} and R_{Lb} are the resistances of inductors L_a and L_b, respectively.

Conduction losses of the series-capacitors are a results of their non-zero equivalent series resistance (ESR). In the DSCBC the current flowing through the series-capacitors is the same, and the power loss is given by

$$P_{cond,Ct1,Ct2} = \frac{6V_{out}}{V_{in}}\left(\left(\frac{I_{out}}{3}\right)^2 + \frac{\Delta I_L^2}{12}\right)ESR \ . \tag{13}$$

7.1.3. Case Study: 48V-to-1.2V, 30A 500KHz Voltage Regulator Module

To verify the power loss analysis an examination using off-shelf power component (from Vishay Inc., see TABLE I) have been conducted to plot the efficiency curve of the DSCBC

for a 48V-to-1.2V 30A server power supply, with a switching frequency of 500KHz, taking into account all the power losses described in the previous subsection. The drive parameters are t_r=t_f=10ns, V_{DRV}=10V. It should be noted that the components have been selected in order to optimize the efficiency for this application.

TABLE I. COMPONENTS FOR THE POWER LOSS ANALYSIS

Component	Q_c, Q_{1a}, Q_{1b}	Q_{2a}	Q_{2b}	**Inductors**
Type	Si4288DY (40V)	SiRA12DP (30V)	SiRA04DP (30V)	IHLP-5050EZ (0.47uH)
$R_{DS,on}$/DCR	20mΩ	4.3mΩ	2.2mΩ	1.1mΩ
C_{oss}	110pF	600pF	1040pF	
C_{iss}	550pF	2070pF	3500pF	
Q_{RR}	7.5nC	15nC	24nC	
V_{SD}	0.8V	0.86V	0.73V	

The distribution of the power loss and the efficiency curve are given in Fig. 7.1 and Fig. 7.2, respectively. As can be observed, the peak efficiency achieved by this design is 93.1% and above 90% for most of the load range, and the results are with good agreement with the experimental prototype from subsection 2.4.

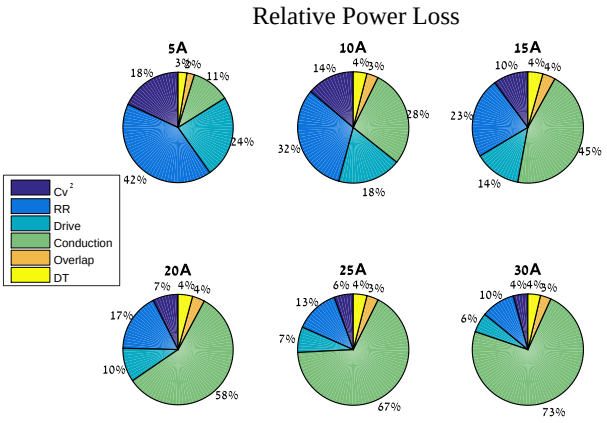

Fig. 7.1 Distribution of the power loss in the DSCBC converter for different load currents.

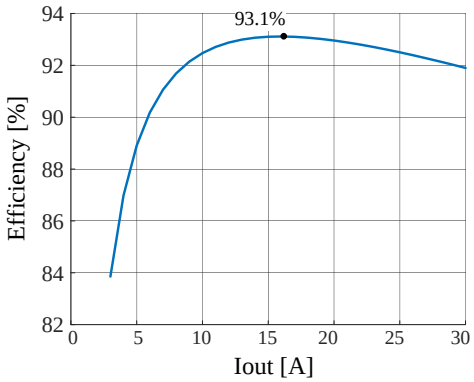

Fig. 7.2 Efficiency curve for the 48V-to-1.2V 30A tested converter.

7.2.Expansion to N-Series Capacitor Buck Converter

An interesting expansion to the DSCBC can be achieved by adding more high-side MOSFETs and capacitors connected to the input. The resultant topology is the *N*-series capacitors buck converter, shown in Fig. 7.3, where *N* is the number of series-capacitors.

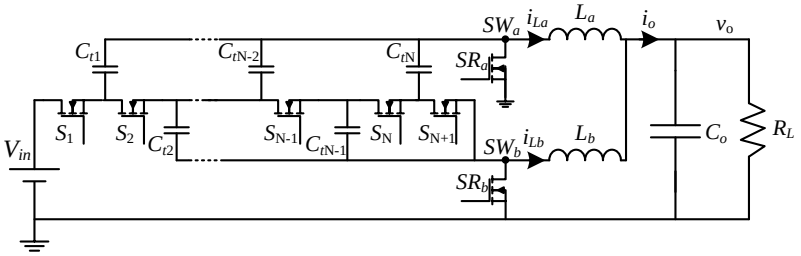

Fig. 7.3 *N*-Series capcacitor buck converter.

For this converter the voltage conversion ratio is given by

$$M = \frac{V_{out}}{V_{in}} = \frac{D}{N+1} \ , \tag{14}$$

the voltage stress on the MOSFETs are

$$\begin{aligned} S_1, SR_a, SR_b: &\qquad V_{DS} = \frac{V_{in}}{N+1} \\ S_2, ..., S_{N-1}: &\qquad V_{DS} = \frac{2V_{in}}{N+1} \end{aligned} \ , \tag{15}$$

and the phases currents are given by

$$\begin{aligned} N \text{ is odd}: \quad & I_{La} = \frac{I_{out}}{2} \\ & I_{Lb} = \frac{I_{out}}{2} \end{aligned} \qquad \begin{aligned} N \text{ is even}: \quad & I_{La} = \frac{N}{2N+2} I_{out} \\ & I_{Lb} = \frac{N+2}{2N+2} I_{out} \end{aligned} \ . \tag{16}$$

As can be observed from the above expressions, adding more capacitors and switches helps to increase the effective duty-ratio and therefore helps to lower the effective voltage conversion ratio by a factor of *N*+1 compared to a buck converter. Although there is a penalty in higher component count and more complicated drive circuitry, this solution may be attractive in terms of efficiency for very high voltage conversion ratio applications.

7.3.Derivation of the state trajectories for buck and boost converters

An example of deriving the state trajectories is given for a buck converter loaded by a constant current load from the state equations (1.5) and (1.6). The trajectories are derived

by using the second method for state trajectories drawing (see subsection 1.3.3) by solving the integral.

Solving the integral for the on state trajectories

$$\int \frac{i_L - I_o}{C}\, di_L = \int \frac{V_{in} - v_C}{L}\, dv_C \tag{1.17}$$

yields the following expression

$$C\left(v_C - V_{in}\right)^2 + L\left(i_L - I_o\right)^2 = C\left(v_{C_0} - V_{in}\right)^2 + L\left(i_{L_0} - I_o\right)^2 , \tag{1.18}$$

that represents an ellipse in the state-plane with a center at the point (V_{in}, I_o).

The same procedure can be used to find the off state trajectories, this yields the expression

$$Cv_C^2 + L\left(i_L - I_o\right)^2 = Cv_{C_0}^2 + L\left(i_{L_0} - I_o\right)^2 , \tag{1.19}$$

that represents an ellipse in the state-plane with a center at the point (0, I_o). Fig. 7.4 shows the on and off state trajectories for different initial conditions.

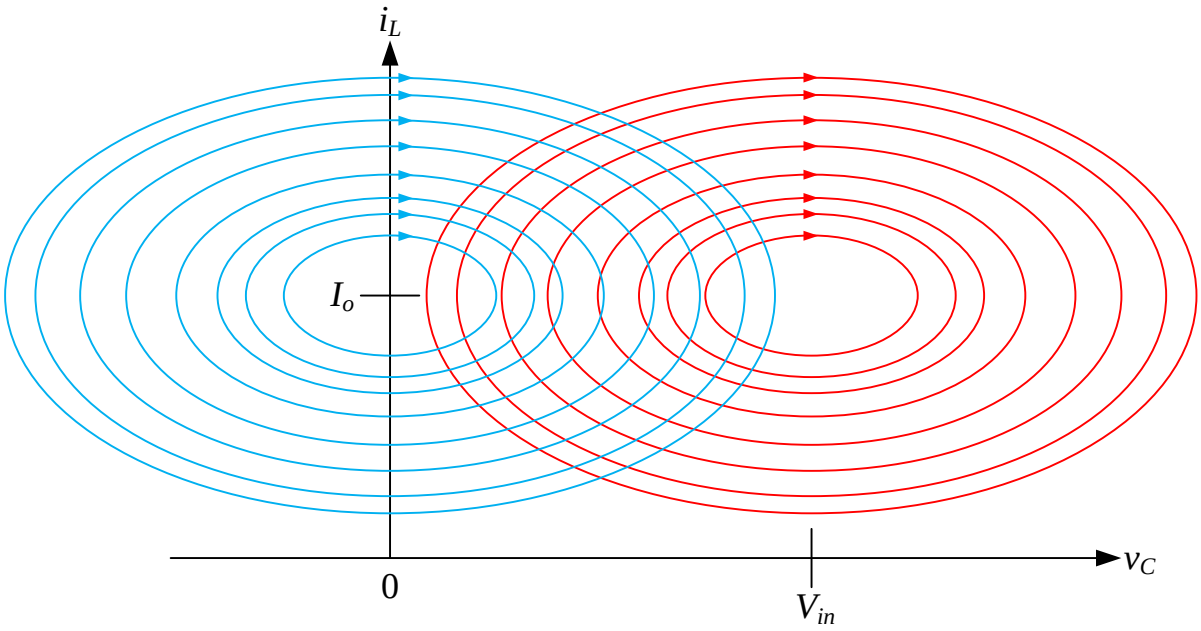

Fig. 7.4 State-plane state trajectories of a buck converter. On state trajectories are in red, off state trajectories are in blue.

Another example is the state trajectories of boost converter loaded by a constant current load. For this case, the on state trajectories are straight lines whereas the off state trajectories are ellipses with center at the point (V_{in}, I_o), as shown in Fig. 7.5.

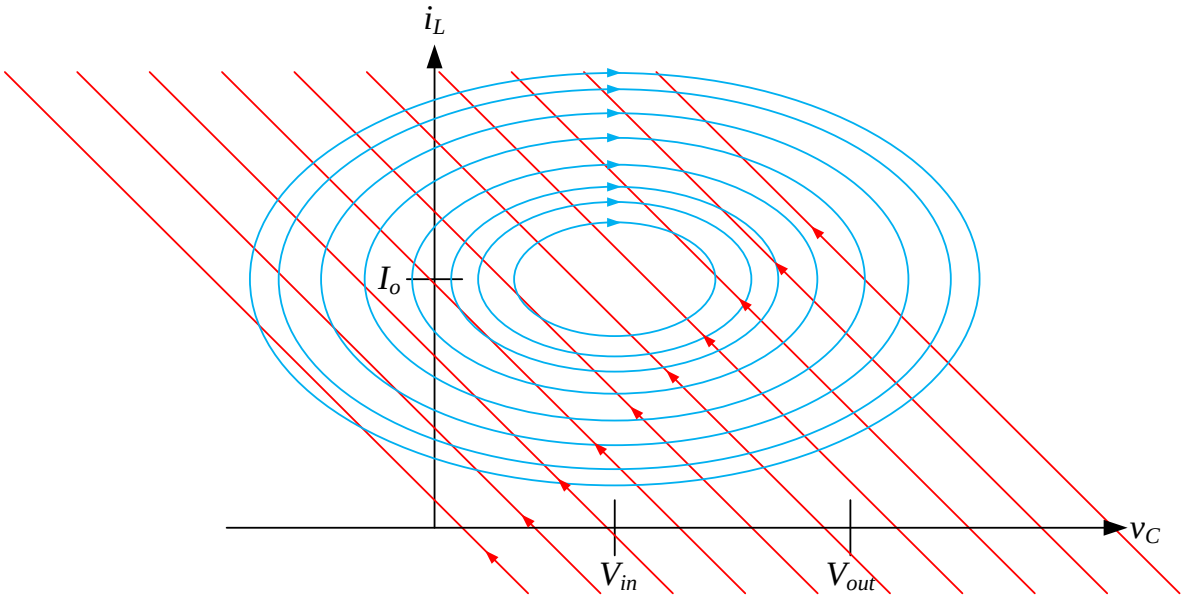

Fig. 7.5 State-plane state trajectories of a boost converter. On state trajectories are in red, off state trajectories are in blue.

The state-plane and state trajectories of the boost converter reveals an interesting property regarding the RHP zero. As can be observed, all the on trajectories are directed towards the negative value of the horizontal axis, the capacitor voltage axis. This means that during on state the capacitor voltage is decreasing, which is a property of indirect energy transfer converters with RHP zero.

8. Additional publications conducted during the PhD program but not included in this thesis

The following publications have been conducted during the research period and are only partially related to the topic of this thesis, and therefore have been excluded from it.

8.1. Merged PWM-Resonant Converter for Direct Panel to Grid-Level Conversion in Localized PV Energy Harvesting

Abstract-This paper presents a merged PWM-resonant dc-dc converter topology for localized PV energy harvesting. The topology merges a boost as the front-end converter and a series-resonant converter as the back-end converter. The two converters are merged by sharing the switches for their operation while they are decoupled by separating their control variables. Merging of the converters is facilitated by a control scheme that can change both the duty-ratio and switching frequency. The boost converter provides the ability to obtain MPPT control by changing the duty-ratio and the series-resonant converter allows for output voltage regulation by controlling the switching frequency. By merging the two power stages, high efficiency is achieved due to zero-voltage switching that is obtained on both transistors and the component count is reduced. Full analysis and characteristics of the converter are detailed, and experimental results using a 400V/240W prototype validate its operation and features.

8.1.1. Introduction

Among the variety of grid-interactive photovoltaic (PV) systems, microinverters are an attractive option for modular and independent energy harvester. This concept disregards any mismatches among PV modules, provides possibility of individual PV-module optimal design, and allows independent maximum power point tracking (MPPT) [1], [2]. In many cases a PV microinverter is supplied by a single solar panel, with typical low voltage in the range of 20-30V. In such cases a high voltage-conversion ratio converter is required to produce the output's ac voltage [1]-[3]. Therefore, it is conventionally achieved by two-stage conversion; a dc-dc converter cascaded by an inverter is the most common arrangement for such systems [4]-[10].

The front-end converter that connects to the PV module steps up the voltage to a level compatible with the grid while performing MPPT. This compromises the output voltage

regulation capability of the converter since the two control objectives that are distinctly different simultaneously super-impose on the control command. In the majority of applications, the tasks are separated for two decoupled converters. One facilitates MPPT and another regulates the voltage [11]-[12].

The idea of one converter performing a specific task and another converter obtaining a different objective has been investigated and implemented in variety of applications such as: power-factor correction applications and LED drivers [13]-[18]. An interesting and attractive solution is to integrate two stages into one, as suggested in [19]-[25]. Merging of the two stages contributes to achieve better power processing characteristics, high efficiency, lower requirements from the DC link capacitor and reduced components count at the cost of slightly more complex control. This has been pursued in this study.

The objective of this study is to introduce a merged PWM-resonant dc-dc converter (MPRC) topology with high voltage gain for localized PV energy harvesting. The topology, shown in Fig. 8.1, combines a boost front-end with a series-resonant converter as the back-end. Merging is facilitated by sharing the transistors for the operation of both converters. Full decoupling is achieved by separation of the control variables and objectives. The boost front-end provides the ability to obtain MPPT and is controlled by variation of the duty-ratio whereas the series-resonant converter regulates the output voltage by changing the switching frequency. In addition, the operation of the converter provides ZVS on both MOSFETs, significantly lowers the power loss and maintains high efficiency.

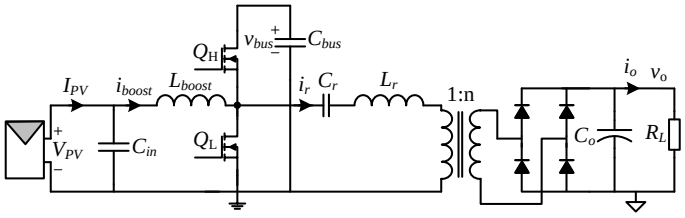

Fig. 8.1 Merged PWM-Resonant converter (MPRC) topology.

The rest of the paper is organized as follows: Section 8.1.2 describes the MPRC topology and details its principle of operation and control scheme. Primary characteristics and simulation results of the MPRC are provided in Section 8.1.3. Experimental results using a MPRC prototype are given in Section 8.1.4. Section 8.1.5 concludes the paper.

8.1.2. Merged PWM-Resonant Converter Topology

The high conversion ratio required for converting a single PV module voltage to the input voltage of a grid-tied inverter can be achieved by variety of ways. For example, a series-resonant converter (SRC) with high turns ratio of its transformer. However, to obtain both regulated output voltage *and* operation at the maximum power point of the PV module, another degree of freedom is required. A possible solution to overcome this challenge is by adding a boost converter between the input and the resonant converter in order to be able to operate at the MPP while regulating the output voltage. However, this reduces the efficiency and results in higher components count.

The MPRC power stage, shown in Fig. 8.1, combines a synchronous boost converter that is connected to the PV module and a SRC that is connected to the input of the inverter (marked as the load R_L). Three components are common for the stages, these are the power transistors (Q_H and Q_L) and the bus capacitor C_{bus}. Using this circuit, several key benefits are simultaneously obtained, the use of only two switches (instead of four) and single bootstrapped gate driver lowers the components count and cost. In addition, although the boost operates in CCM, the resonant nature of the SRC provides the ability to have zero-voltage switching (ZVS) on both transistors, significantly reducing the switching losses.

The key principle in the operation of the MPRC is in the control scheme. The boost's control variable is the switches' duty-ratio D while the SRC control variable is their switching frequency f_s. These two control variables can be simultaneously controlled without having one control variable affecting the other. Therefore, it allows the boost and SRC to use common switching devices for their operation, as shown in Fig. 8.2. It should be noted that since the current waveforms of the two converters have different shapes, a small bus capacitor is still required. The bus capacitor voltage v_{bus} is unregulated and may vary depending on the type of MPPT algorithm that is realized.

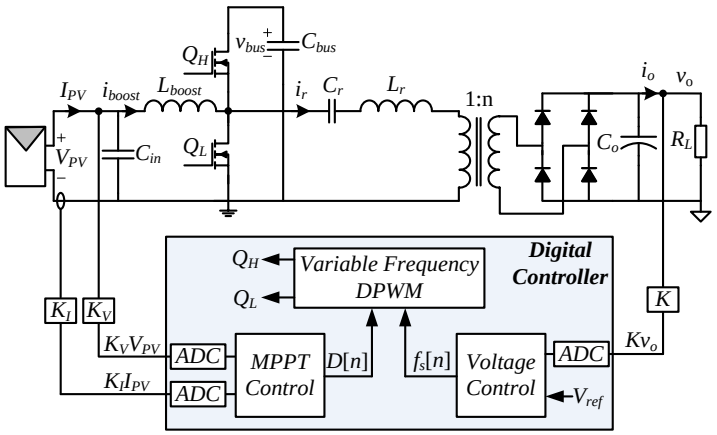

Fig. 8.2 Control scheme of the MPRC topology.

Assuming that under variations of the switching frequency the boost inductor current ripple does not exceed the CCM boundary, the voltage gain of the boost converter depend on the duty-ratio and is given by:

$$M_{boost}(D) = \frac{V_{bus}}{V_{PV}} = \frac{1}{1-D} \quad . \tag{20}$$

where D is the duty-ratio of QL.

The SRC's equivalent circuit under first harmonic approximation (FHA) is depicted in Fig. 8.3 and its normalized voltage gain is given by:

$$M_{SRC}(f_s, D) = \frac{V_{out,ac}}{V_{bus,ac}} = \frac{\sin(\pi D)}{1 + j\dfrac{n^2\sqrt{L_r / C_r}}{R_{ac}}\left(\dfrac{f_s}{f_r} - \dfrac{f_r}{f_s}\right)}, \tag{21}$$

where Vbus,ac and Vout,ac are the first harmonics at the input and output ports of the SRC, respectively, as illustrated in Fig. 8.3. fr is the resonance frequency given by $1/2\pi\sqrt{L_r C_r}$ and Rac is the resistance seen at the transformer's secondary side, given by $8R_L/\pi^2$ [26] and n is the transformer's turns ratio. Fig. 8.4 depicts the expression in (21) for different values of the quality factor Q and D=0.5. It can also be seen in (21) that MSRC depends on D for the amplitude value. However, since changes of the duty command are driven from the MPPT controller which varies D much slower compared to the change of fs by the frequency controller, D can be considered constant for the dynamic response of MSRC. A point that needs to be emphasized is that the resonant tank of the SRC should be designed so that Q is relatively high (typically higher than 5) for any load condition. This is necessary so that the current waveforms at the SRC is sinusoidal, even for cases that D is different from 0.5 as in conventional SRC operation.

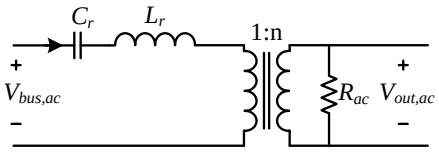

Fig. 8.3 Equivalent circuit of the SRC under FHA.

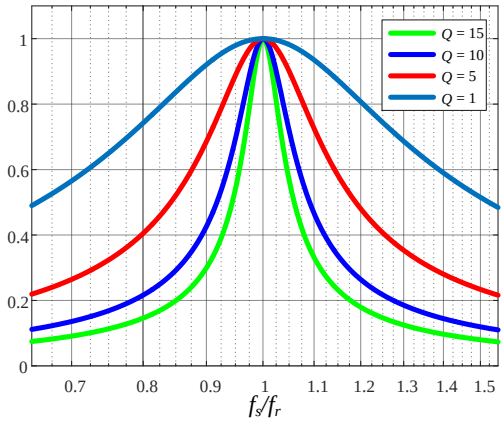

Fig. 8.4 Normalized voltage gain of the SRC.

The total voltage gain of the MPRC is the multiplication of (20) and (21):

$$M_{MPRC}(D, f_s) = \frac{V_{out}}{V_{PV}} = M_{boost} M_{SRC} \quad . \tag{22}$$

The SRC stage can be considered with varying input voltage and regulated output voltage (by frequency control regulation). This varying input voltage is v_{bus} which depends only on D, governed by the MPPT algorithm. Since the output voltage needs to be regulated, in case that the MPPT controller increases D and M_{boost} is increased, the frequency controller increases f_s so that M_{SRC} is decreased and the output voltage remains constant. This way any input power can be extracted by controlling D while the output voltage is maintained regulated by controlling f_s.

8.1.3. Primary Characteristics of the MPRC Topology

Due to the inherent differences between currents waveforms of the boost and the SRC, achieving ZVS on both high and low-side transistors is not immediate. The boost current that enters the switching node is triangular with a DC offset due to the CCM operation, while the SRC current at the switching node is sinusoidal, as illustrated in Fig. 8.5. A necessary condition to achieve ZVS on Q_H is that the current difference $i_d = i_r - i_{boost}$ is negative at its turn-on instance, i.e. $i_d < 0$. To achieve ZVS on Q_L it is necessary that the current difference will be positive at its turn-on instance, i.e. $i_d > 0$. Assuming a converter

efficiency of η, a duty-ratio of 0.5 and under FHA, the resonant current i_r at the switching instances can be approximated to

$$i_r = \pm\left|\frac{\pi\eta V_{PV} I_{PV}}{2nV_{out}}\sin(\phi)\right|, \tag{23}$$

where ϕ is given by

$$\phi = \tan^{-1}\left(\frac{n^2\sqrt{L_r / C_r}}{R_{ac}}\left(\frac{f_s}{f_r} - \frac{f_r}{f_s}\right)\right), \tag{24}$$

And the expression for i_{boost} is given by

$$i_{boost} = I_{PV} \pm \frac{V_{PV}}{4Lf_s}. \tag{25}$$

Using (23)-(25) the necessary condition to obtain ZVS on Q_H is

$$-\left|\frac{\pi\eta V_{PV} I_{PV}}{2nV_{out}}\sin(\phi)\right| - I_{PV} - \frac{V_{PV}}{4Lf_s} < 0, \tag{26}$$

whereas the necessary condition to obtain ZVS on Q_L is

$$\left|\frac{\pi\eta V_{PV} I_{PV}}{2nV_{out}}\sin(\phi)\right| - I_{PV} + \frac{V_{PV}}{4Lf_s} > 0\ . \tag{27}$$

It should be noted that condition (26) holds for any case since at this point the actual current direction of both currents is always directed toward the switching node. The more strict condition is (27) since one current is entering the switching node and the other is pointed out of it. Taking into account the capacitance between the switching node and ground C_{SW} and approximating i_d to a constant current source and v_{bus} to a voltage source for the dead-time period t_{dt} as depicted in Fig. 8.6, the following conditions are sufficient to guarantee full ZVS on both transistors:

$$\begin{aligned} &ZVS\ on\ Q_H: \quad t_{dt} > \frac{2C_{SW}V_{PV}}{\left|\frac{\pi\eta V_{PV} I_{PV}}{2nV_{out}}\sin(\phi)\right| + I_{PV} + \frac{V_{PV}}{4Lf_s}} > 0 \\ &ZVS\ on\ Q_L: \quad t_{dt} > \frac{2C_{SW}V_{PV}}{\left|\frac{\pi\eta V_{PV} I_{PV}}{2nV_{out}}\sin(\phi)\right| - I_{PV} + \frac{V_{PV}}{4Lf_s}} > 0 \end{aligned} \tag{28}$$

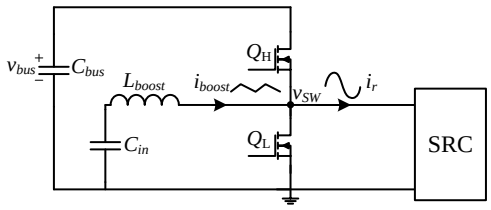

Fig. 8.5 Current waveforms at the switching node of the MPRC.

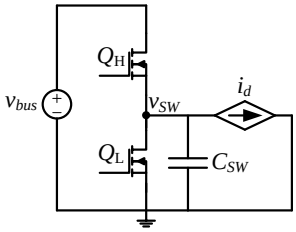

Fig. 8.6 Equivalent circuit for the dead-time period.

Fig. 8.7 shows simulation waveforms of the MPRC (obtained using PSIM) for two situations where D=0.5 and D=0.65. It can be observed that for both cases the two different duty-ratio values result in different values of v_{bus} and therefore it is compensated by the voltage regulation controller that changes the switching frequency accordingly to maintain the output voltage constant. In the case that D=0.5 v_{bus} is lower, and therefore f_s is lower as well. Also depicted is i_d, and it can be observed that for the two cases both conditions (26) and (27) hold at the switching instances and ZVS is obtained.

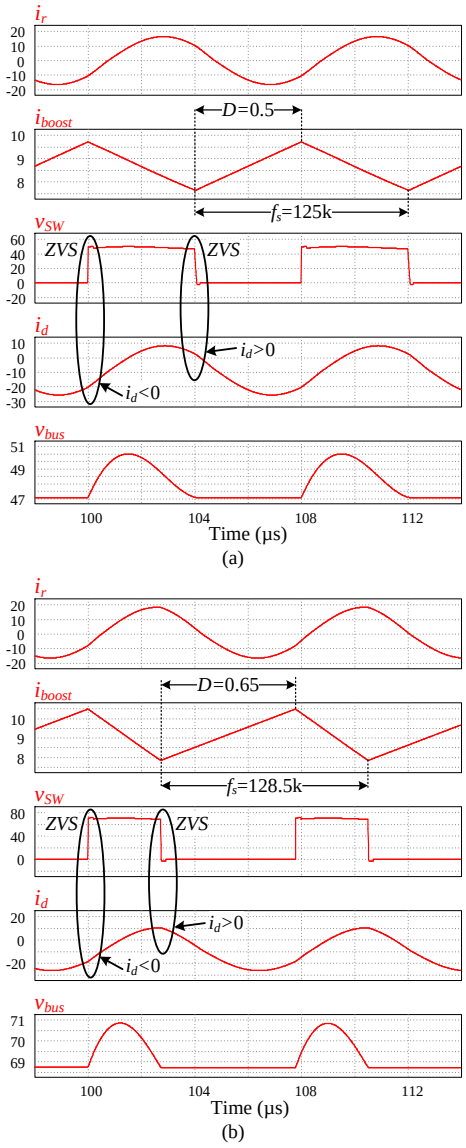

Fig. 8.7 Simulation waveforms of the MPRC for (a) D=0.5, (b) D=0.65.

8.1.4. Experimental Results

To validate the operation of the MPRC topology, a 400V/240W experimental prototype was built and tested. The components' parameters and values are detailed in TABLE II. The converter was digitally controlled by a dsPIC33F series microcontroller from Microchip [27], sensing the PV module's voltage and current for MPPT control and the output voltage for regulation, as illustrated in Fig. 8.2. A picture of the experimental setup is given in Fig. 8.8.

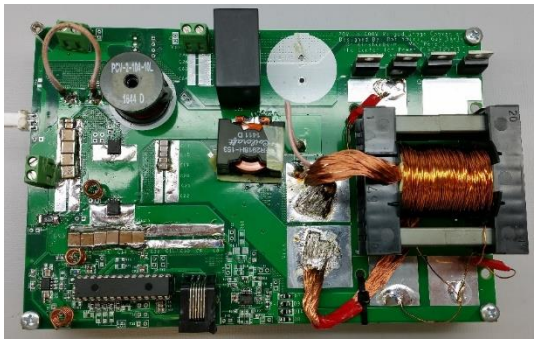

Fig. 8.8 Picture of the MPRC experimental prototype.

TABLE II. EXPERIMENTAL PROTOTYPE'S PARAMETERS VALUES

Component	***Value / Type***
Input voltage V_{PV}	20-30 V
Output voltage V_o	400 V
Bus capacitance C_{bus}	6 µF
Output capacitor C_o	10 µF
Transformer's turns ratio 1:n	1:26
Resonant frequency f_r	~107 KHz
Resonant capacitance C_r	110 nF
Resonant inductance L_r	20 µH
Boost inductor L_{boost}	100 µH
Power transistors Q_H and Q_L	100V, 6.6mΩ

Fig. 8.9 and Fig. 8.10 show the experimental MPRC's prototype waveforms for various load, input voltage duty-ratios conditions. The shown waveforms are the switching node, bus voltage, resonant current, boost current and their difference. Fig. 8.9 shows the case where the duty-ratio is D=0.65. It can be observed that the change between different input voltages [Fig. 8.9(a) vs. Fig. 8.9(b) and Fig. 8.9(c) vs. Fig. 8.9(d)] changes the bus voltage and to regulate the output voltage to 400V this change is compensated by variation of the switching frequency. For example, when V_{PV} is 26V the bus voltage is 73.1V and the resultant switching frequency is 129.3KHz [see Fig. 8.9(c)], and when V_{PV} is reduced to 22V the bus voltage is 62.1V and the switching frequency is lowered to 124.6KHz [see Fig. 8.9(d)] to keep the output voltage regulated. It can also be observed that the average input current (the mean of i_{boost}) is increased when the input voltage is decreased, this is since the load in this case is kept constant. In addition, different load values results in different frequency variation for the same input voltages due to different Q values as expected by the analysis from Section II. When the input voltage changes from 26V to 22V the switching frequency is reduced from 115.5KHz to 113.5KHz for a 160W load [high Q – see Fig. 8.9(a) and Fig. 8.9(b)] while for a 53W load the switching frequency reduces from 129.3KHz to 124.6KHz [low Q – see Fig. 8.9(c) and Fig. 8.9(d)].

Fig. 8.10 presents the same waveforms for a duty-ratio of D=0.5 with different input voltages. Here the bus voltage values are lower and therefore the switching frequency values are lower compared with the cases shown in Fig. 8.9. In all the presented cases ZVS is obtained on both transistors due to the polarity of i_d at the switching instance. Fig. 8.11 zooms in on the switching instances and depicts the switching node voltage v_{SW} and the current difference i_d to better view the ZVS on the transistors. It can be observed that when Q_L is turned off i_d<0 which charges the capacitance during the commutation and the body diode of Q_H conducts before it is turned on. The opposite transition occurs when Q_H is turned off and i_d>0 which discharges the capacitance and the body diode of Q_L conducts until it is turned on. Efficiency measurements of the converter are provided in Fig. 8.12. As can be observed, the peak efficiency is 93.4% and above 89% for most of the load range.

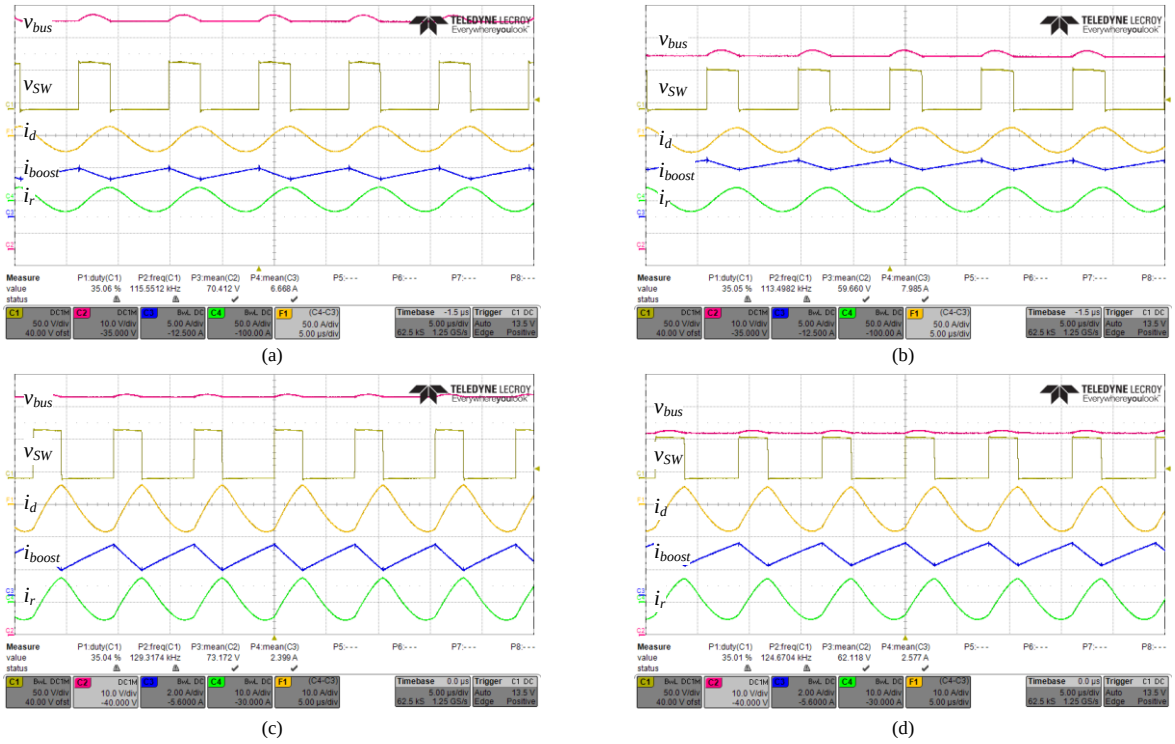

Fig. 8.9 Experimental waveforms of the MPRC experimental prototype in four different load and input voltage conditions for D=0.65: (a) V_{PV}=26V, R_{Load}=1KΩ, (b) V_{PV}=22V, R_{Load}=1KΩ, (c) V_{PV}=26V, R_{Load}=3KΩ, (d) V_{PV}=22V, R_{Load}=3KΩ. Signals from top to bottom: C2 – Bus capacitor voltage v_{bus}; C1 – Switching node v_{SW}; F1 – Current difference i_d; C3 – Boost current i_{boost}; C4 – Resonant current i_r . Time scale is 5µs/div.

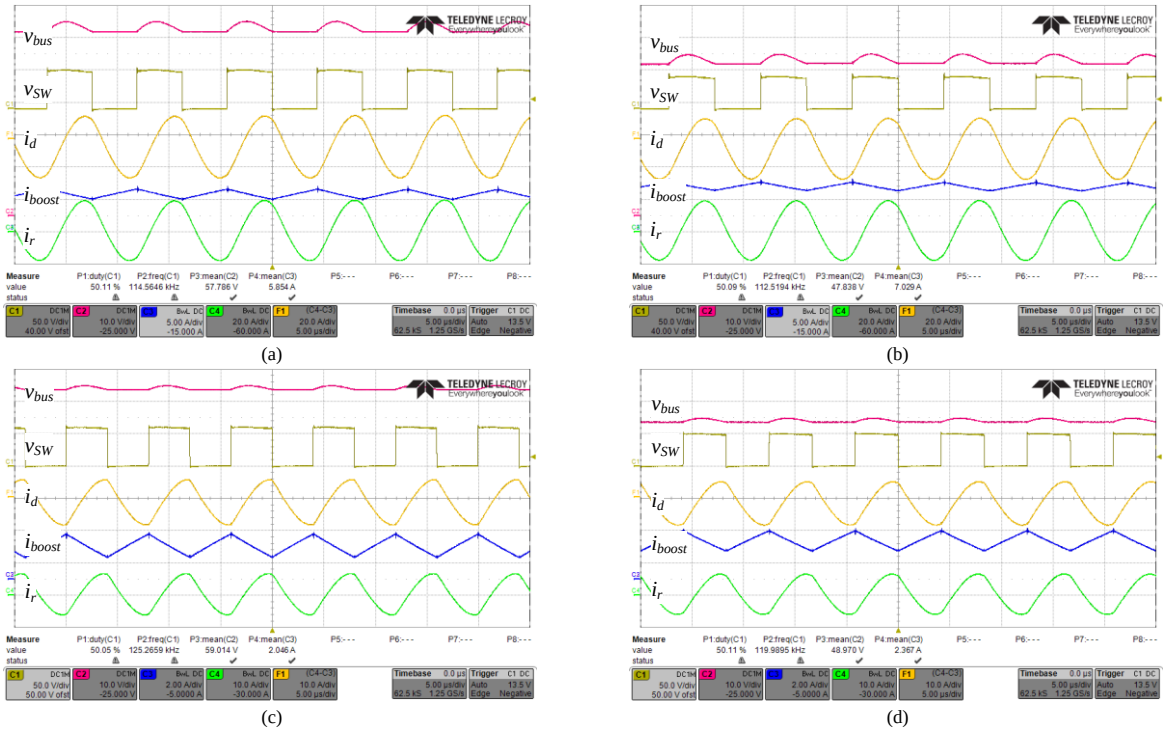

Fig. 8.10 Experimental waveforms of the MPRC experimental prototype in four different load and input voltage conditions for D=0.5: (a) V_{PV}=30V, R_{Load}=1KΩ, (b) V_{PV}=25V, R_{Load}=1KΩ, (c) V_{PV}=30V, R_{Load}=3KΩ, (d) V_{PV}=25V, R_{Load}=3KΩ. Signals from top to bottom: C2 – Bus capacitor voltage v_{bus}; C1 – Switching node v_{SW}; F1 – Current difference i_d; C3 – Boost current i_{boost}; C4 – Resonant current i_r . Time scale is 5µs/div.

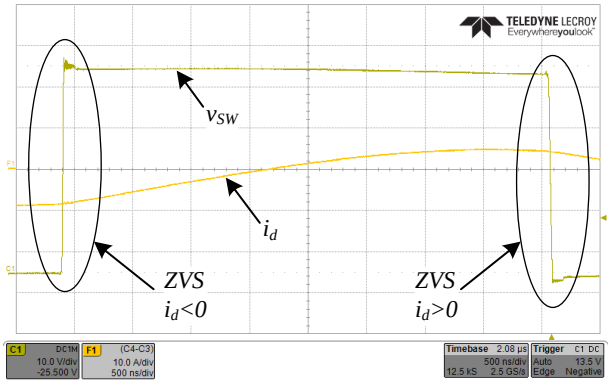

Fig. 8.11 Experimental waveforms of the MPRC experimental prototype demonstrating ZVS transitions. C1 – Switching node v_{SW} (10V/div); F1 – Current difference i_d (10A/div). Time scale is 500ns/div.

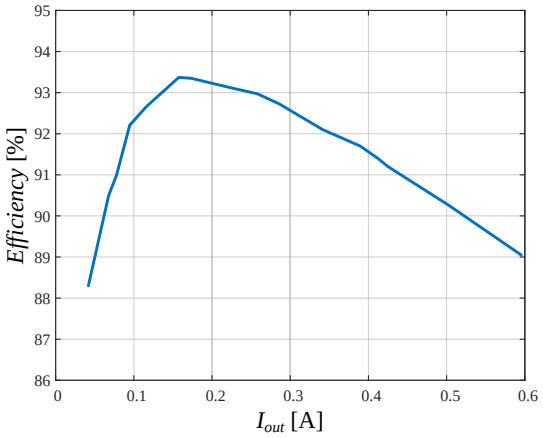

Fig. 8.12 Efficiency measurements of the experimental prototype.

8.1.5. Conclusion

A merged PWM-resonant dc-dc converter topology for localized PV energy harvesting has been presented in this study. The topology combines a boost front-end converter and a series-resonant converter as the back-end converter by using common power switches. Merging of the stages is facilitated by a controller that controls both the duty-ratio and switching frequency, allowing for both MPPT control and output voltage regulation while obtaining high efficiency due to ZVS on both transistors. Steady-state analysis and primary characteristics have been presented, showing the benefits of the converter. The experimental results of the converter are in excellent agreement with the theoretical analysis, showing promising power processing characteristics and making the converter an attractive candidate for localized PV energy harvesting.

8.1.6. References

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