BEN-GURION UNIVERSITY OF THE NEGEV
FACULTY OF ENGINEERING SCIENCES
DEPARTMENT OF ELECTRICAL ENGINEERING

GYRATOR RESONANT SWITCHED CAPACITOR CONVERTER

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE MSc. DEGREE

By: Alon Cervera

Supervised by:

Professor Sam Ben-Yaakov

and

Dr. Mor Mordechai Peretz

December 2013

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December 2013

אוניברסיטת בן-גוריון בנגב

הפקולטה למדעי ההנדסה

המחלקה להנדסת חשמל ומחשבים

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תקציר

עבודה זו מציגה ממיר קבלים מתמתגים תהודתי בעל נצילות גבוהה עבור יחס המרה רחב ורציף. נצילות הטופטלוגיה תלויה בעיקרה בהפסדי מוליכות, ואינה קשורה ליחס ההמרה. תכונה זו מהווה יתרון על פני ממירי קבלים מתמתגים קלאסיים, אשר בהם ישנה תלות ישירה של הנצילות ביחס ההמרה. על פי עקרון העבודה מיושמים שלושה מצבים של מיתוג בזרם אפס על מנת לטעון, לפרוק ולאזן את המטען, אשר נשאר על הקבל המתמתג. שיטת הפעולה מניבה מקור זרם תלוי מתח המתנהג כג'יראטור, ולו תחום המרת מתחים רחב (מעל ומתחת למתח יחידה), כמו גם יכולת העברת הספק דו-כיוונית. העבודה מספקת ביטויים אנליטיים ליחס ההמרה ולנצילויות הצפויות אשר מאומתים על ידי סימולציות ותוצאות ניסוייות. תוצאות ניסויים אשר בוצעו על הממיר מדגימות נצילות שיא של 96%, כמו גם נצילות הגדולה מ- 90% עבור טווח רחב של הגברי מתח ותנאי העמסה. בנוסף, המערכת נמצאה יעילה מאוד במקרי קיצון של עומסים קלים כמו גם כבדים. חלק זה פורסם ב- " proceedings of the IEEE Energy Congress and Exposition (ECCE) 2013" [1] וגם נשלח לעיתון "IEEE transactions on power electronics "

ממיר גשר פותח עבור ייעוד ספציפי של עיבוד הספק דיפרנציאלי למען ייצוב של זרימת הספק דרך תאים המחוברים בשרשרת טורית כדוגמת פאנלים פוטו-וולטאים (PV), קבלים ומצברים. בממיר מגולמים בקרה דיגיטלית ורכיבי חישה, אשר מקנים לממיר יכולות לביצוע איתור לנקודת מקסימום הספק מקומית, מיתוג בזרם אפס, נצילות גבוהה עבור טווח עבודה רחב, ומימדים מצומצמים. הממיר החדש פועל כמקור-זרם תלוי-מתח, ונשלט על ידי בקרת זמן-מת או תדר. פעולת הממיר מודגמת על ידי סימולציות וניסויים. חלק זה התקבל כפרק ממחקר גדול יותר ב- " IEEE Applied Power Electronics Conference (APEC) 2014" , וחלקים מסויימים פורסמו קודם לכן [2], [3].

מייצב מתח חדש, קטן ויעיל, נבנה על ידי שימוש בטכנולוגיית ממיר קבלים מתמתגים תהודתי המתנהג כג'ירטור. ייצוב המתח מיושם על ידי מודולציית רוחב פולס (PFM) דיגיטלית פשוטה. לממיר תגובת מעבר אידיאלית יחד עם התנהגות מסדר אפס עבור כל סוגי ההפרעות. המייצב החדש שפותח מתפקד כמקור זרם תלוי-מתח בעל טווח יחס המרה רחב (גדול כמו גם קטן מיחידה), ובעל מאפייני נצילות קבועים לכל טווח העבודה. פעולת מייצב המתח מאומתת על גבי אבטיפוס ניסויי בהספק 20 וואט. התוצאות מדגימות התאוששות אידיאלית מתופעות מעבר בצד

הספק כמו גם הצרכן, ללא כל נפילות או נחשולי מתח. פרק זה התקבל לפרסום ב " IEEE Applied Power Electronics Conference (APEC) 2014".

בעבודה זו מוצג אלגוריתם ליישום כיול שלא בזמן אמת למיתוג בזרם אפס בעבור ממיר קבלים מתמתגים רזוננטי המתנהג כג'ירטור. בנוסף, ניתנת הצצה אל תוך מחקר מתמשך על האפשרויות של שילוב בין מיתוג בזרם אפס לבין מיתוג במתח אפס. שילוב זה מאפשר מיתוג-רך מדוייק יותר וכיול עצמי מהיר יותר, בהינתן תנאי עבודה לא אידיאליים. כמו כן, העבודה מציגה ניתוח תיאורטי ותוצאות ניסוייות מתוך המחקר המתמשך.

∞

Dedicated to my late grandfather, Bernard,

who bestowed me with the ability to dream far beyond perceptible limits.

∞

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Abstract

A resonant switched capacitor converter (RSCC) with high efficiency over a wide and continuous conversion ratio range is introduced. The efficiency of the topology depends primarily on the conduction losses and is decoupled, to a large extent, from the voltage conversion ratio. This is an advantage by comparison with classical switched capacitor converters, for which the efficiency is strongly related to the conversion ratio. The operation principle comprises the application of three zero current switching (ZCS) states to charge, discharge and balance the remaining charge of the flying capacitor. This results in a gyrator, i.e. a voltage-dependent current source, with a wide voltage conversion ratio range (below as well as above unity) as well as bidirectional power flow capabilities. The analytical expressions for conversion ratio and expected efficiency are provided and validated by simulation and experiments. The experimental verifications of the converter demonstrate peak efficiency of 96% and above 90% efficiency over a wide range of voltage gains and loading conditions. In addition, the system was found to be highly efficient at the extreme cases of both light and heavy loads. This part of the research has been published in the proceedings of the IEEE Energy Congress and Exposition (ECCE) 2013 [1], and submitted to the IEEE Transactions on Power Electronics.

A bridge converter is developed, specifically aimed at differential power processing to stabilize power flow through DC string cells such as Photo Voltaic (PV) panels, capacitors, and batteries. The converter incorporates digital control and sensory elements that give it local maximum power point tracking (MPPT) capabilities, ZCS, high efficiency over a wide operation range and miniature size. The new converter operates as a voltage-dependent current source and is regulated by dead-time or frequency control. The converter's operation is demonstrated by simulation and experiments. This part of the research has been accepted, within a larger study, to be presented at the IEEE Applied Power Electronics Conference (APEC) 2014. Relevant sections have also already been published [2], [3].

A new, small and efficient voltage regulator realized using a gyrator resonant switched capacitor converter (GRSCC) technology is introduced. Voltage regulation is implemented by means of simple digital pulse density modulation (PDM). It displays an ideal transient response with a zero-order response to all disturbance types. The newly developed RSCC acts

as a gyrator with a wide range of voltage conversion ratios (below as well as above unity) with constant efficiency characteristics for the entire operation range. The operation of the voltage regulator is verified on a 20W experimental prototype, demonstrating ideal transient recovery without over/undershoots in response to load and line transients. Simple design guidelines for the voltage regulation system are provided and verified by experiments. This part of the research has been accepted for presentation at the IEEE Applied Power Electronics Conference (APEC) 2014.

An algorithm for applying offline ZCS calibration in the new GRSCC is introduced, alongside an insight into ongoing research on possibilities for integrating between zero voltage switching (ZVS) and ZCS, which would allow for more precise soft switching and faster convergence. Analysis and experimental results are presented.

Thesis Overview

This work addresses the present-day challenges in the advancement of switch-mode converters towards high power density and fast response times, without compromising on conversion efficiency. The research proposes a new converter topology, based on switched-capacitor technology that manages to overcome the discussed challenges. Additionally, various applications are thoroughly investigated. A brief summary of the research and the main results is given next:

The work proposes a high efficiency resonant switched capacitor converter (SCC) topology with a continuous conversion ratio ["A high efficiency resonant switched capacitor converter with continuous conversion ratio," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, 2013]. The topology was developed to *disengage the rigid relationship between the efficiency and the voltage gain* existing in conventional SCCs. Additionally, the topology produces a continuous and controllable conversion ratio, and also enables bi-directional power transfer, allowing the converter to fully achieve the merits of today's switched inductor converters yet maintain the benefits of being a SCC.

The results of the research lay the foundations to develop converters targeted for one's specific demands, providing analytic tools to model the static and dynamic behavior, along with design guidelines and experimental proof.

Another subject of the research addresses several applications and implementation topics regarding the developed topology:

A generic bridge derivative is presented, exemplifying a simple implementation to the generic gyrator topology, for the use of power source balancing [Enhanced Differential Power Processor for PV Systems: Resonant Switched-Capacitor Gyrator Converter with Local MPPT," in *IEEE Applied Power Electronics Conference (APEC)*, 2014]

A resonant switched capacitor voltage regulator with ideal transient response is presented [Resonant switched-capacitor voltage regulator with ideal transient response," in *IEEE Applied Power Electronics Conference (APEC)*, 2014], suggesting a high efficiency regulator with zero order transient response times based on a switched capacitor converter.

The result of this investigation provides a streamlined solution to the high demands from voltage regulators enabling high power density.

The thesis further provides insight into ongoing research on providing true soft-switching in a real-world environment. The work focuses on off-line calibration integrating between zero current and zero voltage switching scenarios. The results enable achieving high efficiencies using limited hardware resources and compensate for the resonant components' value drift, raising the efficiency and reliability of a resonant switching system.

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Acronyms and Abbreviations

SMPS – Switch-mode power supply
SIC – Switched inductor converter
SCC – Switched capacitor converter
RSCC – Resonant switched capacitor converter
MOSFET – Metal oxide semiconductor field effect transistor
CMOS – Complementary metal oxide semiconductor
IC – In-Circuit
DCM – Discontinuous conduction mode
PDM – Pulse density modulation
MCU – Micro controller unit
ZCS – Zero current switching
NC – No charge
PC – Partial charge
CC – Complete charge

Inline References Legend

X.XX – Section / Chapter number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure

1. Introduction

1.1. Overview of linear and switched mode converters [4]

Linear power supplies normally use an operational amplifier feedback network to create a controllable series resistance between rectified filtered supply and the load, regulating the output voltage by feedback to a series transistor (Fig. 1.1). As a given load draws more current, the output voltage drops, feeding back to error compensation circuitry that, in turn, decreases the series resistance, which amends the output voltage.

The series resistance in linear supplies introduces losses that are proportional to the required voltage drop between the input and output voltages. The relationship can be described by (1.1), which is a key equation and will be mentioned numerous times throughout this work, with some variations.

$$\eta = \frac{P_2}{P_1} = \frac{V_2}{V_1}, \tag{1.1}$$

where P_1 and P_2 are the input and output powers, respectively, and V_1 and V_2 are the input and output voltages, respectively. This equation is true when the connection is in series, i.e. the input and output currents are the same. This power regulation method's efficiency profile is a steep linear drop, making it an effective method for regulation when only a small voltage drop is needed. On the other hand, linear converters give a precise output voltage with little to no output ripple.

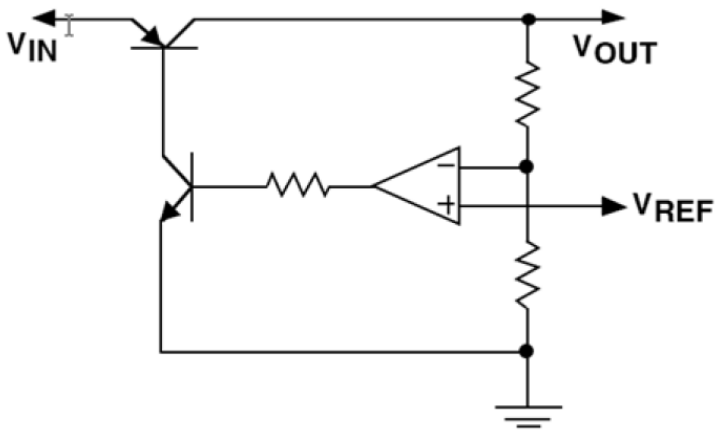


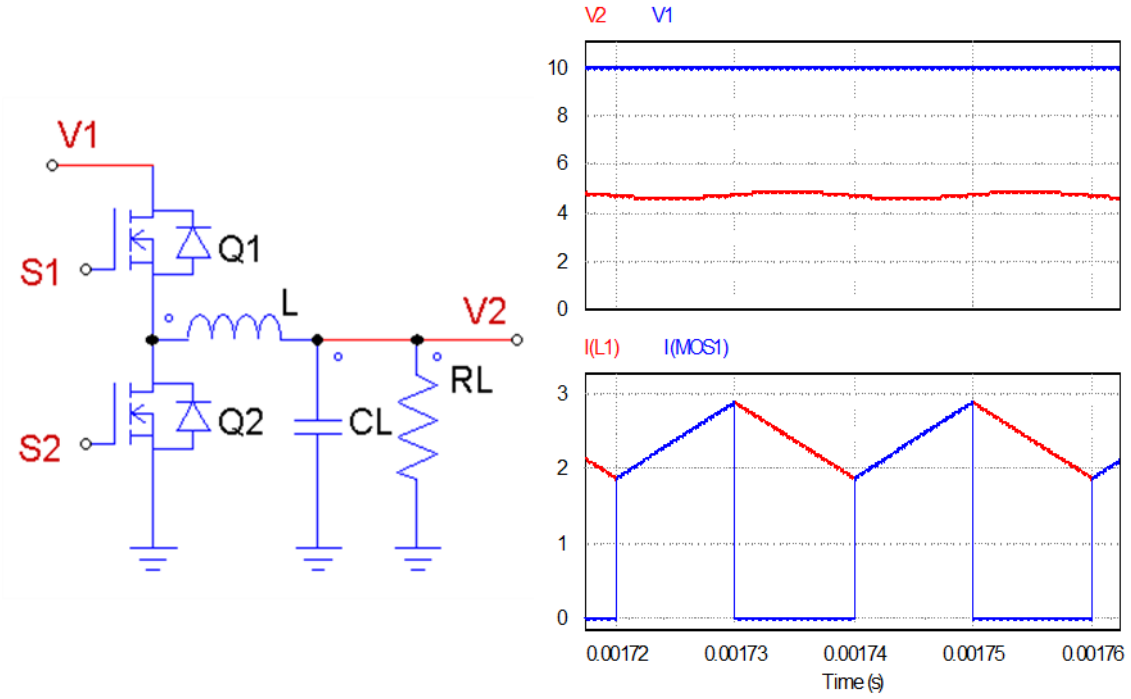
Fig. 1.1 Linear power supply basic example.

Switch Mode Power Supplies (SMPS) and converters aim to use high frequency switching in order to reduce component size. In its simplest form, a reactive element is switched in between an input and an output, charging and discharging, respectively. The reactive element can be either an inductor or a capacitor or both. Even though all the methods have been investigated over the years, an inductor was and still is the most commonly used choice as the main reactive element in a SMPS.

Switched Inductor Converters (SICs) were preferred due to efficiency, cost, simplicity and reliability concerns. Creating an inductor requires winding a coil around a ferromagnetic element. This is a simple and reliable form of energy storage. Storing the same amount of energy in a capacitor required bulky and short lifespan electrolytic capacitors. But most importantly, as will be explained in the following chapters, a method enabling a wide range of conversion ratios maintaining high efficiencies for SCCs was yet to be discovered. SCCs suffer from linear efficiency drops and in some cases have no advantage in terms of efficiency over linear regulators.

An example of an inductor-based converter is given in Fig. 1.2, describing a “Buck” converter – a simple, efficient and commonly used step down converter. The converter sets a voltage conversion ratio by using an inductor that serves as a low-pass filter fed by a pulsed voltage source, delivering mostly the average DC of the pulse. The pulsed source is produced by repeatedly switching the input voltage, creating the high level of the input signal. The low-level is created by connecting a freewheeling diode between the switched input and the ground. The diode naturally opens as the input is disconnected due to current continuity demands of the inductor. The switching frequency now depends on hardware capabilities, e.g.

MOSFET turn on and turn off times, driving components' speed, etc. The limits will be further discussed in 1.3. Raising the frequency decreases the required inductance, significantly shrinking the inductor's volume, but comes at the cost of losses.



(a) (b)

Fig. 1.2 (a) A typical synchronous Buck converter. The transistor Q_2 can either be a switch (synchronous mode) or a freewheeling diode. (b) Traces showing the operation of a Buck converter. The input and output voltages are shown in the top graph and the current seen by the input and output is shown in the bottom graph.

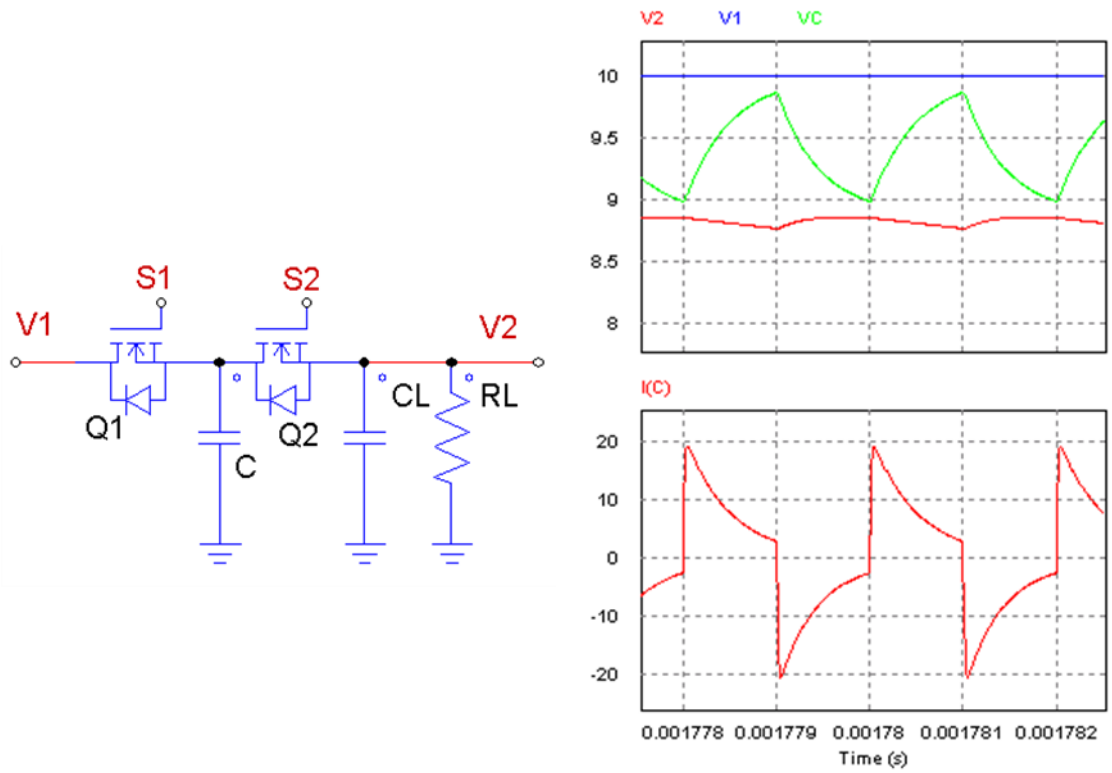
Knowledge about inductor-based SMPS has evolved to a point that high efficiency is easily obtained, especially when implementing soft switching techniques, but size reduction remains somewhat limited. Miniaturization is strongly demanded in current and emerging technologies and CMOS-only realizations are pursued in order to completely embed power supplies on-chip. This poses a problem for inductor technology, since while attempts have been made to create on-chip SICs [5], [6], a way to efficiently mass produce IC inductors retaining high efficiency has yet to be found.

1.2. Switched capacitor converters overview

1.2.1. Hard switched SCC (1st order tank)

A switched capacitor based converter (SCC) works on the principle of voltage potential leveling. In its most simplistic version, shown in Fig. 1.3, a flying capacitor is alternated in

between the input and the output and transfers charge from the higher to the lower potential, aiming to level the potentials. As in most switched converters, if the output load is resistive, an additional capacitor is needed to maintain a steady DC output voltage while the flying capacitor charges at the entrance. To reduce the required size of the flying and output capacitors, switching frequency is raised to a high level, to create multiple charges and discharges.



(a) (b)

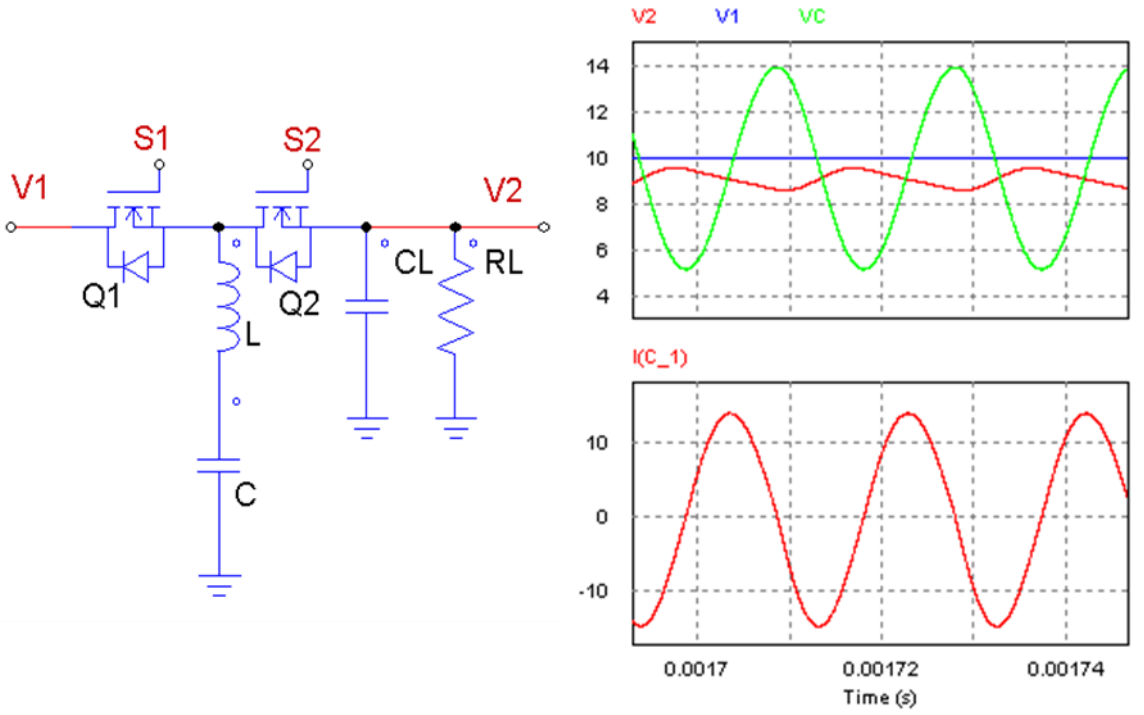
Fig. 1.3 A 1st order SCC: (a) layout (b) traces of the voltages and currents (with some ESR added to the resonant tank).

Many variations of the switched capacitor exist that are able to provide multiple output levels by manipulating multiple flying capacitors, alternating between parallel, series, or mixed parallel-series connections. These yield discrete fractional options to voltage conversion and will be discussed further in section 1.5.

1.2.2. Soft switched SCC (2nd order resonant tank)

In order to reduce the switching losses (discussed in 1.3), working in a resonant mode has been suggested. Adding an inductive element in series with the flying capacitor changes the charge and discharge profiles from an exponent to a 2nd order profile. Switching at exact

resonance, when the current crosses a zero value, as seen from the traces in Fig. 1.4, creates a sinusoidal shaped current and switching can occur on or close to zero current. This eliminates P_{sw} , as modeled in section 1.3.



(a) (b)

Fig. 1.4 A 2nd order SCC: (a) layout (b) traces of the voltages and currents (with some ESR in the resonant tank).

A major drawback in soft switched SCC is the inability to create an output voltage that is different from its natural target voltage (1:1, 2:1, etc.). In soft switched SCC, the resultant charge-balance of the flying capacitor(s) differs from zero after a charge/discharge cycle when $V_2 \neq V_1$. The residual charge left in the flying capacitor(s) impacts the average current and causes it to diverge, which, in turn, eventually increases/decreases the output voltage such that the charge-balance of all the capacitors will be satisfied. The result is that the system naturally drifts back to the target voltage. To better view this problem, consider a generic 1:1 resonant SCC (Fig. 1.4) with a desired output voltage of $V_2<V_1$. The flying capacitor voltage and current are illustrated in Fig. 1.5. The current waveform shows that although ZCS is obtained, the charge received from the source is not equal to the one delivered to the output. This translates into an unbalanced capacitor voltage that continues to rise every cycle.

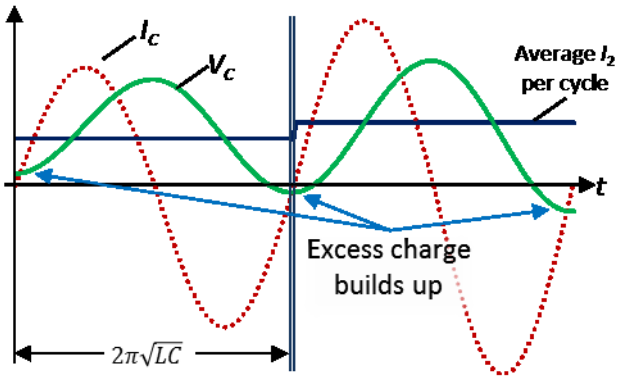


Fig. 1.5 Typical waveforms of the flying capacitor in the SCC described in Fig. 1.4: dotted line - I_C, solid line - V_C, flat step - average I_2 corresponding to each switching cycle

1.3. Switching losses

Switching an element at high frequencies comes at a cost. Switching losses become a dominant factor in overall converter efficiency as frequency rises. In MOSFETs, those losses originate from two main phenomena. One happens just from opening the transition path and is caused by parasitic capacitance in the transistor. In order to activate the MOSFET, voltage has to be applied to the gate, namely V_{gs}, and charge parasitic non-linear capacitances. In short, come capacitance affects the gate, namely C_{iss}, creating an inrush gate current and consumes it's energy from the driver. Other affects the drain, namely C_{dss}. These capacitances need to be charged and discharged within every cycle, i.e. the stored energy is lost in each cycle. Fig. 1.6 shows an example of the charge profile for a gate of a IXTP160N10T MOSFET. This is the charge that is demanded in order to charge the gate to a certain desired level. The power that is lost due to parasitic capacitances when operating a certain MOSFET at a desired frequency of f_s is given by:

$$P_{loss,caps} = (C_{iss}V_{gs}^{\ 2} + C_{dss}V_{ds}^{\ 2})f_s\,, \tag{1.2}$$

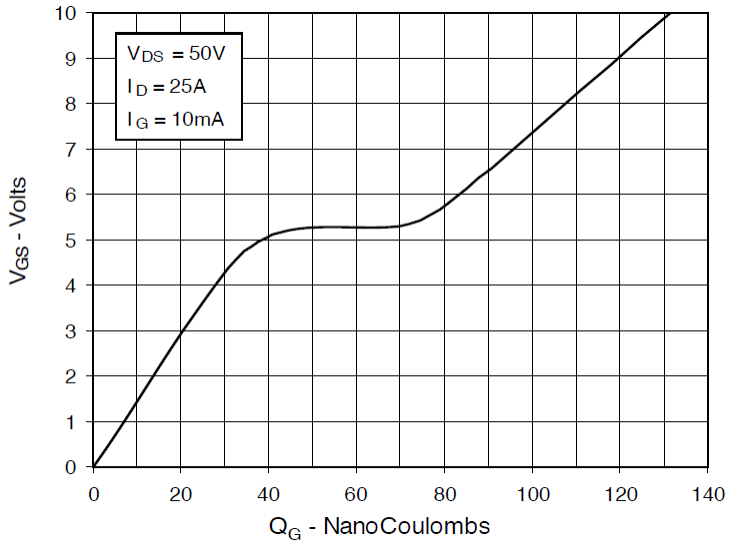


Fig. 1.6 Example of gate charge profile for ixys N-MOSFET model IXTP160N10T [7]

Driving circuitry, or an IC driver, is generally used to supply the charge for opening the gate. The driver capabilities, i.e. the current that the driver is able to supply and sink, determine the time it takes for the gate to open and close. This is a second source of switching losses, with the voltage and current on the MOSFETs' conduction path during switching transitions, V_{ds} and I_d, , being the key factor. Fig. 1.7 illustrates the stress on the transistor during turn on for a general hard switching case. Before turn on, V_{ds} exists on the conduction path with no current; after turn on I_d exists with negligible voltage. During transition, V_{ds} drops, while I_d rises, creating an overlap area where the component dissipates power. The overlap time is shorter than the time it takes V_{gs} to fully swing from rail to rail, and is assumed here to resemble the time it takes V_{gs} to clear the *flat* charge line seen in Fig. 1.6. The flat line is caused by gate-drain capacitance that needs to be discharged for the conduction path to open effectively, being reflected as a large capacitance. In order to provide a simple model for the dissipated power at transitions, the following is assumed: during transition the drive current, I_g, is constant, the overlap times are identical in both turn on and turn off and the dissipated power, V_{ds} and I_d rise and fall linearly. Keeping in mind that two transitions (turn on and turn off) occur in one cycle, the dissipated power, $P_{loss,overlap}$, resulting from the overlap can be estimated by:

$$P_{loss,overlap} = \frac{1}{3} f_s t_r V_{ds} I_d \approx \frac{1}{3} f_s \frac{\Delta Q_{flat}}{I_g} V_{ds} I_d \ , \tag{1.3}$$

where ΔQ_{flat} is the charge needed to cross the flat area in Fig. 1.6.

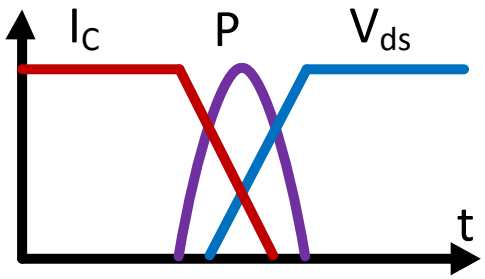


Fig. 1.7 Conduction path switching losses caused by the cross-section between the current and the voltage between the drain and the source

1.4.Modeling losses and efficiency for regulating an SCC

Depending on the configuration of a SCC, it has a specific output target voltage that is correlated to the input voltage, $V_T = NV_{in}$, where N is a *rational* number corresponding to the conversion ratio. The reason why the number is rational originates from the method by which different conversion ratios are achieved. A divider where $N = 0.5$, for example, is achieved by alternating two capacitors between the input and the output; these are interconnected in series when at the input and interconnected in parallel when at the output. The result is that their voltage is summed at the entrance and their currents are summed at the output, leading to $N = 0.5$. Hence in practice, for a given V_{in}, only discrete rational target voltages (V_T) exist.

The effective output voltage, V_o, differs from V_T due to a voltage drop that exists on the series resistances due to current flowing through the load. In hard switched SCC, the series resistance causing the voltage drop can be represented by [2], [8]:

$$\begin{aligned} R_e &= R_{e,1} + R_{e,2}\frac{1}{2f_S C_1}\coth\left(\frac{\beta_1}{2}\right) + \frac{1}{2f_S C_2}\coth\left(\frac{\beta_2}{2}\right), \\ \beta_i &= \frac{t_i}{R_i C_i} \end{aligned} \tag{1.4}$$

where $R_{e,i}$, C_i and t_i are the resistance, capacitance and conduction time of the charging and discharging states. Depending on the load value, altering the series losses can aid in achieving any other desired voltage. This can be done by altering the switching times or the switching frequency, changing the result of (1.4).

In soft switched resonant SCC, the series resistance causing the voltage drop can be represented by [2], [8]:

$$R_e = R_{e1} + R_{e2} = 4Q_1^2 R_1 \cdot \phi_1 \cdot \tanh(\phi_1) + 4Q_2^2 R_2 \cdot \phi_2 \cdot \tanh(\phi_2)$$
$$\omega_{0_i} = \frac{1}{\sqrt{L_i C_i}};\quad Q_i = \frac{\omega_{0_i} L_i}{R_i} = \frac{\sqrt{\frac{L_i}{C_i}}}{R_i};\quad \phi_i = \frac{\pi}{2\sqrt{4Q_i^2 - 1}} \quad , \tag{1.5}$$

where L_i is the RLC loop inductance.

In soft switched SCCs the series resistance cannot be altered. It can be seen that (1.5) only depends on the physical circuit parameters. There is then no way to directly regulate soft switched SCCs, other than to physically introduce further series losses by the addition of some form of linear regulation.

Using the losses model, a SCC can be viewed as a lossless converter with series resistance (Fig. 1.8). The converter's efficiency is then only dependent on the voltage drop created by the series resistance. The efficiency is given by:

$$\eta = \frac{P_o}{P_{in}} = \frac{P_o}{P_T} = \frac{V_o I_o}{V_T I_T} = \frac{V_o}{V_T}. \tag{1.6}$$

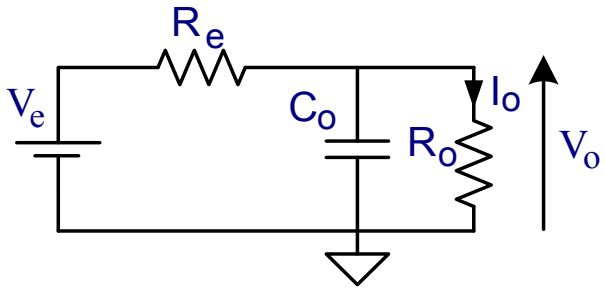


Fig. 1.8 SCC generic equivalent circuit

1.5.Literature survey – overcoming gain-efficiency dependence

Due to the voltage balancing nature of the basic SCC configurations described in 1.2, these converters lack regulation capabilities that do not introduce direct losses, similar to the linear power supplies mentioned in 1.1. In 1st order SCCs, losses can be introduced by

adjusting the switching frequency or duty cycle (seen in (1.4)) and hence increasing R_s. 2nd order soft switched SCCs cannot be tweaked in the same manner if soft switching is to be maintained, effectively locking the conversion ratio. This was a major problem and, along with the small variety of available capacitors with high value and long durability, SCCs were rarely used.

Miniaturization demands and advances in capacitor technology reignited the interest in SCC technology and research in the field resurfaced. Most work accepted the need to compromise on efficiency, some focused on working with limited conversion ratios where efficiency is high or on creating multiple conversion ratios, and some aimed to find ways to break this rigid relationship between the conversion ratio and the efficiency. The following sub-sections review the latest relevant advancements in this field.

1.5.1. Extended binary / Fibonacci multilevel schemes [9], [10]

Research conducted in our laboratory introduced a family of multi-level converters that use a number of flying capacitors with multiple connectivity options. The capacitors are switched in between the input, the output and themselves following a specific algorithm that effectively results in the output being some fraction of the input. Using only the extended binary algorithm, for example, a converter consisting of n flying capacitors can yield $2^{n+1}-1$ conversion ratios from $V_2 = \frac{1}{2^n} V_1$ to $V_2 = \frac{2^{n+1}-1}{2^n} V_1$.

It is sufficient to take three flying capacitors to create 15 different conversion ratios. If the SCC is of 1st order, the duty cycle can be tweaked to achieve only minor losses, in order to achieve a full conversion range. This results in a *saw tooth* efficiency trace, as seen in Fig. 1.9, giving a relatively constant efficiency.

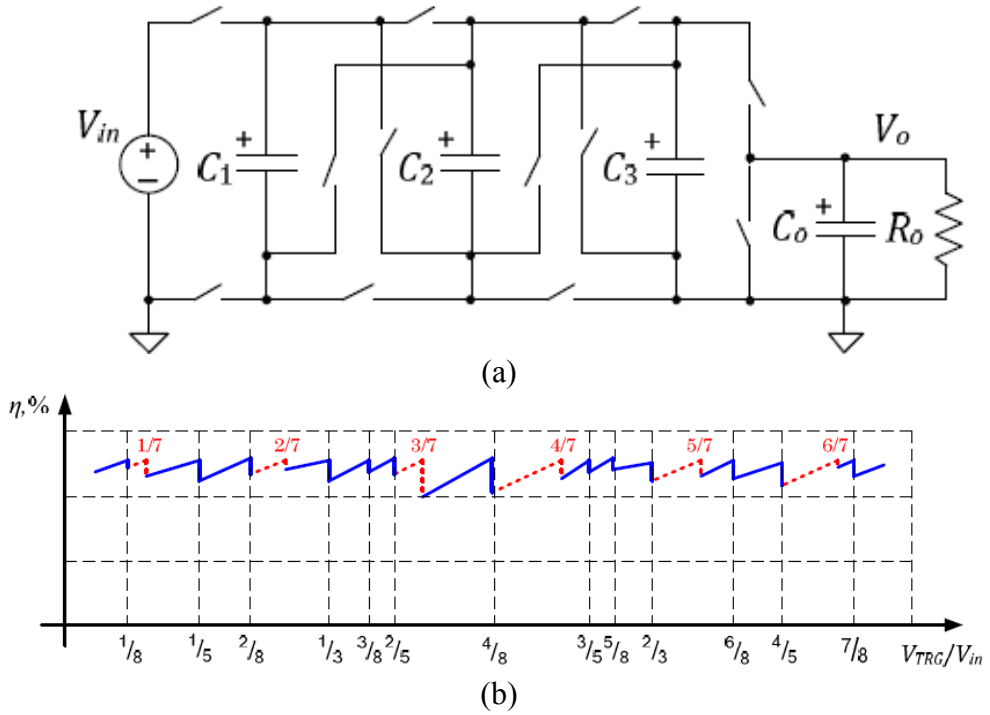


Fig. 1.9 The EXB/Fibonacci converter: (a) topology, (b) typical efficiency graph showing multiple peaks for different conversion ratios. [10]

The down side of this converter is the low achievable nominal efficiency. The number of transistors that are needed is large: all transistors must be four-quadrant, demanding a total of 8 MOSFETs per flying capacitor. Furthermore, current flows through a large and varying amount of the transistors at each state, making it hard and expensive to lower the equivalent series resistance.

1.5.2. A resonant switched capacitor converter for voltage balancing of series-connected capacitors [11]

The work in [11] describes a topology that is a hybrid between SCCs and SICs. The work is designed for series cell-balancing, transferring energy between one cell and its neighbor. The cells can be a series of batteries or capacitors holding up a DC bus, or photovoltaic elements in a solar array. In the proposed configuration shown in Fig. 1.10, a flying capacitor is switched between the two adjacent cells, but instead of charging and discharging in a 1st or 2nd order manner, the energy is transferred in a relatively constant current by a series inductor that is pre-charged to the desired current.

This pre-charging can occur due to the available option of feeding the L-C tank with the voltage of the two cells together, or shorting it to itself. Assuming that the flying capacitor is large enough to maintain a relatively constant value roughly equal to the voltage of one cell, connecting the tank to the cells in series creates a positive voltage on the inductor, charging it

in one direction. Shorting the tank reverses the voltage on the inductor, forcing current to flow the other way. Once the tank is connected only to one cell, the voltage over the inductor is relatively small, leaving the current constant for a considerable amount of time.

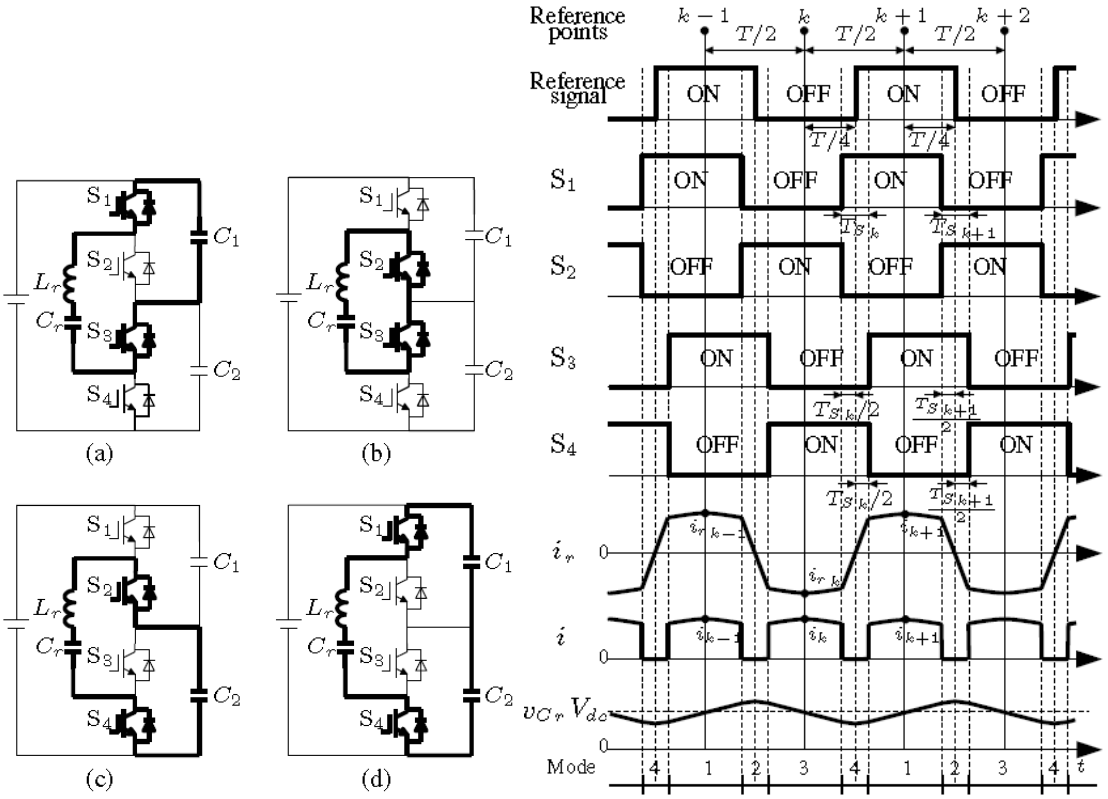


Fig. 1.10 The circuit proposed by Sano *et al.* On the left are the switching modes for the configurations: (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4. On the right are the traces for the switching used switcing sequences.

This mode of operation becomes problematic once the voltage difference between cells becomes noticeable. This creates a voltage drop on the inductor, causing a rapid decrease in current. This means that the time of current inversion (Fig. 1.10 b and d), where no energy is transferred, becomes dominant, raising the overall rms current and decreasing the efficiency. In addition, soft switching does not occur in all stages

1.5.3. Analysis of a step down resonant switched capacitor converter with a sneak circuit state [12]

In [12], a 2:1 step down RSCC was examined, implemented as shown in Fig. 1.11. The study revealed a phenomenon that occurs when using two-quadrant MOSFETS and diodes while switching above or below resonance. Results show that unmatched frequency leads to undesired current circulation paths named *sneak circuits*. When switching above resonance, V_2/V_1 stays relatively constant for a given load, R_L, but if R_L is small enough and f_s is lower

than resonance, the result will be a dramatic decline in V_2/V_1 (originally defined in [12] as V_O/V_I), as can be seen in Fig. 1.12. Reading the study with an efficiency oriented view, one might intuitively assume that the efficiency declines linearly with the drop in V_2, but simulations suggest otherwise (Fig. 1.13). In fact the circulating currents manage to recycle some excess charge, resulting in lower output currents than expected. The direct result is $\eta = P_2 / P_1 > 2V_2 / V_1$, meaning that the rigid relationship between the input and output voltages and the efficiency does not hold, resulting in better-than-expected efficiencies.

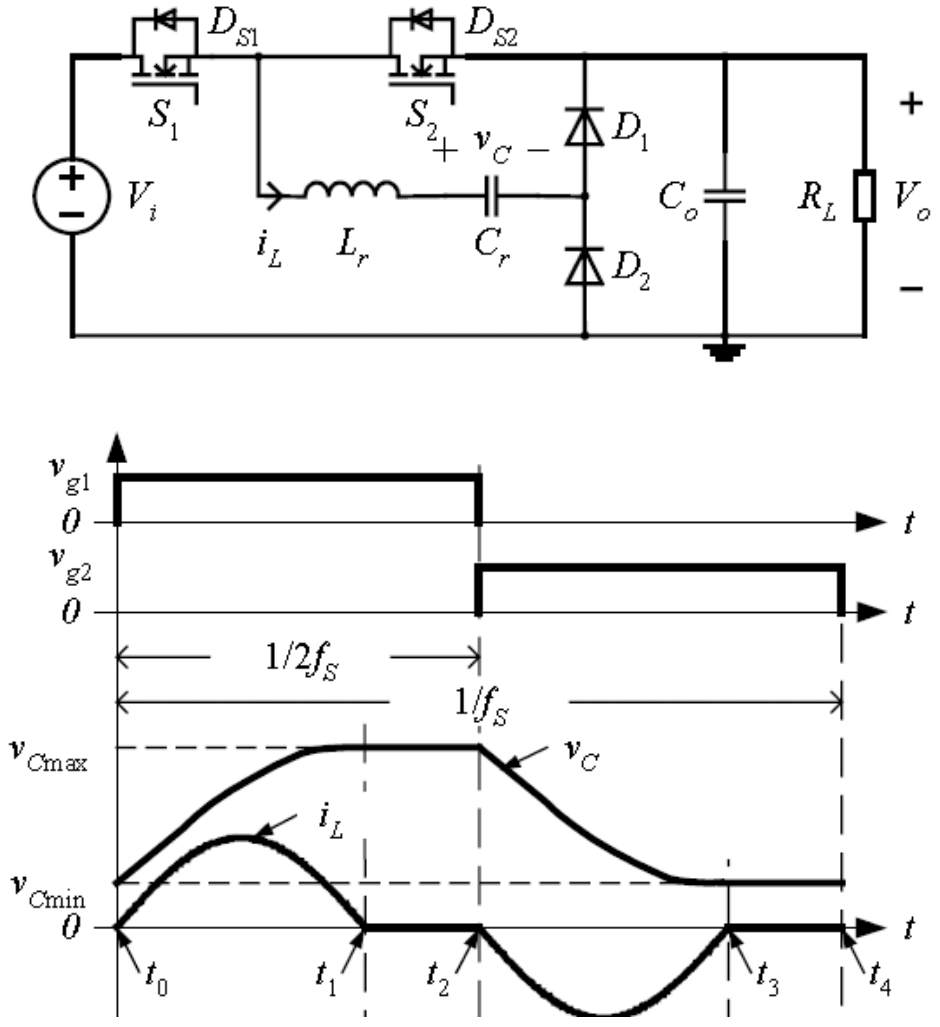


Fig. 1.11 The examined RSCC and traces for the tank given in the paper.

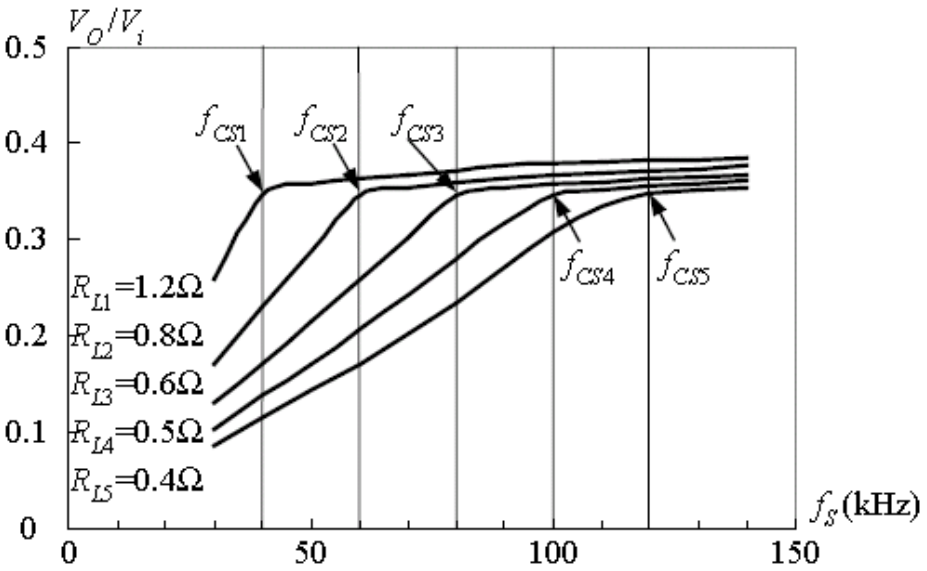


Fig. 1.12 V_o/V_{in} as a function of f, for dfferent values of R_L

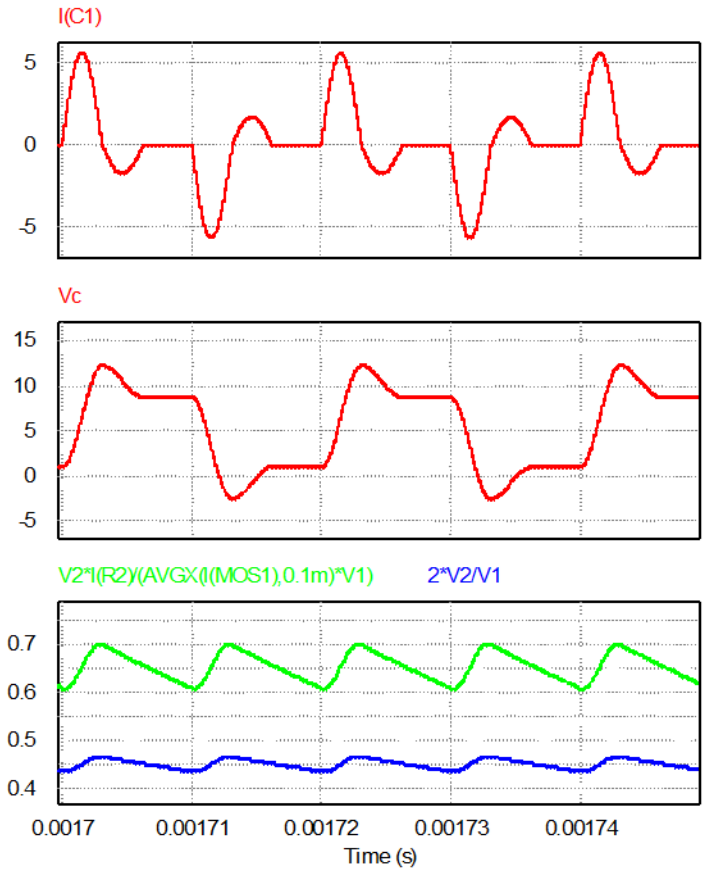


Fig. 1.13 Circuit traces showing a case of $\eta > V_o/V_{in}$. The bottom graph shows the actual efficiency (upper trace) above the V_o/V_{in} (lower trace) conducted in PSIM (powersim inc.).

The work described in this section is not yet complete, and only illuminates a phenomenon that has not yet received thorough analysis.

1.5.4. Unified analysis of switched resonator converters [13]

The study in [13] proposes a family of switched capacitor converters, focusing mainly on the topology of a step down converter. The whole family manages to detach the correlation between the output voltage and the efficiency, with the theoretical efficiency being 100% for all conversions for all output voltages in the conversion range. The proposed topology consists of a standard 1:1 RSCC with an added diode connected antiparallel to the flying capacitor, as seen in Fig. 1.14. In this manner, if $V_2 < V_1$, once the capacitor discharges upon reaching V_2 it reaches 0V before the current reaches zero. In this case, the antiparallel diode opens and lets the inductor discharge any residual energy it maintains. This creates a split discharge profile starting with a resonant shape and ending linearly (Fig. 1.14). The resonant tank meets V_1 empty of any charge, regardless of any occurrence at the output. This means that as long as a whole switching sequence (charge and full discharge or DCM) occurs, the power output will be constant and R_L will dictate the output voltage and current. In this operation mode, power and hence current or voltage regulation can be achieved by applying PDM.

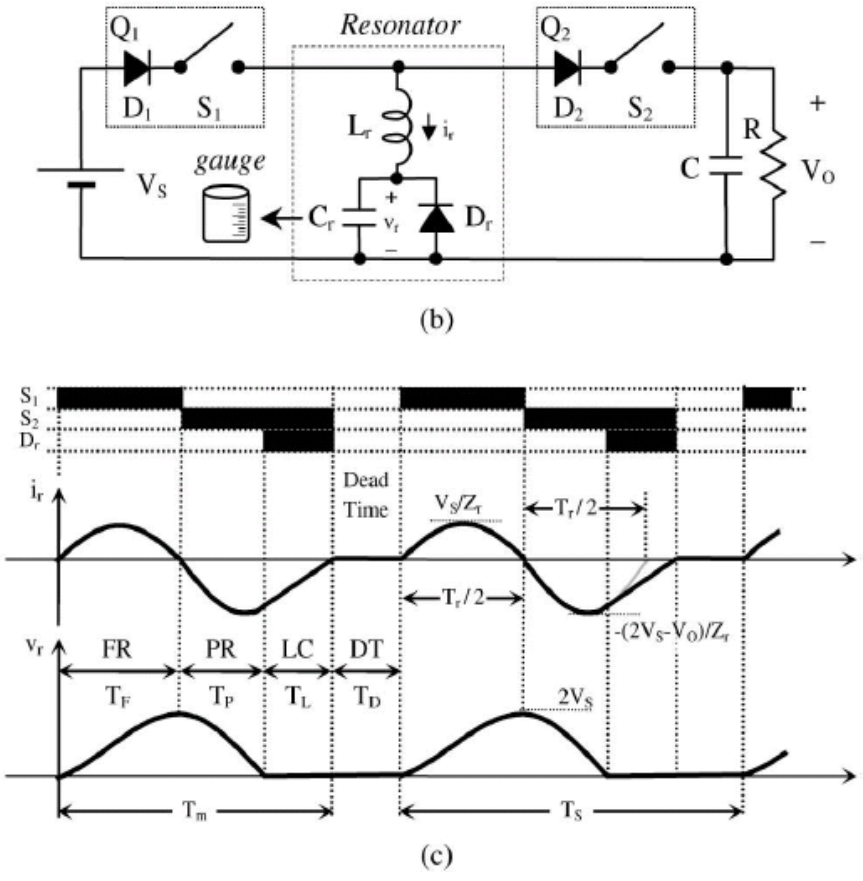


Fig. 1.14 The examined resonator topology and traces.

In [13] many derivatives were presented for the proposed configuration. A drawback of the topology is small conversion ratios (close to 1:1), and conversion ratios above 1:1. As the output voltage gets closer to the input voltage, the linear discharge through the diode takes longer, limiting the frequency and the average current that can be transferred

1.6. Gyrator

This work implements a theoretical network element that is not commonly seen or used, called a gyrator. This element is the inverse of the well-known transformer network element. Instead of in/out voltage dependence, the network transposes the current and voltage; a voltage source applied on one side is reflected as a current source on the other, and vice versa. The theoretical element has a *gyration* coefficient that dictates the I-V relationship such that input and output power is equal, making the network element storage-less and non-dissipative. Fig. 1.15 shows the symbol of the element as proposed by *Tellegen* in 1948 [14] and the gyration relationship is described by the following equation:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} . \tag{1.7}$$

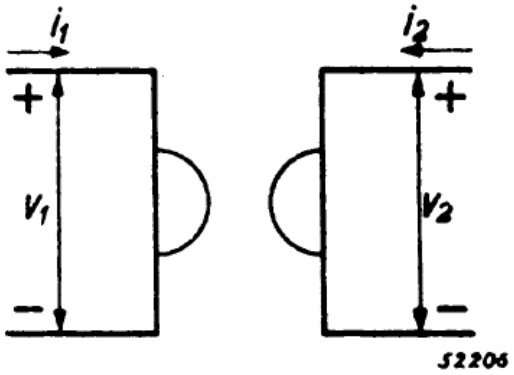


Fig. 1.15 Tellegen's proposed symbol for the ideal gyrator [14]

Simple multiplication of the two rows above shows that the power is maintained between the two network ports. The gyrator element is used in communication systems, where low power signals are needed. One use of the gyrator is to reflect reactive elements as their dual, i.e. capacitor to inductor and vice versa. This element is not commonly used in the field of power electronics.

In [15] a gyrator network was first proposed using switch mode converters. The implementation consisted of a standard switched converter, such as Buck, boost, etc., and a control loop. The converter was designed to transpose between voltage and current using the output or input current as a sensing signal for control (Fig. 1.16).

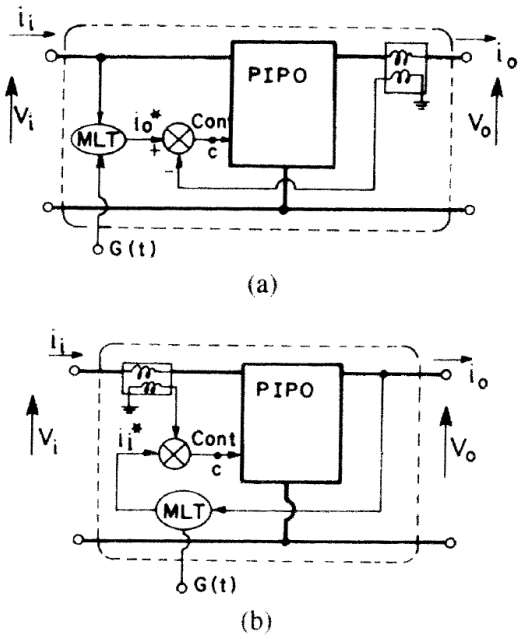


Fig. 1.16 A schematic represetation of the control of a converter (PIPO means input and output power are equal): (a) with current sensing, (b) with voltage sensing.

In [16], a switch mode converter with natural gyrator behavior was introduced. It was implemented using an inverse dual bridge converter, using an AC bus capacitor and two inductors, one on each side, to maintain the DC. This created gyrator behavior with the gyration coefficient depending on the phase between the input and output bridges. The same concept was further developed [17] using a single inductor with no capacitor, and featured a power factor correction realization for the converter to be able to serve in commercialized SMPS. The gyration equation for this case is:

$$g = \frac{\varphi}{2\pi f_s L}\left(1-\frac{\varphi}{\pi}\right), \tag{1.8}$$

where φ is the phase delay between the synchronous operation of the two full bridges at frequency f_s, and L is the inductance. Fig. 1.17 shows the realization for [17], along with the traces showing achievable gyration ratios.

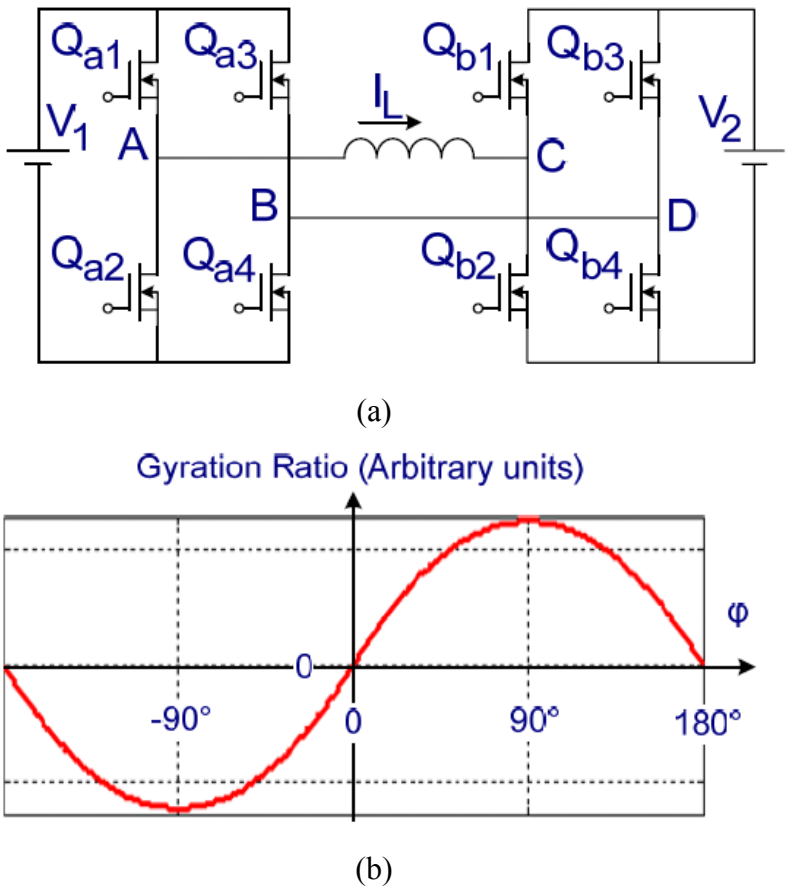


Fig. 1.17 The double bridge gyrator SIC. (a) Topology (b) gyration ratio as a function of φ.

1.7.Motivation, objectives and significance of the research program

These days, DC-DC conversion is dominated by switched inductor converters. Switched capacitor converters have advantages, but as mentioned in the introduction, suffer from bonding between the efficiency and the conversion ratio, which usually leaves them out of the game. Recent studies managed to break the knot, but the results were limited. The main objective of this research is to create *a switched capacitor converter that has features similar to switched inductor converters*, having the advantages of both.

The research includes:

- Full behavioral theorem
- Analysis of the concept for work in open and closed loop
- Development of control algorithms
- Efficiency calculations
- Application examples and design guidelines

The results of this research can directly contribute to the research and development of converters, regulators and integrated power supplies based on switched capacitor technology, having the potential of IC integration at small scales. The study provides tools and theory to further develop this technology.

2. A High Efficiency Resonant Switched Capacitor Converter with a Continuous Conversion Ratio

This chapter presents the theoretical considerations and lays the foundations for the development of the gyrator-RSCC family. A step-by-step overview of the mechanism is first presented, followed by a mathematical analysis for the static model and efficiency modeling with experimental verification. Derivatives of the topology are also presented and discussed.

2.1. Step-by-step overview

The topology in its generic form, as described in Fig. 2.1, requires four-quadrant (bi-directional) switches (Q_1, Q_2 and Q_3) that operate in synchronous/complementary action. This is required to support bi-directional and non-inverting step up/down operations in a single configuration. However, for more specific cases, such as unidirectional power flow and/or specific conversion types (up or down), the number of switches and the configuration complexity can be significantly reduced. A detailed discussion of the topology derivatives is provided in section 2.7

The operation of the converter shown in Fig. 2.1 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 2.2 that illustrates the capacitor voltage, V_C, and the resonant tank current, I_C, for the case of a non-unity step up conversion. By turning Q_1 on, a charge state (S1) is commenced, which resonantly charges the flying capacitor from the input V_1. At zero current, Q_1 is turned off and Q_2 is turned on (state S2). At this point, the flying capacitor resonantly discharges onto the output capacitor. Since the input voltage, V_1, and the output voltage, V_2, are of different values, only a portion of the charge is delivered to the output and results in V_C that is different to its voltage at the starting point of S1. The amount of this voltage difference (neglecting parasitics) equals to twice the residual voltage of the flying capacitor. By turning Q_3 on (S3), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.

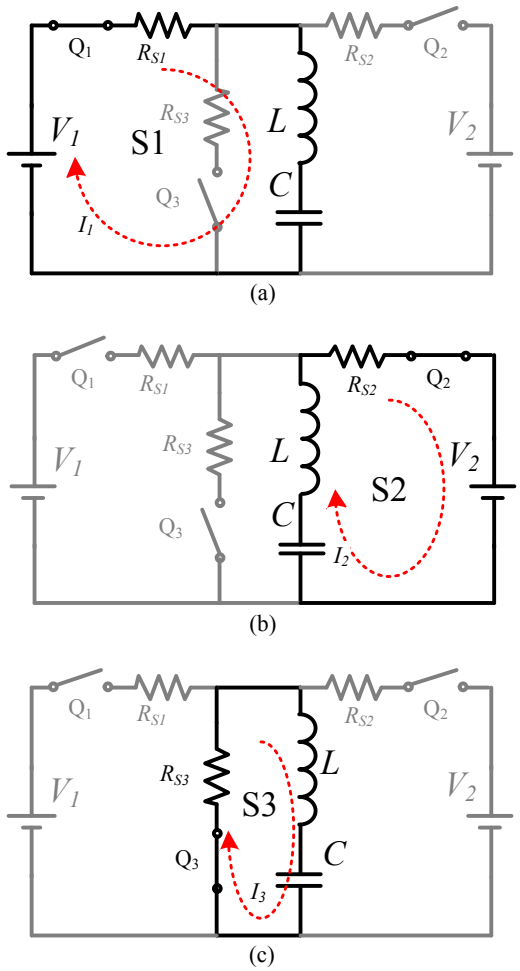


Fig. 2.1 The proposed resonant switched capacitor converter configuration and operation principle: (a) *charge,* (b) *discharge,* (c) *balance* states.

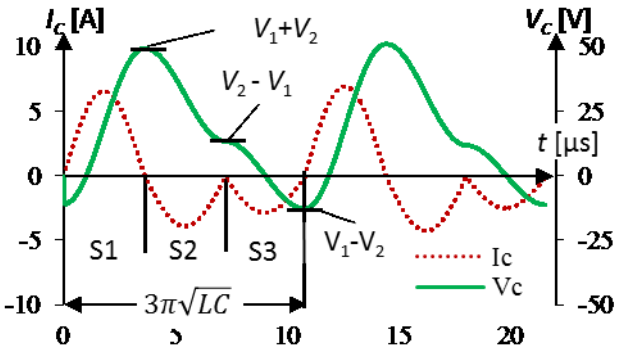


Fig. 2.2 Typical waveforms (obtained from simulation) of the flying capacitor voltage and current. Circuit parameters are: V_{in}=20V, V_o=31V, R_s=0.15Ω, L=5.2μH, C=0.25μF.

As described in section 1.2.2, if the 3rd balancing state does not occur, residual charge changes the overall current until the output voltage is stabilized in relation to the input. As will be explained in detail in the next section, the addition of a third, charge-balancing state to the switching sequence transforms the resonant SCC into a voltage dependent current

sourcing converter that, neglecting losses, is capable of accommodating any input to output voltage gain (below and above unity). It should be noted that under steady-state conditions, the order of the charge/discharge/balance sequence does not affect the operation of the converter for either step up or step down conversion. The order of the sequence will govern the power flow direction, i.e. from V_1 to V_2 or from V_2 to V_1. To deliver power from V_1 to V_2 the sequence will be (S1, S2, S3). That is, *charge* from V_1, *discharge* on V_2 and *reverse* the flying capacitor polarity. In the case of power to be delivered from V_2 to V_1 the sequence will be changed to (S1, S3, S2). The duration of each switching state is half the resonant period and hence the switches are turned on and off at ZCS. Voltage regulation may be applied by introducing a time delay between switching states, applying a delay between consecutive sequences, i.e. Pulse Density Modulation (PDM), or by creating packets using on-off burst mode control [13], [18]. The resistors R_S in Fig. 2.1 represent the parasitic resistances in each loop and are assumed to be negligibly small in the analysis for the current and voltage conversion ratios.

2.2.Static model

In each switching state the *LC* tank connects to a voltage potential of either V_1 or V_2 or 0. Assuming a high quality factor ($Q \gg 1$) of the resonant tank, the resonant current, I_C , and the flying capacitor voltage, V_C , are approximately sinusoidal, hence:

$$\begin{aligned} V_c(t) &\approx V_i - \left(V_i - V_c(0)\right)\cos\left(\frac{t}{\sqrt{LC}}\right) \quad \text{(a)} \\ I_C(t) &\approx \frac{V_i - V_c(0)}{\sqrt{L/C}}\sin\left(\frac{t}{\sqrt{LC}}\right) \quad \text{(b)} \end{aligned}, \tag{2.1}$$

where C is the value of the flying capacitor, and L is the series inductance. $t = 0$ represents the start of each switching state and V_i represents the DC voltage, either V_1 or V_2, or 0V.

Following the principle of operation described earlier, assuming steady-state operation with transition between switching states at zero current, and by using (2.1)(a), an equation set can be formed (2.2) for the voltages at the end of the charge, discharge and balance states:

$$\begin{cases} V_{C,1} \approx V_1 + \left(V_1 - V_{C,3}\right) = 2V_1 - V_{C,3} \\ V_{C,2} \approx V_2 + \left(V_2 - V_{C,1}\right) = 2V_2 - V_{C,1} \\ V_{C,3} \approx 0 + \left(0 - V_{C,2}\right) = -V_{C,2} \end{cases}, \tag{2.2}$$

where $V_{C,1}$ to $V_{C,3}$ represent V_C at the end of stages S1 to S3, respectively. After some manipulation, (2.2) can be rewritten as:

$$\begin{cases} V_{C,1} = V_1 + V_2 \\ V_{C,2} = V_2 - V_1 \\ V_{C,3} = V_1 - V_2 \end{cases} . \tag{2.3}$$

Substituting (2.1)(b) into (2.3) yields the states' peak resonant currents ($I_{pk,S1}$, $I_{pk,S2}$, $I_{pk,S3}$):

$$\begin{cases} I_{pk,S1} = V_2 / Z \\ I_{pk,S2} = V_1 / Z \\ I_{pk,S3} = (V_1 - V_2) / Z \end{cases} , \quad Z = \sqrt{\frac{L}{C}} . \tag{2.4}$$

Assuming identical resonant characteristics for all states, that is, a 1/3 of the operation cycle for each state, the average input and output currents (I_1, I_2) can be obtained and a gyrator relationship between the currents (I_1, I_2) and voltages (V_1, V_2) is formed as follows:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 0 & g^{-1} \\ g & 0 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} , \quad g = g_n = \frac{2}{3\pi Z} , \tag{2.5}$$

where g is the effective gyration gain and g_n is defined as the natural gyration gain.

It is understood from (2.5) that for a synchronously run converter, the dependence of the average terminal currents (I_1, I_2) on the average terminal voltages (V_1, V_2) follows a gyrator relationship [19], [20] with a natural gyration gain of g_n. This expression is generic and holds for the case of power flow from V_1 to V_2 as well as for power flow from V_2 to V_1. However, as mentioned earlier, the direction of power flow is governed by the switching stage sequence and reverses for the case of (S2, S1, S3). It should be further noted that due to the gyration action, the converter behaves as a voltage-dependent current source and there is virtually no restriction on the relative magnitudes of V_1 and V_2. That is, V_2 can be equal to, less than, or greater than V_1.

For the case where one of the terminals is loaded by a resistive load, R_L, in parallel with a filter capacitor, C_L, the resonant SCC operates as a current sourcing DC-DC converter and the magnitude of the output voltage, V_2 , depends on the load resistor as would be expected from a gyrator circuit:

$$V_2 = gR_L V_1 \ . \tag{2.6}$$

The voltage gain, A, will be:

$$A = \frac{V_2}{V_1} = gR_L \ . \tag{2.7}$$

The natural operating frequency, f_n, is composed of three half-resonant sections that are assumed identical. Therefore, f_n can be expressed as:

$$f_n = \frac{1}{3\pi\sqrt{LC}} \ . \tag{2.8}$$

2.3. Regulation

The basic operation mechanism that follows a charge, discharge and balance sequence creates a rigid gyration relationship as in (2.5). In the case where voltage regulation is desired, g should be controlled. By introducing a time delay between cycles, that is, effectively changing the operating frequency, g is made controllable and the gyration ratio, g, and operating frequency can be re-defined as:

$$\begin{aligned} g &= Gg_n = \frac{2G}{3\pi Z} \quad \text{(a)} \\ f_s &= Gf_n = \frac{G}{3\pi\sqrt{LC}} \quad \text{(b)} \end{aligned} \ , \tag{2.9}$$

in which $G \in (0,1]$ is defined as the regulation factor. In this mode of operation, the output current will be determined by the input voltage and g.

2.4. Losses and efficiency

Assuming ZCS, losses of the converter are primarily due to resistive elements in the conduction paths of each sub-circuit. For a full operation cycle at frequency f_s, the current of

each sub-circuit is composed of one sinusoidal pulse (with a peak value as found in(2.4)) followed by zero current for the time duration of the delay plus the conduction time of the other two states. Assuming that the output current is constant and neglecting the voltage ripple, the relationship between the rms currents and the average output current, I_2, will be:

$$\begin{cases} I_{rms,S1} = \sqrt{\dfrac{G}{6}}\dfrac{R_L}{Z} I_2 \\ I_{rms,S2} = \dfrac{3\pi}{2}\dfrac{1}{\sqrt{6G}} I_2 \\ I_{rms,S3} = \left| \dfrac{3\pi}{2}\dfrac{1}{\sqrt{6G}} - \sqrt{\dfrac{G}{6}}\dfrac{R_L}{Z} \right| I_2 \end{cases} . \tag{2.10}$$

The total power dissipation can be calculated by summation of the losses of the three sub-circuits. Given an identical parasitic resistance, R_s, for the three sub-circuits, the total dissipated power, P_{loss} , can be expressed as:

$$P_{loss} = I_2^2 \left(\frac{3\pi^2}{4G} + \frac{R_L^2 G}{3Z^2} - \frac{\pi R_L}{2Z} \right) R_S . \tag{2.11}$$

By substituting (2.5), (2.7) and (2.9)(a) into (2.11) and after some manipulations, the equivalent resistance of the converter, R_e [21], [22] as a function of the load, voltage ratio and the circuit parameters is found to be:

$$R_e = R_L \frac{\pi}{2}\frac{R_s}{Z}\left(A + A^{-1} - 1 \right). \tag{2.12}$$

The efficiency of the converter, η, can now be estimated by:

$$\eta = \frac{R_L}{R_L + R_e} = \frac{1}{1 + \dfrac{\pi R_s}{2Z}(A + A^{-1} - 1)} . \tag{2.13}$$

Fig. 2.3 shows typical curves that were obtained from (2.13) for the expected efficiency as a function of A, for various ratios of $Q = Z/R_s$. As can be observed, maximum efficiency is obtained at unity gain (A = 1), and it is a function of the ratio between the resistance and the resonant network characteristics. In Fig. 2.3, Z was considered to be constant since it is determined by the natural gyration gain g_n. Expression (2.13) also implies that the efficiency

is independent of G, resulting in a constant efficiency in the voltage regulation mode, when the current is controlled.

Equation (2.13) and Fig. 2.3 provide an insight into the operation of the proposed converter and contributing factors of the converter's efficiency. Ideally, assuming negligibly small parasitic resistances, the efficiency of the converter would be *100% for any finite conversion ratio*. A unique feature hitherto only found in switched-inductor converters, is now made available to resonant SCCs as well.

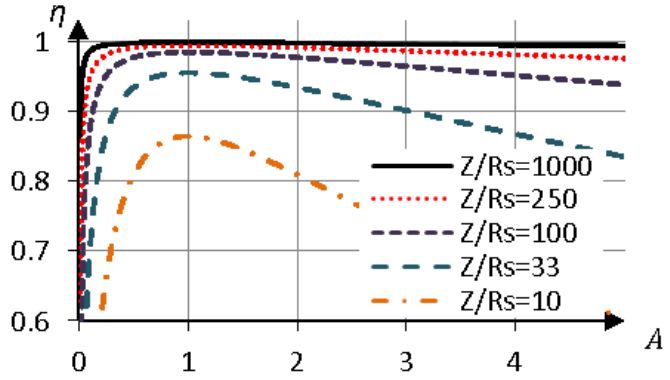


Fig. 2.3 Theoretical efficiency curves as a function of the voltage gain, A, with normalized loop resistance as a parameter.

2.5. Output ripple

Considering the above analysis, the operation of the converter presented in this work resembles the discontinuous-mode Pulsed Frequency Modulation (PFM) operation of conventional switch-mode converters, which are predominantly found as voltage regulators. In this context, estimation of the output voltage ripple is essential for sizing considerations of the output filter. By following the same design rules applied to switch-mode regulators [23], [24], that is, assuming constant output current, the current of the output capacitor (C_L) is similar in shape to the current of the discharge state, but without the average DC offset.

A generic waveform of the output capacitor current is shown in Fig. 2.4. By approximating the negative part of the current shape, the per-cycle charge transfer, ΔQ_{C_L}, can be expressed as:

$$\Delta Q_{C_L} \approx I_2 \left(\frac{1}{f_s} - \frac{1}{3 f_n} \right) . \tag{2.14}$$

Substituting (2.6), (2.7) and (2.9) into (2.14) yields the expression for the normalized output ripple:

$$\frac{\Delta V_2}{V_2}=\frac{1}{A}\frac{C}{C_L}\left(1-\frac{G}{3}\right), \tag{2.15}$$

where ΔV_2 is the amplitude of the output AC ripple. The output ripple, as obtained by (16), is inverse linearly dependent on C_L and A. Furthermore, when voltage regulation is employed by varying G, the ripple is expected to deviate by about 30% for the entire operation range of $G \in (0,1]$.

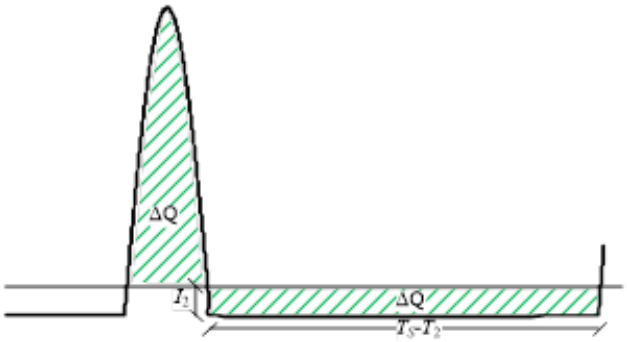


Fig. 2.4 I_{C_L} – the current on the output capacitor, C_L, for one cycle. The confined area is of same size above and below zero, and represents the charge procesed by C_L in each cycle.

2.6. Zero order dynamic behavior

An advantageous feature that the switched capacitor-based gyrator has is zero order response time to transients. This occurs naturally since charge to the output is delivered in portions, in which the portions' rate determines the current. When any transient occurs, the frequency can be immediately updated to compensate and adjust to the changes. This is similar to SICs operating in PFM. This differs from CCM SICs, which act as low pass filters. The current in the inductor has to adjust to the new desired levels, an action that takes several cycles to complete. In the discussed converter, any transients occurring at a frequency lower than the maximal GRSCC switching frequency, f_n, can be followed and compensated for in a zero order. A simulation was conducted with a load that was added in mid operation giving a transient in the current consumption from 10% to 90% of the maximal output current capabilities. Fig. 2.5 shows that the average output current, after being filtered by the output

capacitor, C_L, is the average of the SCC's output pulses. Changes in the load result in changes in the average current. Adjusting the pulse rate accordingly prevents any changes in the output voltage. In a similar manner, changes in the input voltage change the size of the pulses. In this case, changing the pulse rate prevents any changes in the output voltage or average currents.

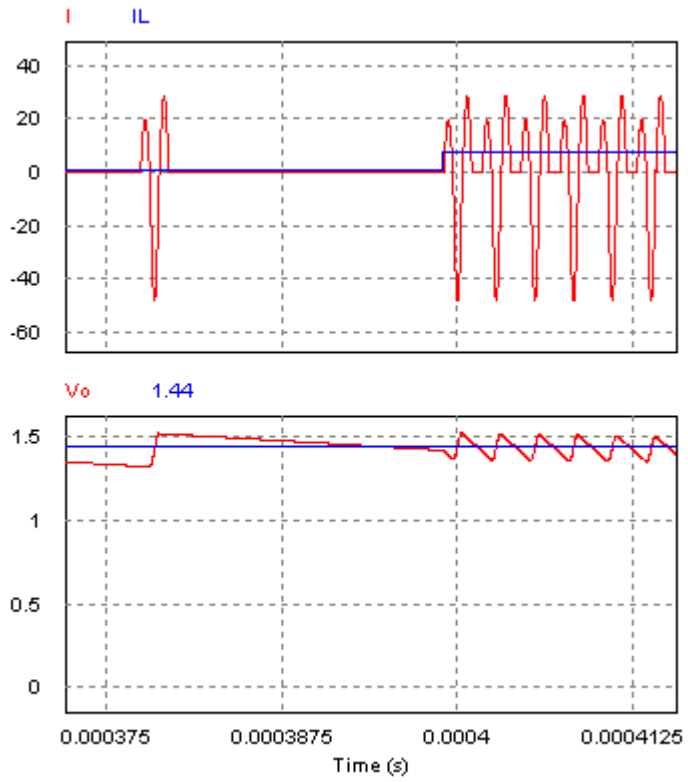


Fig. 2.5 A simulation showing the output current before and after C_L during a step transient in the output load.

Another simulation was conducted to show the zero order response time. In this case a triggering algorithm was implemented in a C block in a simulation of a GRSCC in PSIM. The triggering block was fed with a signal corresponding to the desired frequency. An AC signal was added, creating Frequency Modulation (FM) at 90kHz ± 20kHz. The AC signal frequency (FM) was swept and the output current was measured in relation to the input. Fig. 2.6 shows no zeroes or poles until fairly close to the switching frequency, confirming that the converter's response is of zero order. Irregularities seen at high frequencies are assumed to result from the calculation method of the simulator, which only takes into account the end result of each run, prone to be affected by the ripple.

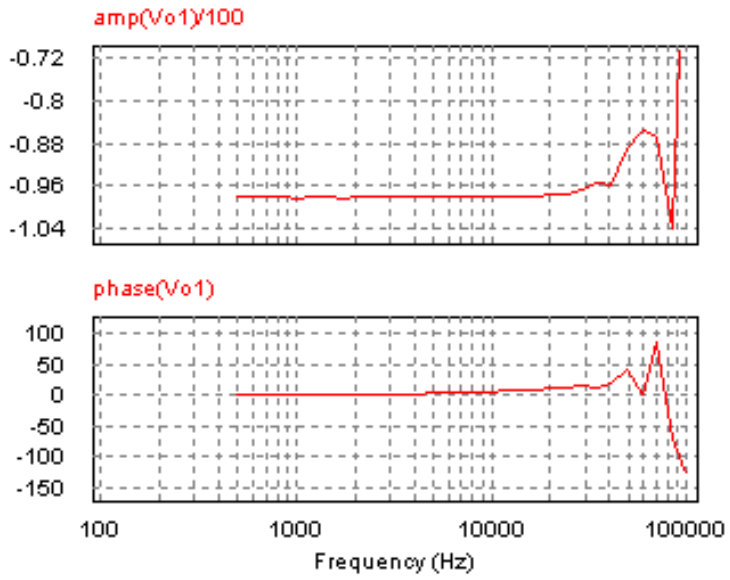


Fig. 2.6 Frequency modulation sweep. Top chart represents the amplitude, with the vertical axis related to simulation conditions. Bottom chart shows the phase.

2.7. Topology derivatives

The converter of Fig. 2.1 may be extended to operate in naturally doubling and dividing configurations, i.e. shifting the peak efficiency points to $A = 2$ or $A = 0.5$, respectively. Fig. 2.7 shows a general topology that is capable of operating bi-directionally at all gains, with the capability of shifting the peak efficiency points. TABLE I. summarizes the possible switch realizations for 7 different unidirectional conversion modes, describing which switches can be either bypassed (S-Shorted), disconnected (O-Open) or replaced by a diode (D). Another attractive option that has voltage inversion properties may also be implemented as a bridge configuration (Fig. 2.8). Possible state-of-the-art applications for the bridge configuration can be as a balancer/equalizer of energy cells [11] or photovoltaic arrays [2]. It was found that for the bridge configuration, the four-quadrant switches can be replaced by conventional MOSFETs, while retaining the converter characteristics.

It should be noted that for configurations that are implemented with two-quadrant switches, such as the bridge assembly (Fig. 2.8), the insertion of a time delay between states for voltage regulation purposes has to be assigned to the proper state to avoid undesired circulating current. The delay should be located between states such that V_C is at the correct polarity to block the conduction of the MOSFET diodes. Taking the bridge configuration for example (Fig. 2.8), the proper sequence for this case would be: *discharge* (S2), *balance* (S3),

charge (S1), *delay*. It should be noted that, as analyzed above, the order in which the sequence is applied does not affect the characteristics of the converter.

TABLE I. SWITCH MAPPING FOR UNI-DIRECTIONAL DERIVATIVES[1]

Converter Function	Q_{1a}	Q_{1b}	Q_{2a}	Q_{2b}	Q_{3a}	Q_{3b}	Q_4
Step up/down[2]	1	D	2	2	3	O	S
Step up[2]	1	D	D	S	3	O	S
Step down[2]	1	D	D	2	D	O	S
Doubler step up/down	S	3	D	S	3	O	1
Doubler step down	S	D	D	S	3	O	1
Divider step up/down	1	S	S	2	O	3	2
Divider step down	1	S	S	2	O	D	2

1. Characters in the table represent the following: S – MOSFET is shorted, O – MOSFET is disconnected, D – only a diode is needed. Numbers represent the stages in which the MOSFETs are active

2. Dashed route is preferred, but not mandatory. Mapping was suggested correspondingly.

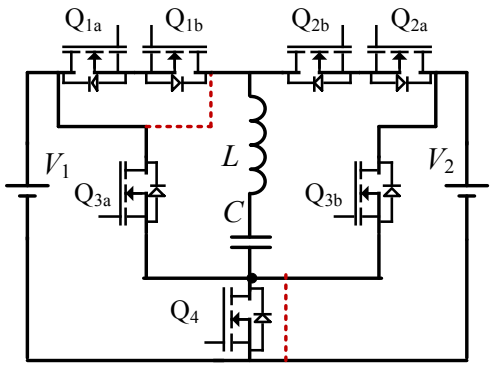


Fig. 2.7 A gyrator converter in a generalized configuration, with optimized efficiency at voltage gains of $A = \{2,1,0.5\}$. The dashed lines represent alternative routes optimized for a 1:1 configuration.

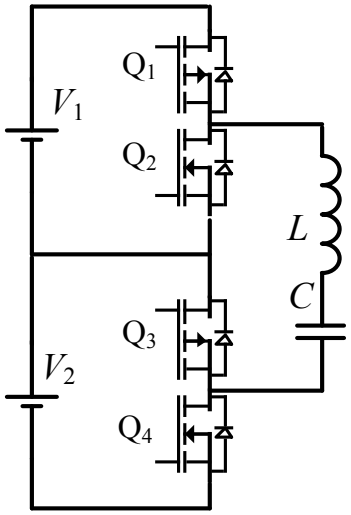


Fig. 2.8 A gyrator converter realized in a full bridge configuration (converter B), with optimized efficiency at voltage gain of A = -1.

2.8. Experimental work

To demonstrate the operation of the proposed converter and to verify the theoretical analysis, an experimental test-bench was constructed. A converter that follows the generic topology of Fig. 2.1 was realized and examined for the fundamental characteristics of the gyrator converter and for efficiency evaluation. TABLE II. summarizes the parameters of the experimental prototype.

In the experimental realization, the bidirectional switches were implemented by two power MOSFETs (IRFP3077) connected back to back. Floating switch drives were implemented by applying isolation transformers driven by a microcontroller (dsPIC30F2020 Microchip Inc.) [25]. The system was tested under open-loop conditions, while the switching frequency and states switching periods were manually adjusted to obtain ZCS. Waveforms showing resonant, step up and step down ZCS operation are given in Fig. 2.9. Validation of the converter's high efficiency along a continuous voltage conversion range is depicted in Fig. 2.10 and was carried out by varying the input voltage and the load resistance, while keeping the output power to be constant at around 10 W. As can be observed, the experimental results closely follow theoretical calculations as well as the results of cycle-by-cycle simulations. The efficiency was measured to be well above 90% for a wide operation range. The natural gyration ratio, g_n, of the converter as a function of voltage gain was evaluated by varying the input voltage, while the output voltage was kept constant. This was done by varying R_L as V_1 changes. Theoretical calculations, simulations and experimental results for this evaluation are

presented in Fig. 2.11. The deviation of experimental results from the theoretical analysis at lower conversion ratios is primarily due to the higher conduction losses and, consequently, lower efficiencies can be seen at these ratios as in Fig. 2.10. Another reason for the deviation is that the resonant characteristics of the three states were not identical and were not accounted for in the derivations of g_n. In particular, as can be observed from Fig. 2.9b, the discharge period (S2) is significantly longer than other states and will have a growing effect on g_n for smaller values of A (larger step down ratios). More experimental results are discussed in section 3.3.

TABLE II. PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value	Notes
C_f	262 nF	
ESR	8.4 mΩ	
L	5.3 µH	
R_S (Inductor)	110 mΩ	measured at 150 kHz
R_S (MOSFETs)	2x 3.3 mΩ	PMOS, NMOS
R_S (total)	130 mΩ	estimated total loop resistance
f_n	~100 kHz	
dead time	~180 ns	between states
V_{in} (max.)	55 V	
V_{out} (max.)	70 V	
P_{out} (max.)	200 W	

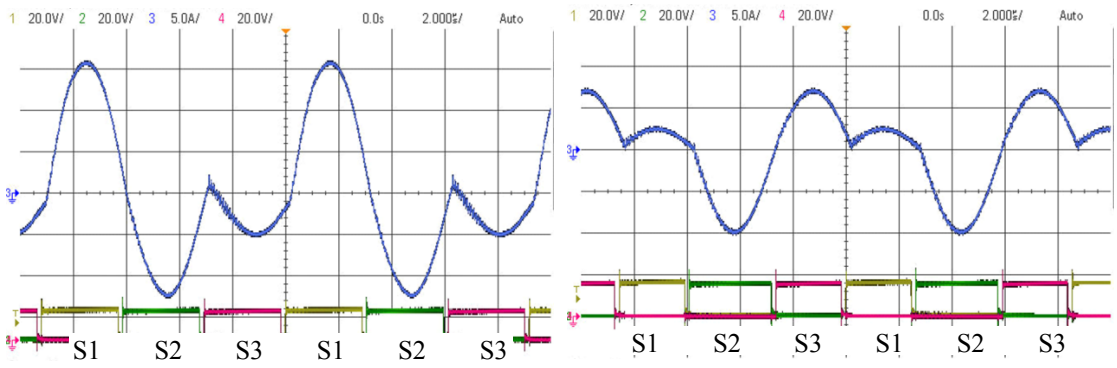


Fig. 2.9 Experimental waveforms: (a) in a step up operation mode, (b) in a step down operation mode. Upper trace – inductor current (5A/Div.), lower traces – S(1,2,3) gate signals. Horizontal scale 2µS/Div.

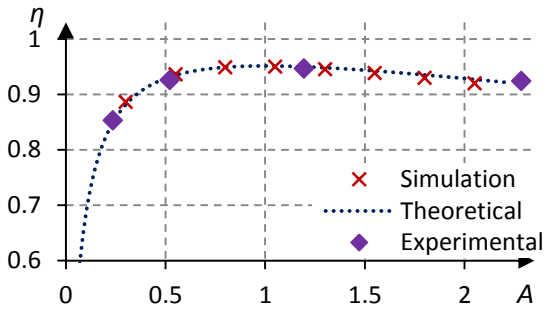


Fig. 2.10 Converter efficiency as a function of voltage gain A.

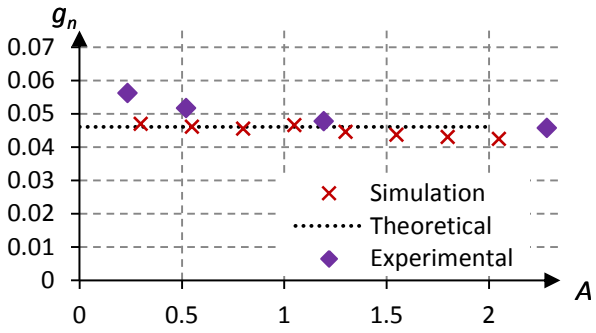


Fig. 2.11 Natural gyration ratio as a function of voltage gain A.

3. Application: Bridge (Inverting) Topology

One derivative of the theoretical gyrator that was thoroughly investigated during this research was an inverting Bridge topology, specifically designated for series energy cell balancing, i.e. transferring energy between one cell and a neighboring cell. These cells can be a series of batteries or capacitors holding up a DC bus, or photovoltaic elements in a solar array. For this, a complete and fully functional module was developed, utilizing the cells as the power source for the switching and controller activity. This configuration has the distinction of using a regular two-quadrant (reverse-conducting) MOSFET for the switching, and does not require any additional hardware to create the needed third charge inversion state, required for proper gyrator operation.

This section reports on the full development of the hardware for creating the gyrator converter, including the power stage and the peripherals, which include on-board power supplies, a microcontroller unit with sensing mechanisms and a unique driving mechanism that was developed to answer the demand for a low-cost, effective and reliable drive.

3.1. Power stage

The power stage along with state sub-circuit routes is depicted in Fig. 3.1. It consists of an L-C resonant tank that has the theoretical ability to be connected in parallel to the top cell (Q_1,Q_3), the bottom cell(Q_2,Q_4) or both cells in series(Q_1,Q_4), or to be shorted out (Q_2,Q_3). Alternating between the first two options results in a standard 1:1 RSCC, assuming frequency is synchronous with the tank's resonance. A similar implementation described in section 1.5.2 utilized all four options. In order to use the configuration as a gyrator the three first options should be used, as shown in Fig. 3.1.

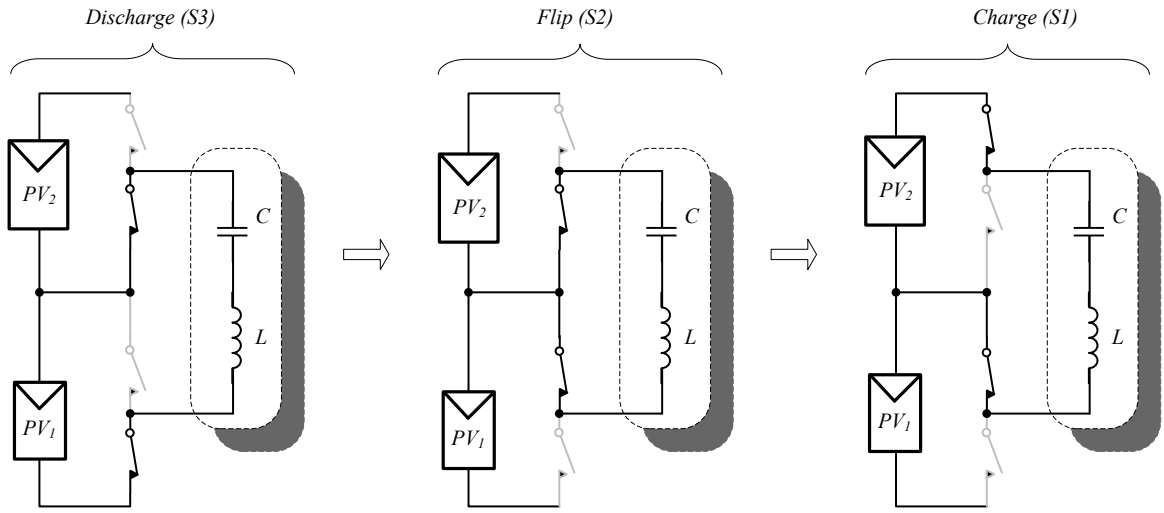


Fig. 3.1 The three stages of the gyrator bridge implementation

In order to have control over the amount of current that is passed between the two cells using the converter, the additional delay state is added. Although theoretically there is no significance regarding the location of the delay (in between which states it is added), in practice, when reverse conductive elements are used the delay should be added only after a state that ends with a positive charge on *C*. The only state that guarantees a positive charge on *C* is S1, the charging state. The sequence for delivering power from V_1 to V_2 will then be S2→S3→S1→*delay*, and for delivering power from V_2 to V_1 will be S1→S3→S2→*delay*. The resulting drive signals that are needed for driving the four switches are shown in Fig. 3.2.

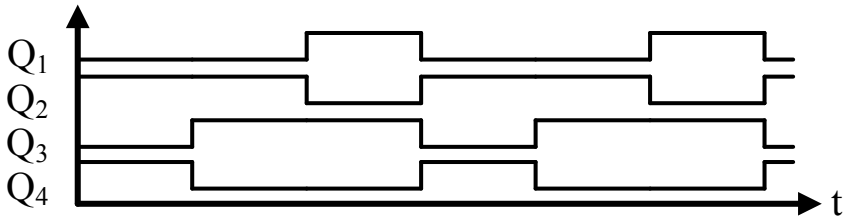


Fig. 3.2 The drive signals needed for the four switches (high means active)

3.2. Gate drive [3]

Driving gates of floating transistors in common power electronics systems, such as inductor-based converters and switched capacitor converters, requires designated driving systems. The driving circuitry needs to create proper isolation to overcome the voltage differences existing between the transistors' sources and the drivers' ground potential. A development of a simplistic solution was published in [3]. The paper investigates a method

that applies capacitive coupling to solve the problem of driving a MOSFET transistor which is not directly connected to the driver's ground. This method is applicable to cases in which the source of the floating transistor (N or P type) can be connected to some DC bus, as in the discussed bridge configuration. The constant potential difference between the ground-referred driver and the driven MOSFET's source can be decoupled using a series capacitor in between the driver and the gate. The DC voltage needed at the gate side for proper drive over the full duty cycle range is then recovered by using a diode to clamp the coupling capacitor to the DC bus voltage, thus maintaining $V_{gs} \geq 0$ for N-MOS or $V_{gs} \leq 0$ for P-MOS. As a result, during the 'on' period, the gate voltage, V_g, will be referred to the DC bus voltage, i.e. the source of the transistor.

Fig. 3.3 shows schematic diagrams of implementations for N- and P-type MOSFET switches. The two key elements are the series capacitor, C_s, and the diode, D, which initially charges the series capacitor to V_{BUS}. A second capacitor, C_{loop}, is added between the MOSFET's source and the driver's ground input, providing an alternative low impedance path, diverting the ground loop currents from the relatively high impedance bus source voltage (Fig. 3.3). Adding a series resistor, R_s , damps the drive circuit, preventing overshoots from further stray inductances that might exist even after choosing an appropriate C_{loop}. A bleeder resistor in parallel with the diode is necessary to allow C_s to follow changes in V_{BUS}. The tracking prevents the transistor from staying active during 'off' periods and, additionally, helps in preventing a potential gate-source breakdown. In [3], detailed analysis is given.

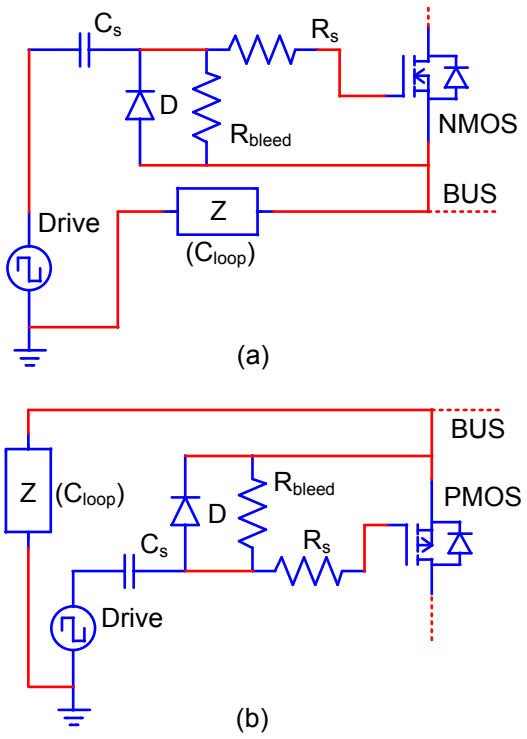


Fig. 3.3 A schematic diagram of the high-side driving system: (a) implemented for N-MOS, (b) implemented for P-MOS

3.2.1. Analysis and design considerations

The size of C_s is determined by the charge delivered to the gate in each cycle. This charge depends on the desired V_{gs} and on the voltage ripple allowed for C_s, as can be described by:

$$C_s \geq \frac{Q_{gate}}{\Delta V_{Cs}} \quad , \tag{3.1}$$

where ΔV_{Cs} represents the voltage ripple on C_s and Q_{gate} is the charge needed to raise the MOSFET's gate and is dependent on the operating voltage.

R_{bleed} can then be chosen, considering (3.2):

$$T_{transient} > R_{bleed} C_s \gg \quad , \tag{3.2}$$

where $T_{transient}$ is the expected circuit transient time and T_s is the switching time. This selection allows the capacitor to follow transients in V_{BUS}, but not to discharge during 'on' periods, when there is a drive signal. C_s should not be much larger than indicated in (3.1) to be able to track V_{BUS}, when needed, within the expected transient time. The value of R_{bleed}

must be sufficiently high to minimize energy dissipation. The selection of R_s is made such that its interference with proper charging of the gate is minimal. The drive circuit needs a harmonic quality factor value, Q, smaller than 0.5 to prevent overshoots. These factors can be expressed as:

$$\begin{cases} R_s << \dfrac{T_s V_{gs}}{2Q_g} \\ R_s > 2 \cdot \sqrt{\dfrac{L}{C_s}} \end{cases}, \tag{3.3}$$

where V_{gs} is the gate-source voltage during 'on' times and L is the stray inductance element in the drive circuit.

The value of C_{loop} needs to be sufficiently high so that ripple from the bus will not affect the drive ground. Considering a maximum allowed ripple of $\Delta V_{C_{loop}}$, the capacitor value can be chosen using the following expression:

$$C_{loop} \geq \frac{Q_{gate}}{\Delta V_{C_{loop}}} . \tag{3.4}$$

$\Delta V_{C_{loop}}$ should be significantly smaller than the drive signal level to minimize ground interferences. A good value would be $\Delta V_{C_{loop}} < 0.01 V_{gs}$.

Since the gate driver sources at turn on and sinks at turn off, an equal amount of charge (the charge on C_s) remains constant after each cycle. This implies that the diode is only needed in order to compensate for charges lost through R_{bleed} and for stabilization during transients in V_{BUS}. Yet, a fast diode with reverse recovery time considerably shorter than the period corresponding the desired switching frequency is still required in order to prevent the discharge of the capacitor during drive 'on' times.

If R_{bleed} is chosen to be high enough, the energy used to replenish charge lost due to R_{bleed} is negligibly small, meaning that no excess energy is consumed due to the addition of the proposed scheme. The switching power will then be:

$$P_{loss} = V_{supply} Q_g f , \tag{3.5}$$

where V_{supply} is the driver's supply voltage and is usually the same as the desired V_{gs}.

3.3. Experimental work

To demonstrate the operation of the developed converter and to verify the theoretical analysis, an experimental test-bench was constructed. A converter that follows the generic topology of Fig. 2.1 was realized and examined for the fundamental characteristics of the gyrator converter and for efficiency evaluation. TABLE III. summarizes the parameters of the experimental prototype.

TABLE III. PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value	Notes
C_f	1 μF	
ESR	1.2 mΩ	
L	500 nH	
R_S (MOSFETs)	13 & 7 mΩ	PMOS, NMOS
R_S (total)	48 mΩ	estimated total loop resistance
f_n	~130 kHz	
dead time	100 ns	between states
V_{in} (max.)	30 V	
V_{out} (max.)	30 V	
P_{out} (max.)	100 W	

The experimental prototype was built according to the methods and guidelines discussed above. A ZCS automatic calibration routine was implemented in the MCU, while the current amount (converter frequency) and direction were chosen manually, controlled by the MCU's debugger program. Test benchmarks were set for obtaining the converter's efficiency. One tested the converter's efficiency as a function of changes in input voltage, operating the converter in a voltage regulation mode. The second test measured efficiency as a function of load changes, namely, load regulation. Both experiments verify steady state operation and to not address transients. More experiments addressing transients that were conducted are described in chapter 4.

Fig. 3.4 shows the steady-state operation of the converter at f_s = 70kHz, V_{in} = 12V, V_{out} = 15V, P_{out} = 22W. As one can see from the current waveform (second trace from the bottom), the converter is operated in a PDM mode; the switching frequency (f_s) is different from f_n, i.e. time-delay is introduced to facilitate regulation.

In the first test, efficiency evaluation of the converter for a range of voltage gains was carried out by changing the input voltage. Manual frequency compensation was performed, changing G such that the output power and output voltage, 22W and 12V, respectively, were

kept constant (Fig. 3.5). The theoretically calculated characteristics were found to be in very good agreement with the experimental and simulation results.

The second test consisted of maintaining constant voltage gain, hence maintaining load regulation. Fig. 14 presents the efficiency of the converter as a function of the control parameter G for the case of A = 1.25. The theoretically predicted constant efficiency behavior is well validated by the simulation and experimental results over a wide operation range. Some mismatches at lower G-s can be explained by the fact that over longer periods (lower G), the output voltage ripple increases, as implied from (2.15). That is, larger voltage differences are present and hence higher peak (and rms) currents are required to sustain the output voltage at the desired value, ultimately reducing the system efficiency. Fig. 3.6 summarizes the experimental traces of converter efficiency for different power levels as a function of the control parameter, G, for several conversion ratios (different traces) and supports the claim that the efficiency of the converter developed is primarily affected by the conduction losses.

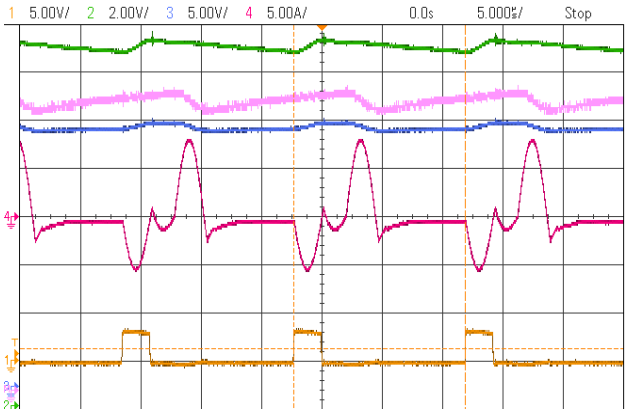


Fig. 3.4 Oscilloscope screenshot of a bridge gyrator converter working at 70kHz with V_o = 15V, A = 1.25, $P_o \approx$ 22W, η = 90%. Traces from top to bottom: V_2, V_1(math funct. 5V/div), (V_1+V_2), I_C, $Q_{4,Gate}$. The order of the states is S3-*discharge,* S1-*invert,* S2-*charge, delay*.

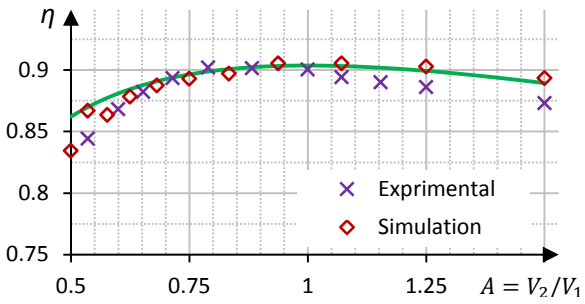


Fig. 3.5 Efficiency graph for the bridge gyrator as a function of the voltage gain.

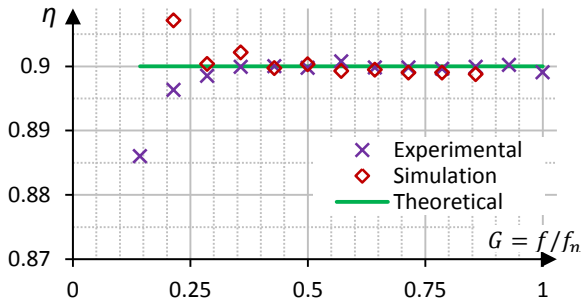


Fig. 3.6 Efficiency for the bridge gyrator as a function of the parameter G.

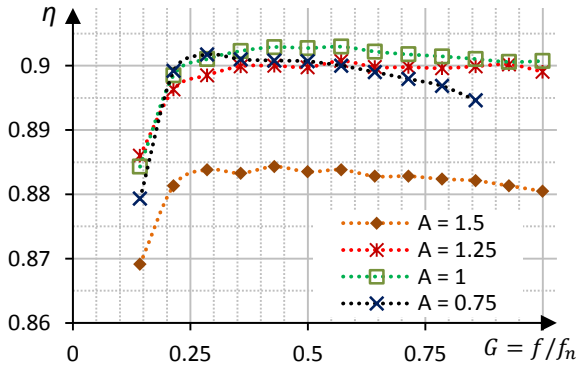


Fig. 3.7 Bridge gyrator efficiency as a function of parameter G, voltage gain is a parameter.

4. Resonant Switched Capacitor Voltage Regulator with Ideal Transient Response

Following the recent proliferation of portable electronics, there has been a sharp increase in interest and demand for more compact, light, energy efficient and economical power sources [26]. As this trend continues, the requirements become more and more challenging. Tighter output voltage regulation, faster response time to load and/or input voltage changes and lower volume are of major concern in the design of present-day SMPS and pose a bottleneck in the advancement of the technology.

State-of-the-art voltage regulators apply switched-inductor converters combined with advanced nonlinear controllers [27]-[34] to minimize size and maximize the power processing efficiency. The main limiting factor of this general concept is the presence of a relatively large inductor that prohibits, to a large extent, miniaturization and power on-chip integration.

Present-day switched capacitor technology has become an attractive alternative for volume-sensitive applications, featuring high efficiency and economical implementation [35], [36]. However, it lacks the capability of accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited. These limitations stem primarily from the fact that the efficiency of SCCs depends on the voltage gain [8], [22], [37], [38].

The RSCC presented in this study has demonstrated unique potential for voltage regulation over a wide range of conversion ratios and power levels, and can be used as the main building block of a voltage regulator.

The objective of this chapter is to introduce a small and efficient voltage regulator that is realized by the gyrator RSCC and a simple pulse density modulation control scheme (Fig. 4.1). The new voltage regulator exhibits an ideal response to load and line transients, i.e. *with zero over/undershoot over the full operation range*, as well as a constant efficiency profile over a wide range of voltage gain and power levels.

The main quality of the new RSCC presented in Fig. 4.1 is that it *disengages the efficiency of the system from the voltage gain*. As described in chapter 2, this is achieved by introducing

an additional switching phase to balance any charge mismatch between the input and the output and, as a result, a conventional SCC topology is transformed into a voltage-dependent current source i.e. a *gyrator* converter. Output voltage control is enabled by a comparator-based PDM, where the charge transfer rate to the output is controlled such that a desired voltage level is maintained. The new voltage regulator combines the virtues of both worlds: wide operation range with high efficiency (from switched-inductor converters) and reduced volume (from SCC).

4.1. Adaptation of the gyrator equations for regulator design

Voltage regulation is obtained by introducing a time-delay between switching states, applying a delay between consecutive sequences, i.e. PDM [39]-[42]. The relationship between the output current, I_2, and the input voltage, V_1, is given by:

$$I_2 = 2V_1 fC \ , \tag{4.1}$$

where f is the operation frequency of the switching sequence, including the added delay. The maximum output current is obtained for zero time-delay between cycles. In this case, the converter operates at the maximum frequency of three half-resonant cycles, that is:

$$f_{max} = 1/3\pi\sqrt{LC} \ . \tag{4.2}$$

For given resonant parameters L and C, the power conversion efficiency, η, can be written as a function of the series resistance, R_s, (seen in each state) and the overall voltage gain, A [1]:

$$\eta = \left(1 + \frac{\pi}{2}\sqrt{\frac{C}{L}}R_s\left(A + A^{-1} - 1\right)\right)^{-1} \quad , \quad A = \frac{V_2}{V_1} \ . \tag{4.3}$$

In the case of topology derivatives such as a voltage divider / multiplier [1], (4.1) and (4.3) would be modified using the normalized gain, $\tilde{A}$, according to the base voltage gain, A_n:

$$\tilde{A} = \frac{A}{A_n} \tag{4.4}$$

For a natural multiplier A_n=2, while for a divider A_n=0.5.

4.2. Voltage regulation

The gyrator converter feeds the output with resonant pulsed current, in a similar operation mode to DC-DC converters in DCM. To facilitate DC output, an output capacitor, C_L, is added such that the average of the current is passed to the load (neglecting ripple). For a resistive load, R_L, the output voltage can be expressed as:

$$V_2 = I_2 R_L = 2R_L V_1 fC \ . \tag{4.5}$$

It should be noted that due to the DCM-like operation of the converter, the input voltage to output current response is of zero order (instantaneous) [40]. Similarly, the output voltage response is of zero order for the case of a resistive load.

If f is made controllable, the system is able to react and compensate for any changes in the input voltage, reference voltage or the load resistance such that the average output voltage is obtained without over/undershoot. The deviation of the instantaneous output voltage from the desired value is in the range of the peak-to-peak output voltage ripple, $\Delta V_{2,\text{p-p}}$, which is proportional to the operating conditions and the output capacitor, that is [1]:

$$\Delta V_{2,p-p} = 2V_1 \frac{C}{C_L}\left(1 - \frac{f}{3f_{max}}\right) \ . \tag{4.6}$$

To utilize the ideal response feature of the converter derived from its DCM operation, a zero-order PDM control scheme is employed, as illustrated in Fig. 4.1. The output voltage is directly monitored by a comparator, referenced to a target value V_{ref}. The reference value is set to the lowest allowed voltage, taking into account the voltage ripple by:

$$V_{ref} = V_2 - \Delta V_{2,p-p}/2 \ . \tag{4.7}$$

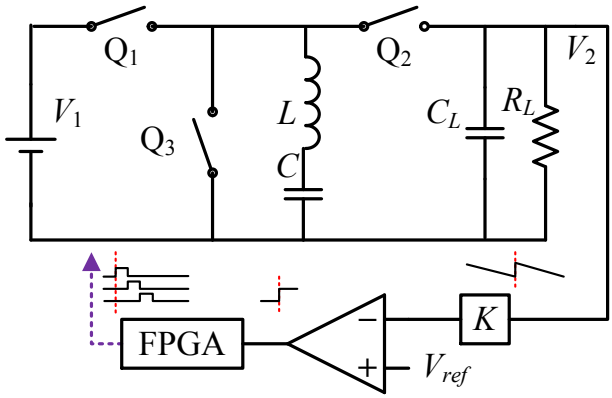


Fig. 4.1 The proposed voltage regulator: A new gyrator resonant switched capacitor converter and feedback loop.

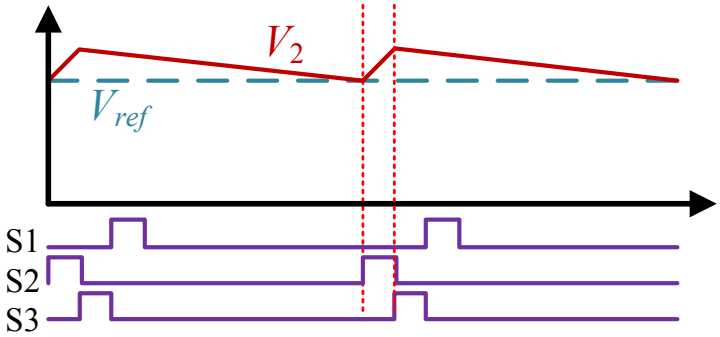


Fig. 4.2 Waveform relations between comparator inputs and the state signals for the proposed voltage regulator from Fig. 4.1

The PDM operation of the controller is illustrated in Fig. 4.2. Triggered by a comparator event (when $V_o < V_{ref}$), a switching sequence of (S2, S3, S1) is initiated and followed by a time-delay until the next comparator trigger. The order of the switching sequence is arranged such that after the time-delay, which allows the output voltage to drop down to V_{ref}, a discharge state (S2) is initiated to charge the output capacitor back to $V_{ref} + \Delta V_{2,p\text{-}p} / 2$. Then, the other two states (S3, S1) occur to *"arm"* the flying capacitor, rendering the converter ready for a new cycle. The rate f in which the switching sequence is activated depends on the slope and the amplitude of the voltage ripple, that is, on the load current and C_L.

Following the PDM method described here, the average output voltage is constant, within the ripple margins, and is independent of R_L and V_{in}. As can be observed from (4.6), the ripple primarily depends on V_1 with maximum deviation of 17% from the total ripple due to changes in the load (varying f). In most cases, this deviation is negligibly small, and $\Delta V_{2,p\text{-}p}$ in (4.7) can be approximated to an averaged ripple amplitude. Since the average output voltage

is maintained at all times, i.e. no transient time, the voltage regulator can be considered to constantly operate at steady-state, and the efficiency estimated in (4.3) is applicable. Furthermore, no-load protection is inherent since no triggering will occur.

Upon startup, the output capacitor voltage is zero ($V_2 < V_{ref}$) and the controller reduces the time-delay to a minimum, constantly charging C_L until the desired voltage is obtained. To limit inrush currents, V_{ref} can be made to slope up slowly.

4.3. Design procedure

This section presents an implementation example demonstrating the design procedures for a voltage regulator based on the gyrator topology. First, the values of L and C are derived by combining (4.1) and (4.2) and taking into account worst-case of f_{max}, $V_{1,min}$ and $I_{2,\max}$ as follows:

$$\begin{cases} C = \dfrac{I_{o,max}}{2V_{in,min}\, f_{max}} \\ L = \left[\left(3\pi f_{max}\right)^2 C \right]^{-1} \end{cases} . \tag{4.8}$$

The second step is to estimate the values of the rms current that circulates in the resonant tank. This is done for the selection of the switches as well as to determine the physical sizes of L and C. Considering (4.3) and after some manipulations, the rms current can be expressed as:

$$I_{rms} = \sqrt{V_2 I_2 \frac{\pi}{2Z}\left(A + A^{-1} - 1\right)} . \tag{4.9}$$

Finally, given a desired target voltage and defining the allowed voltage deviation, the output capacitor value and the reference voltage are calculated using (4.6) and (4.7), respectively.

Consider an example of a 20W step down inverting voltage regulator with the target values of V_o = 5V, V_{in} = 8 to 15V, $f_{(max)}$ < 500kHz. By (4.8), L = 0.1µH and C = 0.56µF are chosen such that 20W of power can be processed for the input range specified. Given loop resistances of R_S = 20mΩ, the expected efficiency is in the range of 85% to 92%. In common with switched-inductor PDM converters, the rms currents are relatively higher than

conventional converters that operate in CCM. As opposed to other PDM converters, no additional losses are present thanks to the resonant current and the resultant soft switching operation. In this particular design the rms current is estimated to be 12A at maximum effort. The main problem with higher rms currents is the stress on the flying capacitor. This can be overcome by paralleling capacitors of smaller values. The inductor, however, is of small volume and can be realized without a ferrite core.

4.4. Experimental results

To verify the operation of the converter as a voltage regulator and to demonstrate the ideal transient features of the system, a 20W experimental prototype was realized using an inverting bridge configuration (Fig. 4.3). The target parameters and the list of components used are summarized in TABLE IV. A digital PDM controller was implemented on a FPGA (Altera Cyclone IV). The ZCS operation of the gyrator RSCC is sensitive to input voltage variations, but since the input range is moderate, satisfactory results were achieved by pre-calibration.

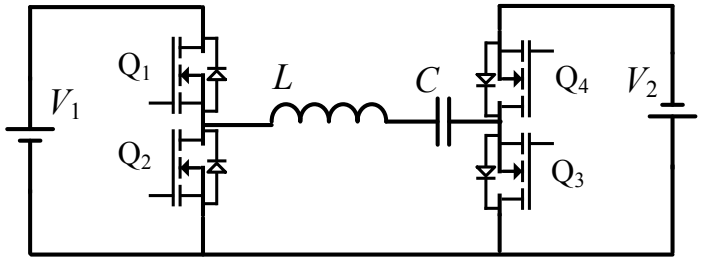


Fig. 4.3 The experimental inverting scheme, using four MOSFETs

TABLE IV. EXPERIMENTAL SPECIFICATIONS

Component	Value	Notes / Model
C	1μF	10×0.1μF
L	0.18uH	Air windings
R_S (per loop)	48mΩ	
MOSFETs		
f_{max}	250kHz	
η_{min} ; η_{max}	0.72 ; 0.83	
$V_{1,min}$; $V_{1,max}$	8V ; 15V	
$I_{2,rated}$; V_2	4A ; 5V	
C_{load} ; $\Delta V_{2,p-p}$	50μF;0.5V	5×10μF

Fig. 4.4 demonstrates the ideal transient response of the voltage regulator with zero-order response for both light-to-heavy and heavy-to-light modes for zero to nominal current (4A)

load transients. The deviation of the output voltage from its average value is measured to be around 100mV. A minor discrepancy is evident between the calculations of L and C for the effective operation range and is due to practical efficiency which is not taken into account in (4.8). This resulted in a slightly higher bound on the input voltage of 9V instead of the original 8V to deliver power of 20W to the output.

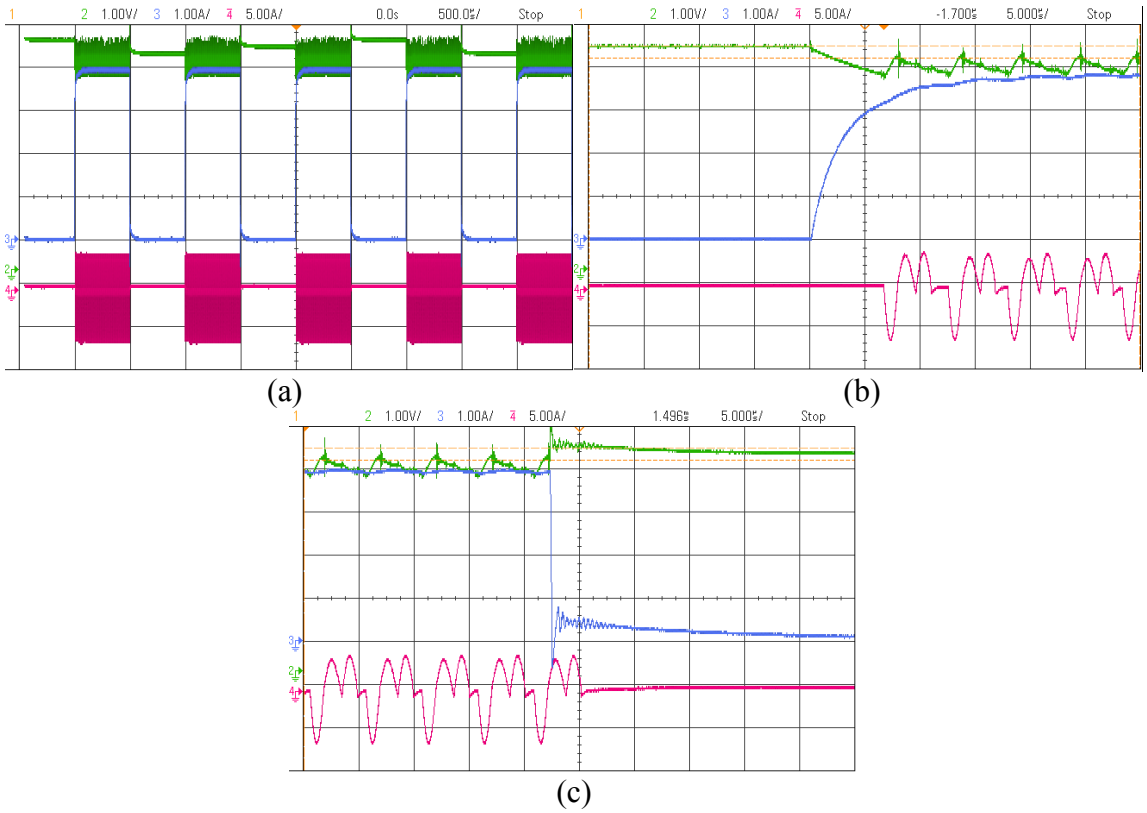


Fig. 4.4 Screenshots obtained from the experimental setup. V_1=12V, V_2=5V, I_2={0A,4A} switched repeatedly at 1kHz. Signals are: top-V_2, mid-I_2, bottom-I_C, (a) broad look upon voltage stabilization, (b) load step-in, (c) load step-out.

4.5. Conclusions

A new, small and efficient voltage regulator based on resonant switched capacitor technology has been developed. Voltage regulation is facilitated by simple PDM control, which demonstrates ideal transient recovery for all disturbance types. Detailed analysis of the new RSCC, in the context of voltage regulation, is provided and verified. Design guidelines for the system are delineated.

5. Soft Switching Issues

Soft switching is a key element in resonant converters, aiding in the achievement of an increase in efficiency by avoiding the switching losses that originate from the MOSFET conduction channel, as previously described in section 1.3. This section will focus on methods to achieve soft switching in the prototype described in chapter 3 and will discuss the behavior of the power stage on late and on early switching.

5.1. Introduction

In resonant converters that implement soft switching, the timing of the switches is crucial. As in many other converters, in the GRSCC there is a certain point in time where the current or the voltage (or both) are zero. Inaccuracies in timing will then lead to increased switching losses due to effective hard switching. There is a fundamental difference between ZCS and ZVS. The former is more straightforward; switching occurs when the resonant tank current reaches zero, a parameter which can be sensed. The latter cannot be sensed directly because the tank's voltage is dictated by the switches connecting the bus to a constant voltage source (input, output or short circuited). Ideally, when a resonant tank has a high quality factor, Q, zero voltage and zero current occur at the same time. However, practically, due to capacitances on the switches and parallel diodes, a lag still exists between the two.

5.2. Adaptive calibration using an ADC module – ZCS

ZCS can be achieved by sensing the current on the resonant tank. Sensing can be done by a passive transformer-based current sensor, rectified and clipped. ZCS solutions compare this signal to a reference voltage to identify near zero currents. Real time solutions demand early triggering to compensate for the delay line that is derived from comparator triggering, decision making in the MCU and driver and gate rise times. Thus, the reference should have a non-zero value. In the GRSCC, pulse sizes might vary dramatically, posing a problem for choosing the reference point. One solution presented in [25] changes the reference point according to the predicted pulse size.

A different approach adopted in this research is adaptive calibration, done by sampling the sensed signal at time points near an expected crossing, before and after. The switching

between states starts by using an initial estimation based on the known resonance frequency of the designed tank. A rectified current signal is sampled around the switching time and analyzed. Based on the relation between the switching time (center of sampled vector, for instance) and the location of the minimum signal, and based on whether or not it reached zero, an estimation can be made as to whether there is a need to increase or decrease the 'on' time of a state and by how much.

Fig. 5.1 shows four possible scenarios, two for early switching and two for late. Two scenarios exist for each, due to the fact that two subsequent states may or may not have reverse current directions. This depends on whether the voltage gain, A, is higher or lower than unity. For example, if the converter increases voltage, then the discharge (S2) and invert (S3) have currents flowing in the same direction, corresponding to Fig. 5.1(a) or Fig. 5.1(c). Between invert (S3) and charge (S1), current direction reverses and the waveform will correspond to Fig. 5.1(b) or Fig. 5.1(d).

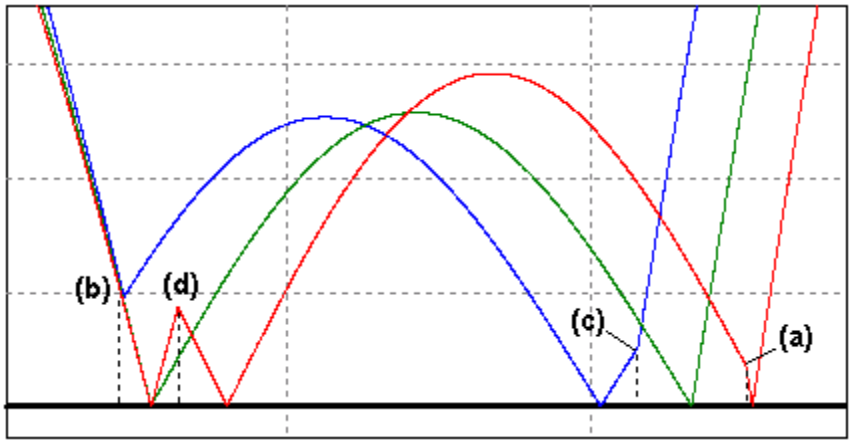


Fig. 5.1 Waveforms revealing early, exact, and late switching scenarios: (a) early, current gradient polarity is maintained, (b) early, current gradient polarity is reversed, (c) late, current gradient polarity is maintained, (d) late, current gradient polarity is reversed.

Sampling the signal and using the switching as the time reference, the location of the first minimum in relation to the switching time can be determined. Assuming that the driver and MOSFET response times are known, the distance between the first minimum and the switching time can be added to the switching time to correct the error. This simple method covers cases (a), (c) and (d) in Fig. 5.1, but not case (b). The case in Fig. 5.1(b) can be identified by checking if the minimal value is larger than zero. In that case, a linear approximation from the gradient until the minimum can be made to estimate the error, as illustrated in Fig. 5.2.

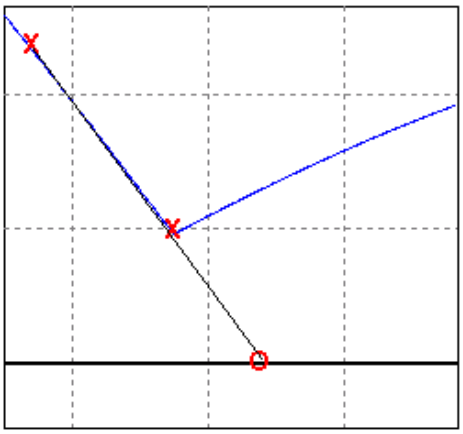


Fig. 5.2 Linear prediction of the required timing for ZCS, when a case of Fig. 5.1(b) is identified.

For the calibration process to converge, error correction is done in steps rather than jumping straight to the estimated value. This prevents missing the correct time value and creating oscillations in the calibration process. The calibration algorithm is portrayed in Fig. 5.3, applying the presented instructions. The algorithm assumes that the steps are S2→S3→S1→delay.

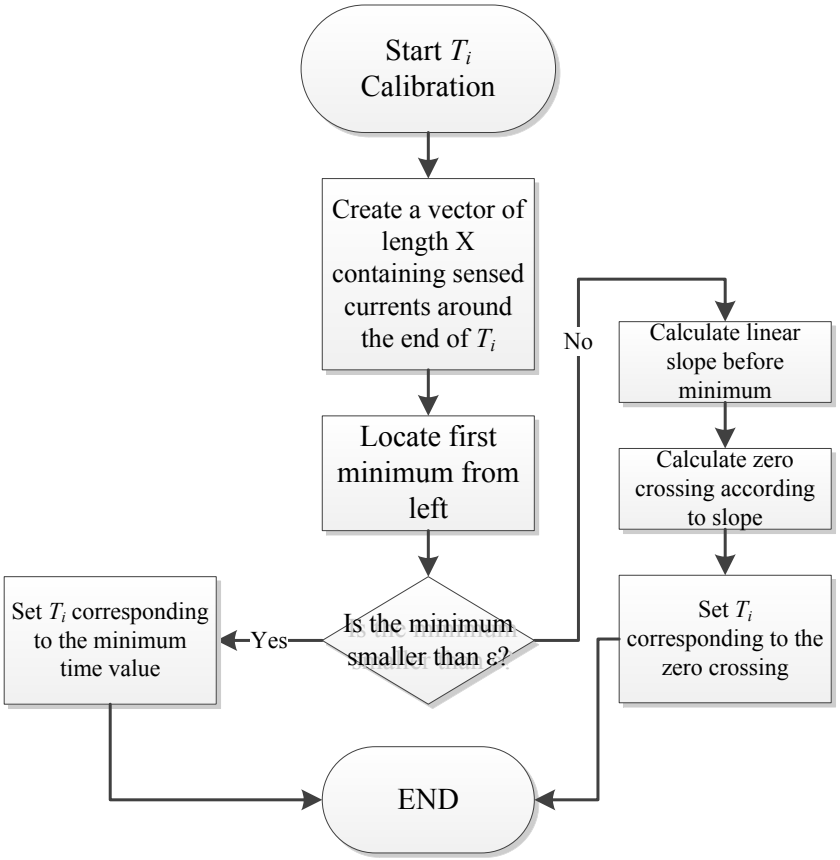


Fig. 5.3 Flowchart describing the ZCS algorithm, calibrating the 'on' time, T_i, of switching stage Si {i=1,2,3}. ϵ is a constant to create a noise margin in order to consider a minimum value that is non-zero.

5.2.1. Low-frequency sampling technique

Ideally, sampling requires a moderate number of points in the tight time interval around the zero crossing area, demanding sampling frequencies of ~10 times f_s. Effectively, when the cycles are recursive, samples do not all have to be from the same cycle. This means that the sample frequency can be like or even less than the converter's operating frequency, reducing the hardware demands and the power consumption. In order to reduce noise and error, multiple samples can be taken for each point and then be averaged. Since the calibration is performed offline, the converter continues to operate while calibration is being done.

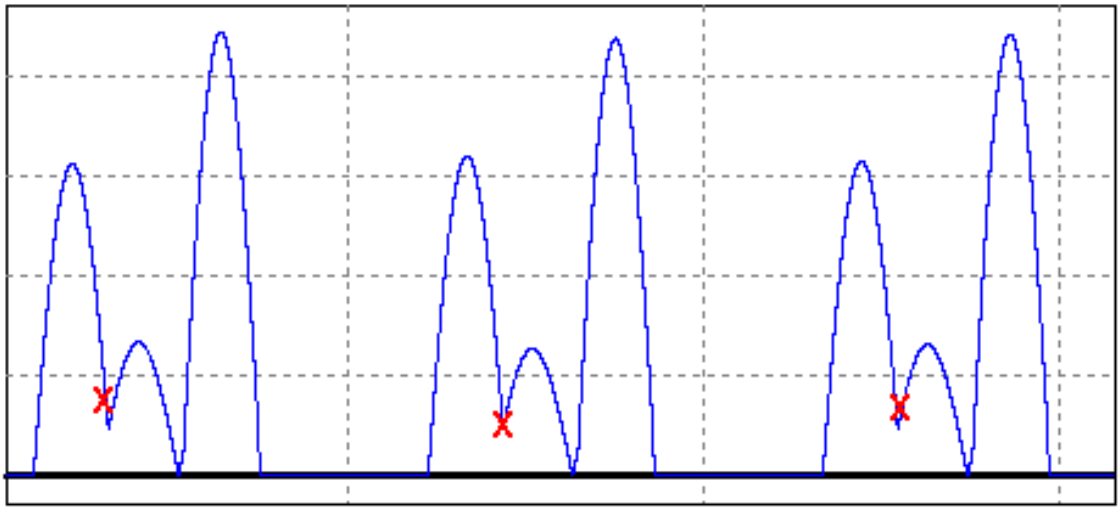


Fig. 5.4 Sampling of the current can be done whithin different cycles.

5.2.2. Experimental results

The adaptive zero crossing calibration algorithm was applied in the system described in section 3.3. Fig. 5.5 shows a typical waveform after calibration. Between cycles, good calibration can be seen, but after S1, it seems that the calibration is unsuccessful. Further investigation shows that the switching occurs on time. As seen from (2.3), V_C after S1 will be the sum of the input and the output. However, effectively, the input and output levels change during the cycle due to ripple, leading to excess voltage that continues to discharge through the parasitic diodes in the switches (Q_1, Q_4).

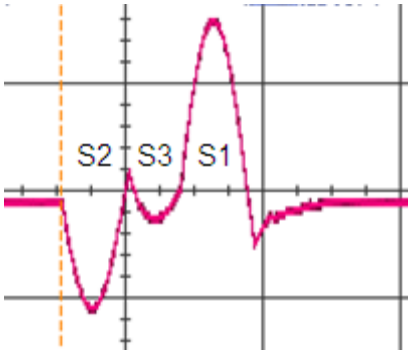
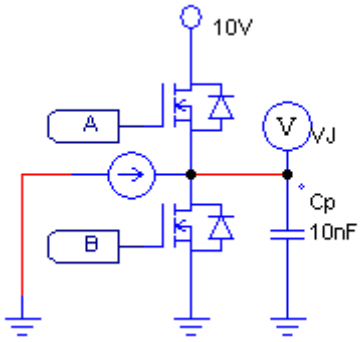


Fig. 5.5 An example of a bridge converter (TABLE III.) with active zero crossing calibration applied. The converter works at 70kHz with V_o = 15V, A = 1.25, $P_o \approx$ 22W.

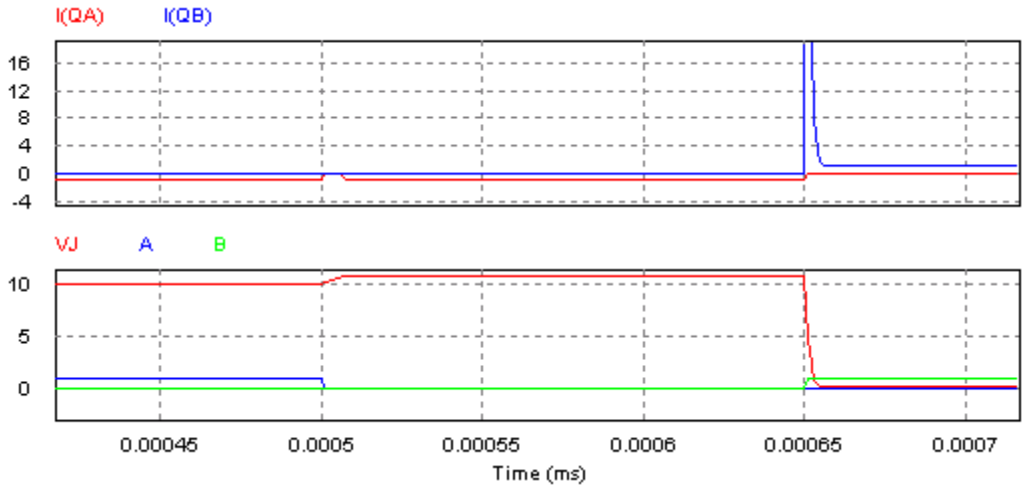
5.3. Future work for adaptive soft switching

ZVS is now a part of the ongoing work within my current research, with various methods under investigation for creating an algorithm to apply the theory that will now be explained. I have chosen to disclose some details due to the relevance of the subject to this thesis.

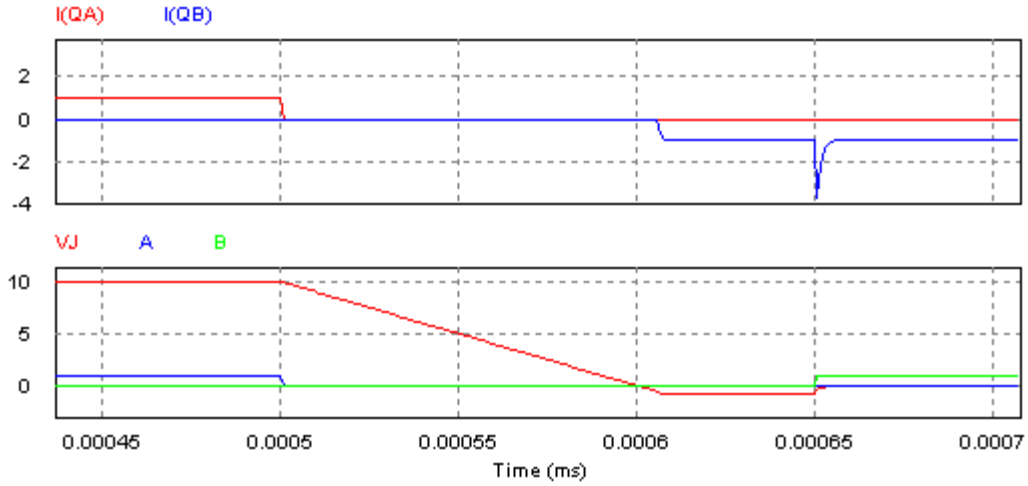
The algorithm that is described in the previous section gives good results, but demands resources that may not always be available and until full calibration is accomplished a considerable amount of losses occur. In order to improve the accuracy of the ZCS, ZVS can sometimes be applied, benefiting from the switches' reverse conductiveness in a bridge implementation. Depending on the state, turning the switches off does not necessarily render the state to be at cut-off due to the parasitic diodes in the MOSFET. Depending on the direction of residual current (none or near ZCS), if it is in the conductive direction of the diode, the current continues until the inductor is discharged or a complementary MOSFET is switched on, diverting the current and initiating the next state.



(a)



(b)



(c)

Fig. 5.6 A simulation of a MOSFET half-bridge switching under current with 100ns dead-time: (a) simulated circuit, (b) transition from A to B with 1A of current flowing in the direction shown in (a), (c) transition from A to B with 1A of current flowing in the opposite direction.

Fig. 5.6 shows the behavior of a MOSFET bridge when switching under current with dead time between switches. Capacitance from the two MOSFETs and their parasitic diodes is represented by an added capacitance, C_P, connected between the switches and needs to be (dis)charged in order for the transition to occur. The example of Fig. 5.6(b) shows the case where one MOSFET is switched off and its diode continues conducting. When the complementary MOSFET starts conducting after the dead-time, current from both the tank and the C_P flows through the conduction channel, seen in the figure as a big spike at t=0.65μs and dissipating power within the process. The result is that the 'breaking' switch disconnects at zero voltage, while current continues via the parasitic diode. On the other hand, the 'making' switch connects in a hard manner, i.e. it tries to pull down the junction potential when conduction starts. Fig. 5.6(c) shows the opposite case where current initially flows against the conductive polarity of the parasitic diode. When the conducting transistor is disconnected, the voltage is initially held by C_P and the remaining tank current flows to linearly (dis)charge the parasitic capacitance until the diode of the complementary switch conducts. If the ‘breaking’ switch acts faster than the time constant of the parasitic capacitance, breaking will occur at zero voltage. Timed correctly after the diode conducts, the complementary MOSFET will start conducting likewise, at zero voltage.

The calibration algorithm can be improved by utilizing these transients and aiming towards achieving a hybrid algorithm that integrates between ZVS and ZCS.

6. Discussion

6.1. Contributions of the research

High efficiency SCC – For the first time, a switched capacitor converter, which performs at high efficiencies largely independent of changes in the conversion ratio is presented. Its performance is more similar to a SIC, while retaining the benefits of a SCC.

Continuous conversion ratio in SCC – The presented topology offers the capability of a continuous conversion ratio range, from below to above unity. This feature does not exist in conventional SCCs and contributes to the high efficiency of the topology.

Voltage-dependent current source – The gyrator behavior of the presented topology gives it unique current sourcing capabilities. When operated from a constant voltage source, it has a current sourcing output, enabling it to be applied in chargers, LED drivers, etc.

Zero order dynamic response – When regulated, the proposed topology can work in PDM, enabling immediate response to sensed changes in current consumption. One application that was thoroughly investigated in this research was an immediate response voltage regulator that displays no transient recovery times.

Adaptive zero crossing calibration – An offline calibration algorithm was implemented when testing the different prototypes. Calibration is important in soft switching topologies for maintaining high efficiencies and the adaptive method enables the use of simple peripherals for maintaining soft switching.

6.2. Future work

In-circuit implementation – The interest in miniaturization is a key factor motivating renewed interest in switch-capacitor technology. Since the proposed topology incorporates an inductance with relatively low values, a packaged implementation can be investigated, yielding a converter with high power density.

Voltage regulating module – A high power voltage regulating module (VRM) for computer applications is the natural next step for the voltage regulation theorem presented in

this research. A VRM should be capable of delivering over 100W at extremely low output voltages. This poses challenges that need to be overcome through further research.

Large conversion ratios – Conversion ratios of more than 3 or less than 1/3 are generally inefficient using the basic configuration. Multilevel configurations should be further investigated with the aim of achieving high gains.

Interleaved converter – An option that should be considered is creating high-power converters out of multiple low-power converters. Interleaving the switching timings of the converters can significantly reduce ripple and aid in reducing the size of the converter by lowering the peak currents in each module.

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