BEN-GURION UNIVERSITY OF THE NEGEV
FACULTY OF ENGINEERING SCIENCES
DEPARTMENT OF ENERGY ENGINEERING

ENHANCED PROCESSING AND CONVERSION CAPABILITIES IN MULTI-MODULAR ENERGY MANAGEMENT SYSTEMS

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE MSc. DEGREE

By: Bar Halivni

Supervised by:
Prof. Mor Mordechai Peretz

October 2019

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Chairman of graduate studies committee:

Name: Dr. Vitaly Gitis …… Date: 26.09.2019

Abstract

This thesis addresses enhanced performance multi-modular energy management systems for high-end applications using advanced controller architecture and circuit design optimization. The work mainly aspires to achieve superior energy management system transient performance that limits the miniaturization of these systems. The primary goal of this thesis is to reduce the overall volume of power converters and to improve the energy density of the full energy management system. Future generation of energy supply chains in data centers and other high-end applications must keep pace with the rapid advancement in cloud computing technologies.

One objective of this thesis is to improve the load transient response of interleaved multiphase buck voltage regulator modules (MPVRMs). The reactive components of PMVRMs are selected and sized to satisfy the load regulation during transient events. Effective implementation of advanced control methodologies can provide a great improvement to the output transient response. Reduction of the output voltage deviation and transient time can be translated into a significant reduction of the reactive components' size and volume or to accommodate even more powerful loads. To obtain the highly desired improvements this thesis introduces a new all-digital controller for high-performance MPVRM and all the relevant peripherals and supporting circuitry.

Another objective of this thesis is to study the optimization principles and design considerations for MPVRM in high-end energy management system. Within the context of this objective, detailed analysis of the control methods implemented into the MPVRM hybrid controller with the necessary adaptation for multi-modular operation. The supporting analog interface for the MPVRM controller is also analyzed and adjusted for high-performance environments. The research also includes an in detailed design guideline covering design consideration, component selection, layout notes and validation of 12V-to-1.xV high-power MPVRM. The introduced MPVRM design is meant to be used as an energy management system in the next-generation CPUs and DDR4 memory modules in data center applications. This part of the research has been submitted to the IEEE Applied Power Electronics Conference and Exposition (APEC) 2019, and within a larger study that has been submitted to the IEEE Transactions on Power Electronics.

Acknowledgments

I would like to thank my supervisor Prof. Mor Mordechai Peretz for his invaluable guidance and support throughout this thesis. Through a profound professional passion and expertise combined with patient guidance, Prof. Peretz has impelled me to excellence, all the while being a true friend providing me with the opportunities for enjoyment and for the self-fulfillment of accomplishing my professional and academic goals.

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With great appreciation I thank my girlfriend Noy, for her immense support, patience and care. Last but not least, I would like to express my profound gratitude to my parents and my dear sister, who have always supported and cheered me along this wonderful journey.

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Acronyms and Abbreviations

IC – Integrated circuit
EMS – Energy management system
PMIC – Power management IC
OCP – Open computing project
HPHPL – High-power high-performance load
PCB – Printed circuit board
CPU – Central processing unit
DDR – Double data rate
FPGA – Field-programmable gate array
UPS – Uninterruptible Power Supply
VRM – Voltage regulator module
VID – Voltage identification
AVP – Active voltage positioning
PWM – Pulse-width modulation
MOSFET – Metal oxide semiconductor field effect transistor
VMC – Voltage-mode control
CMC – Current-mode control
TOC – Time-Optimal control
ADC – Analog-to-digital converter
ESR – Equivalent series resistance
BW – Bandwidth
ACM – Average-current mode
PCO – Phase count optimizer
DL – Delay line
DPWM – Digital pulse-width modulation
TSU – Transient suppression unit
LEM – Load emulation module

Inline References Legend

X.XX – Chapter / Section number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure

1. Introduction

1.1. Energy management systems

Energy is the foundation to the operation of every electronic device, from the single IC level to a massive building-sized data centers, all rely on energy management systems (EMS) to provide the energy required for their operation. The EMS consists of two parts, the power converter which delivers the power to the load and the power management IC (PMIC) that controls the power converter operation. EMS can be divided into three main groups: AC-to-AC, AC-to-DC, and DC-to-DC power conversion, this work will focus on the latter. DC-to-DC EMS is shown in Fig. 1.1 where the input voltage V_{in} is converted to output voltage V_{out}, the desired voltage level at the output is usually dictated by the load and can be lower, higher or equal to V_{in}.

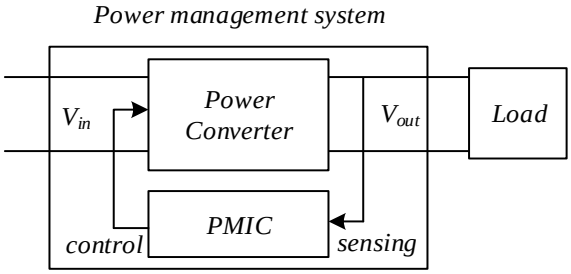

Fig. 1.1 Basic energy management system block diagram.

Data centers use large number of high-end loads like CPUs, DDR memory modules and FPGAs to deliver the required computing power to support recent evolution of cloud computing. High computational power data centers consume an increasing amount of power [1], as a result new EMS are required by the industry. The new EMS performance requirements increase constantly as new more powerful loads are being developed. The EMS improvement is carried out by new power converters topologies and control methods that introduce:

- Better system dynamic performance
- Higher overall power
- Improve efficiency
- Size reduction and higher power density

1.1.2. Data centers energy supply chain

The full energetic path to the end loads in data centers is composed of multiple EMS stages as shown in Fig. 1.2, this state-of-the-art data centers energy delivery systems standardization is formed by the open computing project (OCP) in recent years [2]. The power processing chain of data centers applications starts with an AC-to-48V EMS that provides a $48V_{DC}$ unregulated bus as the main source of power for multiple cabinets. The unregulated $48V_{DC}$ is then down-streamed to the load in two-stage EMS architecture. The first stage is a 48V-to-12V EMS to provide a $12V_{DC}$ regulated bus that supplies multiple motherboards within the cabinet.

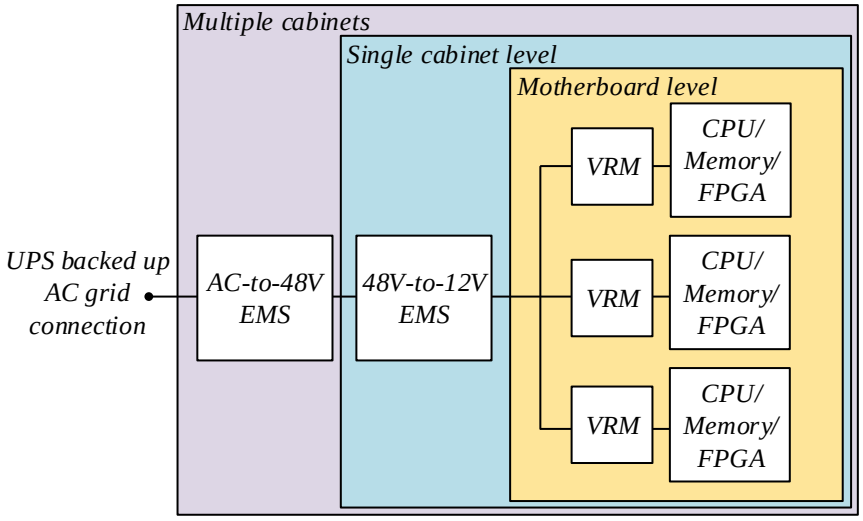

Fig. 1.2 Modern data center energy supply chain.

At the motherboard level, the $12V_{DC}$ voltage bus reaches the second level voltage regulation module (VRM) EMS that converts the $12V_{DC}$ to lower voltage, usually in the range between 0.8V to 1.8V. The VRM most important goal is to maintain a highly-regulated output voltage under any loading conditions, typical VRM loads require a well-regulated voltage even under extreme transient conditions as detailed in the following subsection. Besides the primary task of voltage regulation, modern VRMs are required for additional functionalities such as [3]-[6]:

- Support dual output voltage rails for two different load power rails [7]
- Advanced control features for improved efficiency and dynamic performance
- Real-time adjustment of the output voltage
- System and load protection: over-voltage, under-voltage, over-current, and thermal protection

- Telemetry: send real-time data about different system variables (voltage, current, temperature, etc.)

All the VRM functions above and more are maintained by the PMIC, in a similar way to the VRM, modern PMIC are more than just simple power converter controllers and can be recognized as full system-on-chip IC.

1.1.3. Data center high-power high-performance loads

On the receiving end of the data center power chain there are the high-power high-performance loads (HPHPL), these loads pose a challenge to the VRM with high current slew rate during transients and extremely strict regulation requirements. Fig. 1.3 shows the current profile of HPHPL, the full current profile (Fig. 1.3 (a)) show how the load current changes based on the computing power required. In data centers, the HPHPL usually operate in full power as there is little to none downtime. Two main current values are defined at high computing power, the absolute maximum current I_{max} is the current drawn by the load at full computing power for short periods of time and the thermal design current I_{TDC} which is the maximum current where the HPHPL can operate indefinitely without having to thermally shut down. Although the high operation currents can reach up to 200A [7] the real challenge are the high-speed transients with current slew rate of over 1000A/µs shown at Fig. 1.3 (b). With transient time ($t_{transient}$) of less than 1µs, the bandwidth-limited VRM relies on large output capacitance assistance in order to mitigate these high-speed transients.

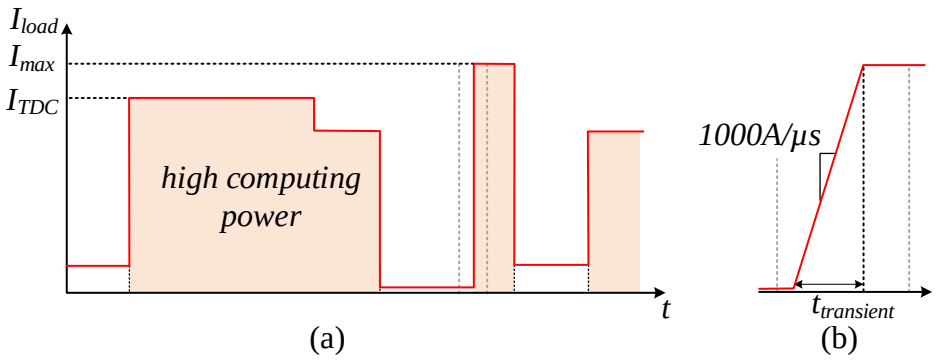

Fig. 1.3 High-end load current profile (a) full profile with maximum current and thermal design current (b) current shape zoom-in during loading transient event.

Other than high-speed current profile the HPHPL also demand strict output voltage regulation during both transient and steady-state operation, typical output voltage waveform

during unloading transient event is depicted at Fig. 1.4. During steady-state operation, prior to the transient event, the output voltage is at its nominal value v_{VID}, modern VRMs support multiple voltage identification (VID) values, digitally sent to the VRM by the load or predefined by the system designer. The transient begins at $t_{trnasient}$ and lasts until v_{out} return to its nominal value. During a single transient event v_{out} overshoots twice, the first overshoot lasts less than a microsecond and cannot be suppressed, the second overshoot is more prolong and handled by the VRM. The overshoot time T_{os} is defined as the entire period when v_{out} is outside the steady-state tolerance band of V_h-V_l. At any given time v_{out} is not allowed to rise beyond the absolute maximum overshoot voltage V_{osmax}.

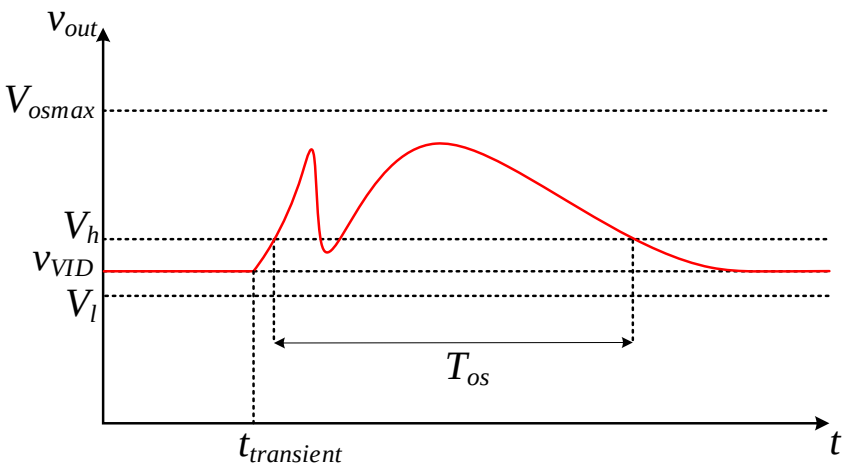

Fig. 1.4 HPHPL voltage waveform during unloading transient event.

An additional requirement of the HPHPL is active voltage positioning (AVP). The AVP function is implemented to dynamically change the nominal output voltage value according to the output current (Fig. 1.5). The load power dissipation constraint is the maximum allowed load continues power (P_{max}), commonly limited by the component packaging thermal limit. At high current operation the output power exceeds P_{max}, by lowering the output voltage to V_{min} the power requirement is met and the load can maintain high-current operation.

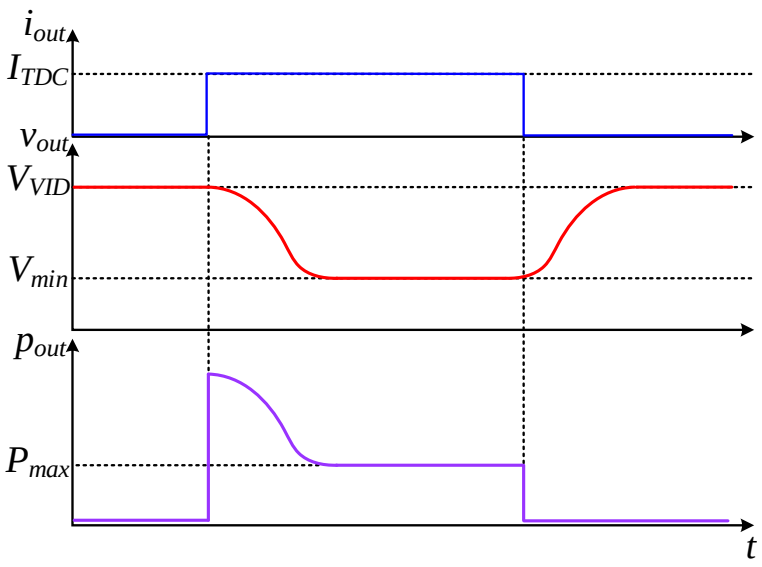

Fig. 1.5 AVP implemented VRM output power waveforms at high-current operation.

1.1.4. High-end VRM signal measurement methods

Fulfilling the high-performance of HPHPLs requirements is a challenging task on its own, this challenge is growing even further when the VRM is implemented on a populous data center motherboard [8]. New standard server motherboards use multiple VRM to accommodate up to two CPUs with 16 memory modules per CPU, all these components alongside other peripherals generate a large amount of noise. With the intention of overcoming these noise sources the VRM controller utilizes differential sensing for its most critical measurements of output voltage and inductor currents. Fig. 1.6 (a) shows a differential to single-ended measurement, the generated measurement signal v_{sns} is a product of the subtraction of v_{ref} from v_{sig}. The v_{ref} signal can be ground signal in the case of output voltage sensing or both signals can be carried by a common mode voltage commonly used in modern VRM current monitoring. By employing full deferential measurements any noise collected by the signals along the routing path is treated as common-mode noise and filtered out by the amplifier. The relatively clean signal v_{sns} can then be used by the controller to perform high-quality regulation. The lesser noise-sensitive measurements like temperature and input voltage can be measured in a single-end fashion using a single wire (Fig. 1.6 (b)) to spare PCB area and layout efforts. In case noise problems dose occur in the single-ended measurements, digital filters offer a low-cost solution with a rather small impact on the system operation in comparison for more expensive analog filtering which requires further design effort and on-board components.

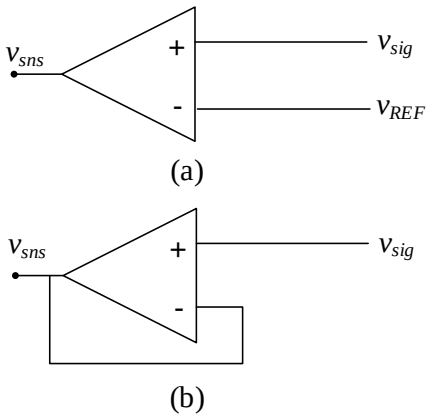

Fig. 1.6 VRM measurements methods (a) differential measurement (b) single-ended measurement.

1.2. Overview of multiphase buck converters

1.2.1. Step-down switched-mode converters

Common practical implementation for high-power converters used in VRMs are the step-down switch-mode power converters [9]-[12]. The converters fundamental principle of operation is to create a square-wave output voltage by applying an on-off switching pattern using a solid-state device acting as an ideal switch. Fig. 1.7 (a) shows a simplified representation of the converter circuit, the ideal switch (SW) is toggled to connect (on) and disconnect (off) the input voltage source V_{in} to the output. The square-wave output voltage generated by the switching action is shown in Fig. 1.7 (b), the square-wave period T_s is defined by the sum of the switch on and off state times, t_{on} and t_{off} respectively. The signal average (DC) component V_{avg} is proportional the average switching duty ratio ($D=t_{on}/T_s$) and equal to DV_{in}. Control over the output voltage average value is performed by varying the duty ratio to any value between 1 and 0, as a result V_{avg} limits are V_{in} and 0. Pulse-width modulation (PWM) XXX is a frequently used method to control V_{avg} by adjusting the relations between the on and off times while T_s remain constant.

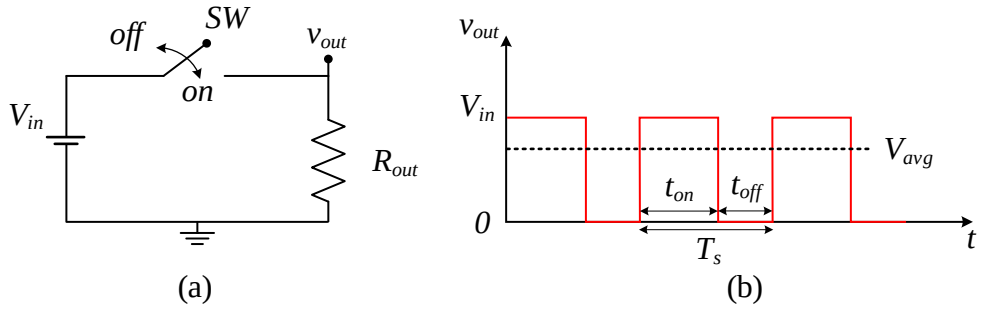

Fig. 1.7 Elementary step-down switch-mode converter (a) simplified ideal switching circuit (b) output voltage waveform.

The VRM loads typically require pure DC output voltage, the output waveform produced by the circuit in Fig. 1.7 (a) contain both a controllable DC component and an AC component. The desired pure DC of the waveform in Fig. 1.7 (b) can be extracted by adding a low-pass filter of passive reactive components. The reactive components can be an inductor connected in series between the switch and the output (Fig. 1.8 (a)), a capacitor connected in parallel to the load (Fig. 1.8 (b)) or both options can be used together to create a higher-order low-pass filter (Fig. 1.8 (c)). Incorporating both filtering methods into the step-down switch-mode converter construct the single-phase buck converter.

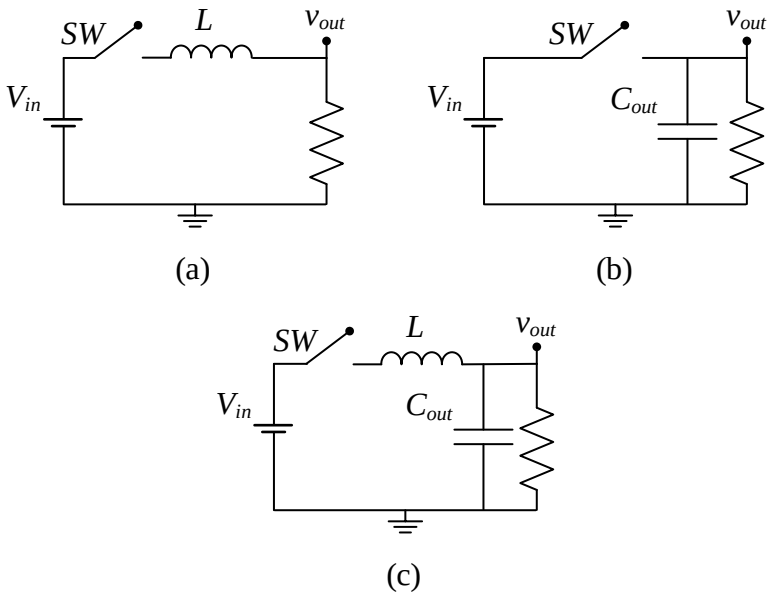

Fig. 1.8 Reactive low-pass filter options (a) series inductor (b) parallel capacitor (c) capacitor and inductor low-pass filter.

1.2.2. Single-phase synchronous buck converter

The buck converter provides a step-down voltage conversion with a high-quality DC voltage at the output, this thoroughly researched converter is one of the most common solutions for high-power step-down power conversion. The basic synchronous buck converter circuit is depicted in Fig. 1.9 (a), a complementary MOSFET transistor half-bridge is used to realize the ideal switch shown in Fig. 1.7 (a). The reactive low-pass filter of capacitor and inductor (Fig. 1.8 (c)) is used to filter the switching node voltage v_x to a DC output voltage at the output as shown in Fig. 1.9 (b). During t_{on} the high-side transistor M_1 is on and M_2 is off, the voltage across the inductor is V_{in}-V_{out} and the inductor current increase. At t_{off} the low-side transistor M_2 is on and M_1 is off and the inductor voltage is -V_{out}, during that time the inductor current decreases. Same as the switch-mode converter the average output voltage $V_{out} = DV_{in}$ of the buck converter is controlled by changing the duty ratio.

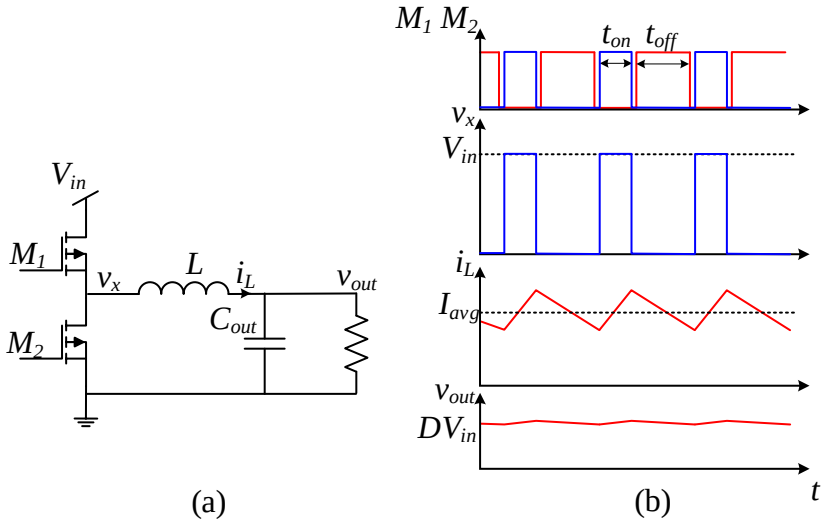

Fig. 1.9 (a) Synchronous buck DC-DC converter (b) current and voltage waveforms of an ideal converter.

The buck converter is usually selected over other alternatives because of its high efficiency curve. Typical buck efficiency curve is shown in Fig. 1.10 and can be divided into three main sections: low-current, optimal-current, and high-current. During low-current operating and high-current operation the switching losses of the transistors and components conduction losses respectively are becoming rather significant, lowering the converter efficiency.

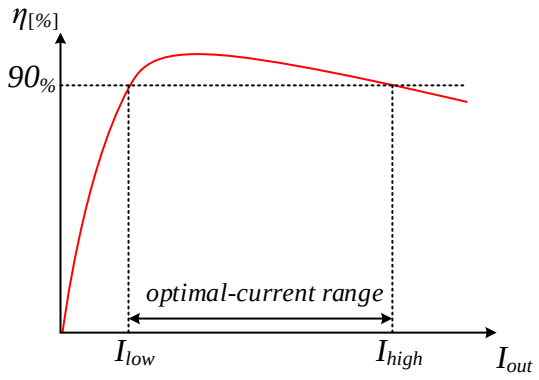

Fig. 1.10 Typical buck converter efficiency curve.

1.2.3. Multiphase buck converter

The single-phase buck converter is a great solution for medium-power VRM where the maximum current is relatively low to keep the converter efficiency high and the passive component size low. A further drawback of the single-phase buck is the bandwidth-limited transient response, incapable of providing the regulation required by the HPHPLs. The multiphase buck converter topology is commonly used in high-power high-performance VRM and overcome all the single-phase buck converter limitations. The core idea of multiphase buck is to connect multiple single-phase buck converters outputs into a single output (Fig. 1.11). Ideally all the load current is now shared among the phases keeping each phase current ($i_{1\text{-}4}$) relatively low, allowing smaller passive components and overall higher converter efficiency [15]-[20], even at high current loading conditions [21]-[24]. The use of multiple phases also increases the system overall redundancy as operating phases can cover for a malfunctioned phase and even allow on-the-fly repair of the damaged phase.

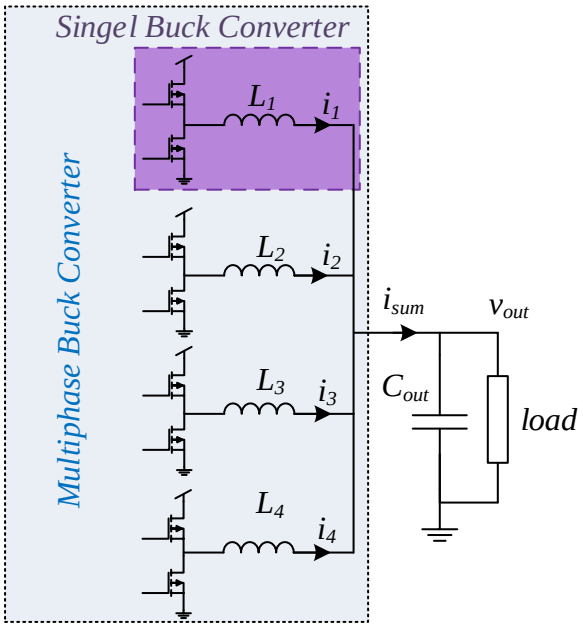

Fig. 1.11 Four single-phase buck converter to single output to create a four-phase multiphase buck converter.

The simplest way to operate the multiphase buck converter is to send the same PWM signal for all the converters, while this is a straightforward method it introduces two main issues for multiphase buck converters. The first problem is the large sum current (i_{sum}) created by joining all the phases together, in the example given in Fig. 1.11 the sum current ripple will be four times larger than a single phase ripple. One way to negate the large current ripple is to scale up the passive component's values, this method deemed impractical in low-space applications where minimal converter area is mandatory. Phase interleaving [25]-[30] is another way to keep the current ripple low and even smaller than in a single-phase buck. In Fig. 1.12 each phase switching cycle is shifted so each phase current cancels some of the other phases current ripples. By implementing phase interleaving the sum current ripple is significantly decreased allowing to scale down the passive components values and reduce the system overall size.

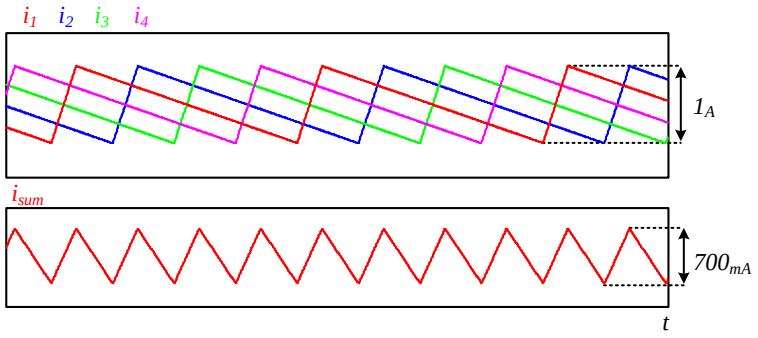

Fig. 1.12 Per-phase current and sum current in a four-phase interleaved multiphase buck.

The second problem created by providing the same PWM single, even in an interleaved manner, is the per-phase DC current unbalance created by each converter output resistance [38]. Fig. 1.13 (a) shows the average model for two single-phase bucks connected to the same output. In the ideal case (Fig. 1.13 (b)), $R_{Ph1}=R_{ph2}$ hence the output characteristics would be identical and for the same V_{out} the phases currents will be equal. At practical multiphase buck converter, the parasitic resistances of components and layout create different output slopes (Fig. 1.13 (c)). The difference between the output resistances of each phase create current unbalance between the phases, therefore independent duty ratio for each phase is required to balance the phases currents. Further information on current balancing motivation and implementations is brought in the following subsection.

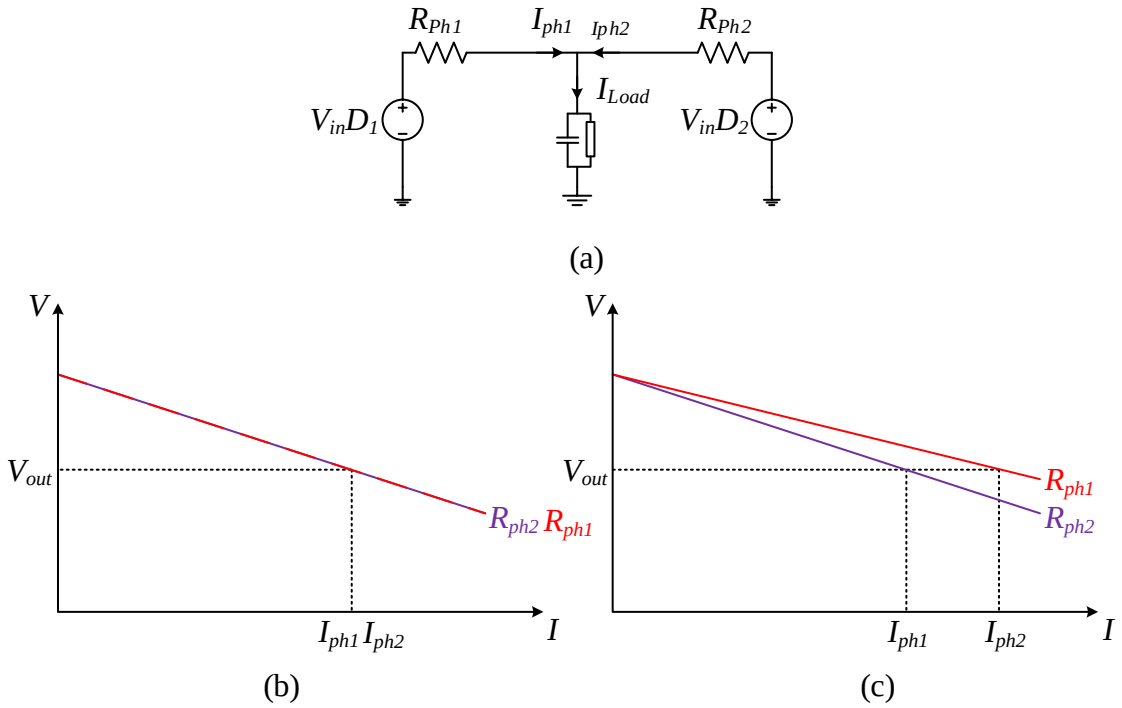

Fig. 1.13 Two single-phase buck converter output characteristics (a) average model (b) ideal case where $R_{Ph1}=R_{Ph2}$ (c) practical case where $R_{Ph1}\neq R_{Ph2}$.

The combination of the independent duty ratio of each phase and interleaved operation also result in higher converter bandwidth. In comparison to a single-phase buck where the duty-ratio command can be updated only once per switching cycle. In multiphase converters the duty ratio can be updated up to the number of phases (N) in each switching cycle, effectively increase the system bandwidth by N. High phase-count converters can utilize the superior dynamic capabilities [31]-[37] to maintain a well-regulated transient response when powering HPHPL.

1.2.4. Current balancing in multiphase buck converters

1.2.4.1. Motivation for current balancing in multiphase buck converters

Current balancing is crucial for the correct operation of the multiphase buck converters. The balance of different phase currents not only properly equally share the load current among the phases but also to allow even thermal distribution to improve cooling efficiency and reduce component degradation. In severe cases of current imbalance some phases may completely shut down when others operate in their maximal current limitation, therefore it is necessary to implement current balancing in multiphase buck converters.

1.2.4.2. Current balancing methods in multiphase buck converters

The most common method to equalized currents in multiphase buck converters is droop current sharing [39]-[45], the current balance is achieved by adjusting all the converters output resistance to match the ideal case shown in Fig. 1.13 (a). Basic passive implementation of droop sharing is to add series resistance to each converter output as shown in Fig. 1.14 (a), the converter parasitic resistance is fairly neglectable to the added resistance R_D so both the converters output characteristics are matched (Fig. 1.14 (b)) and their respective currents equal I_{Droop}. Due to efficiency considerations, R_D can't be realized in high-power systems using physical resistor in the high-current path. A more practical implementation for droop current sharing at high-power systems is to control the phase output impedance by fine-tuning each phase duty ratio by the controller as shown in [46]-[50].

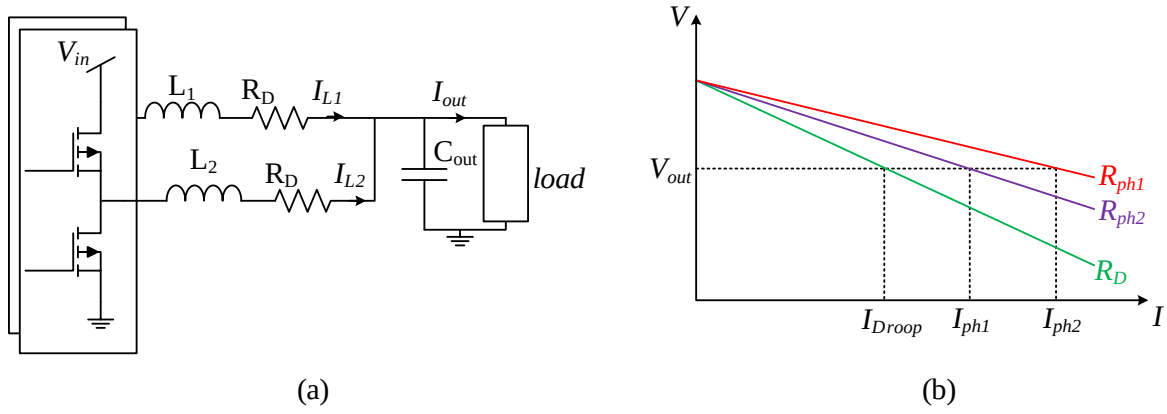

Fig. 1.14 Passive droop current sharing implementation (a) two single-phase buck converters with droop resistance RD (b) droop assisted matched output characteristics of the buck converters.

Droop current sharing either performed in a passive or active manner result in that the output voltage regulation has to be degraded due to the steep output characteristics to achieve high-quality current sharing. Balancing the currents of different power rating phases add additional complexity when using droop current sharing [39]. An alternative approach for current balancing is to use and regulate the per-phase current information in program-mode current control and achieve current sharing without manipulation the converter output characteristics. The programed-mode current control implies additional control loop in order to control each per-phase current (Fig. 1.15) and operate to equalize them to a single control signal v_c, that way current balancing is achieved without damaging the voltage regulation and with no complexity regarding the converters power ratings.

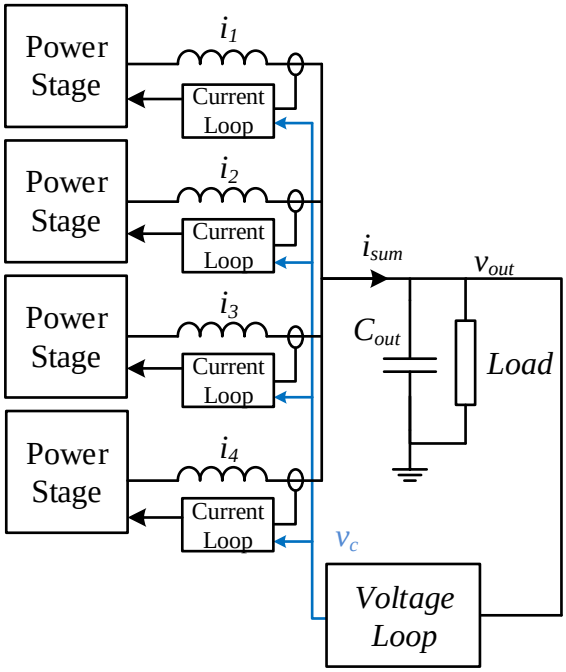

Fig. 1.15 Simplified programed-current mode control for multiphase buck converter.

1.3. Control of witched-mode converters

The primary objective of switched-mode converters is to provide a constant DC voltage to the load. Practical converters that suffer from non-idealities such as parasitic resistances, temperature effects, component tolerance and degradation, and input voltage changes, cannot provide the desired constant DC voltage. In order to turn the unregulated converters to a VRM, a controller is needed to sense the output voltage and adjust the control signals to the converter so the output voltage will remain constant.

1.3.1. Linear control methods

Voltage-mode control (VMC) is a widely used control technique to regulate the converter output voltage by tuning the converter duty ratio to compensate for the error between the measured output voltage to its desired value [51]-[56].

A simplified structure of voltage-mode control loop contains four main components and is illustrated in Fig. 1.16. These four components are the power stage, the sensor, the modulator, and the voltage loop compensator. The sensor extracts the output value from the system and transfers it to the controller where it is compared with the reference value to produce the voltage error v_e. The compensator processes the voltage error and calculates the desired duty ratio value as a correction signal v_c. The compensation network calculations are performed to provide the controller the highest possible bandwidth while also maintain system stability. Finally, the correction signal is procced by the modulator to generate a PWM signal (d) and its complementary signal in proportion to v_c.

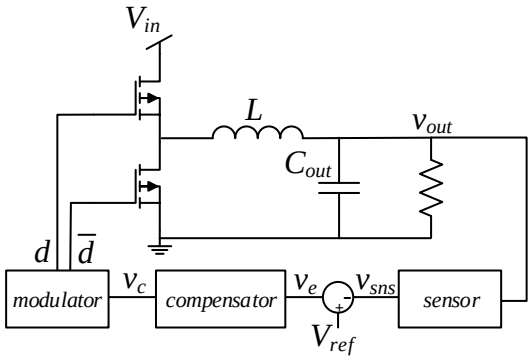

Fig. 1.16 Simplified structure of the voltage-mode control loop implemented on a single-phase buck converter.

Each of the components that construct the VMC shown in Fig. 1.16 can be implemented in a wide variety of options. The three main consideration for the selection of the most suitable realization of each component is dependent on mainly, by not exclusively, cost, performance, and design complexity. One example can be the compensator unit, where common compensator like proportional-integral (PI) compensator can be used, if higher bandwidth is required, the more complex proportional-integral-derivative (PID) can be used instead.

In current-mode control (CMC) a dual-loop architecture is implemented (Fig. 1.17). The additional inner current loop within the VMC single-loop architecture directly controls the inductor current in the same way the VMC regulate the output voltage. The sensed inductor

current i_{sns} is compared with the loop reference to generate the current error and calculate the correction signal i_c. The outer voltage loop correction signal becomes the inner current loop reference. In typical dual loop architecture, the inner loop bandwidth should be much higher than the outer loop bandwidth to prevent oscillations and maintain stability. When implemented correctly the dual loop design turns out to be less complex as the inner loop addition lower the system order so only PI compensators are needed instead of PID.

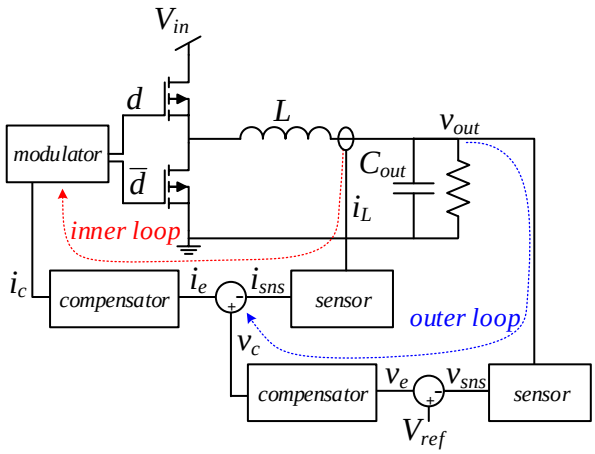

Fig. 1.17 Current-mode control implemented on buck converter.

1.3.2. Non-linear control methods

Switched-mode converters are discontinuous as a result of the switching action and therefore non-linear by nature. The design of linear controllers relies on averaging and linearization techniques to provide a linear behavioral model of the converter. Based on the behavioral models of the converter, linear control methods design offers an excellent regulation of a VRM output voltage under small changes in converter parameters. The linear small-signal approximation limits the linear controller's ability to ideally suppress large-signal load changes. Advanced non-linear control methods are employed to provide a better dynamic response during large-signal changes in the system and to approach ideal transient suppression during large load changes.

1.3.2.1. Time-Optimal control

Time-Optimal Control (TOC) is a nonlinear control method that future ideal transient response with minimum possible output voltage deviation and minimum transient duration [57]-[69]. The ideal TOC transient response in synchronous buck converter includes two switching actions on-off or off-on depending on the transient direction, a loading transient

response is demonstrated at Fig. 1.18. The TOC switching sequence introduces minimum voltage deviation by matching the buck inductor current to the new load current using a single on switching action, when the currents are matched the voltage reaches its extremum point. The minimum time convergence is achieved by the charge recovery phase where the capacitor missing charge is restored and v_{out} return to its steady-state value. The recovery phase switching timings are calculated using T_0 and the average system parameters.

To successfully implement ideal TOC, the minimum point exact time must be measured to calculate the correct charge recovery phase timings, both these actions demand advance controller sensors design and high computational power. Other than the controller requirements the TOC utilize high inductor currents for fast charge recovery which in turn increase components stress and design considerations. TOC implementation is widely researched in an attempt to reduce the computing power required, making it's more accessible for practical applications.

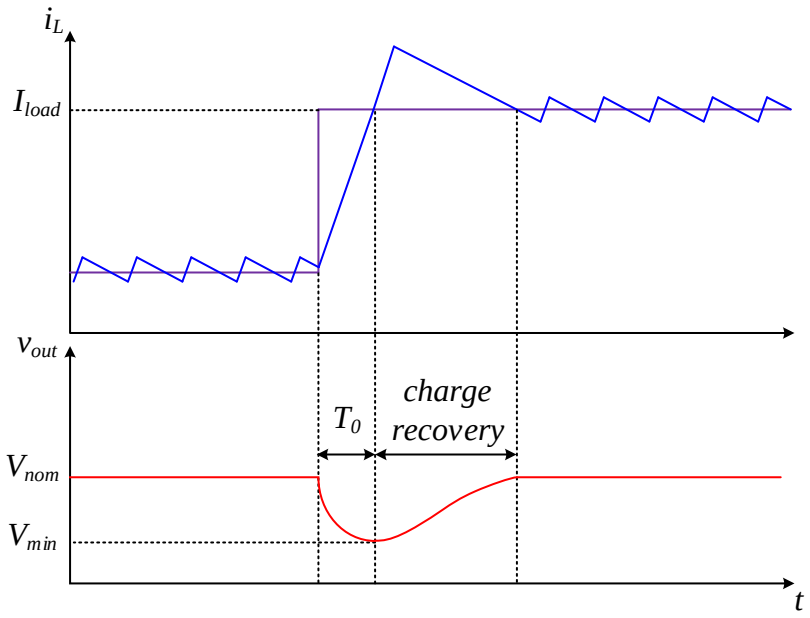

Fig. 1.18 TOC loading transient response in single-phase buck converter.

The minimum deviation transient response is an example for near-ideal TOC transient response with significant reduction in computing power and components stress [70]-[72]. The ideal minimum-deviation sequence is depicted in Fig. 1.19, the current matching prosses is identical to the ideal TOC response with a single on action and detection of the voltage extremum. The charge recovery however, is carried out by the linear controller in the system moderately restore the capacitor charge over several switching periods. Since the charge

recovery phase is now carried out by the liner controller the computational power required diminishes and the alongside components stress.

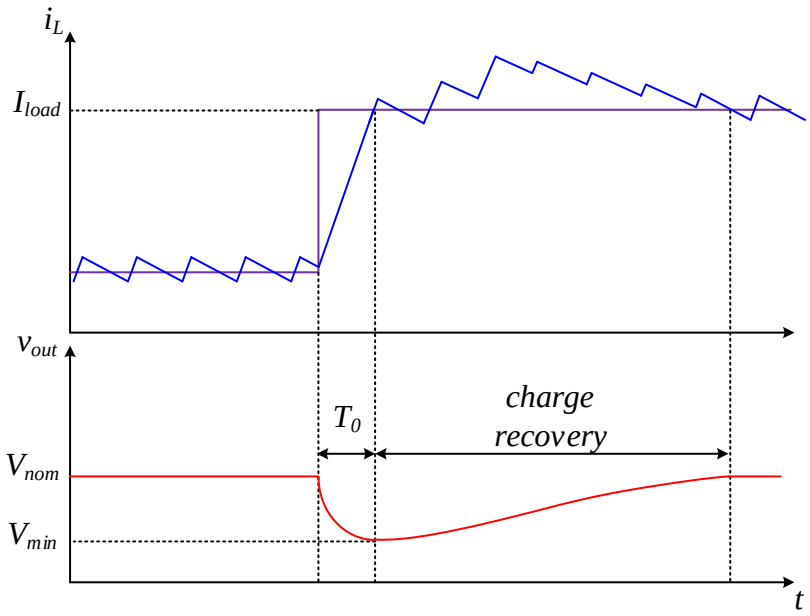

Fig. 1.19 Minimum-deviation loading transient response in single-phase buck converter.

1.3.3. Hybrid control

Hybrid control combines two or more control methods (linear and non-linear), each method operating within well-defined control laws [73]-[76]. The combination of multiple control methods aims to extract each method optimal performance. Fig. 1.20 shows an example for hybrid controller architecture where the linear controller handles steady-state operation to maintain high DC accuracy and stability while the non-linear control takes over for optimal transient suppression. When focusing each control method for its advantageous operation, the hybrid controller provides performance superior to a single method controller.

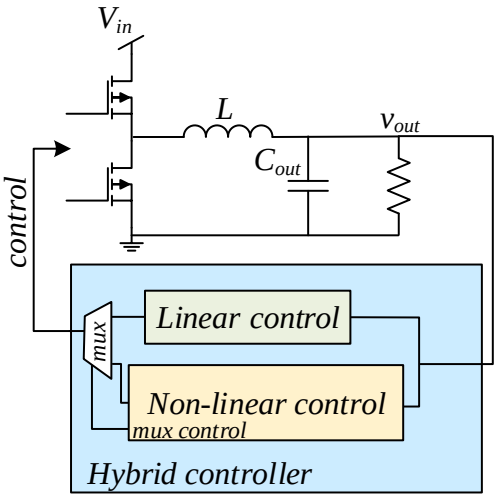

Fig. 1.20 Hybrid controller architecture with linear controller for steady-state and non-linear controller for ideal transient performance.

Closed-loop stability is important for any regulation system. In hybrid controllers, this limitation is removed from the non-linear control in order to approach optimal transient mitigation. The system stability requirements are filled by the linear controller, after the transient suppression is complete the converter is in vicinity to its new operation point, the linear controller then takes over to bring the converter to the desired steady-state operation. Large-signal stability exists in hybrid control if the large-signal compensator can bring the converter from any initial condition to the post transient steady-state operating point.

1.3.4. Digital control of multiphase buck VRM

Digital control approach for switched-mode converters offers several advantages compared to the analog counterpart, the ability to perform complex control algorithm, flexibility to match a wide variety of systems, self-calibrations, and component variation immunity. Despite these potential benefits, PEMICs are limited in high-frequency operation where it is hard to achieve dynamic performance that is comparable to those of the analog controllers. The digital control suffers from significant control delays and quantization effects that limit the dynamic response. Combining the flexibility of digital control together with hybrid controller architecture it is possible to match modern PMIC performance to analog controllers. State-of-the-art digital high-performance controllers usually require high-resolution analog-to-digital converter (ADC) and digital-pulse-width modulator (DPWM), as shown in Fig. 1.21.

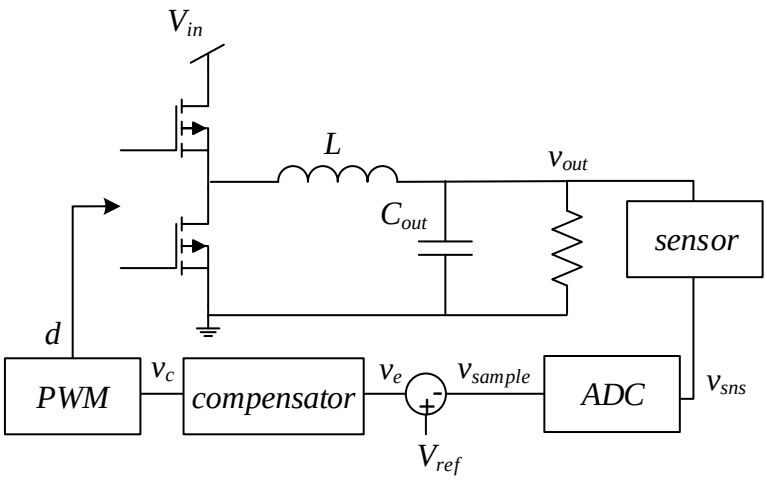

Fig. 1.21 Digital controller functional block diagram.

Analog controllers are dominant nowadays when the controller is implemented on a single-phase buck converter, low costs, as well as low design efforts and faster overall application time to market, make analog controllers dominant over digital controllers. In multiphase buck VRM, digital control is highly advantageous versus the analog multiphase controllers. TABLE I compare digital and analog multiphase controllers characteristics.

TABLE I. DIGITAL AND ANALOG MULTIPHASE BUCK CONTROLLER COMPARISON

Characteristic	***Analog controllers***	***Digital controllers***
Controller count per VRM	Per-Phase controller	Single controller
Maximal phase count	One phase per controller	Up to 14 phases per controller
Flexibility	Made for a specific type of application	Can be adjusted for a wide range of applications
Current sharing	Supported using current share bus	No external bus needed
Calibration	Passive component calibration may be required	Can be calibrated on-the-fly using communication protocols
Number of outputs available	Single output voltage	Can support multiple outputs
Programable AVP	May not support AVP	Supported
Control methods	Linear controller, typically VMC	Linear controller (VMC or CMC) or hybrid controller architecture

1.4. Motivation, objectives and significance of the research program

With the proliferation of cloud computing, the power consumption of data centers has grown significantly. The data center's numerous HPHPLs require a well-regulated dc voltage, under extremely strict requirements and specifications. MPVRM enables low-voltage high-current operation, featuring high power density, high conversion efficiency, and fast dynamic response. MPVRM can be ultimately used to relax the passive components requirements or to further increase the computing power. The conventional setup of a multiphase interleaved buck converter paralleling several phases to power the load. Typically, a single controller IC is employed to oversee the operation of all power stages. This allows better synchronization of the signals, data acquisition with higher signal-to-noise ratio, and saves PCB area.

The primary objective of this research program is to introduce a new high-power high-performance MPVRM that utilize hybrid digital control architecture for optimal transient response for high-end applications.

More specifically, the objectives of the research program are:

1. To improve the load transient response of MPVRMs with the aim of reducing VRM overall volume.
2. Introduce a new digital controller for MPVRM implementing hybrid architecture with a near-ideal transient response.
3. Provide design guidelines and methodology for the design of high-end MPVRM for DDR4 memory and the controller analog interface.

2. Plug-and-Play Optimal Transient Mitigation Control Circuitry for High-Power High-Performance VRM

2.1. Overview

A target feature of high-power, high-performance, VRMs is the ability to maintain a well-regulated, virtually constant, output voltage under wide and rapid load changes while maximizing power density. A key consideration to achieve this goal is an immediate and accurate detection and identification of the load transient.

The objective of this chapter is, therefore, to introduce a plug-and-play circuitry and controller to facilitate time-optimal and minimum deviation control for high-performance VRM under large and rapid load changes. In particular, the control approach is suitable for multiphase buck regulators where the load transient requirements are extremely stringent, the output voltage deviation is primarily resulted by the charge mismatch at the output capacitor, without significant information that can be obtained from the output capacitor's ESR. As presented in Fig. 2.1, the transient suppression unit (TSU) comprises load transient detection as well as its information (signal's extremum point), which extracted directly from the output voltage measurement, without the need for further manipulations neither calibrations of the sensing circuit to comply with the board parameters. This chapter further highlights several practical challenges and constraints that are associated with the signal acquisition in multiphase VRMs, such as differential measurement requirement and hardware bandwidth limitations, a plug-and-play solution of these is delineated as well.

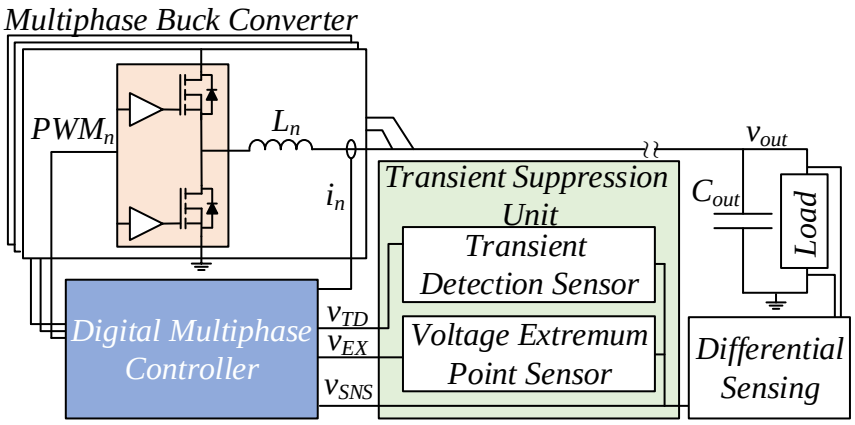

Fig. 2.1 Simplified schematic diagram of a multiphase buck system.

The rest of the chapter is organized as follows: Section 2.2 revises the fundamentals of time-optimal recovery and describes the main challenges in execution of the control. The plug-and-play circuitry and control are thoroughly described in Section 2.3, which also includes a detailed discussion on the practical aspects of the implementation. Section 2.4 details a simulation case study of the controller and is followed by experimental validation on a multiphase buck VRM platform. Section 2.5 concludes the chapter.

2.2. Time-Optimal recovery for high energy loads

In buck converters, TOC achieves minimum voltage deviation within the minimum possible convergence time [57]. These ultimately lowers the overall output capacitance that is required and increases power density. In some cases to lower the peak inductor current without compromising the voltage deviation, minimum-deviation approach [72] is preferred, at the cost of slightly longer convergence time. Both methods employ single on-off cycle and rely on the same information, but with slightly different convergence profile, beyond the charge balance point. To facilitate either method, the following information is required: (a) an indication of load transient event and its direction (the corresponding transistor is turned on), and (b) the time duration from the start of transient until the point that charge balance is obtained. Typical TOC operation can be viewed in Fig. 2.2 (a) which presents waveforms of a single-phase buck converter operation under loading transient event with load variation between two steady-state currents I_{ss} and $I_{ss\text{-}new}$. The transient recovery divides into two main sections, the first section is the initiation of the inductor current ramp up T_0 while the second is the charge balance point, denoted by T_{min}. In a system with non-negligible output capacitor ESR, the actual capacitor voltage v_C differs from the v_{out}. When the inductor current reaches $I_{ss\text{-}new}$, the output capacitor voltage is at V_{min} and the output capacitor charge recovery phase begins.

The recovery phase comprises an extended on-time portion which is then followed by an off phase. This is done to fully recover the capacitor charge balance, which is manifested by output voltage at its original steady-state value at T_{end}. The reminder T_{on} and T_{off}, beyond T_{min} can be expressed as:

$$T_{on} = T_{peak} - T_{min} = (T_{min} - T_0)\sqrt{D}\,, \tag{2.1}$$

$$T_{off} = T_{end} - T_{peak} = (T_{min} - T_0)\left(\frac{1}{D} - 1\right)\sqrt{D}, \tag{2.2}$$

where D is the system average steady-state duty-cycle ratio.

One method to determine the exact location of T_{min} has been presented in [72] by mimicking the output capacitor voltage behavior using R_sC_s network that matches to $R_{esr}C_{out}$ and the sensor is presented in Fig. 2.2(b). This method has been found extremely effective in cases that the ESR is significant such as in single-phase or lower current VRs. It should be noted however that, the circuit of Fig. 2.2(b) requires on-board calibration, which in some cases may be found quite complex. In addition, as in the case on-hand, with high-current multiphase converter, where the effect of R_{esr} is negligibly small, the output voltage equals the capacitor's voltage, and there is a need for an alternative method to obtain T_{min}.

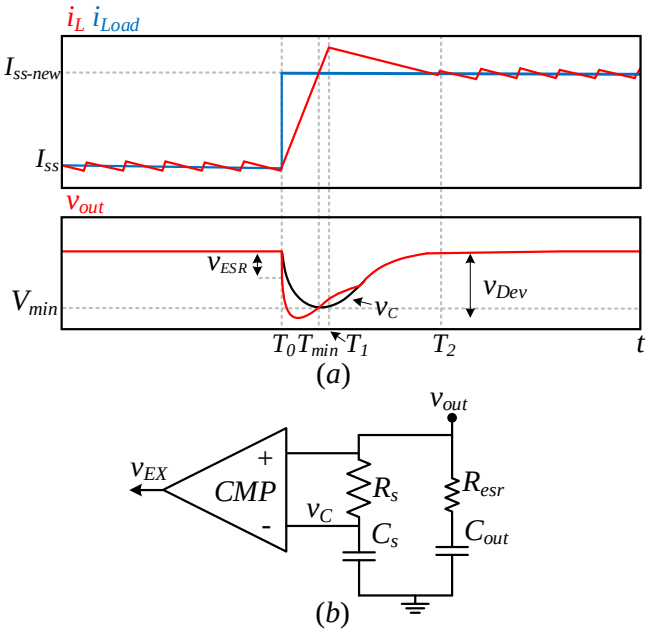

Fig. 2.2 (a) Typical waveforms of Time-Optimal recovery in single-phase buck for loading transient, with the presence of relatively high ESR. (b) Circuit for output capacitor voltage reconstruction and minimum voltage detection.

TOC with multiphase buck VRM further increases the system's transient performance as can be seen in Fig. 2.3. Since the current slew during ramp up is quite steep (due to the high voltage that is applied on the inductor during the on time), charge balance at loading transient is achieved relatively fast and with small voltage drop. Fig. 2.3 demonstrates a more challenging scenario where the system slopes are more moderate. The TOC operation is shown for an unloading transient event in two-phase multiphase buck for two recovery

options. The first option is to force both phases to ramp down together upon detection of a transient event, paralleling the converters operation which results in smaller voltage deviation. The second option is to retain the synchronized operation of the interleaved converters, which comes at the cost of larger voltage deviation. Within the context of this study, which focuses on the detection circuit and aims to support any prescribed transient mitigation scheme, since the voltage maximum point occurs when the summed inductor current reaches the new load current, then the TSU is oblivious to the chosen method.

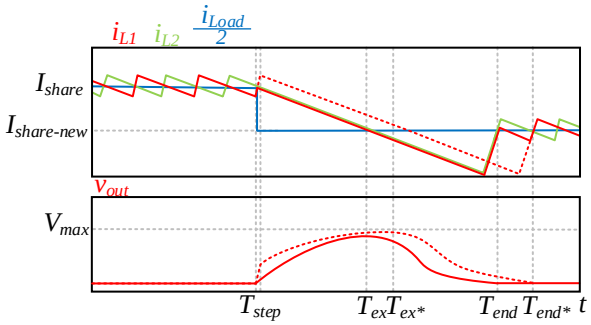

Fig. 2.3 Two phases interleaved buck converter operation with Time-Optimal Control during unloading transient. Recovery patterns for (a) Synchronized operation. (b) Asynchronous, all-aligned ramp down.

2.3. *Plug-and-Play Transient Mitigation Circuit*

In order to facilitate TOC, two timing points are required for the controller, commencing of transient T_0 (and its direction) and the charge balance point T_{min}. In the context of multiphase VRM, the information can be extracted directly from the output voltage signal by evaluation of change in value and extremum point, respectively.

The operation of the transient mitigation circuit is detailed for a case of loading transient (unloading case requires few minor modifications). It identifies the critical points (T_0 and T_{min}) in the absence of output capacitor ESR and does not require calibration to the system's parameters. As can be seen in Fig. 2.4, loading transient is detected at T_0 where v_{SNS} drops below a detection threshold, marked by v_{TDL} goes high, signaling the controller to ramp up the inductors current. This signal also triggers a counter for the duration of T_{min}. The charge balance point T_{min} is identified by the minimum point of v_{out}, stopping the counter by v_{EX} rising edge signal. The minimum point is detected using a valley detection circuits (as detailed later) which is reset slightly after the valley point for preparation for the next transient. Following is specific description of the sensor's hardware for implementation.

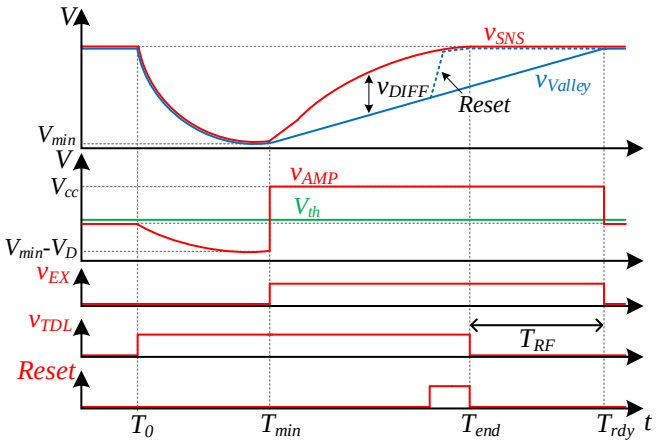

Fig. 2.4 Operation of the transient mitigation unit describing loading transient recovery.

In spread hardware setup as in multiphase supply, the output voltage sensing point can be located a fairly long distance away from the controller, accumulating noise and other potential errors. Therefore, it is quite impractical to sense v_{out} using a single-ended sensor, and the common practice is to use a lengthy differential pair and a differential to single-ended amplifier (Fig. 2.5) to provide the controller with as clean as possible v_{SNS} signal accurately representing the v_{out} signal at it sensing point. The differential to single-ended front-end sensor is realized using an op-amp differential amplifier and a $R_f C_f$ low-pass filter to remove any high-frequency noise that may be added to the v_{out} signal.

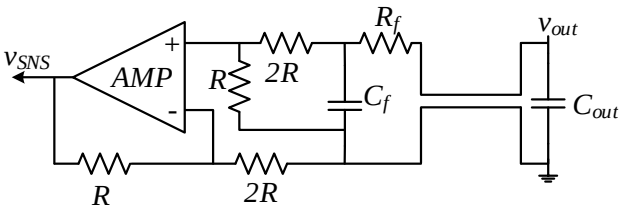

Fig. 2.5 Differential v_{out} sensing to single-ended interface.

Fig. 2.6 and Fig. 2.7 show the tracking window transient detection circuit and its operation waveforms, respectively. During steady-state operation, v_{SNS} is within the steady-state window between the two threshold voltages $V_{th\text{-}H}$ and $V_{th\text{-}L}$. The threshold voltages can be adjusted by selecting different relations between $R_{1\text{-}3}$ according to the system specification. These can be expressed as:

$$V_{th-H} = v_{SNS} \frac{R_2 + R_3}{R_1 + R_2 + R_3}; \tag{2.3}$$

$$V_{th-L} = v_{SNS} \frac{R_3}{R_1 + R_2 + R_3}. \tag{2.4}$$

In many cases, high-performance loads require droop load-line voltage profile, i.e., slightly lower output voltage as the load increases. As a result, the steady-state point of the output voltage changes, and the sensor tracks the average state of the output voltage. This is facilitated through the dependency of $V_{th\text{-}H}$ and $V_{th\text{-}L}$ in v_{SNS} , as expressed in (2.3-2.4), where the thresholds track around v_{SNS} to its new nominal value after transient. While a straightforward approach is to create an even-sized margins v_{mH} and v_{mL}, an alternative option is to space the margins unevenly for better compensation of unloading transients. Ultimately, the threshold voltages are desired to be as close as possible to V_{nom} without false triggering due to the steady-state ripple or any switching noise. Since in such applications, the output voltage ripple is negligibly small, the window width is designed within that range of few mV, excluding any noise.

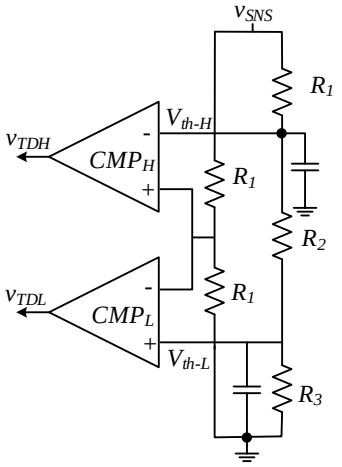

Fig. 2.6 Output voltage tracking window transient detection circuit.

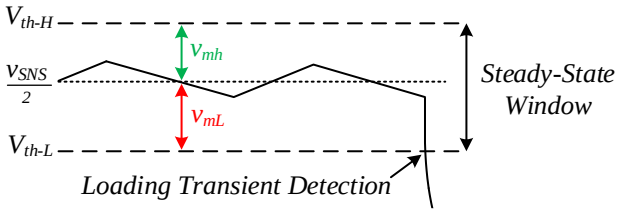

Fig. 2.7 Illustrative waveforms of window tracking and transient detection operation.

The output voltage minimum point V_{min} is sensed by the extremum point sensor showed in Fig. 2.8 and its related waveform shown in Fig. 2.4. At the period between T_0 and T_{min}, v_{SNS} fall below the nominal value, reaching minimum value (V_{min}) at T_{min}. During this time, v_{Valley} (Fig. 2.8) follows v_{SNS}. Once the output voltage reached V_{min}, while the output voltage start to rise back towards V_{nom}, the signal v_{Valley} rises slower, or clamped at its V_{min} value. This difference can be identified via several methods, one is using a difference amplifier,

however, the gain-bandwidth limitation of any difference amplifier renders this method impractical. An alternative approach that has been employed in this study is by looking at the large signal at the peak detector amplifier output, v_{AMP}. In this way, the signal swing is substantial and the transition can be detected by a simple comparator. It should be noted however, that to facilitate fast detection, the peak detector gain bandwidth is of importance, as analyzed by Fig. 2.9. Still this method is of significantly lower complexity and high immunity to noise compared to the former.

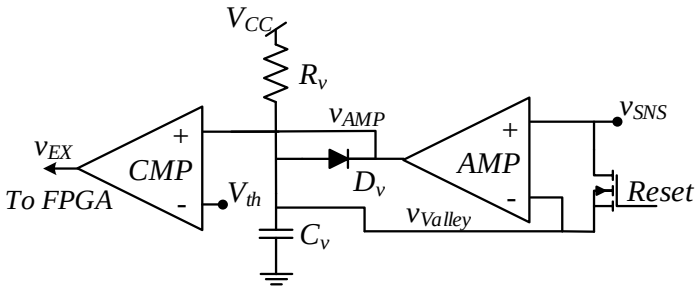

Fig. 2.8 Circuit description of extremum point detection; demonstrated for loading transients (valley point detection).

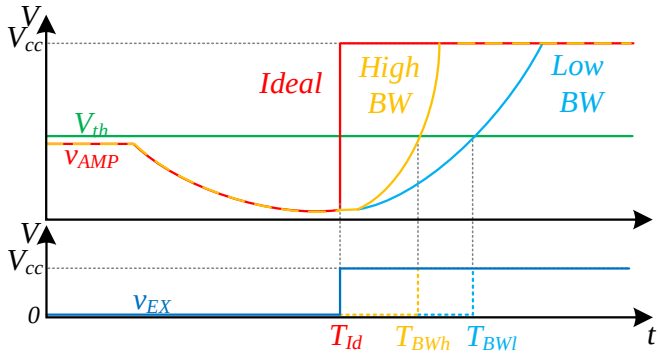

Fig. 2.9 Illustration of the impact of the sensor BW on the detection performance.

To complete the sensor operation and output charge recovery phase the controller can now use T_0-T_{min} when v_{SNS} return to nominal value a refresh time T_{RF} is required in order to allow v_{Valley} to return to v_{SNS} at T_{rdy}. When the refresh phase is complete the sensor is ready for the next transient event. Rapid consecutive transients may occur in high-performance systems, therefore it is essential to reset the detector as soon as the required values are read. The peak detector reset is facilitated by a transistor, pulls v_{Valley} back to v_{SNS} (Fig. 2.4).

Since the accuracy of the time information is essential to satisfy accurate TOC, and since the entire load transition under this scheme is very short, reducing the potential delays and properly defining the sensor's components is of importance. A key consideration is the

bandwidth of the peak detector op-amp. Depicted in Fig. 9 is the behavior of an idealized detection, alongside detection with lower bandwidths. It can be seen that the detection accuracy of the minimum point is proportional to the amplifier bandwidth. Assuming first order response of the op-amp, the delay time, T_{Delay}, can be expressed as:

$$T_{Delay} = 1 - 0.1 \cdot ln(BW_{MHz})[\mu sec], \tag{2.5}$$

where BW_{MHz} is the operational amplifier bandwidth in MHz.

2.4. Simulation and Experimental Validation on Multiphase Buck Converter

The transient mitigation operation has been validated using 12V to 1V four-phase multiphase buck converter on simulation and two-phase multiphase buck for the experimental prototype. The converter parameters are presented at TABLE II. The extremum sensor operation is validation in loading transient event as explained in section 2.3 is shown in Fig. 2.10 using PSIM simulation. A loading transient of 40A (10A per phase) causes the output voltage to drop and enter Time-Optimal transient suppression. The extremum sensor successfully senses the minimum voltage point marked by v_{EX} rising edge. Additionally, Fig. 2.10 shows the reduction in refresh time with sensor reset is showed by $v_{EX\ Reset}$, inducing the minimal time before next transient by T_{RF} of approximately 10µs.

TABLE II. EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	***Value/Type***
Input voltage V_{in}	12V
Average output current $I_{out,AVG}$	10A,35A
Power Stage	SiC620A, 60A
Inductor	1µH
Output capacitance, C_{out}	1.3mF
Switching frequency ,f_{sw}	500KHz
Amplifier bandwidth	100MHz

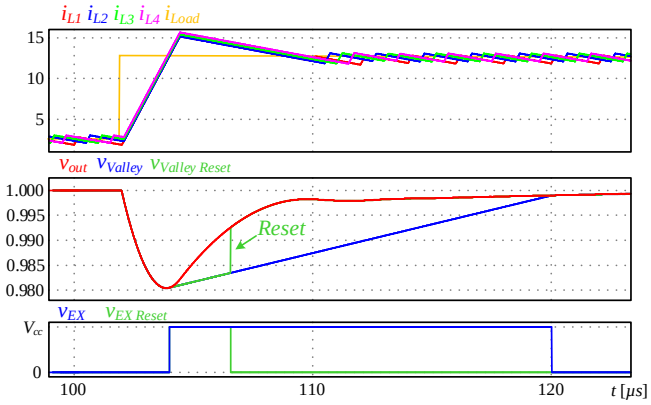

Fig. 2.10 Simulation results of the transient mitigation unit in case of loading transient.

The impact of amplifier bandwidth on the extremum sensor accuracy is shown in Fig. 2.11, comparing different bandwidth influence on the rising of v_{AMP} under the same transient conditions in Fig. 2.10. The ideal case represents the optimal sensor response using unlimited bandwidth amplifier providing zero delay extremum detection, lower amplifier bandwidth provides deviation from the ideal case, which increases sensor's delay. In practice, implemented amplifiers have limited bandwidth because of die area and power-consumption considerations, thus the sensor delay needs to be considered.

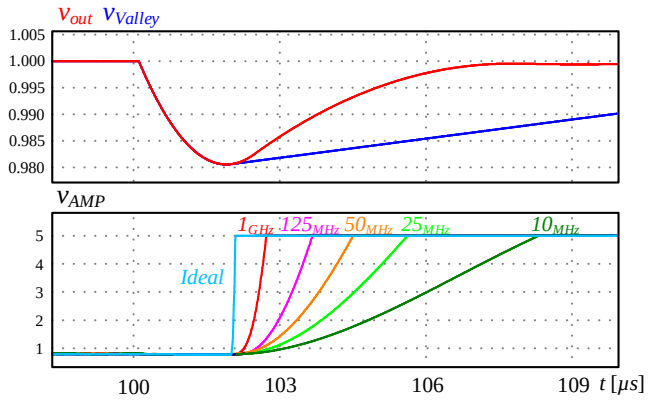

Fig. 2.11 Effect of sense amplifier bandwidth on extremum point detection.

The experimental prototype realized with all the related peripherals and a multiphase controller implemented on Altera Cyclone IV FPGA. Experimental results shown in Fig. 2.12 (a) and (b) demonstrate the operation of the transient mitigation unit executing time-optimal control. Fig. 2.12 (a) shows a loading transient response from 10A to 64A load step. The signal v_{EX} indicates the minimum point as v_{out} and v_{Valley} split. In Fig. 2.12 (b) the inductor's current waveform is depicted for 20A load step, marked on v_{EX} here the period T_{min}-T_0.

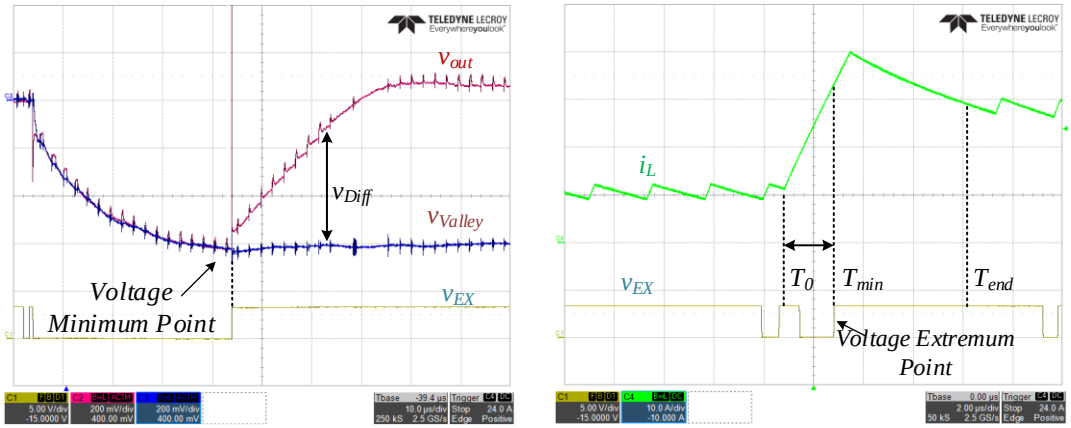

Fig. 2.12 Transient mitigation unit experimental results (a) two-phase multiphase buck converter 10A → 64A loading transient output voltage waveform (b) single phase operation 10A → 30A loading transient current waveform.

2.5. Conclusion

A Plug-and-Play optimal transient mitigation control circuitry for high-power high-performance VRM has been introduced, and verified in simulation and on experimental 12V-to-1V multiphase buck prototype. The new TSU provides all the necessary information for successful TOC operation in near ideal remotely sensed high-performance systems with non-quantifiable ESR. The TSU does not require on board calibration and accommodates any number of either interleaved or paralleled phases.

3. Digital Controller for High-Performance Multiphase VRM with Current Balancing and Near-Ideal Transient Response

3.1. Overview

With the proliferation of cloud computing, power consumption of datacenters has grown significantly [1]. Datacenters typically use a large number of CPUs and DDR memory modules, each requires a well-regulated dc voltage, under extremely strict requirements and specifications. The predominant solution to sustain and satisfy the high current load requirement is phase paralleling and/or interleaving of multiple lower power converters. The distribution onto multitude of converters is done to achieve higher steady-state efficiency (by optimization of components to the operating conditions as well as advanced current sharing features) [46]-[51], increase the overall power density with utilization of smaller magnetics [63]-[65], and accommodate the extremely demanding requirements of load transient without significant increase of the output capacitance [66]-[68]. Since a multiphase solution inherently dictates spread hardware and distributed sourcing of the load, transient mitigation, and in general the load management, have become more complex on concept as well as the practical implementation.

The objective of this study is therefore to introduce a new all-digital controller for high-performance multiphase buck VRM as shown in Fig. 3.1. The new controller includes current balancing modules that enable even load distribution between the phases. The outer voltage regulation loop encompasses a linear compensation for steady-state and small deviations, along with a large-signal transient suppression unit to mitigate large change in the load. In addition, a higher-level system governor overseas tasks of phase balancing, synchronization, load sharing and phase shedding. It is a further objective of this study to present in detail a new controller implementation that enables time-optimal transient recovery in multiphase regulators.

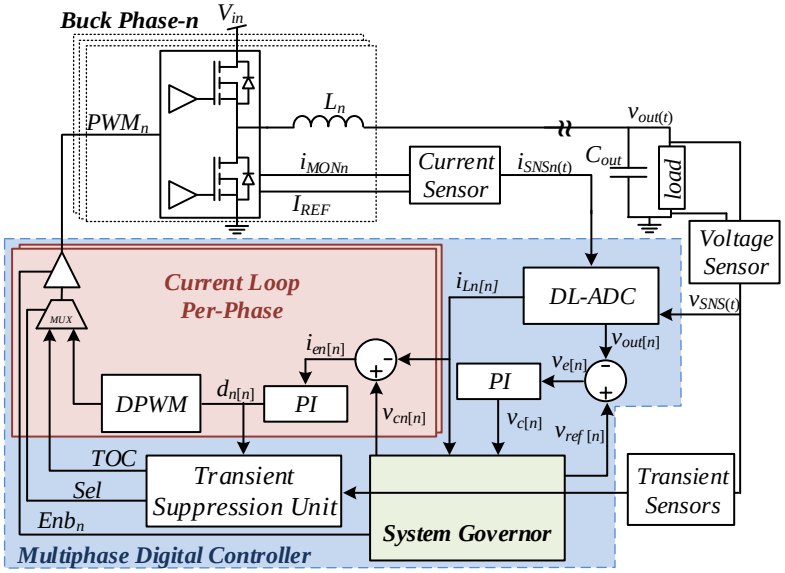

Fig. 3.1 Simplified schematic diagram of a multiphase buck system.

The chapter is organized as follows, Section 3.2 describes the new controller architecture and its principle of operation, Section 3.3 delineates the large-signal compensation scheme. Practical implementation aspects and details of the system governor are provided in section 3.4. Experimental validation is carried out in section 3.5. Section 3.6 concludes the chapter.

3.2. Controller architecture and principle of operation

The multiphase buck VRM controller that has been developed in this study and illustratively presented in Fig. 3.1 consists of two main control units, a small-signal ACM controller and a large-signal transient suppression unit (TSU) incorporated together into a hybrid controller architecture [57]-[62],[69]-[76]. Each controller is designed for superior performance within its control law operation. The TSU is designed to accommodate large load changes and utilizes a nonlinear, state-variable based recovery pattern to accomplish the best possible transitioning from one loading condition to another. The small-signal controller is structured around a current-programmed linear compensation scheme and operates in fixed-frequency PWM. By doing so, it enables simpler design of the power stage, and more importantly high steady-state accuracy can be achieved as well as high static efficiency, and good thermal distribution between the phases, which is important in the context of multiphase converters. Forming this type of hybrid controller structure provides flexibility, where the tasks are separated between the compensators. Load transients are remedied with time-optimal or minimum-deviation patterns, utilizing the advantage of

paralleling phases to expedite the recovery process. The design of small signal linear compensator, encompasses minimum dc error, accuracy, and current sharing. This arrangement provides simplification of the design, and at the same time steady state features are retained and significant improvement in transient mitigation is achieved by the TSU. It should be noted that by defining the task of the transient controller to bring the state variables from the old state to the vicinity of the new state, while the task of the linear control remains regulation, the issue of the controller stability is inherently resolved and can be examined by conventional tools, such as Nyquist, or phase margin test [77]-[79].

Sensing diagram that is required to facilitate the hybrid controller is schematically detailed in Fig. 3.2 This is an important interface for any high-performance VRM and particularly in multiphase applications, since reliable acquisition of circuit parameters is pivotal for issues of accuracy, rapid timing, sensitivity to changes, and accommodating noise and other disturbances. The practice employed in this study, as can be seen from Fig. 3.2, is to employ a differential-type acquisition of the state-variable signals. By doing so, the distance from the measurement point to the controller front-end is compensated. Once the signal is obtained, it is further manipulated according to the required task (regulation, detection, information, etc.). Average value readings, i.e. one sample per cycle readings, such as information of the output voltage and the current of each phase, are processed by the steady-state controller. Continuous signal information of the output voltage is further manipulated by the TSU.

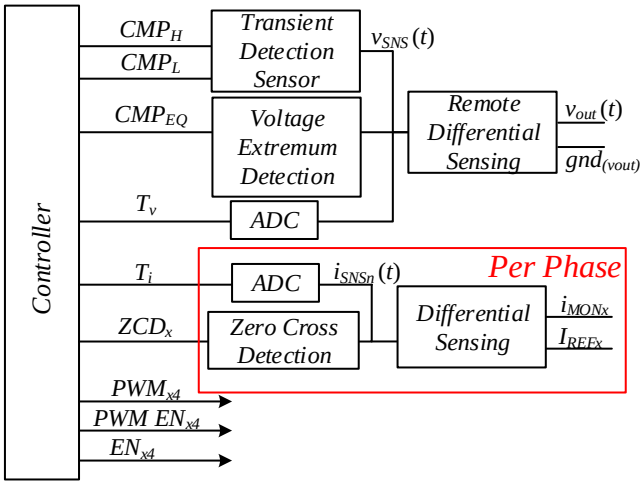

Fig. 3.2 Schematic illustration of the sensing scheme for multiphase controller operation.

A fundamental challenge of multiphase architectures is the parallel connectivity of multiple power stages and the need to adequately distribute the efforts between them while maintaining a well-regulated voltage at the output. This mandates some form of current or load sharing protocol. In this study, average current-programmed mode (ACM) control for the operation of the steady-state compensation scheme has been pursued as can be seen in Fig. 3.3(a). Under the assumption that the control bandwidth of the current loop is sufficiently wider than that of the output voltage, the individual power stages that feed the output capacitance can be treated as controlled current sources as in Fig. 3.3(b). This enables multiple converter phase paralleling, simple adjustment of the phase currents, and therefore current sharing. Equal currents eventually result in even thermal distribution between the phases at no additional cost, which is important to multiphase applications.

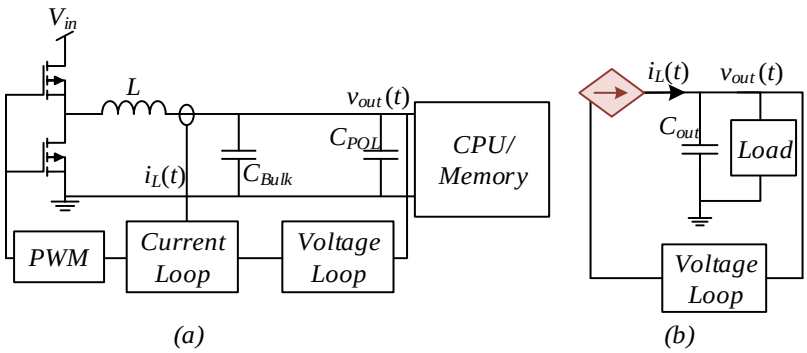

Fig. 3.3 Dual loop ACM buck VRM (a) current-controlled buck converter (b) equivalent diagram.

Additional important feature of multiphase controllers required by the load due to the thermal restrictions when operating at high current [80], is active voltage positioning (AVP). A typical droop curve that represents the target $v_{out}(t)$ level as a function of the load current $i_{load}(t)$ is shown in Fig. 3.4. The output voltage level reduces as a linear function of the load current where V_{VID} defines the nominal output voltage at no-load conditions, and V_{min} is the required voltage at I_{max}. Droop control is implemented by shifting down the target reference voltage with load increase, and can be expressed as:

$$v_{ref}[n] = V_{VID} - R_{VID} \cdot i_{sum}[n], \tag{3.1}$$

where $v_{ref}[n]$ is the voltage loop reference, V_{VID} and R_{VID} are the user selected AVP parameters to fit the desired V_{VID} curve, and $i_{sum}[n]$ is the digital value of the total converter current. It should be noted that in order to avoid oscillations at the output and since the droop

relates to the steady-state voltage level only, its bandwidth is significantly lower than the response of the voltage control loop.

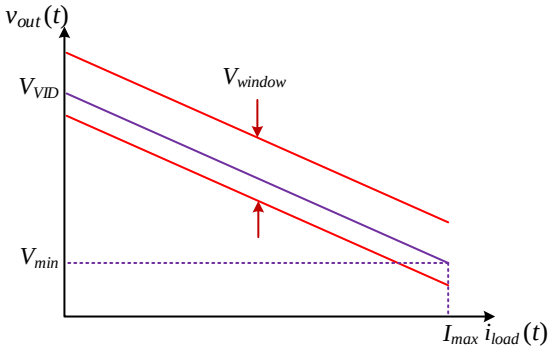

Fig. 3.4 Active voltage positioning VID curve required in high-end loads.

The principle of operation of the ACM controller is described with the aid of Fig. 3.5 and Fig. 3.6, which show the conceptual block diagram of the ACM controller and its timing sequence diagram during steady-state operation respectively. Since this study focuses on all-digital implementation of the controller, the description is carried out with sample-data domain notations. The voltage loop creates a digital reference $v_c[n]$ for the inner current loops based upon the error signal $v_e[n]$ as given in (3.2):

$$v_e[n] = v_{ref}[n] - v_{out}[n], \tag{3.2}$$

where $v_{ref}[n]$ is the AVP generated reference and $v_{out}[n]$ is the sampled output voltage. The current error $i_e[n]$ is then calculated per-phase using the sampled average inductor current $i_L[n]$ of each phase. The current error $i_e[n]$ used as the input for the current loop compensator, which generates the duty command for the DPWM module $d[n]$, and a pulse width modulated signal $c(t)$ is formed.

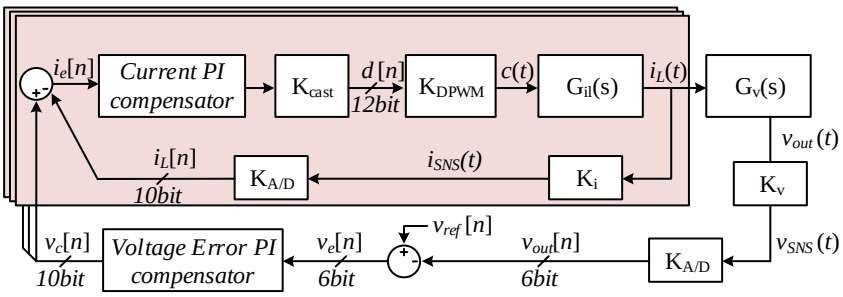

Fig. 3.5 Conceptual block diagram of the multiphase buck ACM control system.

In the classic approach for ACM control, the samples of $v_{out}[n]$ and $i_L[n]$ (Fig. 3.5), are sampled in a successive manner so that the resources of high-performance hardware such as

ADC units can be shared, to save on power consumption and area. Furthermore, it is a common practice to position the sampling events away from switching actions to increase the measurement signal-to-noise ratio. In interleaved multiphase systems however, switching events are scattered along virtually the entire switching cycle T_s and become more frequent with the number of phases, resulting in limited time slots suitable for data acquisition. To overcome this obstacle, this study formulates a unified data acquisition sequence that synchronizes per-phase measurements and gains the benefit of increasing the number of allowed interleaved phases to be limited by the acquisition time alone. Since the realization of the ADCs hardware in this study is carried out by delay-lines and combinatorial circuits as previously described in [81], the hardware penalty per phase is negligibly small.

A timing sequence diagram for the ACM controller is presented in Fig. 3.6, where $v_{out}[n]$ and $i_L[n]$ are both sampled at the same time. To utilize the enhanced bandwidth option of multiphase operation, the reference $v_c[n]$ signal is updated by the voltage loop compensator, the relevant phase duty command $d_n[n]$ is generated by the individual current loops and updated to its DPWM port at the beginning of each phase. By sampling $v_{out}[n]$ and $i_L[n]$ simultaneously at a fixed location within T_s, the timing logic in Fig. 3.6 can be duplicated and applied to accommodate any number of phases, limited by the data acquisition capabilities of the controller hardware.

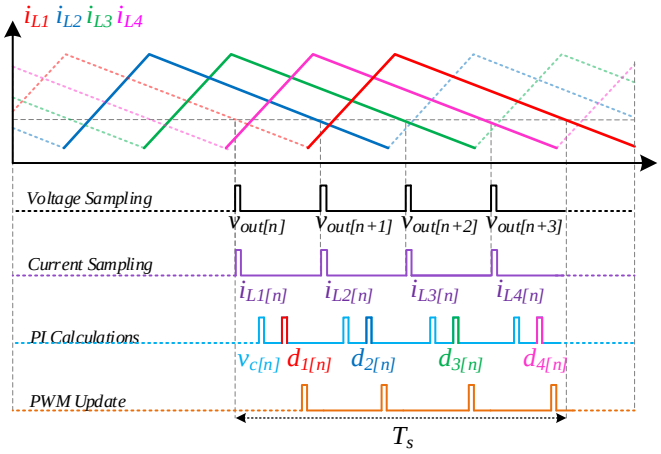

Fig. 3.6 Multiphase ACM controller timing sequence diagram of key blocks, during steady-state operation.

Small load changes, defined within the range of the inductor current ripple (approximately 30% of the rated current) do not trigger the operation of the TSU and are accommodated through the steady-state compensation. Fig. 3.7 shows a typical response of the linear controller to a loading transient with four-phase operation (results obtained from PSIM

simulation). Prior to the point t_{step} the controller is in steady-state, where each phase provides I_{low} to the output, sharing the load equally. At t_{step} the load changes so that each phase is required to carry I_{high}. Zoomed-in frame in Fig. 3.7 shows that the load step takes place between switching cycles of two adjacent phases. The small-signal compensator responds to the transient event immediately as the next closest phase cycle begins, at t_{update}. This is a much quicker response than the conventional practice, where the controller waits for a full switching cycle to complete. During the transient period, and under any transient conditions the ACM architecture of the small-signal compensator maintains current sharing between the phases, reducing the current sharing convergence time to zero, and the output current is fully shared when the system is back to the steady-state operation.

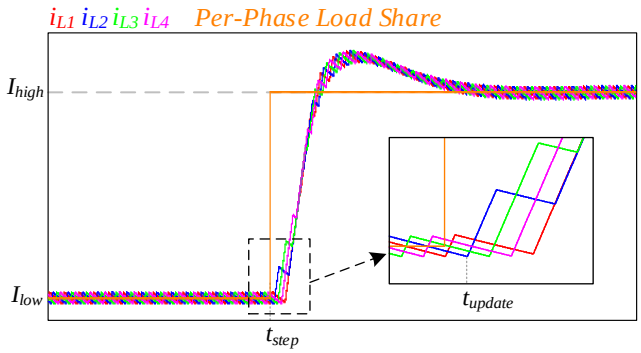

Fig. 3.7 Loading transient recovery of four phases interleaved buck converter controlled by linear compensation scheme.

3.3. Large-signal Compensation Scheme

Hybrid controller architecture facilitates a large-signal recovery pattern to suppress extreme transient events which exceed the regulation capabilities of the linear, small-signal compensator. Effectively, the limitations of the transient-oriented controller are the slew-rate imposed by the passive components, and the delays of the system (detection, calculation etc.) [62],[83]-[86]. Typical waveforms of transient recovery are depicted in Fig. 3.8 (obtained by PSIM simulation), demonstrating a loading transient event, followed by an unloading transient event as the load changes between the values of I_{low} and I_{high} respectively. The details of the transient and extremum detection sensors as used in this study are shown in section 2.3, and are based on [82].

Prior to the first transient event, the output voltage is within the steady-state window defined by $V_{th\text{-}H}$ and $V_{th\text{-}L}$ (Fig. 3.9 (a)) and controlled by the steady-state controller. At the

time of t_{load} the load increases to I_{high} and the output voltage decreases, which triggers CMP_L. Past this point, the operation of the steady-state controller has been halted, the large-signal compensator takes over the control of the gating outputs and forces all available phases to turn on. The time duration (T_0) between transient beginning and the point of output charge balance, is measured using a counter. The charge balance point manifested at the output voltage as an extremum point. Given that T_0 is attained by the controller the rest of the operation can be completed with a single on-off switching cycle as demonstrated in [57]-[70], to fully recover the output voltage back to its nominal value. In the unique case of loading transient, where the small inductors greatly increase the total system current slew rate producing faster transient response and virtually no voltage drop at the output, a minimum deviation approach can be implemented instead of the full TOC operation. Beyond this point, the control is returned back to the steady-state controller that maintains the operation at the new steady-state conditions.

In opposite to the loading transient event, the case of unloading transient present a more challenging task due to the low current slew rate which prolongs the transient recovery time. The result of the current slew rate mismatch is shown in Fig. 3.8 as the voltage overshoot caused by the unloading transient v_{max} is far greater than the voltage undershoot v_{min}, therefore a longer off time is required to bring the output voltage back to its nominal value. In some cases, the output capacitor is actively discharged by the multiphase VRM as the inductor currents turn negative to further induce the transient mitigation process. The output capacitor current i_{cap} shown in Fig. 3.8 can also demonstrate the differences between the two transients as the charge loss during loading transient Q_{loss} is recovered quickly in comparison to the injected charge Q_{inj} in the unloading transient case.

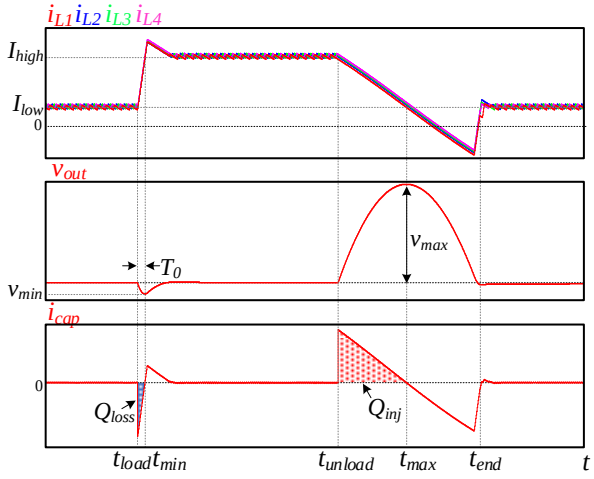

Fig. 3.8 Large-signal compensation waveform during loading and unloading transient events.

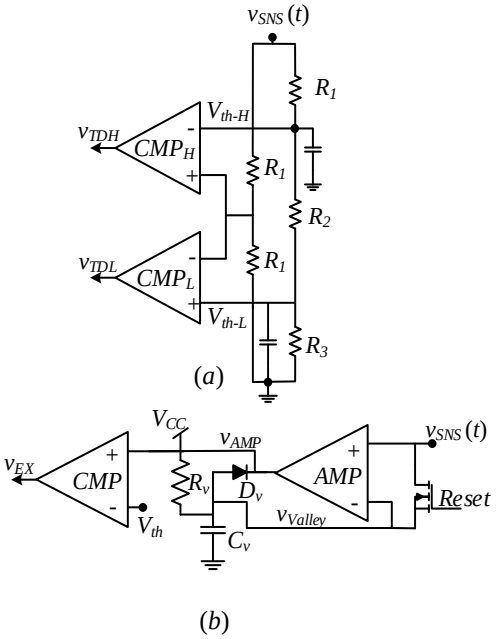

Fig. 3.9 Large-signal compensation sensors (a) transient detection sensor (b) output voltage extremum point detector (minimum).

The current ramp up/down phase in the large-signal compensation can be implemented with different levels of phase synchronization during transient. Fig. 3.10 shows three options for ramp-up initiation with and without phase synchronization, each with its pros and cons. The first option in Fig. 3.10 (a) maintains phase synchronization while also addressing the transient with the closest phase available upon detection, in this case the dashed line phase continues its ON state immediately upon transient detection. The second option in Fig. 3.10 (b) is to maintain full phase synchronization during transient when each phase is turned on at the beginning of its next cycle respectively. The third option is to turn all available phases as soon as transient event is detected, as a result, this method presents the poorest phase synchronization, nevertheless the transient performance is superior in comparison to the first two methods. When looking into the current sharing attribute during transient time the latter option maintains good current sharing, while the worst current mismatch possible is according to the size of the current ripple.

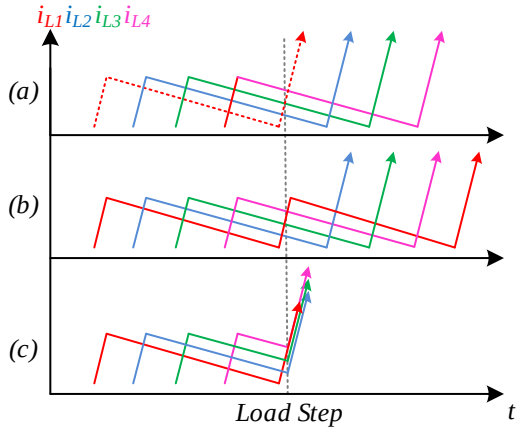

Fig. 3.10 Phase synchronization during transient current ramp up.

In this study the method described in Fig. 3.10 (c) is chosen due to the fastest transient performance as well as current sharing attributes. Another advantage of this method is that during a transient event, the system can be treated as a one single phase buck, with effectively increased bandwidth and with effective inductance of L_{eq}, given by $L_{eq}=L_{ind}/N$ (N represents the number of active phases).

3.3.2. State-Space trajectories

When treating the multiphase converter as single phase buck the state-space trajectories can be easily extracted as shown in Fig. 3.11. The dashed lines mark the OFF state trajectories, and the ON state trajectories are rendered as the vertical straight lines because of the small inductor size and large output capacitor. The loading transient between the two steady-state current of I_{low} and I_{high} is marked with the bold dashed line in Fig. 3.11, the loading transient can be completed with a single on cycle and during that time the output voltage remains virtually constant, therefore the full TOC operation can be reduced to a minimum deviation approach without extending the recovery time. Dissimilar to the latter, the unloading transient response between I_{high} and I_{low} include the full TOC approach starting with a long OFF state which can be completed with negative inductor current, followed by short ON state to return the system to I_{low} in the shortest possible time. The operation for both loading and unloading transients is verified experimentally in section 3.5.

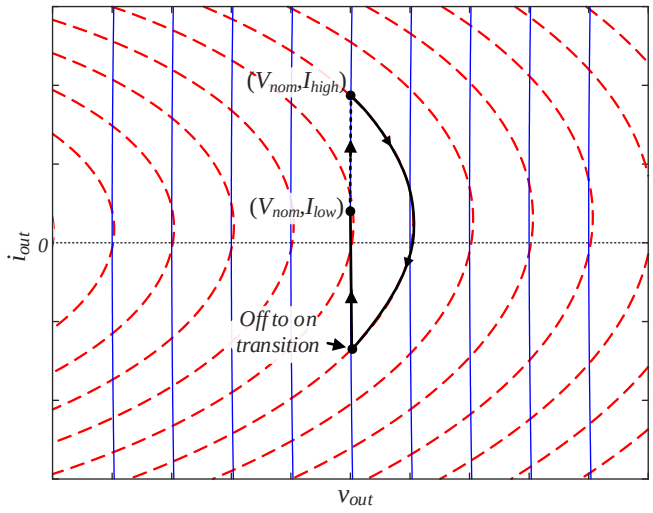

Fig. 3.11 State-space trajectories of multiphase buck in loading and unloading transients.

3.4. Practical implementation aspects and System Governor

3.4.1. System Governor

In addition to the regulation requirements carried out by the hybrid architecture, and described in previous sections, state-of-the-art multiphase controllers are required to accommodate high-performance loads with additional features like AVP and Fault management. In this study, the additional features are carried out by the system governor unit shown in Fig. 3.12. The system governor collects information of the following system variables: input voltage $v_{in}[n]$, output voltage $v_{out}[n]$, temperature $temp[n]$, and inductor currents $i_{Ln}[n]$. Using currents $i_{Ln}[n]$ the total inductors current $i_{sum}[n]$ is calculated every cycle. The AVP function, presented in section 3.2, can be calculated using the total inductor current to dynamically adjust the voltage loop reference $v_{ref}[n]$ (Fig. 3.12). It is done to reduce the converter output voltage in high-currents operation.

An additional important feature carried out by the system governor is dynamic phase shedding. By changing the number of active phases during steady-state operation according to the loading condition, the overall converter efficiency can be further increased. The dynamic phase shedding is performed using the phase count optimizer (PCO), sharing control, and phase enabler are shown in Fig. 3.12. During a long steady-state operation, the PCO compares $i_{sum}[n]$ with a user-selected thresholds table to decide the N value, number of active phases, to the existing loading condition. In high output current operation, more

phases are needed, so N is increased, the phase enabler determines the relevant phase to be turned on by controlling the phase tristate output buffer (Fig. 3.1). After the phase has been enabled, the sharing control adjusts the relevant phase duty command to integrate the phase. This is done in a slow controlled fashion to prevent the system from going into transient during phase insertion. In low current operation, the phase is shed out by the sharing control unit before it is disabled by the phase enabler when the phase current reaches zero. During the transient event the phase shedding feature is disabled by the *All-on* signal form the TSU and force N to be changed to its maximal value, this is done to use all the available phases during transient assuring the best transient response.

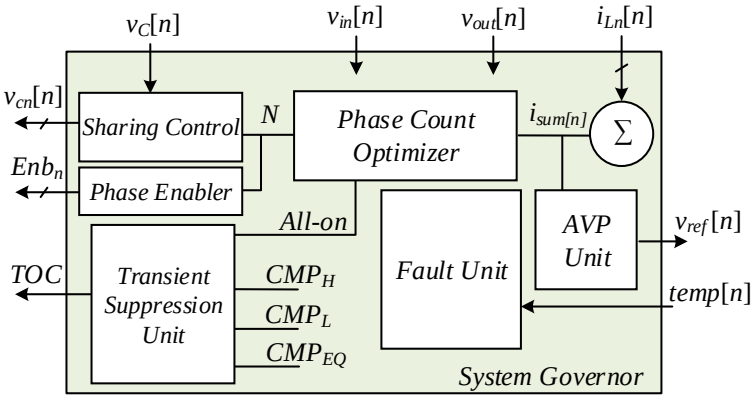

Fig. 3.12 System governor block diagram.

3.4.2. Single DL multiphase DPWM module

Practical implementation of multiphase systems suffers from any imbalance between the different phases impacting the current sharing quality. A DPWM model based on multiple DL realization, especially on an FPGA custom designed modules, can introduce non-identical PWM signals for two different phases under the same duty command. The signal DL multiphase DPWM realized in this study as shown in Fig. 3.13 is based on a single DL ring oscillator to generate the PWM signal to all the phases. Given a duty command $d_n[n]$ a $c_n(t)$ signal is generated using the DL ring oscillator and the duty cycle logic. The single DL design cancels out the system sensitivity to both synthesis and silicon level differences between multiple modules. In the presence of very small inductors and very large output capacitance in multiphase systems, a soft start unit is essential to prevent any startup current or voltage overshoots and bring the system into the steady-state thresholds. The soft-start

unit is incorporated into the DPWM module (Fig. 3.13) and provides a power good indication after the soft start process is complete.

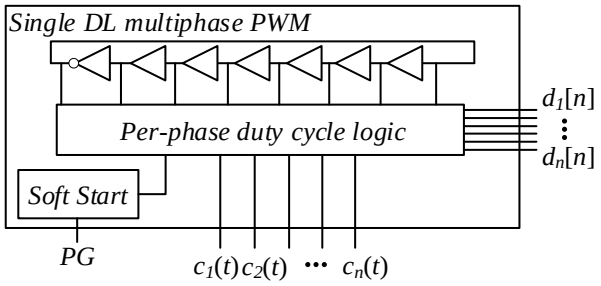

Fig. 3.13 Single DL multiphase DPWM module with built-in soft start unit.

3.5. Experimental Validation on Multiphase Buck Converter

The multiphase buck VRM controller operation has been validated using a 12V-to-1.xV four-phase multiphase buck converter, an experimental prototype with all the analog front-end peripherals has been built and tested. The converter parameters are shown in TABLE III. Fig. 3.14 shows the experimental prototype setup, which comprises a specifically designed PCB to supply DDR memory, digital controller realized on FPGA, and an Intel-certified DDR4 load emulation modules. Each DDR4 module capable of sourcing or sinking up to 14A and the gating signal pattern is generated by a signal generator, asynchronous to the controller operation. The load slew-rate utilized in the experiments is 1000A/µs. The digital hybrid controller architecture, system governor, and custom-made peripherals such as the DL-ADC and single delay-line multiphase PWM has been entirely implemented on a Cyclone V FPGA.

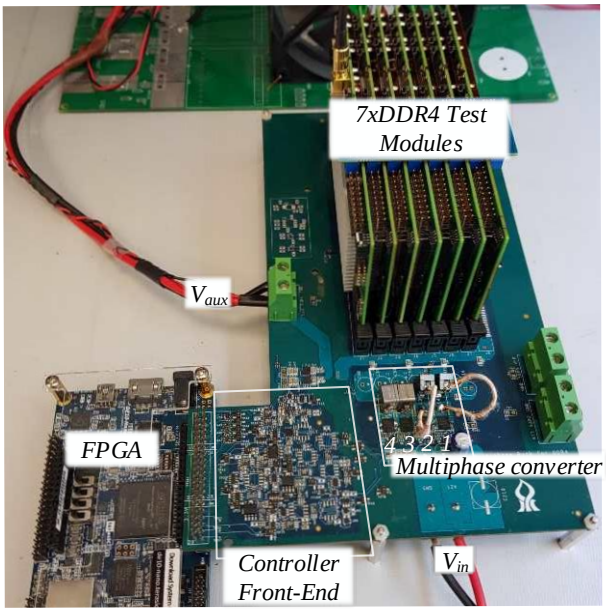

Fig. 3.14 Four-phase multiphase buck VRM experimental setup, including all the front-end peripherals and seven DDR4 test modules.

TABLE III. EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	***Value/Type***
Input voltage V_{in}	12V
Maximum Phase Count	4
Power Stage	SiC820, 70A
Inductor	120nH
Output capacitance, C_{out}	5mF
Switching frequency, f_{sw}	900KHz

Fig. 3.15 shows the transient response handled by the small-signal compensator of a loading transient event from 16A to 88A. i_{L1} and i_{L2} represent the inductor currents of phase 1 and phase 2 respectively, stepping up from the average current of 4A each to 22A each as the load changes. The output voltage at the load point is denoted as v_{out} and shows a maximal voltage deviation of 350mV and a full recovery period after 220µs. The small-signal controller maintains current sharing between the phases for the entire transient mitigation period.

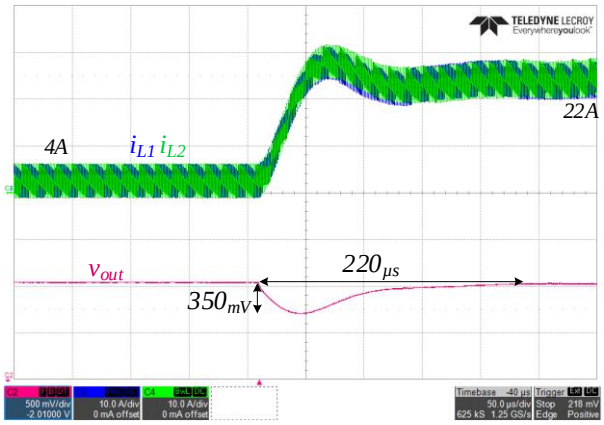

Fig. 3.15 Small-signal compensator operation during a 16A → 88A loading transient event.

In Fig. 3.16 the large-signal compensation scheme is activated to mitigate a loading transient event from 16A to 88A. Here, the controller realizes minimum-deviation recovery profile with output voltage v_{out} deviation of 30mV and recovery to steady-state within 12µs. TSU operation demonstrates excellent current sharing during transient and during the transition back to the steady-state controller.

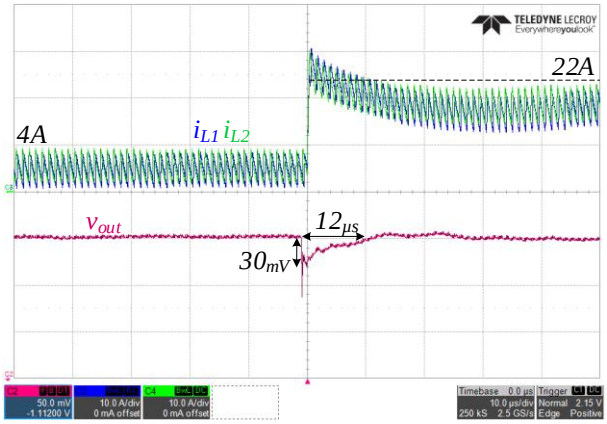

Fig. 3.16 Large-signal compensator operation during a 16A → 88A loading transient event.

The unloading transient case is demonstrated with an 88A to 24A load step as shown in Fig. 3.17 (small-signal compensation) and Fig. 3.18 (TSU). While the overshoot obtained by the linear compensation scheme is measured at 360mV and recovery within 300µs, the transient-oriented recovery resulted in 43mV with recovery time of 7µs.

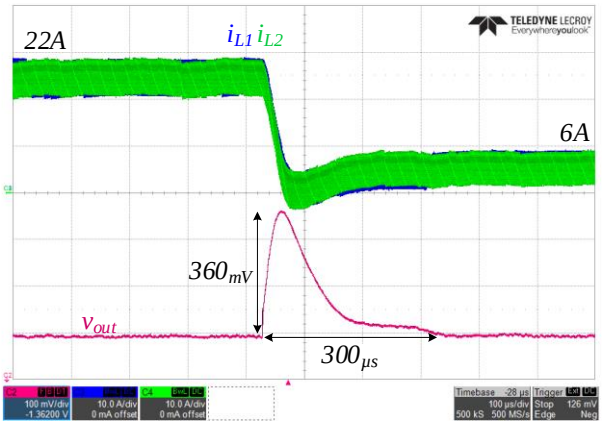

Fig. 3.17 Small-signal compensator operation during an 88A → 24A unloading transient event.

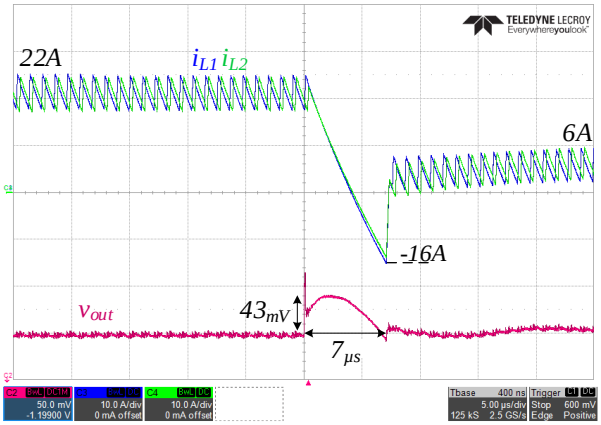

Fig. 3.18 Large-signal compensator operation during an 88A → 24A unloading transient event.

3.6. Conclusion

A digital hybrid controller for high-performance multiphase buck VRM has been demonstrated using a four-phase experimental prototype and a DDR4 emulation test modules. The hybrid controller architecture incorporates two main control laws, a per-phase ACM controller with current sharing capabilities for steady-state and minimized steady-state error, and a TSU for optimal load transient response. Control features such as phase shedding and AVP are implemented in the system governor to facilitate the efficiency and regulation requirements of high-performance loads like CPUs and DDR memories.

The experimental 12V-to-1.xV prototype has been validated using Intel-certified load emulator and demonstrated optimal transient mitigation capabilities of the TSU under extreme transient conditions. Both the ACM steady-state controller and the TSU show excellent current sharing attributes during the entire operation of the controller.

4. MPVRM design and practical implementation for DDR4 memory

As presented in the previous chapters the modern MPVRM need to address wide variety of challenges from minor housekeeping duties up to extreme transient performance. In order to support all the MPVRM functions and enabling cutting-edge performance this chapter introduces a design guideline for a high-power four-phase MPVRM for DDR4 memory (Fig. 4.1).

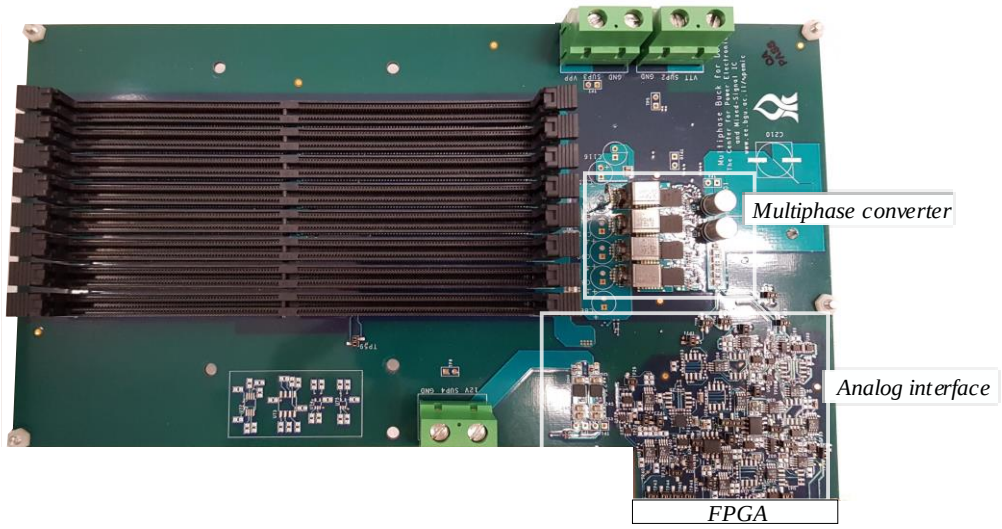

Fig. 4.1 MPVRM PCB with a four-phase converter and analog peripherals.

4.2. Multiphase buck converter design

The multiphase buck converter design is highly impactful on the overall power-quality of the VRM. Correct PCB setup and performance-oriented layout of the converter power-path provide the MPVRM the best platform for high-efficiency operation during steady-state as well as excellent transient performance.

The first step to the design process is to set-up the PCB cross-section, Fig. 4.2 show the cross-section of 12-layer (overall thickness: 74.6_{mil}) PCB (Fig. 4.1) where the layers divide into two main groups, the power planes layers (blue and yellow), routing layers (green) and dielectric layers (gray). All copper layer's thickness is 1.2_{mil} except for the central power planes which are doubled to 2.4_{mil}. The power planes are used to transfer power to the load and to other components on the PCB such as sensors or power stages. Power layers are exposed to a lot of different noise sources such as switching noise, therefore the control

traces should be kept off these layers as much as possible. The external layers (1 and 12) operate as a mixed layer that contains both power and control signals.

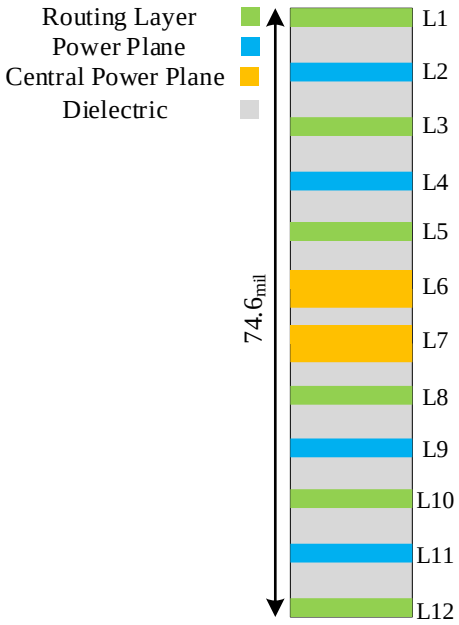

Fig. 4.2 MPVRM 12 layer PCB cross-section and overall thickness.

After all the design layers are set up the next stage is planning the core of the MPVRM which is the four-phase multiphase buck converter. Fig. 4.3 shows the top layer view of the multiphase buck converter layout, the red plane is the v_{out} plane, the blue planes are ground planes and the purple planes are the V_{in} plane. In this work each buck converter (PS1-4) can operate fully on its own with all the required per phase peripheral components, this approach provides a more flexible converter with increased redundancy in case of malfunction.

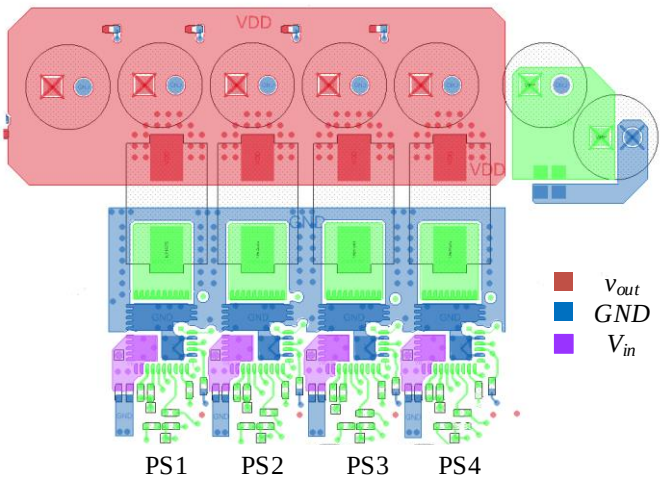

Fig. 4.3 Four-phase multiphase buck converter layout (L1 layer view).

4.2.2. Power stage

The integrated power stage chosen in this work is the 12V to 1.xV optimized Vishay's SiC820 [87]. The SiC820 provide high current capability of 70A as well as live I_{MON} current monitoring. Current monitoring reduces the need for complex and inefficient current measuring methods such as DCR sensing or using a serial resistor which can damage efficiency in high current applications. Fig. 4.4 and Fig. 4.5 show the layout of the SiC820 on top and bottom side respectively, the SiC820 are placed as close as possible for each other, primarily for a space conservation to minimize the converter PCB area and secondly to provide each phase with the same conditions as its adjacent phases. Moreover, each phase layout is identical and therefore can be easily replicated for additional phases.

Important pointers for power stage layout:

- Make switching node planes as small as possible and in proximity to the SiC820 switching node
- Place two high-speed (X7R) capacitors at C_{in} as close as possible to the v_{in} pins of the SiC820 (Fig. 4.4) to minimize parasitic inductance, further capacitance may be placed at bottom side
- Tightly connect logic ground and power ground of the SiC820 together as shown to prevent unwanted current loops
- Always add a series resistor to the bootstrap capacitor C_{Boot} for current limiting if required
- Tie bottom and top ground planes together with multiple via under the SiC820 and around the inductors
- Place R_{DRV} in Fig. 4.5 between the C_{DRV} and the 5V supply to reduce noise into the logic circuit of the SiC820

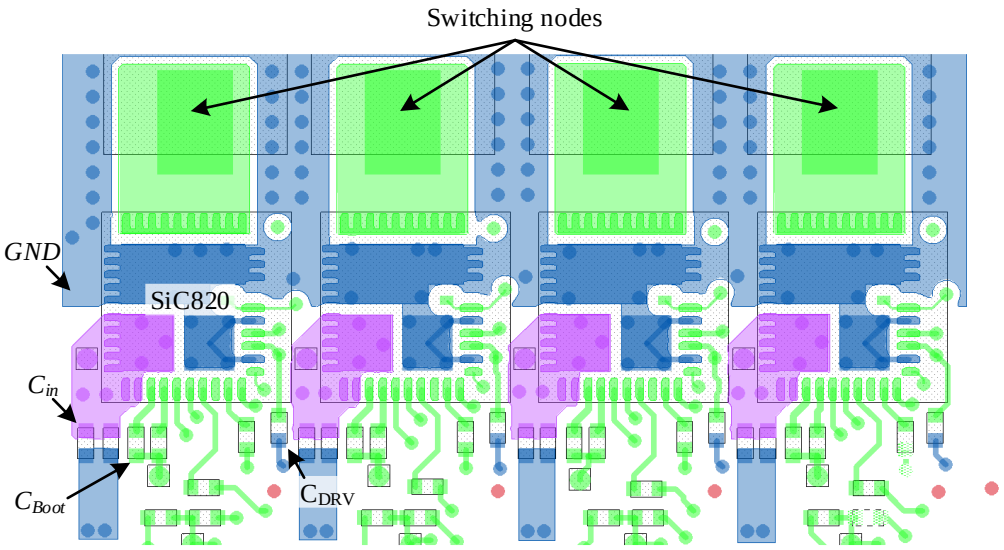

Fig. 4.4 Multiphase buck converter power stages layout top side view.

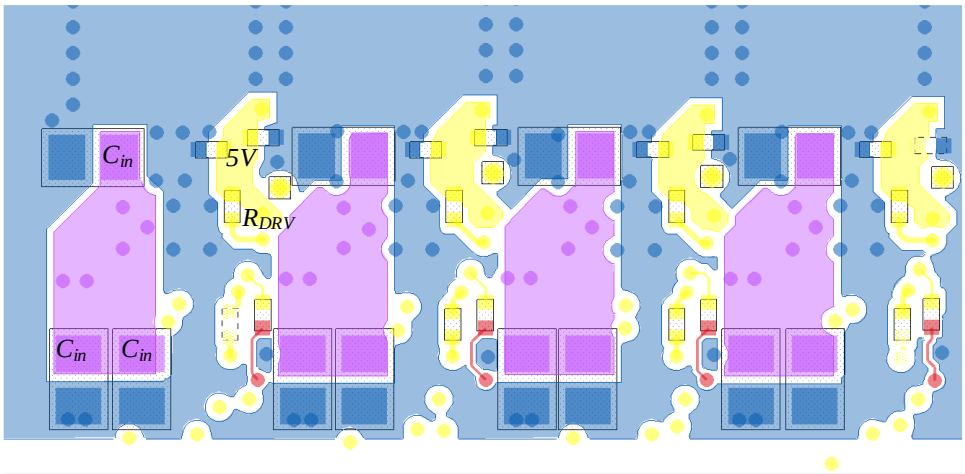

Fig. 4.5 Multiphase buck converter power stages layout bottom side view

4.2.3. Output voltage power plane

The output voltage plane and the output capacitors located across the plane, provide the power for the DDR memory. During transient events at high slew rate loads, the transition time between two loading condition is above the converter bandwidth, therefore the only immediate energy source for the load are the ceramic high-speed output capacitors.

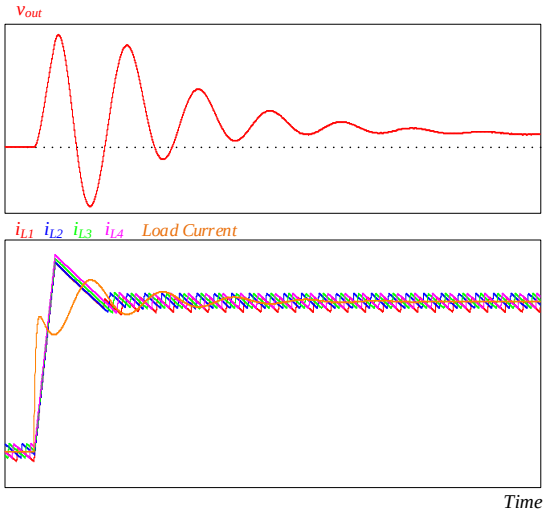

Fig. 4.6 Output voltage oscillations in simulation due to parasitic inductance between the output capacitor and the load.

Fig. 4.6 demonstrate the impact of parasitic inductance between the output capacitor to the load during a transient event. The output voltage oscillation may exceed the load regulation requirements; therefore, it is crucial to minimize the parasitic inductance by using large power planes and evenly distribute the output capacitors in proximity to the DDR power pins that are shown in Fig. 4.7.

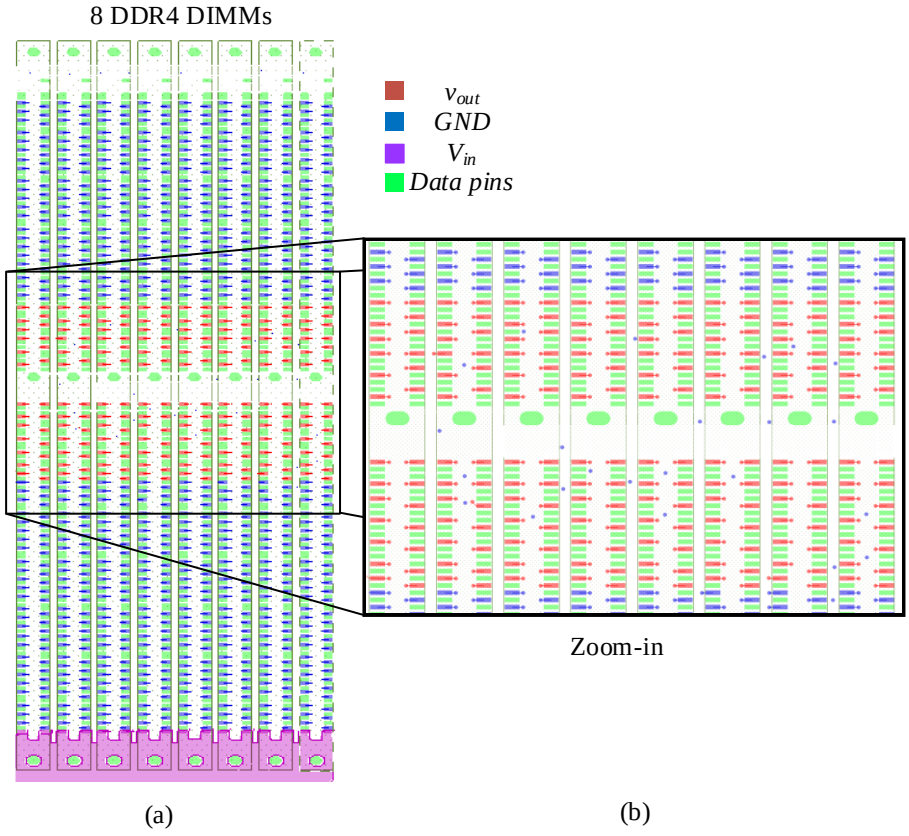

Fig. 4.7 DDR4 DIMM slots power pin configuration (top side view) (a) full slot (b) zoom-in to the v_{out} pins (red) at the center of the slots.

The layout of the v_{out} plane implemented in this work is shown in Fig. 4.8 (a), the full v_{out} plane start from the bulk capacitors through holes where it connects to the MPVRM (Fig. 4.3) all the way up to cover most the v_{out} power pin area (the rest of the vias are connected using internal layers). Fig. 4.8 (b) shows a zoom-in onto several output ceramic capacitors, the capacitors are placed in high proximity to the power pins vias. In order to control each capacitor current path, the ground terminal of each capacitor is connected directly to ground via of the DDR slot, that way the current loop between the capacitor terminals can be controlled and reduced to a minimum. Both the capacitor location and the ground connection ensure low parasitic inductance for all the ceramic output capacitors. The large amount of output capacitors also reduces the effective ESR in the system which is essential to high-power high-performance MPVRM.

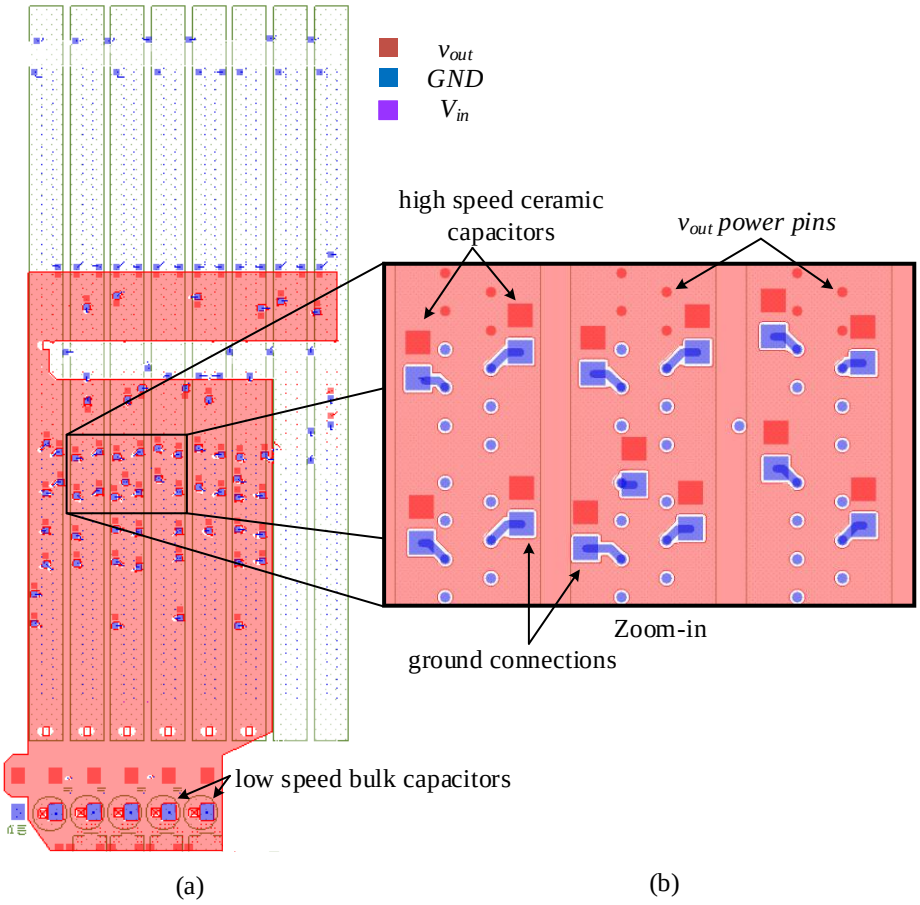

Fig. 4.8 v_{out} power plane (bottom side view) (a) full v_{out} plane (b) zoom-in on the layout of the ceramic capacitor at the v_{out} plane.

4.3. MPVRM sensors circuitry

4.3.1. Steady-state measurements

High-quality steady-state measurements are vital to the MPVRM controller, noisy signal and bad component selection can affect the controller performance and miss the regulation requirements set by the load. This section will cover the sensitive measurements of output voltage and I_{MON} current monitoring. As opposed to other sensed variables like input voltage or temperature the voltage and current information is fundamental for the MPVRM controller operation. Due to the importance of the signal quality, a fully differential measurement is implemented to mitigate any noise added to the signals along the way.

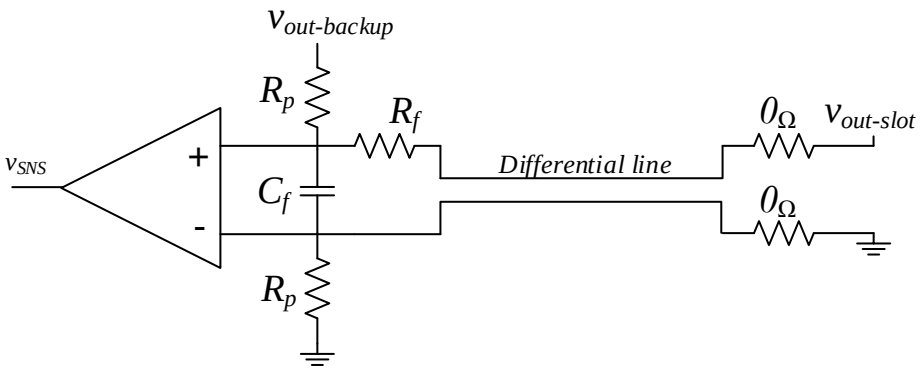

Fig. 4.9 Output voltage differential dual measurement circuit.

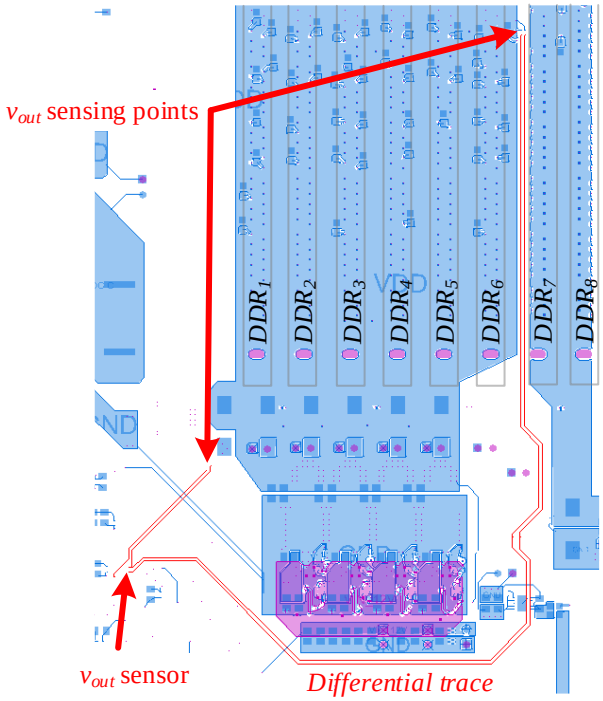

Fig. 4.10 Output voltage differential dual measurement layout

Fig. 4.9 and Fig. 4.10 show the differential dual sensing circuit and layout of the output voltage measurement. $v_{out\text{-}slot}$ signal is the primary source of measurement and it represents the voltage measured directly under the DDR slots, $v_{out\text{-}backup}$ represent a backup sensing point that is intended to provide the controller alternative measurement in case the primary measurement fails. Each signal is then low pass filtered using its respective resistor (R_p and R_f) using the filter capacitor C_f, the primary measurement resistor should be at least 10 times smaller than the backup resistor in order to damp the backup measurement during standard operation.

Following the differential measurement, the signal is then converted to a single-ended representation v_{SNS}. In this work an off the shelf component *ADA4830-1* (Fig. 4.11) is used for the following reasons:

- The high bandwidth of 84MHz in comparison to other integrated difference amplifiers ICs
- Integrated matched resistor bridge to maintain high CMRR and lower the sensor DC error
- Integrated offset amplifier that can be easily controlled by external resistors connected to the VREF input

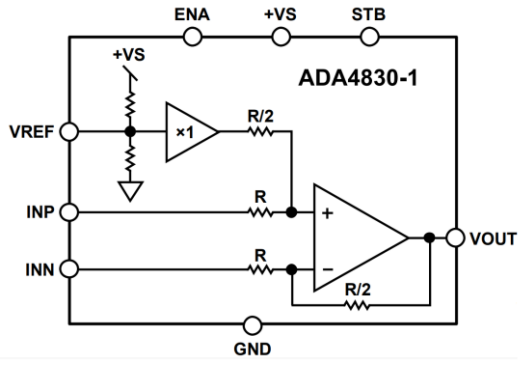

Fig. 4.11 ADA4830-1 functional block diagram [88].

The amplifier conversion of the differential input to a single output is given by:

$$v_{SNS} = \frac{(v_{INP} - v_{INN})}{2} + V_{REF} = \frac{(v_{out} - v_{gnd})}{2} + V_{REF}\,, \tag{4.1}$$

where VREF is the offset voltage.

The amplifier normalized gain as a function of the input signal frequency is shown in Fig. 4.12. Since v_{SNS} is used in order to sense the transient event starting point and the output voltage minimum point, it is highly important that the amplifier is selected is able to mimic the exact output voltage shape during a transient event. To precisely replicate the output voltage waveform shape, the amplifier gain pole must be at least a decade higher than four times the converter switching frequency f_s. In the given example the 84MHz pole is sufficiently larger than f_s so no phase is added input-to-output phase.

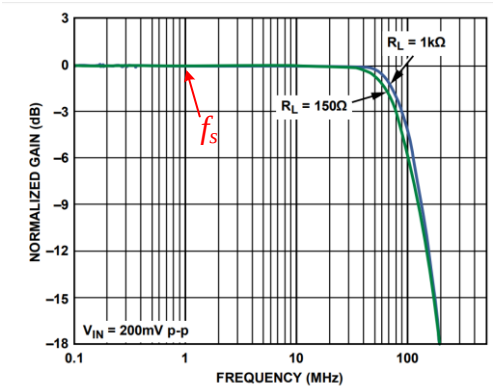

Fig. 4.12 Amplifier normalized gain as a function of the input signal frequency graph [88].

The final stage in the steady-state measurement is the voltage-to-time (VTC) conversion unit. In this work, the VTC is implemented using a non-inverting amplifier in a buffer configuration and a one-shot circuitry (Fig. 4.13 (a)). Using a short trigger pulse the VTC generates a digital pulse at the output. The output pulse duration is given by:

$$T_{pulse} = R_{OS} C_{OS} \cdot ln\left(\frac{V_{DD}}{v_{OS} - V_{th}}\right), \tag{4.2}$$

where V_{th} is the input low to high threshold of the NOR gates (N_1,N_2) and V_{DD} is the supply voltage. The one-shot circuitry suffers from a problem of charge injection during the measurement time T_{pulse}, large one-shot resistor (R_{OS}) and high-bandwidth amplifier can help to minimize the impact on the measurement v_{OS}. Fig. 4.13 (b) and (c) show simulation and experimental results of the v_{OS} during the measurement where the buffer bandwidth is 25MHz (red) and 125MHz (blue), the higher bandwidth amplifier maintains v_{OS} constant during T_{pulse}.

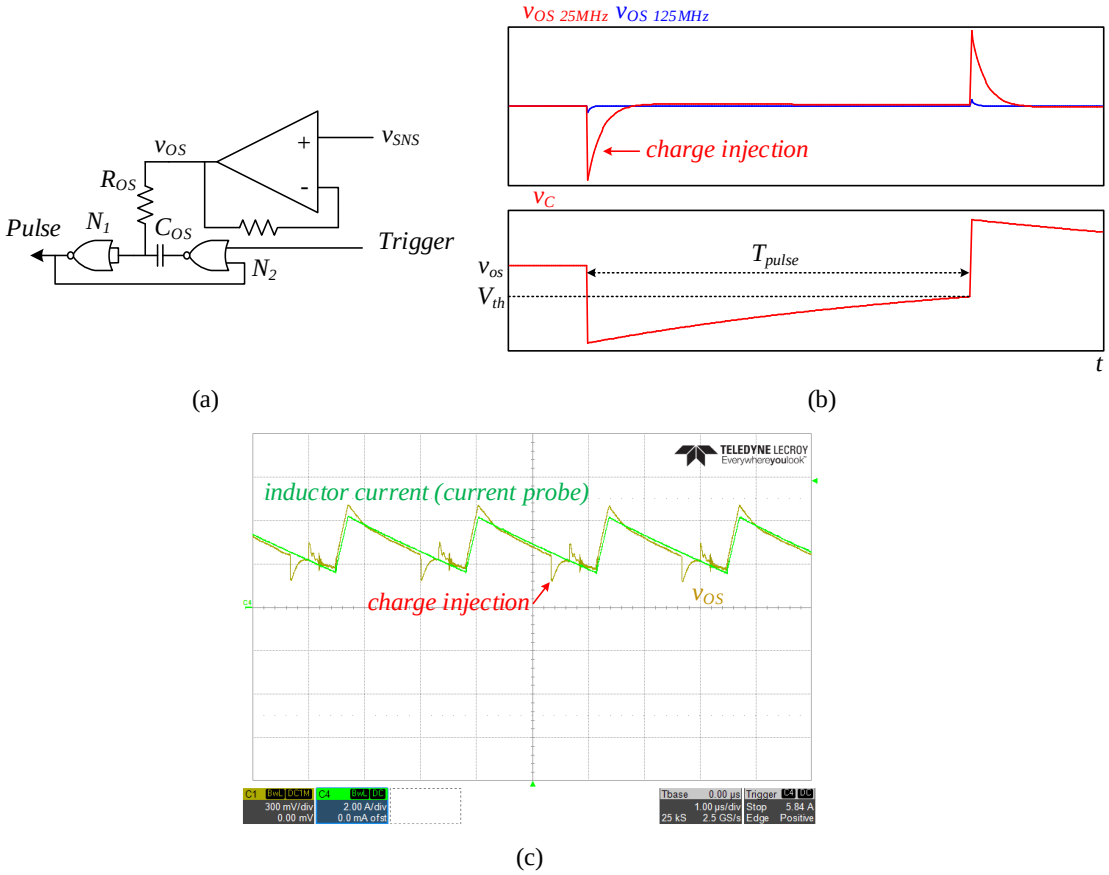

Fig. 4.13 VTC circuitry with non-inverting amplifier in a buffer configuration and a one-shot (a) VTC circuit (b) buffer's bandwidth impact on v_{OS} during the measurement (simulation) (c) experimental results of low bandwidth v_{OS} buffer.

The steady-state current measurement can be executed just like the voltage differential measurements. The differences between the measurements that need to be considered are that while the output voltage differential measurement does not contain a common-mode voltage, typical current monitoring signal is given in differential manner with a common-mode voltage v_{IREF} (Fig. 4.14 (a)). The common-mode voltage is usually provided by the controller, in the SiC820 v_{IREF} is supplied by the integrated power stage and equal $1.5V_{DC}$. Fig. 4.14 (b) shows an experimental result of the current monitoring conversion, the green signal is the differential to single-ended amplifier output and the blue signal is the actual inductor current measured by a current probe. The best place to perform the measurement is the down-slope area where there is excellent correlation between the inductor current and the current monitoring signal.

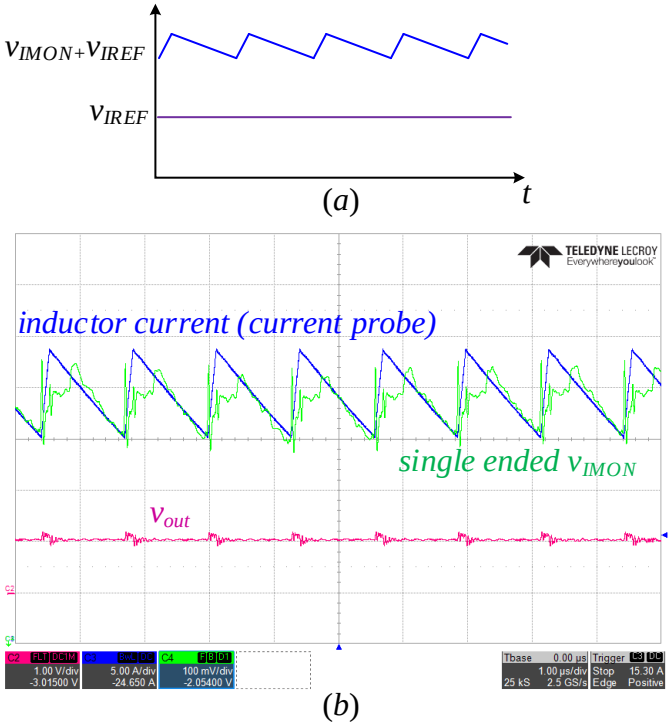

Fig. 4.14 IMON differential signal conversion (a) current monitoring differential signal with v_{IREF} common-mode voltage (b) experimental result of the current monitoring conversion.

4.3.2. Transient detection sensors design

The transient detection sensor design (Fig. 2.6) is crucial for successful TOC transient response, the detection of the exact moment the load changes is highly impactful on the TOC calculations. The small output voltage deviations of high-power VRM due to the extreme regulation requirements, challenge the sensors to provide an accurate transient event indication event when the input signal overdrive as low as few mV (Fig. 4.15). The steady-state window is selected tightly around the output voltage, the voltage ripple can be neglected due to the large output capacitance in typical high-power VRM. The comparator input offset also needs to be considered when detecting small voltage deviations. In further attempt to reduce the sensor reaction time, a dual supply comparator is selected in this study. The dual supply design supports the connection of the comparator output directly to the FPGA without a buffer for voltage translation.

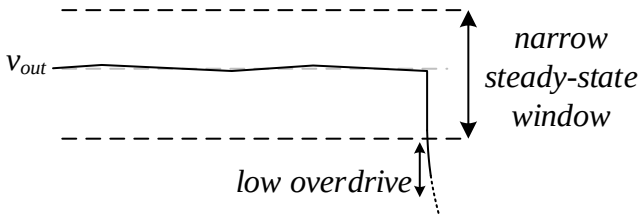

Fig. 4.15 Transient detection sensor steady-state window.

4.4. Multiphase buck VRM testing and validation

The DD4 PMVRM performance and utilities are tested to validate that the PMVRM strict regulation requirements are met. In order to drastically reduce the design effort and time, an Intel-certified DDR4 load emulation modules (LEM) Fig. 4.16) are used instead of fully functional DDR4 modules.

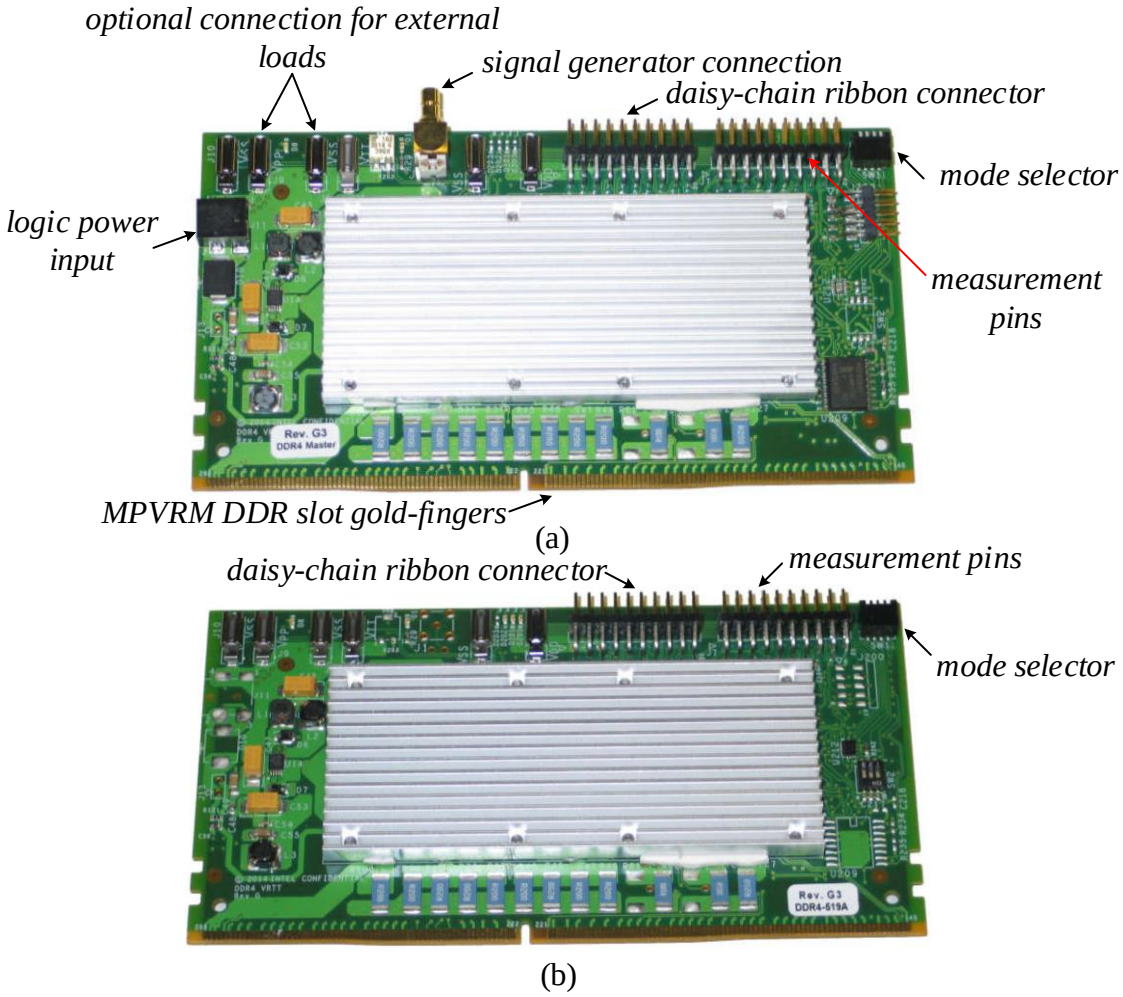

Fig. 4.16 Intel-certified narrow DDR4 load emulation modules (top side view) (a) master module (b) slave module

Each of the LEM is capable of sinking up to 15A and able to dissipate up to 18W under forced air cooling using an external fan. Since a narrow slot design is used in the MPVRM PCB, a maximal 15W operation per card is recommended due to the limited airflow of the narrow design. The LEMs are used to test each of the DDR4 power lines (V_{DD}, V_{PP}, $V_{TT,}$ and *12V*), in this work we focus on the V_{DD} rail which is the DDR4 main power rail. To select a VDD power rail testing, the mode selector pins need to be configured as shown in Fig. 4.17, for accurate measurement a single power rail must be selected.

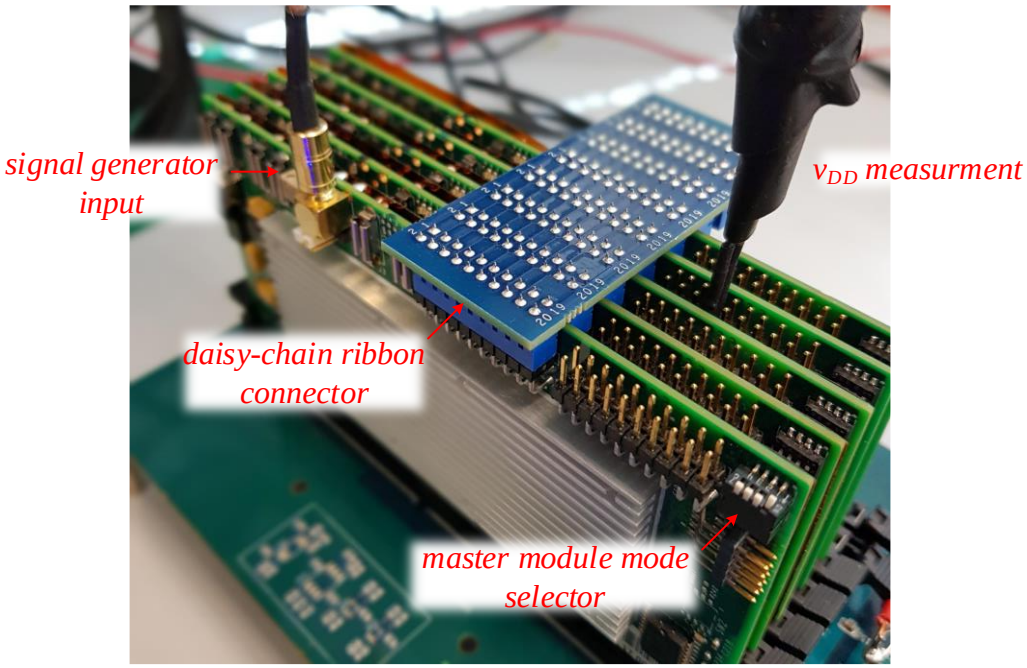

Fig. 4.17 LEMs placed on the MPVRM PCB for V_{DD} power rail testing.

The control over the load is performed using an external signal generator which is connected to the single master LEM, the signal generator input is calibrated for 50Ω input impedance. Control signals and 5V power is transferred to the slave LEMs using the daisy-chain ribbon connector. The signal generator output amplitude is used to set the LEM modules currents where the maximal value of 15A is achieved at 1050mV. The voltage to the overall current drawn by the LEMs is given by:

$$I_{sum-LEM} = \frac{V_{sig} \cdot MC}{62.5m}[A], \tag{4.3}$$

where V_{sig} is the signal generator output amplitude, MC is the number of LEMs connected. To sink the desired current by the LEM the following equation is used to calculate V_{sig}:

$$V_{sig} = \frac{I_{sum-LEM} \cdot 62.5m}{MC}[mV]. \tag{4.4}$$

The amplitude information obtained from (4.4) can now be used in a waveform pattern such as square wave to create load changes events for the MPVRM. The only limitation on the waveform pattern other than the maximum (1050mV) and minimum (0V) amplitude values is the waveform slew rate limited to a pulse edge of minimum 50ns.

The LEMs provide a direct measurement of the MPVRM output voltage that is supplied to the V_{DD} pins of the LEM, via the measurement pins as shown in Fig. 4.17 the voltage is directly measured form DIMM socket pin-233 and the output ground from DIMM socket

pin-236. In addition, the LEMs provide analog information about each module current using their local measurement pins, the sum current of all the LEMs is gathered by the master module with a gain of 25mV/A and maximum current reading of 135A.

The LEM turn on and off procedure is summarized in the following bullets and must be kept to prevent damage to the emulators:

1. Make sure the VRM is turned off and there is no voltage at the output capacitance
2. Make sure all the mode selector units are correct in all LEM modules
3. Fit the wanted amount of LEM into the DDR4 slots (up to 8 cards)
4. Connect all the assembled LEM with the daisy chain ribbon provided (Fig. 4.16 (c)) in its appropriate connector
5. Make sure the signal generator output is zero and connect it to the signal generator connection on the master card
6. Connect the logic 5V input from the external supply
7. Turn on the VRM and make sure the output is steady
8. Gradually (in both amplitude and duty) enter the desired current signal waveform using the signal generator
9. Initiate the required testing
10. After testing is complete Gradually lower the signal generator amplitude to prevent significant output overshoots.
11. Turn off the signal generator output
12. Turn off the MPVRM output, make sure that v_{out} is near zero.

5. Discussion

5.1. Contribution of the research

The key contributions of this work are summarized as follows:

Hybrid multiphase buck voltage regulator module – To mitigate the extremely fast load changes of HPHPL, the MPVRM hybrids an ACM controller for steady-state operation and a non-linear control for optimal transient response, each of them excels in its intended operation mode. The linear ACM controller excels in high-accuracy steady-state operation to maintain good efficiency and stability, the non-linear controller handles load transients with near-ideal response. The hybrid dual controller architecture has been proven throughout the research that it can reduce the overall volume of MPVRMs and improve the power processing density.

Integration of TOC and minimum deviation transient response – The highly desired non-linear control methods offers an ideal transient response. It is especially required by high-performance VRM to sustain larger transients and to achieve system miniaturization. In this work, a TOC was successfully incorporated into a hybrid controller for a highly complicated system to begin with, the MPVRM. The addition of TOC managed to substantially reduce the output voltage deviations during transient.

Hardware development for high-speed high-power environments – The controller supporting hardware circuity was designed and optimized to provide accurate high-quality measurements in a noise saturated environment.

MPVRM design guidelines and validation – In addition to the thoroughly analyzed hardware design in the introduced MPVRM, an in detail design guideline covering design consideration, component selection, layout notes and validation of 12V-to-1.xV high-power MPVRM for DDR4 memory modules.

5.2. Suggestions for future research

Some suggestions for future lines of investigation that can be developed as a result of this thesis are outlined below:

Self-calibration of the VRM controller coefficients – The controller coefficients selection process is a time-consuming process that is required for the implementation of the VRM controller into new systems. Calibration automation can induce the implementation process of the VRM into the new applications, preventing man-made errors and help to compensate for component degradation.

ASIC implementation of the MPVRM controller – During the development progression of the controller core units, a highly flexible development platform is required. The FPGA offers a dynamic solution for development platform but at the same time is limited by its core logic units design and synthesis tools. A costume ASIC design can offer higher design flexibility even in the single gate level to further enhance the controller capabilities and the overall VRM performance

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תקציר

עבודה זו עוסקת ביכולות המרה ועיבוד אנרגיה משופרות של מערכות מולטי-מודולריות לניהול אנרגיה אשר מיועדות לאפליקציות הדורשות ביצועים גבוהים בעזרת הטמעה של שיטות בקרה מתקדמות, תכנון ואופטימיזציה מערכת העברת ההספק והמעגלים האלקטרונים הנלווים לה. העבודה מתמקדת בהשגת שיפור משמעותי בביצועים של מערכות לניהול אנרגיה בזמן של תופעות מעבר בעומס של ספקי כוח, תופעה אשר מגבילה את היכולת לבצע מזעור של המערכת. מטרתה העיקרית של עבודה זו היא להקטין את הנפח הכולל של מערכות מולטי-מודולריות לעיבוד אנרגיה ועל-ידי כך להגדיל את הצפיפות האנרגטית של מערכות אלו. הדורות הבאים של מערכות לניהול אנרגיה אשר פועלים באופן נרחב במרכזי עיבוד נתונים יהיו חייבים לספק פתרונות אשר יעמדו בקצב ההתפתחות הגובר של מחשוב בענן.

אחד מן היעדים המרכזיים של עבודה זו היא שיפור התגובה של מערכות מולטי-מודולריות להספקת מתח מיוצב כנגד תופעות מעבר בעומס. הרכיבים הריאקטיבים במערכת אלו נבחרים בגודלם ובערכם כדי לתת מענה לדרישות הרגולציה של מתח העומס בזמן תופעות המעבר. אימפלמנטציה מוצלחת של שיטות בקרה מתקדמות יכולה לספק שיפור משמעותי בתגובת המערכת לשינוי בעומס. את השיפור ברגולציית מתח המוצא של המערכת בזמן שינוי בעומס ניתן לתרגם להורדה במספר הרכיבים הפסיביים במערכת או לאפשרות להכיל עומסים בעלי ביצועים גבוהים אף יותר. בכדי להשיג את השיפור הרצוי במחקר זה פותח בקר דיגיטלי חדש למערכת מולטי מודולריות לעיבוד אנרגיה בעלות ביצועים גבוהים ביחד עם הפריפריות הנדרשות וכל המעגלים התומכים לפעולת הבקר והמערכת.

יעד נוסף של עבודה זו הוא לחקור את האופטימיזציה ואת שיקולי התכנון הנדרשים ליצירת מערכת מולטי-מודולרית להמרת אנרגיה אשר ניתן לשלבה בתוך מערכות הדורשות יכולת המרת אנרגיה עם ביצועים גבוהים. לצורך מטרה זו שיטות הבקרה אשר ייושמו בתוך בקר כלאיים אשר משלב שתי שיטות בקרה להשגת ביצועים משופרים, נחקרו לעומק בכדי להתאימם לפועלה של מערכת מולטי-מודולרית, בעלת סיבוכיות גדולה יותר. גם המעגלים האנלוגיים והדיגיטליים התומכים של המערכת הותאמו לפעולה בקצב ודיוק גבוה אשר נדרש בכדי לספק את דרישות הרגולציה של העומס. מחקר זה מכיל גם מדריך תכנון מקיף ויסודי אשר מכיל את כל שיקולי התכנון, בחירת רכיבים, עריכת המעגל וכן גם לבדיקה ואשרור של ביצועים של מערכת המרת אנרגיה מ 12V ל 1.xV. המערכת אשר תוכננה, נבנתה ונבדקה בעבודה זו יכולה לשמש להספקת אנרגיה לדורות הבאים של עומסים מתקדמים כגון מעבדים או זיכרונות.

אוניברסיטת בן-גוריון בנגב
הפקולטה למדעי ההנדסה
המחלקה להנדסת אנרגיה

יכולות המרה ועיבוד אנרגיה משופרות של מערכות מולטי-מודולריות לניהול אנרגיה

חיבור זה מהווה חלק מהדרישות לקבלת תואר מגיסטר בהנדסה

מאת: בר הלבני

מנחה:

פרופ' מור מרדכי פרץ

המחבר: בר הלבני ..... תאריך: 24.09.2019

מנחה: פרופ' מור מרדכי פרץ ..... תאריך: 24.09.2019

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יכולות המרה ועיבוד אנרגיה משופרות של מערכות מולטי-מודולריות לניהול אנרגיה

חיבור זה מהווה חלק מהדרישות לקבלת תואר מגיסטר בהנדסה

מאת: בר הלבני

מנחה:
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October 2019