BEN-GURION UNIVERSITY OF THE NEGEV
FACULTY OF ENGINEERING SCIENCES
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

POWER MANAGEMENT OF HIGH CONVERSION RATIO RESONANT CONVERTERS

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE M.Sc DEGREE

By: Doodi Dayan

Supervised by:
Prof. Mor Mordechai Peretz

February 2020

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Chairman of graduate studies committee:

Name: …….. ……..…..... Date: ……

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Abstract

This thesis develops a new and unique approach which enables the design and implementation of charging and discharging of energy storage cells and miniaturization of the volume of the entire system. The design includes charger, cells balancer, logic control and several additional backend electronic circuits to sustain all together. The system is connected to a low voltage power supply as a single energy source for the power delivery as well as for all periphery units.

Charging energy storage cells used in high pulsed-power application, where high energy is accumulated in big energy storage elements and then discharged abruptly in a short period of time. Charger for high voltage is needed in order to accumulate as much energy as possible.

The main objective of this thesis is to design and implement a power management system for a high ratio resonant converter. Additional objective is to shrink the system's volume to the minimum size. The main enabler to scale down the size of such system is an approach based on choosing optimal energy storage cells and switching components in terms of energy and power per volume rating. The work explains the specifications of such system: the amount of energy it should hold and the rate of charge for specific application, coilgun. Those parameters and more are included in the considerations for choosing the right converter topology, electronic components, storage cells, control method, etc. In practice, common voltage ratings, e.g. 12V, 24V, 50V, 100V, etc. are preferred by the industry and electronic components manufacturers make the effort to manufacture the best electronic components used with those values. Choosing the main components as explained, to be the building stones for designing high voltage charging system is a strong enabler for miniaturizing. While the components rating and stresses are only fraction of the total voltage, much more components are used in comparison to the conventional approach that using several bulky high voltage rating components. In the end, the total volume decreases considerably.

Additional objective of this thesis is to focus on the charger's design as part of propulsion system, coilgun. The charger is basically a DC-DC converter, connected to a low voltage source at the input, generates high voltage at the output to charge a single storage cell which is part of a chain consists of several storage cells stacked on top of each other. Therefore, another important issue discussed in this work focuses on: (a) transferring energy from the first cell to the upper cells in the chain and (b) balancing all cells in the chain. The influence of unbalanced cells on the reliability from high level perspective is discussed in this work. Storage cells employed in this study are capacitors to sustain high voltages, but from topological perspective can be replaced by either supercapacitors, batteries or any other energy storage cells.

The research includes all stages required to show proof of the concept: capacitor charger topologies literature review, choosing and modifying the best topology for a specific application (coilgun), designing all peripherals circuits needed for a full system, analyzation of the system with electronic circuit simulation software. Beyond this, the research includes full implementation of the system: a PCB was designed and manufactured, electronic components selected based on the approach mentioned above and experimental results are shown. The research was published in the IEEE Workshop on Control and Modeling for Power Electronics [55] and in the IEEE Applied Power Electronics Conference and Exposition (APEC).

Acknowledgments

I would like to thank my supervisor Prof. Mor Mordechai Peretz for his invaluable guidance and support for the last two years. Prof. Peretz taught me how to explore and research, how to look differently about electronic circuits and electronic systems and how to handle when things don't work as expected. Prof. Peretz guided me to excellence in every mission, showed me the main goals and the important subjects and reveal me to big success and for that I am very grateful.

I would like to express my sincere thanks to Dr. Michael Evzelman for the time he invested to help me during the last two years. Dr. Evzelman taught and guided me in scientific writing, showed me the right way to achieve my targets and also assisted me with practical work in the lab. I really appreciate him for all that effort.

My special thanks are also extended to my office colleagues from our research group, and from others; they became very good friends of mine during this time, and I would like to thank them for providing ideal conditions for research, as well as a fun and comfortable atmosphere. I will always have a soft spot for them.

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I would like to express my profound gratitude to my family: my father and my brothers, who have always supported and cheered me.

Above all, I want to express my thanks to the person I love more than I can describe, my beloved mother. She accompanied me throughout difficult times, listened carefully and helped me with love with everything she could. I appreciate her for the care she took of me in the last years in the academy. I could not do it without her.

Many thanks,

Doodi Dayan

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Acronyms and Abbreviations

SOC – State of charge
ESS – Energy storage system
ESC – Energy storage cell
ZCS – Zero current switching
ZVS – Zero voltage switching
PFM – Pulse frequency modulation
CW – Cockcroft-Walton
BMS – Battery Management System
SCC – Switched-capacitor converter
DCM – Discontinuous conduction mode
MCU – Microcontroller unit
SCC – Switched-capacitor converter
RSC – Resonant switched capacitor
EMI – Electromagnetic interference
ESR – Equivalent series resistance
FEM – Finite element Method

Inline References Legend

X.XX – Chapter / Section number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure

1. Introduction

Power supplies are used everywhere. Any electronic device needs an energy management unit to handle and regulate the input power and keep it balanced. Some example for devices where power management is important are: mobile phones, TVs, screens, computers, chargers, audio amplifiers, servers, modems and many more.

Power converter defined as any electronic circuit which convert energy of one form to another. Usually both the input and the output are voltages but sometimes we convert voltage into current and vice versa. Typically, when talking about converting some voltage into another voltage there are four types of conversion: DC to DC, AC to DC, DC to AC, AC to AC. Each type of conversion can be made in many different ways and methods. Also, we can step-up the input voltage to a higher voltage or step it down to a lower voltage. For example, an AC/AC converter usually used a transformer to step-down or step-up the input AC voltage. More complex systems include many passive elements such as capacitors and inductors.

Converting input voltage to another one is not enough if we want to feed a load. It because an electronic load has a distinct specification which determine some tight boundaries. Those boundaries must be concerned, especially if the load is sensitive to deviation from nominal values. Therefore, an entire power management control system is added to the converter. That system handles the converter to keep the voltage or current stable at the output. The control system made with a negative feedback loop, tracking the output voltage or output current, create an error signal and then the system generate a correction signal called “control signal”. A stable converter (with control system) is called power supply or regulator.

Behind every converter stands an electronic circuit with specific behavior and operation. The resonance circuits have many versions, all used for different applications not only for power converter: RF application, logic circuit, oscillators and many more.

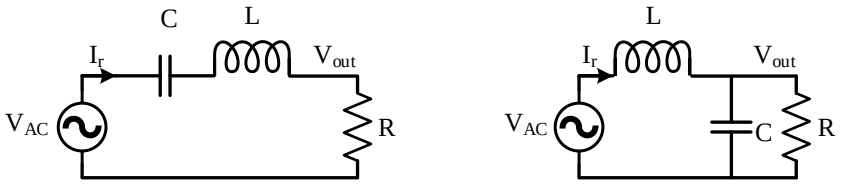
1.1. Resonant circuits

Resonant circuit involving capacitors and inductors. Those passive elements can store and release energy during each cycle of operation. Usually, a capacitor connected serially to an inductor called together a “resonant tank”. Resonant circuit connected to an AC voltage source with generates at frequency f_{sw} (sometimes to current source). The capacitor and inductor determine the resonance frequency, f_r, with the following value:

$$f_r = \frac{1}{2\pi\sqrt{LC}}\ [Hz]. \tag{1.1}$$

Resonance frequency is the frequency that the impedance of the resonator is at the minimum and the impedance of an inductor connected in parallel to a capacitor is at the maximum. Therefore, when we can generate a source with switching frequency that equal to the resonant frequency, i.e. $f_{sw} = f_r$, and say that the circuit is at resonance. A common resonant circuit is the RLC circuit. It consists of a resistor, an inductor and a capacitor connected in series or in parallel. The effect of the resistor is damping and does not influences the resonant frequency. In many cases the resistor represents the load when the resonance circuit is become to be a resonant converter. The RLC circuit is described as a second order circuit. Meaning that any voltage or current in the circuit can be described as a second-order differential equation in circuit analysis. Many applications use RLC circuit: tuning in radio application, filters, power converters and more.

Usually, RLC circuit is either the series-resonant series-loaded converter or the series-resonant parallel-loaded converter [1].



(a) Series-resonant series-loaded (b) Series-resonant parallel-loaded

Fig. 1.1 Two common RLC resonant circuits

The AC-voltage source which can be seen at Fig. 1.1 is implemented by a set of switching elements, usually, semiconductors devices, uses in two main states: on and off. The switches can be any transistor (BJT, MOSFET, etc.) but mainly MOSFET is used because of their higher efficiency, low cost and simple driving. By the switches the circuit can be in several states. In each state it applied different voltages and currents on the capacitors and inductors of the system. By changing the switching frequency, f_{sw}, we can control the power delivers to the output but basically, f_{sw} should be in the vicinity of the resonant frequency, f_r.

1.1.1. Series-resonant series-loaded circuit

The resonance of a series RLC circuit, Fig. 1.1a, occurs when the inductive and capacitive impedances are equal in magnitude but cancel each other because they are 180 degree apart in phase. The equivalent phasor of the impedance of the circuit is

$Z = R + Jx_l - Jx_c$ and at resonance, $f_{sw} = \frac{1}{2\pi\sqrt{LC}}$, $Z = R$ where R is the ohmic load and X_L and X_C are the inductor and capacitor phasor, respectively.

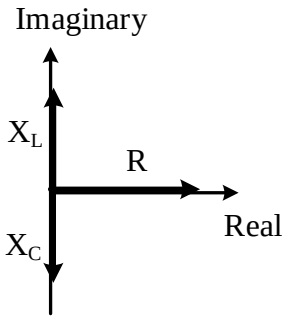


Fig. 1.2 Phasor diagram in series resonant circle

The quality factor of the circuit defined as:

$$Q = \sqrt{\frac{L}{C}}\frac{1}{R} \text{ or } Q = \frac{f_r}{BW} = \frac{f_r}{f_H - f_L} \quad (1.2)$$

where f_r is the resonance frequency, $BW = f_H - f_L$ is the circuit bandwidth and f_H, f_L defined as -3db points.

The quality factor is defined as the maximum or the peak energy stored in the circuit (the reactance) divided by the average energy dissipated in it (the resistance) per radian (each cycle of oscillation at resonance). Fig. 1.3 describes how the current in the circuit is changed with the switching frequency. The quality factor of the circuit influence that graph: the higher the circuit's Q, the smaller the bandwidth *BW*. With higher value of Q, the graph become sharper.

Another parameter is the **selectivity** of the circuit and it measures the ability of the circuit to reject any frequencies either side of f_H and f_L. A more selective circuit will have a narrower bandwidth whereas a less selective circuit will have a wider bandwidth. The selectivity of a series resonance circuit can be controlled by adjusting the value of the resistance only, *R*, keeping all the other components the same.

$I_{\max}$ is the maximum circulating current that can flows in the circuit and equal to $I_{max} = \frac{V_{in}}{R}$. Also, this peak value is reached at resonance as shown in Fig. 1.3. The meaning of that is that the maximum gain $\frac{V_{out}}{V_{in}}$ of the circuit (where V_{out} is the voltage of the resistor, represent the load) is unity: $V_{out}^{max} = R \cdot I_{max} = V_{in}$.

Further information can be found in [2], which gives a detailed analysis of the series resonant converter.

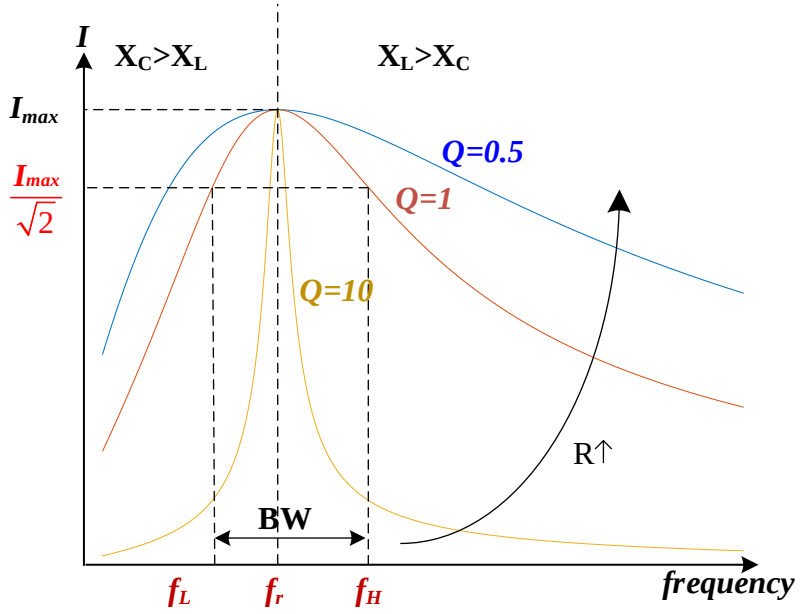


Fig. 1.3 Series resonant series loaded circuit current gain for different load values. Higher *R*, lighter load, leads to smaller *Q* and low selectivity (less sharper graph). For $f>f_r$ circuit has inductive characteristic. For $f<f_r$ circuit has capacitive characteristic.

1.1.2. Series-resonant parallel-loaded circuit

The resonance frequency of the series-resonant parallel-loaded circuit (Fig. 1.1b) is the same as the series-resonant series-loaded circuit: $f_r = \frac{1}{2\pi\sqrt{LC}}$. The main difference here is that the voltage gain can reached more than unity. The ac gain of the circuit is given by [1]:

$$G_{AC} = \frac{V_{out}}{V_{in}} = \frac{1}{1-\frac{X_L}{X_C}+j\frac{X_L}{R}}, \tag{1.3}$$

where $X_C = \frac{1}{\omega C}$ and $X_L = \omega L$ are the phasors of the capacitor and inductor, respectively. The quality factor of the series-resonant parallel-loaded circuit is $Q = R\sqrt{\frac{C}{L}}$. When $\omega = \omega_r$ their values are equal and the gain reaches his maximum:

$$G_{AC}^{max} = G_{AC}(\omega_r) = -j\frac{R}{X_L} = -jQ. \tag{1.4}$$

Circuit with higher *Q* have sharper gain graph and their selectivity is higher. This circuit can reach high output voltage amplitude but the main disadvantage is the high circulating current running in the circuit since $I_L = I_C + I_R$. High circulating current requires bigger inductor which can handle the current and dissipate power.

Further information can be found in [3] and [4], which give a detailed discussion and analysis of the parallel-loaded converter.

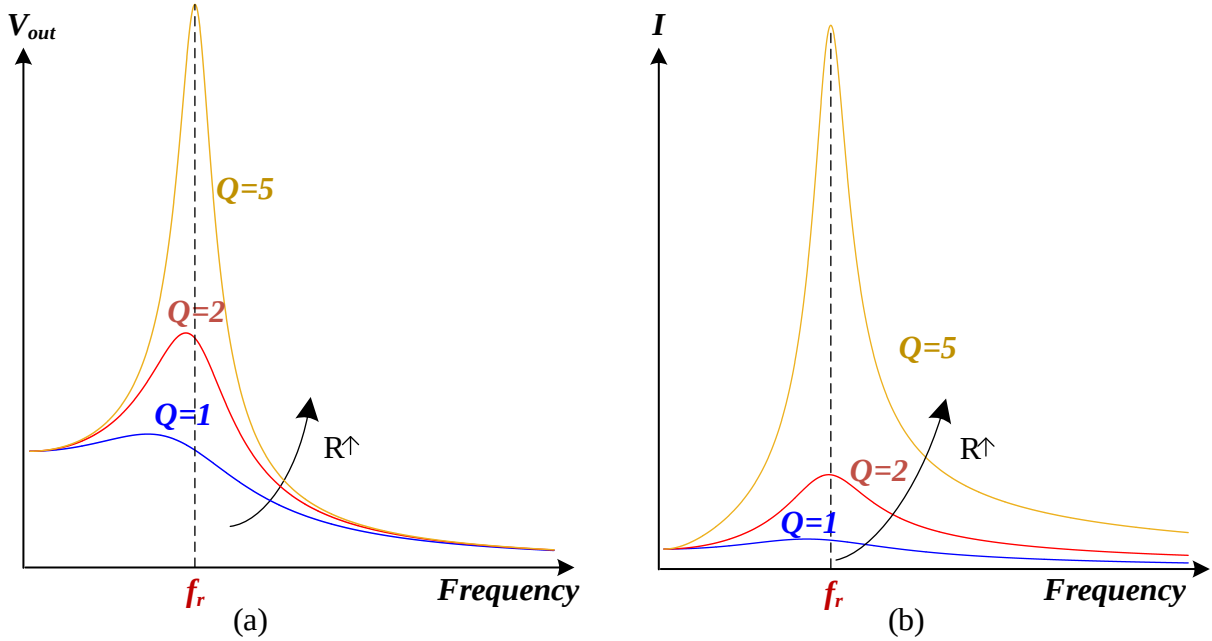


Fig. 1.4 Series resonant parallel-loaded circuit gain for different load values: (a) output voltage vs. frequency (b) resonance current vs. frequency. Higher *R* (light load) leads to higher *Q* and higher selectivity (sharper graph). For $f>f_r$ circuit has inductive characteristic. For $f<f_r$ circuit has capacitive characteristic.

1.1.3. Input stage of resonance circuits

Resonant circuit should be connected to an energy source to stimulate the resonant tank. The energy source (voltage) should be an AC source because the resonant tank has no response to DC voltage. Practically, the input voltage source is a DC power supply and therefore, an input power stage is needed to create a sinusoidal perturbation. An input stage, usually, gets a DC voltage at the input and generates a square wave with some frequency at the output. This frequency is called the switching frequency, f_{sw}. Two common input stages are the half bridge and the full bridge.

A half-bridge, built with two switching elements (Fig. 1.5a), *S1* and *S2* .At the first phase, when the high side switch, *S1*, is on, the voltage applied across the resonant network, V_x, (also called the switching node) is V_{in}, i.e. $V_x = V_{in}$. Current flows from the input DC source into the resonant network and the load, charging the resonant capacitor and resonant inductor. At the second phase, the high side transistor, *S1*, is switched off and after time called 'dead-time', the low side transistor, *S2*, switched on and V_x=0V. In both phases power is flows to the load: at the first phase, the input voltage source supplies the power and charging the resonant capacitor, and at the second state the capacitor discharges deliver power to the load.

A full bridge is built with four switching elements (Fig. 1.5b) *S1-S4*. At the first phase, *S1, S4* on and *S2, S3* off and $V_x = V_{in}$. At the second phase *S2, S3* on *S1, S4* off and V_x=-V_{in}.

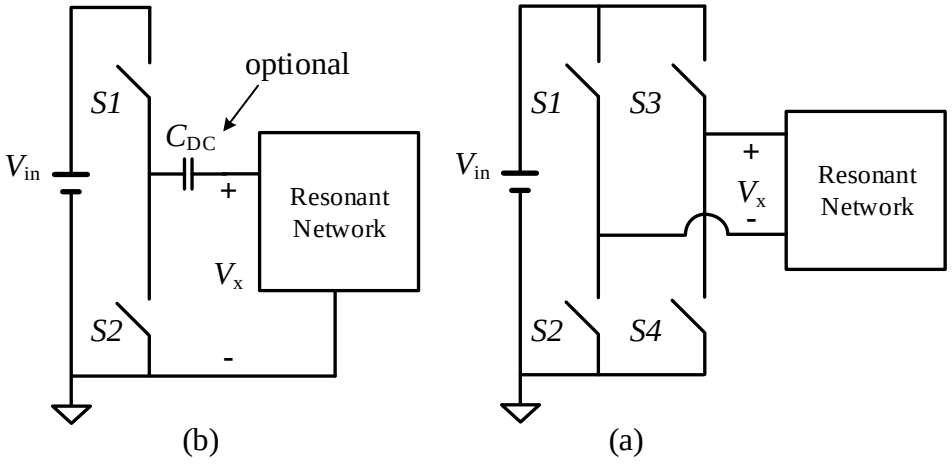


Fig. 1.5 Input stage for resonant circuit: (a) full bridge, (b) half bridge

Unlike the half bridge input stage which creates V_x with a dc level equal $\frac{V_{in}}{2}$, the full-bridge input stage generates V_x without dc level. Fig. 1.6 presents waveforms of switching node, V_x,, of half-bridge and full-bridge input power stages. The voltage of the switching node, V_x, can be expressed using the Fourier series:

$$V_x = \frac{2V_{in}}{\pi} \cdot \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} \sin(n \cdot 2\pi f_{sw} t) + \frac{V_{in}}{2}, \tag{1.5}$$

or, if the square wave is symmetrical around 0V, i.e. average voltage is zero, V_x can be express as follows:

$$V_x = \frac{4V_{in}}{\pi} \cdot \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} \sin(n \cdot 2\pi f_{sw} t). \tag{1.6}$$

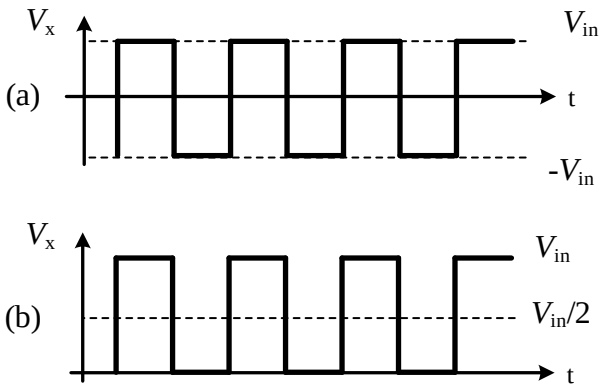


Fig. 1.6 Voltage applied to the resonant network with: (a) full-bridge, (b) half-bridge

When switching frequency f_{sw} is in the vicinity of the resonant frequency f_r, $f_{sw} \approx f_r$, a first harmonic approximation can be applied and bridge inverter is described as sinusoidal source connected to a resonator as shown in Fig. 1.1 [5]. The voltage V_x can be described as:

$$V_x \approx \frac{2}{\pi} V_{in} \sin(2\pi f_{sw} t) + \frac{V_{in}}{2}, \tag{1.7}$$

$$V_x \approx \frac{4}{\pi} V_{in} \sin(2\pi f_{sw} t). \tag{1.8}$$

The dc component in (1.7) will charge the resonant capacitor to this value. Because of that, sometime a dc block capacitor, C_{DC}, is added in series with the resonant capacitor. The capacitance value of C_{DC} should be high enough to block the dc voltage during a switching cycle, T_s, and still not affect the resonance frequency designed before. In addition, the amplitude of V_x in resonance circuit with a full bridge is doubled compared to a half bridge input stage, as can be seen from the equations above, what leads to doubled voltage gain on the output resistor.

1.1.4. Switching operation

As described at the previous section, a switching method should occur inside the input stage to excite the resonance circuit. The switching frequency, f_{sw}, of the circuit should be in the vicinity of the resonant frequency, f_r (see Fig. 1.3). Basically, when $f_{sw} = f_r$ the output voltage can reach maximum gain, unity in series-loaded circuit and higher than unity (close to *Q*) in parallel-loaded circuit. Although this advantage, in practical system we will prefer to switch before or after the resonant frequency i.e. $f_{sw} > f_r$ or $f_{sw} < f_r$. Main reasons for that are efficiency and stress on the switching elements. Operating the resonant circuit at the exact resonant frequency i.e. $f_r = f_{sw}$ named "hard-switching" but when $f_{sw} \neq f_r$ we can reach "soft-switching" operation.

In short, soft-switching operation is reached when MOSFET (as the switch) turns on when the voltage across it is zero, $V_{DS} = 0V$ (called Zero Voltage Switching or ZVS) or when the current through it is zero, $I_{DS} = 0A$ (called Zero Current Switching or ZCS). ZVS can be reached by operating the resonant circuit above resonance i.e. $f_{sw} > f_r$ and ZCS can be reached by operating the resonator under resonance i.e. $f_{sw} < f_r$.

1.2. Balancing circuit

1.2.1. Energy storage system

Energy storage system (ESS) is a device that stores energy in multiply forms including chemical, gravitational potential and electrical potential. When talking about electrical energy systems this device is essential to the operation of power systems. Electricity generated from renewable sources, which has shown remarkable growth worldwide, can rarely provide immediate response to demand. ESS is a bank of energy, users can charge and use it afterwards. Therefore, ESS's application is mainly driven by a demand for load shifting or optimization between a generation infeed and load demand. ESS can range from large scale storages (e.g. pumped hydro) to micro storage systems (e.g. mobile phone battery).

Today ESS can be found in consumers' home equipped with solar panels on the roof, as the energy generator. ESS captures the extra power not use by the consumer at noon and at the evening the consumer has power directly from the ESS [6].

When talking electronics, ESS are not only used within a context of renewable energy but with any system that consists of more than a single energy storage cell (ESC). An ESC is a (relatively small) device that can store a limit of energy within it. Connecting many ESC together in some topology reveals to an ESS that can stores much more energy. Some examples for application are: laptop battery, cell phone battery, electronic weapons as coilgun, railgun and many more pulsed power applications like magnetic pulse welding etc.

1.2.2. ESS - Topologies and types

As mention before, ESS is built with many small energy storage cells (ECSs or 'cells'). The configuration of the ECSs determines the voltage and the maximum current could be charge/discharge the ESS.

N cells can be connected in series, parallel or in series and parallel. Each configuration is described as a size of a matrix: some cells in series and some of them are parallel. The following equation describes the configuration of ECSs inside the ESS:

$$N = (\#\_series\_cells)\ x\ (\#\_parallel\_cells). \quad (1.9)$$

Fig. 1.7 shows some optional configuration of *N*=12 cells inside an ESS:

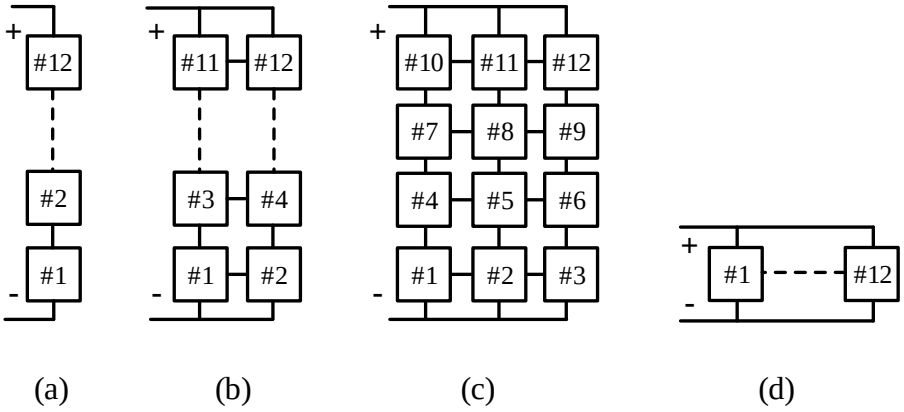


Fig. 1.7 optional configurations for 12 energy storage cells: (a) 12x1, (b) 6x2, (c) 4x3, (d) 1x12

Each configuration shown in Fig. 1.7 is right for different uses. For example, Fig. 1.7a shows a topology with the highest voltage but minimum current it can supply, while Fig. 1.7d shows a topology with a highest current but minimum voltage. Other topologies, i.e. (b) and (c), are compromise between voltage and current can get in/out of the ESS.

From a topological perspective the storage cells can be either capacitor, supercapacitor or battery cells. ESS for high voltage and very high voltage application is usually implemented by capacitors. Also, pulsed-power-application needs very high current amplitudes coming out from the ESS or rapid charge of the ESS for the next cycle of operation (peaks of power) and therefore the best device for the mission is the capacitor. ESS for low-medium voltage with restricted low volume requirement probably implemented by super-capacitors as an ECS because they have much higher energy per unit volume ratio. ESS for home application (e.g. capturing energy from PV panels) will be constructed from battery cell since it is cheap and has pretty good performance but moreover the leakage current is much smaller compared to capacitor. Batteries are the first choice when storage time is about hours and days.

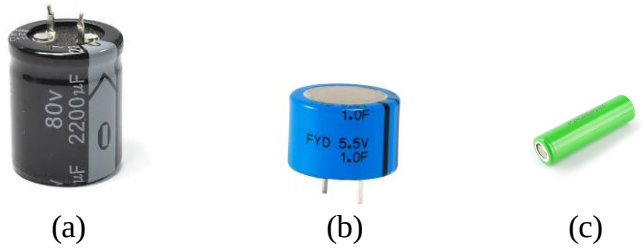


Fig. 1.8 Energy storage cells: (a) capacitor, (b) super-capacitor and (c) battery-cell

1.2.3. Cells' balancing in ESS

Basically, the number of cells in series inside the ESS's topology, determines his nominal voltage. The number of cells in parallel determines the maximum current we can consume from the ESS or charge it. Of course, it determines the energy capacity (in Ah). We choose

those numbers according the application uses it. Ideally, all cells are identical one to each other, but practically, cells have somewhat differences between capacitances. The reason is due to manufacturing variances, assembly variances, different histories experienced amongst the cells in a battery pack (e.g. charging/discharging, heat exposures, etc.) or even a fatal fault happened in one or more cells. As a result, the ESS has some limits and restrictions. For example, discharging must stop when any cell first runs out of charge or charging must stop when any cell is fully charged. The problem here is that the chain (the ESS) is no stronger than its weakest link (the cell). And so, without appropriate balancing, the system is limited and could not reach its maximum potential. Fig. 1.9 and Fig. 1.10 describe situation of charging and discharging of six cells, respectively, when one cell (no. 4) is unbalanced relatively to the others. It's easy to understand now that ESS's capacity is **not** six times one capacitor cell capacity, as expected, but practically the total capacity ready to be used (charge/discharge) is only a part of it. In Fig. 1.9 charging stops because cell #4 is fully charged and current gets into the ESS will overcharge and damage it although the other cells can store much more energy. In Fig. 1.10 discharging stops because there's some cells fully discharged and limit the access to the energy stores in cell #4.

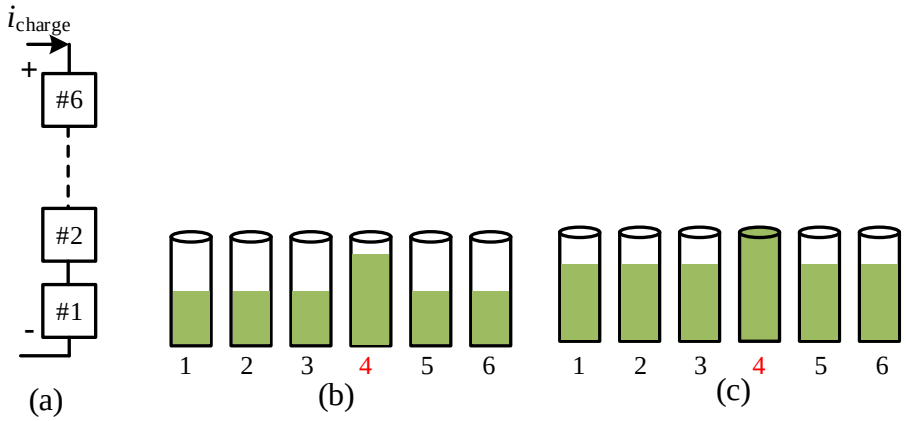


Fig. 1.9 Charge of 6 cells in series with single unbalanced cell: (a) connection topology, (b) cells' capacity before charge, (c) cells' capacity after charge.

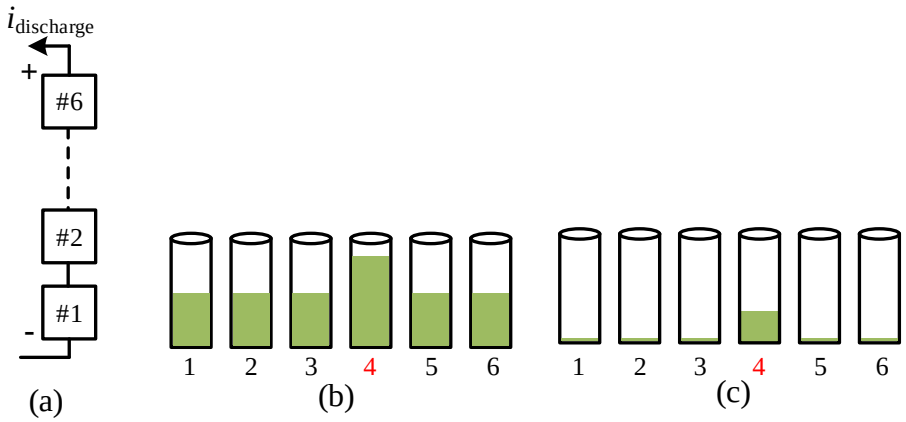


Fig. 1.10 Discharge of 6 cells in series with single unbalanced cell: (a) connection topology, (b) cells' capacity before discharge, (c) cells' capacity after discharge.

The previous two figures describe situation of only one unbalanced cell but after some cycles of charging and discharging all cells are out of balance referenced to each other. The technique that improve the available capacity of a pack with multiple cells is called cell balancing.

Cell balancing can be manipulated with any ECSs. The electrical device that performs cell balancing is the battery balancer but Battery Monitoring Systems (BMS) is a common name for a full system connected to ESS to perform temperature monitoring, over current/voltage protection, charging, balancing and other features to maximize the life of the ESS.

Balancing can be active or passive (both methods discussed in the following sections). During operation, the balancer compares between the capacity of the cells and then using decision-making system and control system. It does some actions to close the gap and reach fully balanced cells in series. How does the balancer determine which cells are not balanced? In other words, what is the criterion to decide when specific cell is not balanced? Tracking the difference of cell voltages is the most typical and easy method to obtain, but it is greatly affected by factors such as working conditions, making it difficult to provide accurate parameters for the equalization system [7]. More sophisticated to determine is the SoC (State of Charge). Here the performance is related to the accuracy of SoC estimation [8]. A complex algorithm is necessary to estimate the SoC of each cell which leads to many calculations and complexity [9],[10]. Most paper use the SoC control but consider SoC of each cell to be known and accurate [11]-[13].

1.2.4. Passive balancing

A battery pack or storage product is consisting of many small storage cells. But over time, the cell matching degrades due to charge/discharge cycles, elevated temperature and general ageing. Passive balancing is a common and simple way to perform balancing between energy storage cell. The idea is to bring all cells to the same energy level as the weakest cell. Using a relatively low current, it drains a small amount of energy from high SoC or high voltage cells during the charging cycle so that all cells charged to their maximum SoC/voltage. This is accomplished by using a switch and bleed resistor in parallel with each battery cell. Passive balancing allows all cells have the same SoC/voltage level by wasting energy on a resistor (heat) in a very simple and low-cost method.

The system connects each cell to a discharge resistor through a switch. When the controller's algorithm recognize that the cell is over charged it send a control signal to let the switch conduct. The cell is connected to the discharge resistor for a period of time determine by the controller, and energy is wasted upon the resistor. Fig. 1.11 presents a single cell, connected to a discharging resistor and a switch.

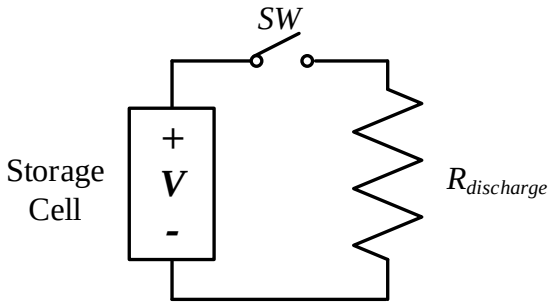


Fig. 1.11 Passive cell balancer with bleed ressitor.

Fig. 1.12 presents *N* cells connected serially with a passive balancer connected to each cell.

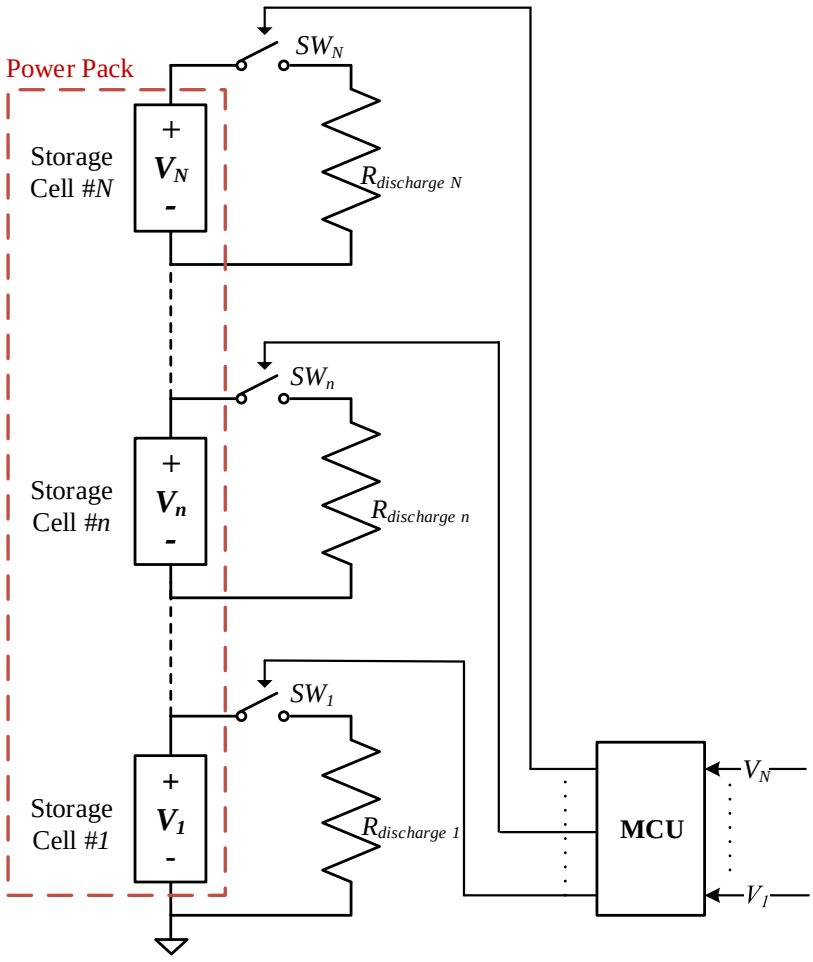


Fig. 1.12 A power pack with N cells connected to passive balancing system. MCU samples the cells' voltages and determine which cell should be balanced.

1.2.5. Active balancing

Active balancing method is based on the active transport of the energy among the cells. There are several types of active balancing methods based of the type of energy transfer. The energy transfer can be from one cell to the whole battery, from the whole battery to one cell, from cell to cell or all methods together. The energy transfer can be done using a DC-DC converter. The energy is transferred from the strongest cells in order to charge the weakest cells.

Fig. 1.13 shows a power pack consists of *N* storage cells connected to an active balancer based on bi-directional converter. The connection is through a switching network. The switching network choose a single cell to be connected to one side of the converter while the other side of the converter connected to the whole chain. Then, control signals, coming out of an MCU, select the cell and determine the direction of energy flow.

Fig. 1.14 shows cell-to-cell energy transfer controlled by MCU through a switching network.

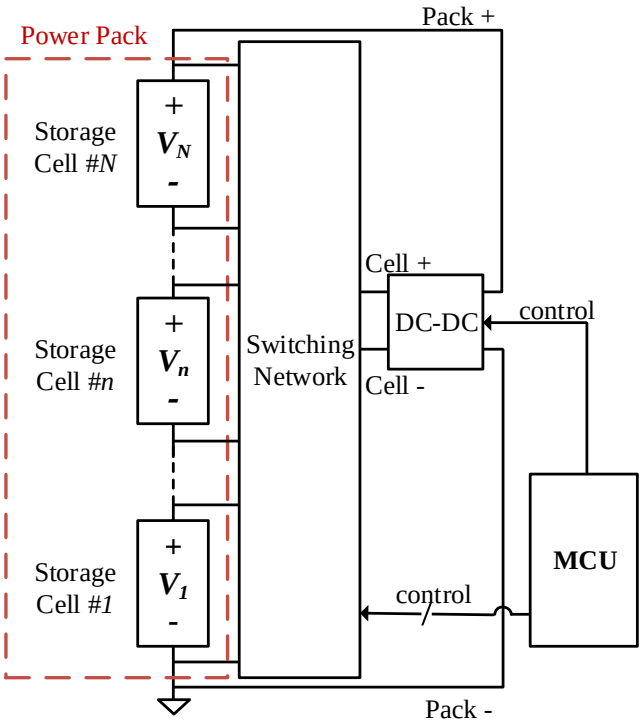


Fig. 1.13 Active balancer: a bi-directional DC-DC converter transfer energy between one cell to the whole power pack.

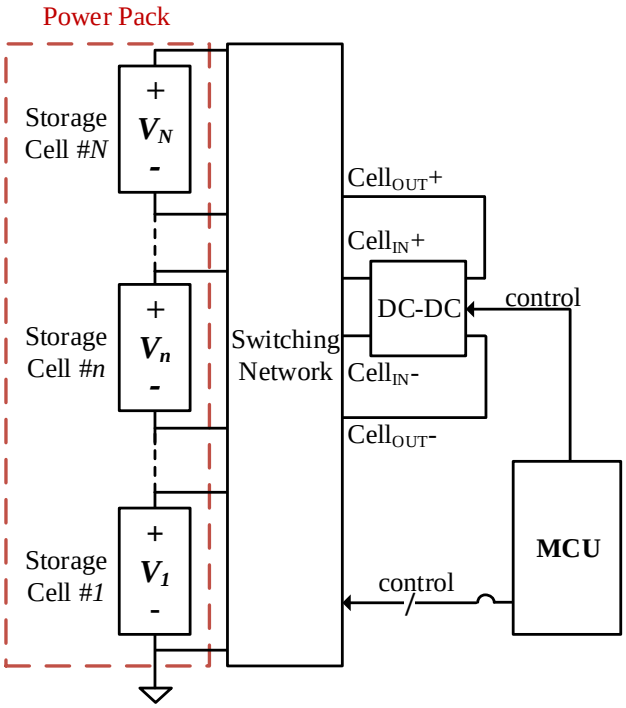


Fig. 1.14 Active balancer: a DC-DC converter transfer energy from one cell to another cell.

As one can understand, active balancer is a very effective method, it can save the energy without waste it. Basically, we can recycle the energy and organize it inside the pack's cells to reach balanced cells. The DC-DC converters should be very efficient because balancer should always work since the cells always lose from their balance. Therefore, as most efficient the converters are, the more energy will be saved especially for high power pack.

The main disadvantages of active balancing are: first, it's a complicated method. As long as the energy transfer is more flexible (i.e. we can transfer energy from in any form), the more complicated implementation and algorithm are. Second, implementation of active balancer is much expensive related to passive balancer. Active balancer includes many components: switches, magnetic elements and many more passive elements. In addition, an MCU must be included in the design, to handle the balancing method and to control the DC-DC converters. Of course, a driving circuitry should be added to drive dozens or hundreds switches and therefore makes a complicated design. As a result, the active balancing method is more expensive and has bigger volume than the passive balancer.

An easier method to perform an active cell balancing is by transferring an energy only between adjacent cells. In this method a switching matrix is not needed but between every two adjacent cells there's a small DC-DC converter. It based on a small reactive component, inductor or capacitor, which can store small amount of energy from one cell and deliver it to

the adjacent cell. The main methods' work as mention, are the switched-inductor and switched-capacitor active balancing.

1.2.5.1. Switched-inductor active balancing

Fig. 1.15 shows cells with active switched-inductor balancer. Both Fig. 1.15a and Fig. 1.15b present a balancing cycle operation with four steps. Fig. 1.15a presents energy transfer from bottom up and Fig. 1.15b presents energy transfer from top down.

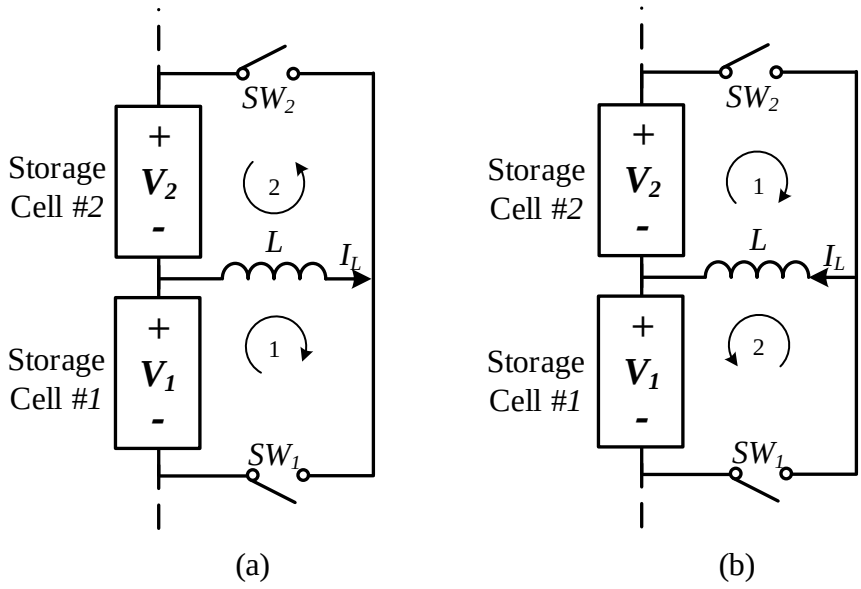


Fig. 1.15 Switched-inductor active balancing: energy transfer between every two adjacent cells: (a) from lower cell to upper cell, (b) from upper cell to lower cell.

Usually, a DCM operation is used: every cycle starts and ends with zero inductor's current, i.e. I_L=0. During the first half of the cycle inductor's current is ramping up and some energy is taken from the more energized cell and stored in the inductor. Then, that energy is delivered to the second cell in the second half cycle. The peak value of the current is varying as a function of the first cell's voltage. Each cycle has four phases. Four phases, in the case of Fig. 1.15b, are described as follows (see also Fig. 1.16):

$t_0 < t < t_1$: sw_1 in conducting and cell1 with the higher SoC/voltage, is connected to the inductor. The voltage across the inductor is almost DC and his current is ramping up with slope: $\frac{di}{dt} = \frac{V_1}{L}$. The inductor is charged with some energy $E_L = \frac{1}{2} \cdot L \cdot I_p^2$.

$t_1 < t < t_2$: short dead time: Neither sw_1 nor sw_2 are conducting. I_L continues to flow with ZVS to the upper cell, the voltage across the inductor is V_2.

$t_2 < t < t_3$: the cell with the lower SoC/voltage, cell2, is now connected to the inductor through sw_2 and current is flows to the second cell. The energy stored in the inductor is

transfers to the cell and charges him up. The voltage across the inductor is the cell voltage and also $\frac{di}{dt} = \frac{V_2}{L}$.

$t_3 < t < t_4$: long dead time. Neither *sw₁* nor *sw₂* are conducting. I_L=0 when the inductor's energy is fully discharged.

As mentioned before, inductor's current peak is determined by the first cell voltage as follows: $I_{L_{peak}} = \frac{V_1}{L} T_{ON}$. We must ensure that the current reaches zero until the end of the second half cycle in order to operate in DCM. The negative slope of the current during the second half cycle is a function of the second cell's voltage: $\frac{dI_{L_{peak}}}{dt} = \frac{V_2}{L}$ therefore, we need to be provide enough time, i.e. $T_{OFF}^{min} = \frac{V_1}{V_2} T_{ON} > T_{ON}$.

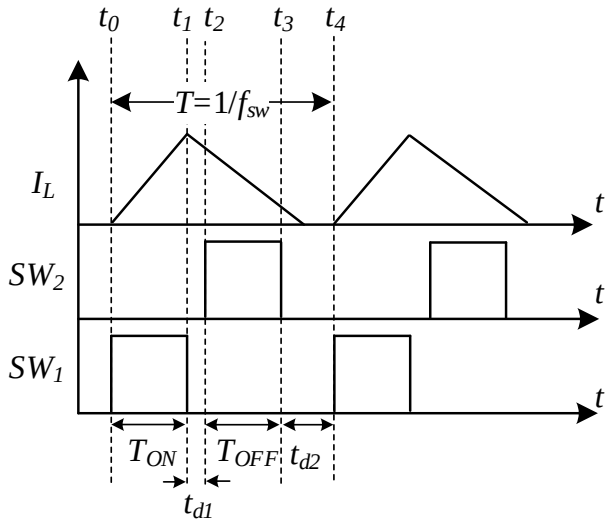


Fig. 1.16 Typical waveforms of switched-inductor active balancing method. Energy transfer from upper cell to lower cell (Fig. 1.15b).

From an efficiency perspective, if, for example, the cell with the lowest voltage is the lower cell in the chain, and the cell with the highest voltage is the upper cell in the chain, the way for the energy to transfer is down through all the cells in the pack. So, for example, if the efficiency of energy transfer from adjacent cells is $\eta_{adj} = 95\%$, the total efiiciency of the whole process is dependent on the number of cells the energy should pass through, *N*. For example, if *N*=10 then the total efficiency is about $\eta = \eta_{adj}^{N} = 0.95^{10} < 60\%$!

1.2.5.2. Switched-capacitor active balancing

Switched capacitor circuits (SCC) are implement by a filter includes only capacitors without any resistors or magnetic elements. The main advantages of this method are: first, it

can be very small in volume because no magnetic elements are needed and second, it can be fabricated as an IC (integrated circuit). Another advantage is minimal EMI.

The simplest switched-capacitor balancer, consists of a single capacitor and four switches as presented in Fig. 1.17. Typical waveforms during operating cycle demonstrated in Fig. 1.18:

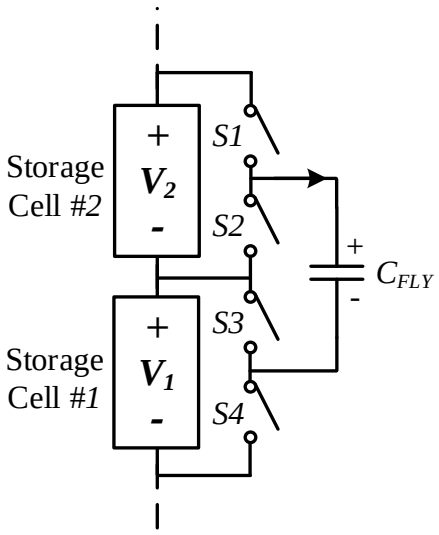


Fig. 1.17 Switched-capacitor active balancer circuit, switching sequence is: S1, S3 and S2, S4.

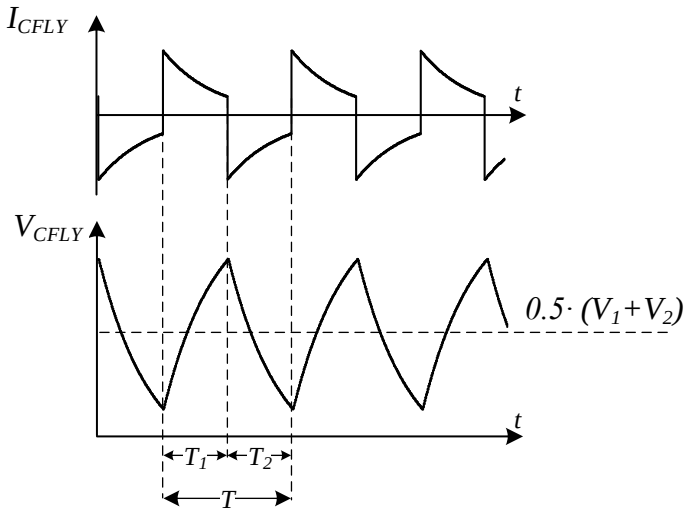


Fig. 1.18 Switched-capacitor active balancer voltage and current waveforms of the flying capacitor during steady-state operation. T_1: (*S1, S3* ON) flying capacitor is connected directly to the cell with the higher voltage,V_1, the curent jumps up and capacitor charged toward V_1. T_2: (*S2, S4* ON) flying capacitor is connected firectly to the lowest voltage cell and discharged his energy until $Vc_{FLY}=V_2$.

The switched-capacitor (C_{FLY}), sometimes calls 'flying capacitor', is alternating in between two cells and transfers charge ***q*** from the higher to the lower potential with a given frequency f_{sw}, aiming to level the cells' SoC/voltages. Switched-capacitor method based on the difference between the cells' voltage. Charge is running from cell to cell as long as there is a difference. During balancing, the delta between voltages is get smaller and smaller and

also the current flows in the switched-capacitor decreases down to zero with full equalization. The main problem with this method is that significant energy losses occur during operation capacitor charging, as maximal efficiency of this process is 50%. Another disadvantage is that the transfer rate of this method is proportional to the voltage differences between the unbalanced cells – inefficient method with low transfer rate.

1.2.5.3. Resonant-switched-capacitor active balancing

An improved way to transfer charge with switched capacitor is by changing the behavior of the charge transfer process from flying capacitor behavior into resonant switched-capacitor (RSC) behavior. The resonant behavior allows volume reduction of the magnetic element by allowing higher frequency operation. Thanks to the soft-switching capabilities, the overall power conversion efficiency is not compromised due to the higher operating frequency [14], [15].

RSC method is built from a capacitor and a small inductor. The addition of a small inductor in series with the capacitor, help in determine the exact resonant frequency. This changes the waveforms of the current and voltages in the balancer to a more sinusoidal and smoother shapes. Those kinds of waveforms reduce the stress across components (MOSFETs, switched-capacitor, inductor) and let the designer choose components for lower voltage, current and stress which are much smaller. Also, from efficiency perspective, sinusoidal shapes enable soft-switching operation (ZCS) reduces power loss and thermal efforts.

Efficient operation of the RSC should be with switching frequency equal (or very close) to the resonant frequency:

$$f_r(RSC) = \frac{1}{2\pi\sqrt{LC}}. \quad (1.10)$$

RSC requires precise capacitance in order to achieve particular resonant frequency or else it needs special control do detect zero current[16]. The following figures demonstrate the topology and operation of the RSC active balancer:

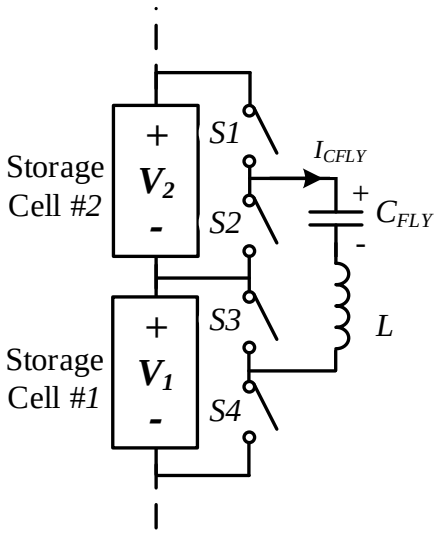


Fig. 1.19 Resonant-switched-capacitor active balancer circuit. switching sequence is: S1, S2 and S3, S4.

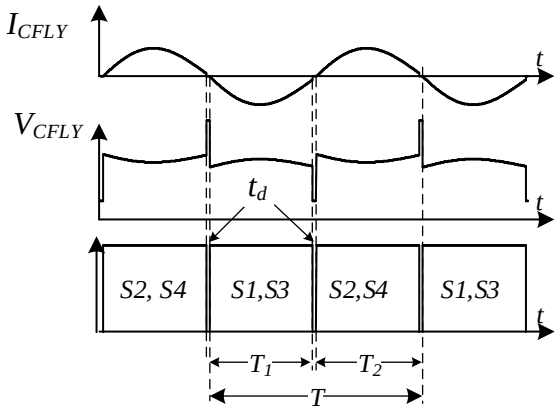


Fig. 1.20 Resonant-switched-capacitor active balancer voltage and current waveforms of the flying capacitor during steady-state operation: T_1: (*S1*,*S3* ON) resonant current flows from cell2 to the flying capacitor charges it with some energy, T_2: (*S2*, *S4* ON) the flying capacitor discharges upon cell1 with resonant current.

2. Capacitor Charger

As already mentioned in the previous section, the ESC (energy storage cell) are stacked on top of each other to increase the voltage of the power pack, and also in parallel to increase the energy and power of the ESS (energy storage system). At this work, particular storage cell was used to implement the thesis on - capacitor.

Capacitor can accumulate and stores high voltage for a period of time. Just like a battery, the capacitor can be charged to a maximum energy as function of its capacitance and the voltage across him by the following equation:

$$E = \frac{1}{2}CV^2. \tag{2.1}$$

But unlike the battery, capacitor can be charged and discharged by a high current, in seconds, and can withstand many cycles of operation without being damaged. That characteristic, let the capacitor be the primary component in every pulsed power application.

Pulsed power is a technology that accumulate energy in capacitors charged to high voltages over some period of time, and then release that energy, across any load, very quickly. Very high energy is delivered very quickly which means that the power released is huge. That instantaneous power let us build many useful and powerful applications: coilguns, railguns, spot welding machine, and more.

Capacitor charger intended to charge single or multiple capacitors as quick as it can. It should charge the energy bank, capacitors, quickly enough so the energy will be ready for the next cycle consumed by the application. In order to get a high pulse of energy, huge bulky capacitors, with high capacitance values are used (2.1).

The simplest approach, is to use a single stage low voltage converter to charge the storage capacitor. Fig. 2.1 presents a capacitor charger based on that approach:

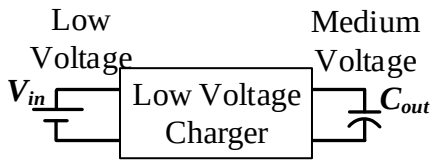


Fig. 2.1 Low voltage capacitor charger, with a single capacitor at the output, rated to medium output voltage.

In this approach charge time could become lengthy and the final voltages are rather limited.

Capacitor Charger

Another approach is to use a high voltage charger, which could include several stages. While being able to reach high voltages, this solution becomes rather bulky with multiple stages and buffers. Fig. 2.2 shows a typical high voltage charger approach.

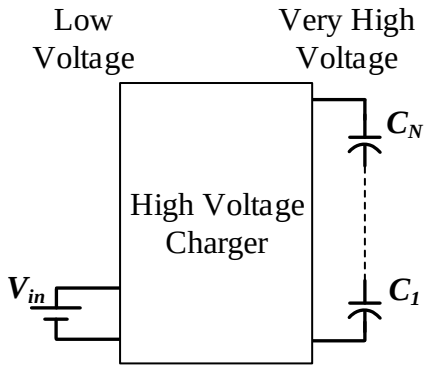


Fig. 2.2 High voltage capacitor charge, with multiple capacitors stacked at the output with very high output voltage.

Both of the approaches are generally charge a single bulky capacitor at the output, which limit the utilization of energy storage to a single discharge source. Basically, large number of storage capacitors can be used serially and in parallel (see section 1.2.2), we can except that they will be subject to a higher failure rate than a single storage capacitor. The more capacitors used, the greater the opportunities to fail and the worse the reliability. Because of production tolerances, uneven temperature distribution inside the pack and differences in the aging characteristic of particular capacitor, it is possible that individual capacitors in a series chain could become overstressed leading to premature failure of the capacitor. During the charging cycle, if there is a degraded cell in the chain with a diminished capacity, there is a danger that once it has reached its full charge it will be subject to overcharging until the rest of the cells in the chain reach their full charge.

More convenient approach to charge many capacitors to very high voltages, is to boost the input voltage to some intermediate level, and then employ multiplying circuits to create a number of equally charged capacitors, stacked on top of each other. Fig. 2.3 demonstrates the capacitor charger consists a voltage multiplier.

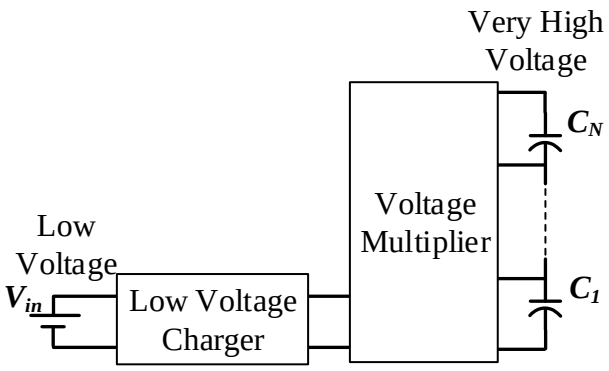


Fig. 2.3 Capacitor charger rated to a very high output voltage utilizes a low voltage charger and voltage multiplier.

Fig. 2.4 shows 3 modes of a typical capacitor charger supply. First is the charging mode when the output capacitance is being charged to the targeted value, V_T (blue trace). The shape of the output voltage during charging is drawn as a linear for illustration purpose only but many times capacitor charger power supplies designed to operate as a current source.

During charging, the output voltage varies over a wide range in comparison to a conventional DC power supply and that means the output impedance is also varies dramatically (from zero to very high impedance) during the charging mode. When the output capacitor is fully charged, i.e., $V_{out}=V_T$, the energy is ready to be used for the application. During the refresh mode the charger operate in a low power, compensate for capacitors leakage. Finally, discharge mode, very high-power releases from capacitors but the charger is not powered.

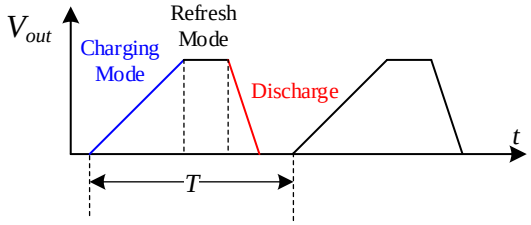


Fig. 2.4 Three modes of operation of a capacitor charger

2.1. Voltage multiplier

One common structure used with capacitor charger power supply is the voltage multiplier. A voltage multiplier converts low AC voltage to a higher DC voltage using a network of capacitors and diodes. Voltage multiplier can double the input voltage once, twice or multiple times and so reach hundreds of kilovolts. The first voltage multiplier was created by Walton and Cockcroft in 1932 but since then voltage multipliers have become very essential for high voltage application like capacitor charger power supply. Voltage multiplier

is a rectifier circuitry that increase the amplitude of the input signal and it's constructed as a ladder built with many diodes (or switches) and capacitors while the voltage across each one of those components is much smaller in comparison to the output voltage.

2.1.1. Cockcroft-Walton multiplier

The classic multistage diode/capacitor voltage multiplier generating high voltages at low currents. It is used in virtually every television set made to generate the 20-30 kV from a transformer putting out 10-15 kV pulses. Also, it inherently produces a series of stepped voltages which is useful in some forms of particle acceleration. The disadvantage of Cockcroft-Walton (CW) multiplier is a poor voltage regulation, thus heavy load makes a drop at the voltage output. Fig. 2.5 presents CW voltage multiplier with input voltage source, V_s, with an amplitude equal to V_{in} which multiply the input sinusoidal voltage by four, i.e. $V_{out}=4V_{in}$. Also, two more stepped voltages are generated: $3V_{in}$ and $4V_{in}$.

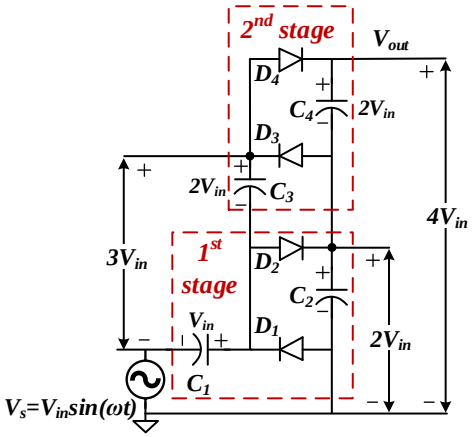


Fig. 2.5 Double stages Cockcroft-Walton voltage multiplier with ac input source, V_{in}, and series of stepped voltages.

The operation of one stage, i.e. double output voltage, is showed in Fig. 2.6 described as follows: in the first positive half-cycle (1st phase) diode D_1 is in reversed biasing condition while D_2 is in forward biasing condition. Current flows through both capacitors and will charge C_1 to negative voltage and C_2 to positive voltage. In the negative half-cycle (2nd phase) D_1 is in forward biasing condition and C_1 is charged in the positive polarity with much higher current than at the 1st phase which lead to inclined charging. Diode D_2 is in reversed biasing condition. Fig. 2.7 presents currents and voltages waveforms during the first cycles of operation.

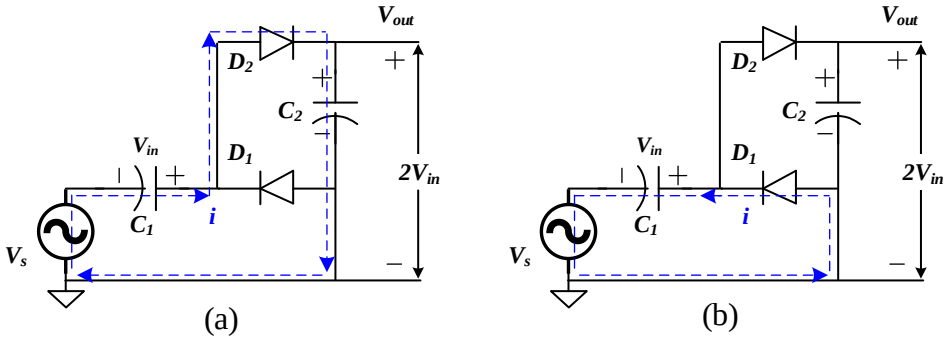


Fig. 2.6 Single stage CW voltage multiplier configuration and operation principle: (a) positive half-cycle, (b) negative half-cycle

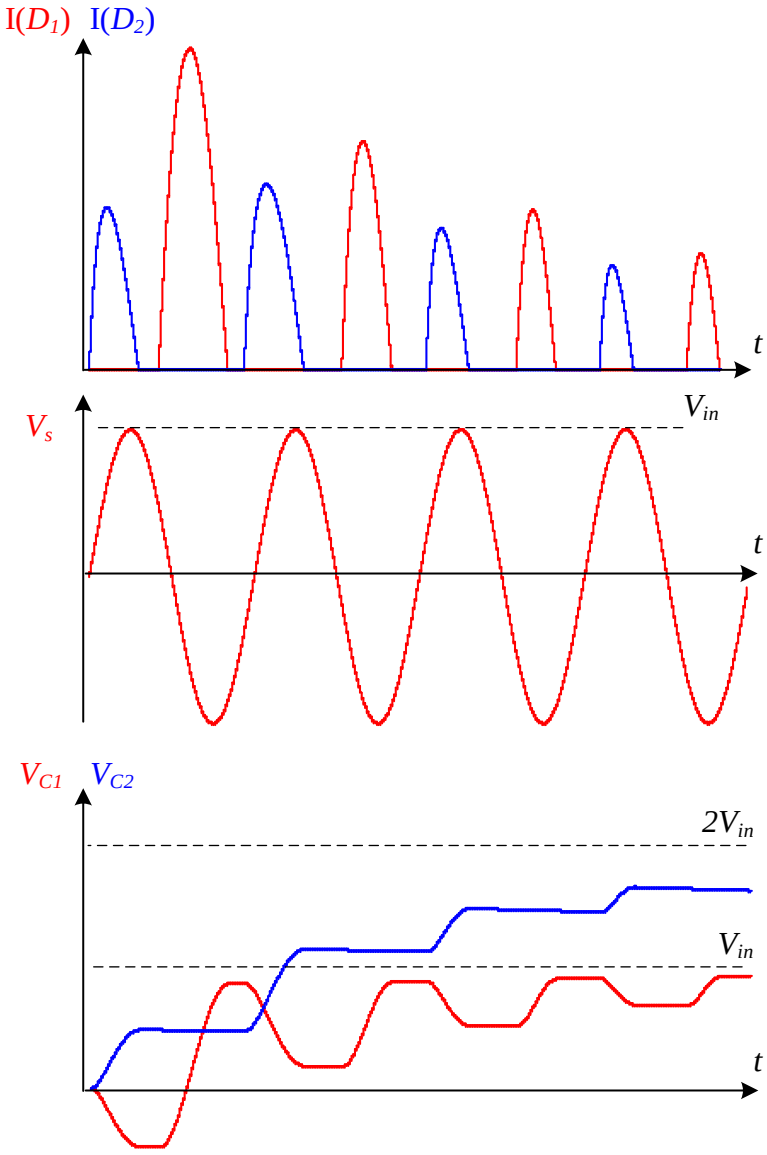


Fig. 2.7 Single stage CW typical waveform capacitors voltages and diodes currents.

Now, to understand the operation of double stages CW voltage multiplier, we can look at the 2nd stage just like the 1st stage but now the whole stage is ramped up by the capacitors' voltages, VC_1 and VC_2. Fig. 2.8 presents double stages CW voltage multiplier with marked

potential points: A, B, C, D where points A and B are the input and ground reference voltages points of 1st stage, respectively and points C and D are the input and reference voltage points of the 2nd stage, respectively. Output voltage of 1st stage is between points B and D while output voltage of 2nd stage is between V_{out} and point D. Each stage generates DC voltage equal twice the amplitude of the voltage source. Attention should be paid that the voltage of the odd capacitor of 1st stage is $V_{C1}=V_{in}$ while the voltages of the odd capacitor in higher stages is equal to $2V_{in}$, i.e. $V_{C(2i+1)}=2V_{in}$ for i=1,2,3,…

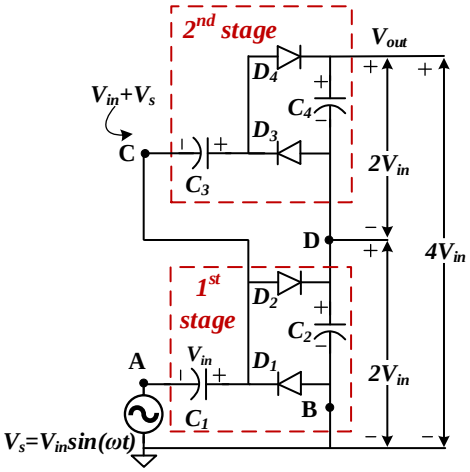


Fig. 2.8 Double stage CW voltage multiplier

2.1.2. Full-wave voltage doubler

That kind of voltage multiplier rectifies symmetrically the ac input voltage V_{in}. In each half cycle one of the diodes conducts, and one of the capacitors is being charged to V_{in} amplitude: when the input voltage is positive, capacitor C_2 charges up through diode D_2 and when the input voltage is negative, capacitor C_1 charges up through diode D_1. As a result, each of the output capacitors charged to the input voltage amplitude, V_{in}, and the output voltage taken across them both. Fig. 2.9 shows two full wave voltage multipliers with different power input stage circuit. Fig. 2.10 shows input and output voltages. As can be seen, in this voltage multiplier, the output voltage capacitors charged in doubled frequency in relation to input voltage source frequency. A half wave voltage multiplier's capacitor, for example, get charged once in a cycle and not twice, forcing a bigger capacitor value for the same load.

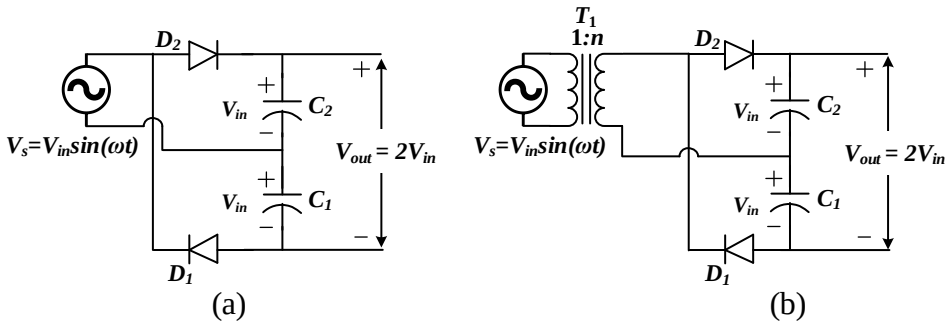


Fig. 2.9 Full wave voltage doubler circuit: (a) non-isolated topology charged to $V_{out}=2V_{in}$, (b) isolated topology implimented with transformer with *1:n* turns ratio for higher gain, $V_{out} = n \cdot 2V_{in.}$

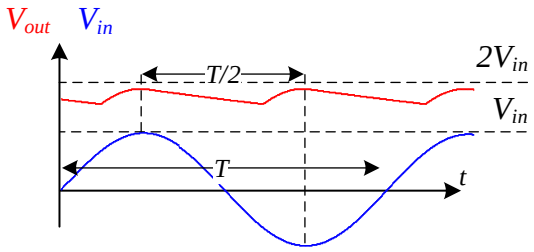


Fig. 2.10 Typical waveforms of full-wave voltage doubler. Every half-cycle one of the output capacitor charged, refreshing the output voltage in doubled frequency.

3. Multilevel High-Voltage Modular Rapid Capacitor Charger

This chapter introduces a multilevel high-voltage modular capacitor charger. The unique architecture allows a single front-end to charge several capacitors connected in series with actively balanced voltages. Charge redistribution between the capacitors is carried out using a switched-capacitor balancing circuits. The system's multilevel structure, and modularity that stems from isolated design, enables charging of a distributed energy storage to very high voltages, while the component ratings and stresses are only a fraction of the total voltage. Using this approach, the designer is free to choose optimal energy storage and switching components, rather than using bulky, limited in options high voltage components. The architecture has been validated by simulations as well as on an experimental prototype of 1kW that has been constructed, validating capacitor charging to 1.2kV per module from a 12V input.

3.1. Overview

Pulsed power applications are mostly implemented in a structure where high voltage, high power energy storage is discharged to the load [17]-[23]. The best candidate for high power energy storage is a capacitor, or bank of capacitors. The common implementation approach of these systems is selecting a high voltage single capacitor which is then charged to the voltage proportional to the amplitude of the pulse. Some obvious drawbacks of this approach include the fact that high voltage capacitors are large and bulky, rendering the design to be bulky as well. Another drawback is a complex high voltage capacitor charging power converter, required to charge the energy storage. To mitigate two of these down sides, a new multilevel high voltage modular capacitor charger architecture is introduced in this study (Fig. 3.1). Multilevel architecture enables the designer to select lower voltage capacitors and charging converter components, which are superior in size and power density comparing to their higher voltage counterparts, reducing the overall size and volume of the system. The modularity of the system enables to extend the voltage of the energy storage to much higher amplitudes than a single module, while still maintaining the advantage of the very low stress per component. The unique architecture utilizes cell equalization approach to keep the capacitors in the chain equally charged [24]-[39]. Additional advantage of the multilevel architecture is the ability to design multisource discharge pattern to accommodate multistage loads such as a multi-winding magnetic acceleration device targeted in this study. The rest of the chapter is organized as follows: section 3.2 describes system architecture, section 3.3

presents design and optimization considerations, section 3.4 presents some validation results, and section 3.5 concludes the chapter.

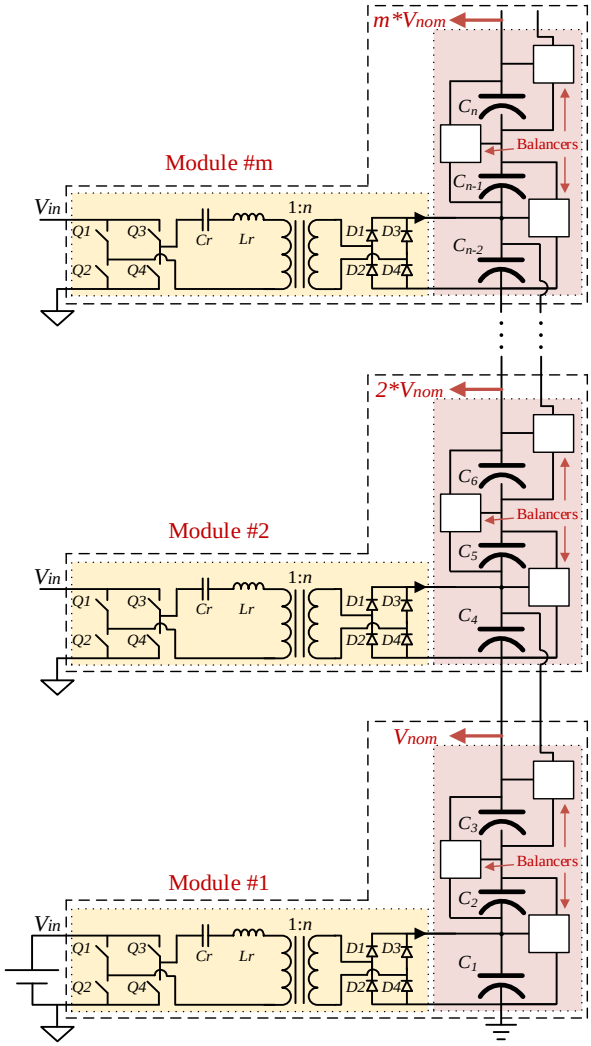


Fig. 3.1 Multilevel high voltage modular capacitor charger

3.2. System architecture

3.2.1. System overview

The system is built around *m* modules on top of each other, where each module has a number of serially connected storage capacitors, three in this study. The module consists of an isolated charging converter that is connected to a bottom storage cell out of a chain of serially connected energy storage cells. Storage cells employed in this study are capacitors to sustain high voltages, but from a topological perspective can be replaced by either supercapacitors or battery cells. The charging converter is programmed to transfer charge from the source to the bottom capacitor, limited by the maximum converter power. The chain of serially connected capacitors is interconnected with balancing circuits that are responsible to redistribute the charge from the bottom cell, receiving capacitor, to the rest of the cells in

the chain. In this architecture, the charge from the source arrives to each of the serially connected capacitors, and is distributed between them. One extra balancing circuit per module is added to maintain equalization between the modules.

3.2.2. Capacitor charger

There are several options to implement a capacitor charger [40]-[44]. As can be seen in Fig. 3.2, in this study the capacitor charger is built around a double bridge series resonant converter, where the input bridge is active (comprises of transistors), and the output rectifier is realized with diodes. Within the context of a capacitor charger, a resonant converter is preferred over a PWM type converter because of several factors: (a) regulation of charge transfer to the load; (b) operation in ZCS; and (c) the output impedance characteristics it presents to the output capacitor. A step-up transformer is used for both isolation and step up of the input voltage. The resonant tank consists of a resonant capacitor C_r and resonant inductor L_r, while leakage inductance of the isolation transformer can function as a resonant inductor [38], [45]. Capacitor charger operation is similar to a conventional resonant converter operated in DCM. The switching frequency, f_s, is set to be lower than the resonant frequency, f_r, i.e. $f_s < f_r$, to maintain DCM operation. An additional switch Q_5 is introduced to enable DCM operation at all time, and to avoid current back flow to the source. Current back flow takes place due to the large voltage difference between the input voltage and the output voltage mirrored to the primary during the charging operation of the system. Due to the high-quality factor the resonant tank charges up and develops resonant capacitor voltage that exceeds the input voltage. High resonant capacitor voltage flips the direction of the resonant current during the dead time, forcing the body diodes of the active bridge MOSFETs to conduct. This condition results in energy loss and unnecessary current circulation that is overcome with additional switch Q_5, which is turned on and off under ZCS conditions.

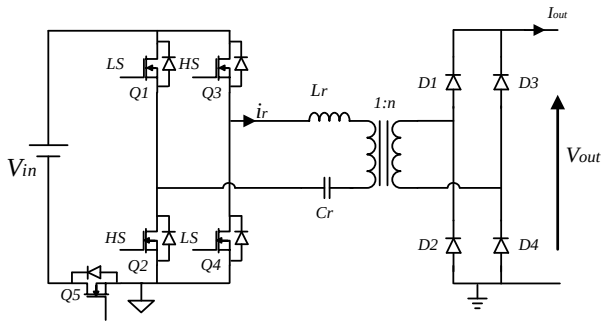


Fig. 3.2 Full bridge isolated capacitor charger

3.2.3. Balancing circuit

To enable charge flow between the bottom capacitor, charged by the capacitor charger and the rest of the storage capacitors, a network of charge redistribution converters is used, the balancing circuits [24]-[39]. Each balancing circuit is built around a resonant switched-capacitor converter and designed to support two adjacent capacitors. Each balancer consists of two half bridges each in parallel to the storage capacitors, and a resonant tank, which is the switched capacitor cell. Each pair of storage capacitors has balancing circuit attached to it as can be seen in Fig. 3.3a. Running the switches at the resonant frequency of the switched capacitor cell with approximately 50% duty cycle enables voltage equalization of adjacent energy storage cells [25]-[29].

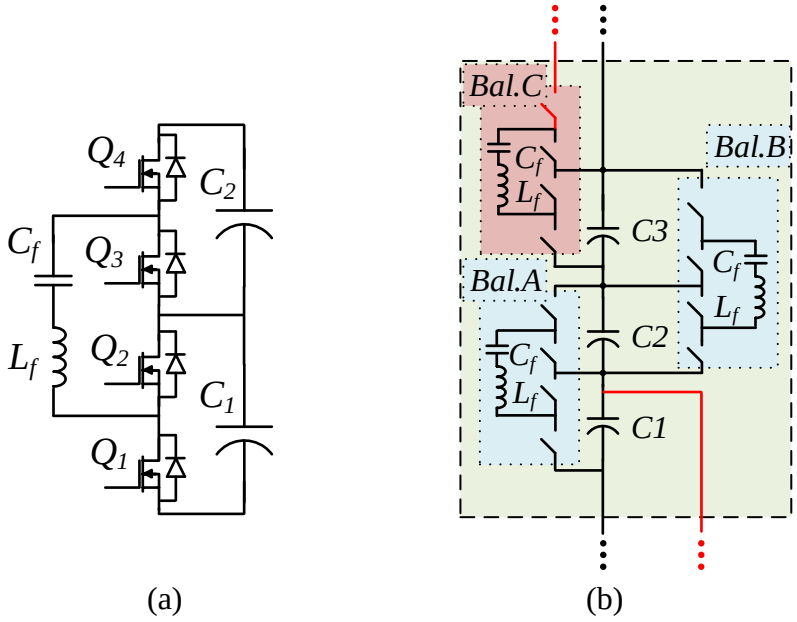


Fig. 3.3 Balancing circuits: (a) A single balancer schematic; (b) Balancers extra hardware for multimodule compatibility (balancer *C* and traces highlighted in bold red).

3.2.4. Extension to m modules

The multilevel capacitor charger employed in this study is compatible to be extended serially to increase the maximum voltage of the energy storage. Each unit that includes the charger and balancer is treated as a single independent module rated for a nominal voltage of V_{nom} (Fig. 3.1). It becomes possible due to the isolation transformer used in between the primary and the secondary bridges of the double bridge charging converter, and independent operation of each of the modules, where balancing circuits equalize the cells within each module. Connecting in series *m* of these modules enables to extend the voltage rating of the energy storage. The primary side of each charger is connected in parallel to the voltage source, while the output part is connected in series to each other, (Fig. 3.1), stacking the

storage capacitor chains on top of each other. An extra balancing circuit, Balancer C, (Fig. 3.3b), is added to each module for serial connection compatibility. The extra balancer is in charge to equalize between the last storage cell of its own module and the first storage cell of the module above in the chain, maintaining continuous balancing along the whole serial stack of storage capacitors.

3.3. Design and optimization considerations

3.3.1. Industry inclined system optimization

Technology development in the modern world is majorly incremental, with rare exceptions that bring a break through and push us to a new technological level. In this environment, freshly invented technology becomes mature in a period of several years to a decade, and it is commercialized to support new or improved product. Commercialization process doesn't necessarily treat equally every application. Some applications are favored by higher consumer demand, or governmental legislation and standards. As a result, favored products get an increased interest and see increased incremental development over their peers from the same technology, until the next break through arrives.

An example of component selection based on industry inclined optimization related to this study, would be a selection of an energy storage, a capacitor, which occupies minimum space and supports maximum charge storage rated for 1.2kV. Fig. 3.4 demonstrates commercially available aluminum electrolytic capacitors spread, where the energy per unit volume is the performance metric, while rated capacitor voltage is the parameter. Several maximum performance points are outlined, which coincide with industry interest voltage ratings in the fields of automotive (12-24V point A in Fig. 3.4), data centers (48V point B in Fig. 3.4), and grid connected applications (250V for US points C and D in Fig. 3.4, and 350-400V for EU points E, F and G in Fig. 3.4). Examining Fig. 3.4, the capacitor at point G has been selected to achieve the best energy per volume for the maximum voltage of a 1.2kV. The approach is to connect in series 3 capacitors rated for 450V each that are optimized for the EU grid, to achieve 1.2kV. The common practice of selecting a single bulky capacitor rated for the maximum required voltage is the least favorable approach in terms of energy per volume. The same industry inclined optimization is true in regards to switching elements. Switches rated for 500V for example, are better in terms of power density than the switches for 1.2kV. To achieve the benefit of industry inclined optimization a unique multilevel modular architecture is required, similar to the one introduced in this study. Three serially

connected capacitors constitute the energy storage of each module, to provide output of 1.2kV.

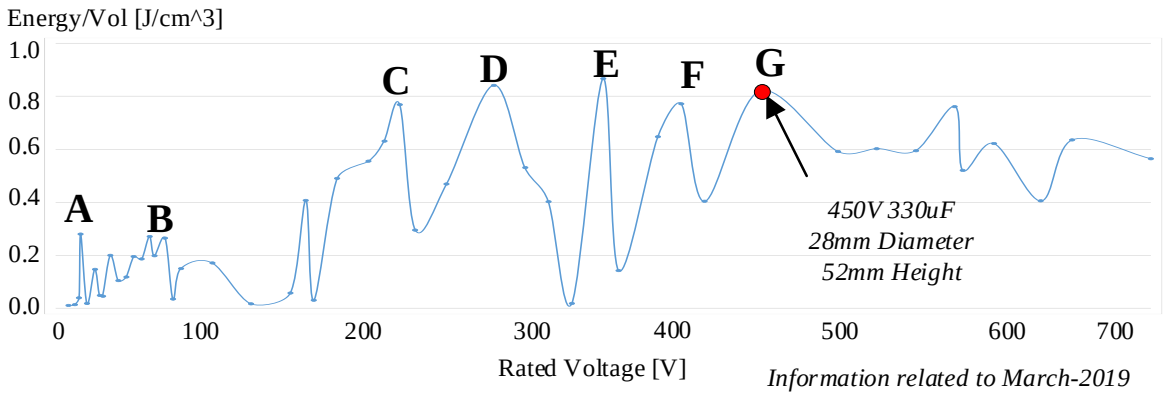


Fig. 3.4 Capacitor's energy density vs. maximum voltage rating

3.3.2. Design considerations

The regulation approach of the charging converter used in this study is the Pulse-Frequency Modulation (PFM). Input voltage source is connected to provide current for a predefined time frame, the half resonant frequency period of the tank and the width of the pulse, $T_r/2$. Regulation parameter in this case is the switching frequency, which controls the density of the pulses and the amount of the processed energy. The ratio between the pulse width and the switching cycle length, T_s, is defined as $D = T_r / T_s$, where T_r is always smaller or equal to T_s.

Next to the voltage considered as the full charge, and capacity of the energy storage, which are dictated by the application, the major parameter to be considered by a designer is the time available to charge the capacitor, T_{chrg}, which sets the nominal power and physical volume of the charger. To calculate T_{chrg} for presented topology we assume that the balancing circuits are lossless, and shuttle the charge instantaneously between storage capacitors, which is a reasonable assumption as long as the balancers are sized according to the required power level. As a result, the total output capacitance of the charging stage equals the sum of all the storage capacitors in the module, three times the capacitance in the case presented here. Averaging the net amount of charge provided by the charger to the output each half of its switching cycle, we calculate output voltage increment that took place from the end of the previous cycle. The increment, ΔV_{out} is a function of switching period and the average current:

$$\Delta V_{out} = \frac{I_{avg}}{C_{out}} \frac{T_s}{2}, \tag{3.1}$$

substituting the expression for average current I_{avg} into (3.1), voltage increment takes the form of:

$$\Delta V_{out} = \frac{2}{\pi} \cdot I_{r\_pk} \cdot D \cdot \frac{T_S}{2C_{out}} = \frac{2}{\pi} \cdot \left(\frac{V_{in} - \frac{V_{out}}{N}}{R} \frac{1}{N} \right) D \frac{T_S}{2C_{out}}, \tag{3.2}$$

where N is transformer's turn ratio. Finally rearranging (3.2) into (3.3) results in a straightforward expression.

$$\Delta V_{out} = \frac{D \cdot T_s}{N \cdot R \cdot C_{out} \cdot \pi} \cdot \left(V_{in} - \frac{V_{out}}{N} \right). \tag{3.3}$$

The voltage in n-th half-cycle can be calculated by adding the voltage at the previous half-cycle, i.e. $V_{out}[n\text{-}1]$, plus the voltage increment developed in (3.3):

$$V_{out}[n] = V_{out}[n-1] + K \left(V_{in} - \frac{V_{out}[n-1]}{N} \right), \tag{3.4}$$

where K is the ratio between the output time constant and the switching period $K = DT_s / (NRC_{out}\pi)$ and R is the total loop resistance including stray resistance, capacitor ESR, MOSFETs R_{ds_on} and inductor resistance. Applying (3.4) for each of the half cycles preceding n-th half cycle, an equation for the voltage $V_{out}[n]$ could be written, where a first member is the initial capacitor voltage $V_{out}[0]$:

$$V_{out}[n] = K \cdot V_{in} \left[1 + \left(1 - \frac{K}{N} \right) + \left(1 - \frac{K}{N} \right)^2 + \cdots + \left(1 - \frac{K}{N} \right)^{M-1} \right] + \left(1 - \frac{K}{N} \right) V_{out}[0] \tag{3.5}$$

The expression in the square brackets in (3.5) is a geometric series, which can be rearranged to express the target charge voltage V_T as a function of the number of half cycles M:

$$V_T = V_{out}[M] = KV_{in} \sum_{n=0}^{M-1} \left(1 - \frac{K}{N} \right)^n, \tag{3.6}$$

where $V_{out}[0]$ is assumed to be 0 volts, i.e. a charge from completely discharged capacitors. The sum of (3.6) has a finite expression:

$$V_T = NV_{in} \left[1 - \left(1 - \frac{K}{N} \right)^M \right]. \tag{3.7}$$

Rearranging (3.7) for M, the number of **half** switching cycles to charge the output capacitor to targeted voltage, V_T, can be summarized as:

$$M = \frac{\log\left(1 - \frac{V_T}{NV_{in}}\right)}{\log\left(1 - \frac{K}{N}\right)}. \tag{3.8}$$

Multiplying (3.8) by the switching **half** period and dividing by the duty cycle, the charging time to reach a target output voltage can be expressed as:

$$T_{chrg}(V_T) = \frac{\log(1-\frac{V_T}{NV_{in}})}{\log(1-\frac{K}{DN})} \frac{T_r}{2} \frac{1}{D}, \tag{3.9}$$

where the resonant time is defined as: $T_r = 2\pi\sqrt{L_r C_r}$. Equation (3.9) presents a finite and closed solution for the time required to achieve a certain final capacitor voltage, considering the changes in the charging conditions along the process.

To estimate the heat dissipation an efficiency calculation is carried out. The calculation considers conduction losses only. Since capacitor charging involves extremely wide variation in the output voltage the efficiency constantly changes with the rise of the output voltage. The efficiency of these systems lies in the range of a converter that operates in constant transient mode rather than a converter that operates in steady state, and expected numbers are hover around 30% or sometimes go even lower.

A calculation of an average efficiency of the charging process is based on per cycle efficiency calculation, and averaging of the results. The basic efficiency equation used is shown in (3.10):

$$\eta_{AVG} = 1 - \frac{P_{loss}}{P_{in}}, \tag{3.10}$$

Input power and the losses are calculated in the similar way as described for V_T in (3.6), using the finite sum of the geometric series (full mathematical derivation given in the Appendix). The number of switching cycles is $M/2$ as calculated in (3.8):

$$1 - \frac{P_{loss}}{P_{in}} = 1 - \frac{\frac{DV_{in}^2}{2R}\sum_{n=0}^{M}\left(1-\frac{K}{N}\right)^{2n}}{\frac{2DV_{in}^2}{\pi R}\sum_{n=0}^{M}\left(1-\frac{K}{N}\right)^{n}}, \tag{3.11}$$

Rearranging (3.11) the average efficiency to charge the capacitors to the target voltage $V_{out}=V_T$ can be summarized as:

$$\eta_{AVG} = 1 - \frac{\pi}{4}\frac{1+q^{(M+1)}}{1+q} * 100\ [\%], \tag{3.12}$$

where $q = 1 - \frac{K}{N}$.

3.4. Simulation and experimental validation

To validate the theoretical concepts and operation of the system introduced in this study, a multilevel modular capacitor charger unit has been designed and fabricated. The validation of the concepts using numerical simulation is carried out and three modules of the multilevel modular capacitor charger are built and evaluated in numerical simulator PSIM. The

schematic of the system follows the structure of Fig. 3.1, where three modules are stacked on top of each other, in parallel at the input, and in series at the output. TABLE I summarizes the main parameters of the system including the storage capacitors.

TABLE I. SYSTEM'S PARAMETERS

Parameter	***Symbol***	***Value/Type***
Input voltage	V_{in}	12V
Transformer ratio	N	1:50
Resonant inductor	L_r	1µH
Resonant capacitor	C_r	1µF
Resonant frequency (charger)	f_{r1}	160kHz
Flying capacitor	C_f	0.1µF
Flying inductor	L_f	1µH
Resonant frequency (balancer)	f_{r2}	500kHz
Storage Capacitor	C_{out}	*330µF*
DC Voltage rating	V_{DC}	*450V*
Equivalent series resistance	*ESR*	*1mΩ*

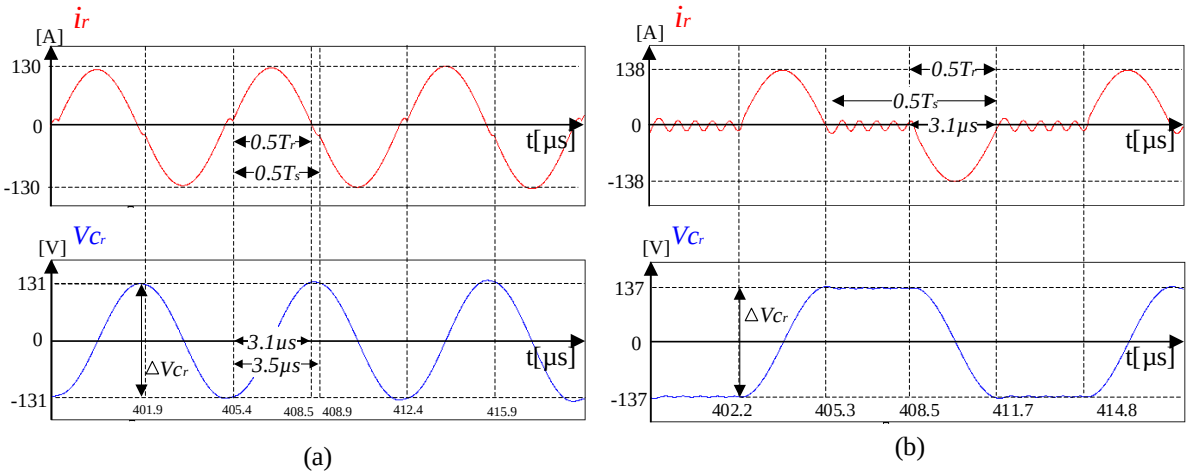
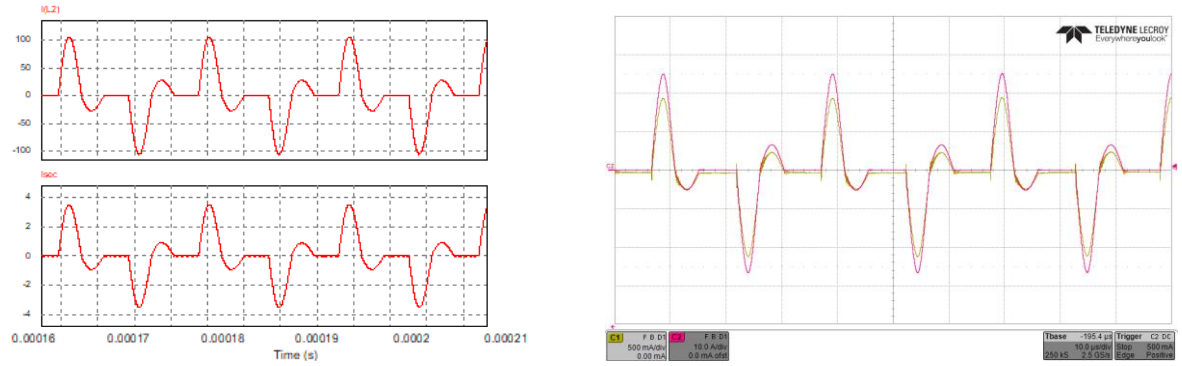


Fig. 3.5 Simulation of charging operation with: (a) D=0.9; (b) D=0.5.

Basic charging operation waveforms are presented in Fig. 3.5 where a 90% duty cycle and 50% duty cycles are demonstrated.

Transformer resonant currents are shown in Fig. 3.6. Simulation results are presented in Fig. 3.6a, and experimental results are shown in Fig. 3.6b. Converter operation includes a main high peak sinusoidal current followed by a smaller resonant shape immediately after it. The second resonant shape is induced due to the high quality factor resonant tank that results in resonant capacitor voltage exceeding the input voltage during some time at the beginning of the charging process when the difference between the input and the output voltages is high. Since the gating of the charger allows some extra time to ensure zero voltage switching in the presence of resonant tank component variation, a reverse current flow from the capacitor is developed and creates a lower amplitude sinusoidal follow up. This follow up however, doesn't impacts efficiency, since it is rectified by the passive rectifier at the

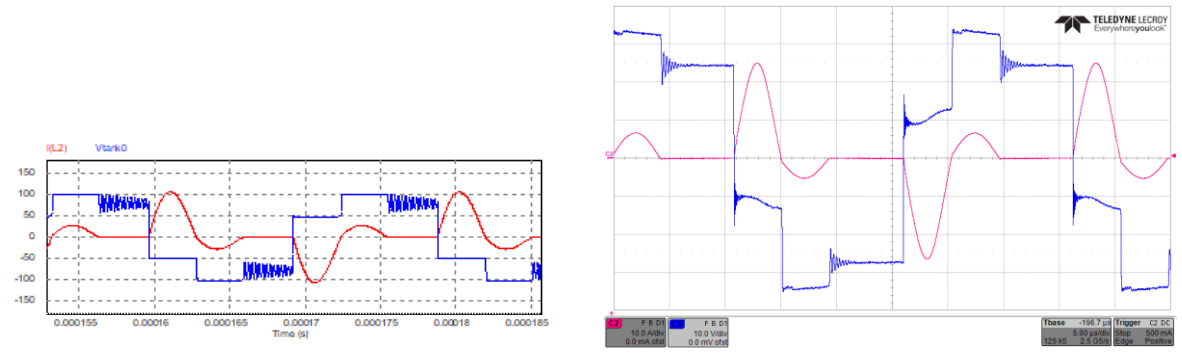
secondary side, and adds to the total converter energy transfer to the output. A good agreement between the simulation and experimental results as demonstrated in Fig. 3.6 was obtained.



(a) (b)

Fig. 3.6 Transformer resonant currents experimental vs. simulation results. (a) Simulation: primary current (top) 50A/div., secondary current (bottom) 2A/div.; (b) Experimental results: primary current (pink) 10A/div., secondary current (yellow) 0.5A/div.

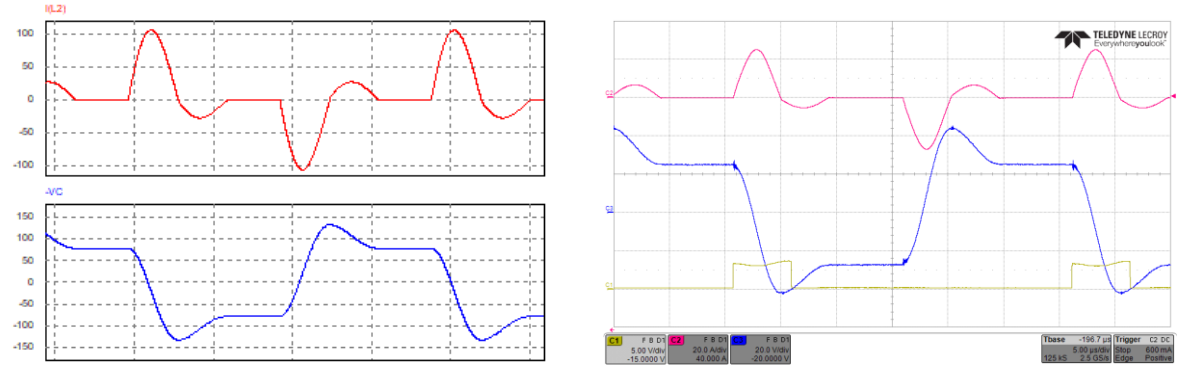
A resonant tank voltage generated by the full bridge rectifier is presented in Fig. 3.7. Simulation results are shown in Fig. 3.7a, the current in the resonant tank is shown in red, and the voltage across it is shown in blue. Experimental results are presented in Fig. 3.7b. The waveforms in both simulation and experimental evaluations are within a close fit to each other.



(a) (b)

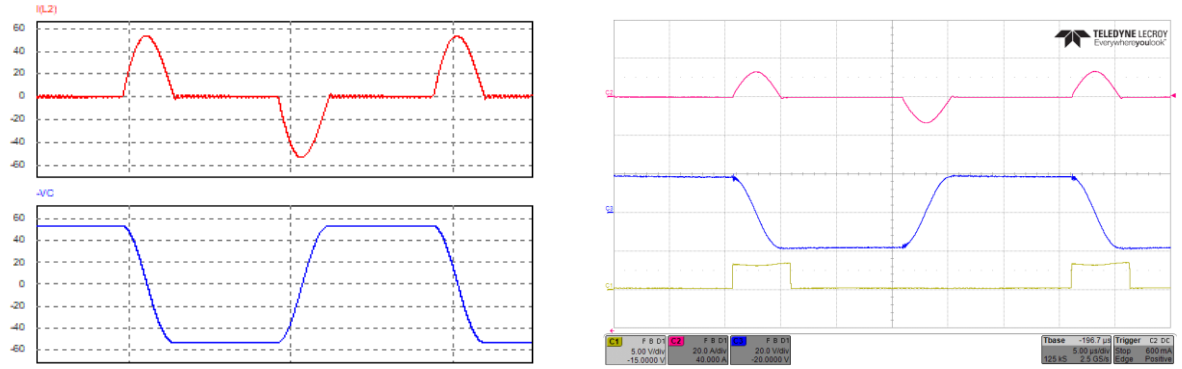
Fig. 3.7 Resonant tank voltage. Experimental vs. simulation results. (a) simulation results: transformer primary resonant current (red) 50A/div., resonant tank voltage (blue) 50V/div., (b) Experimental results: transformer primary resonant current (pink) 10A/div., resonant tank voltage (blue) 10V/div.

The voltage and the current of the resonant capacitor, V_{Cr}, and I_{Cr} at the begging of the charging process and at the middle of the charging process are presented in Fig. 3.8 and Fig. 3.9, respectively. The simulation results of V_{Cr} are shown in Fig. 3.8a and Fig. 3.9a while the experimental results of V_{Cr} are shown in Fig. 3.8b and Fig. 3.9b.



(a) (b)

Fig. 3.8 Resonant capacitor C_r voltage and current at the beginning of the charging process: (a) Simulation results: from top to bottom: transformer primary resonant current 50A/div., V_{Cr} 50V/div., gate signal. (b) Experimental results: transformer primary resonant current (pink) 20A/div., V_{Cr} (blue) 20V/div., gate signal (Q_2) (yellow) 5V/div.

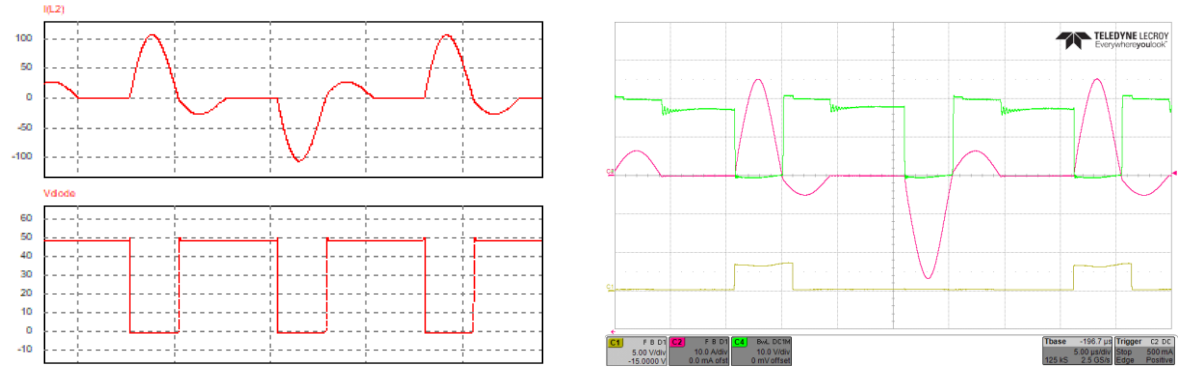


(a) (b)

Fig. 3.9 Resonant capacitor C_r voltage and current in the middle of the charging process, at 60% point to target voltage: (a) Simulation results: from top to bottom: transformer primary resonant current 20A/div., V_{Cr} 20V/div., gate signal. (b) Experimental results: transformer primary resonant current (pink) 20A/div., V_{Cr} (blue) 20V/div., gate signal (Q_2) (yellow) 5V/div.

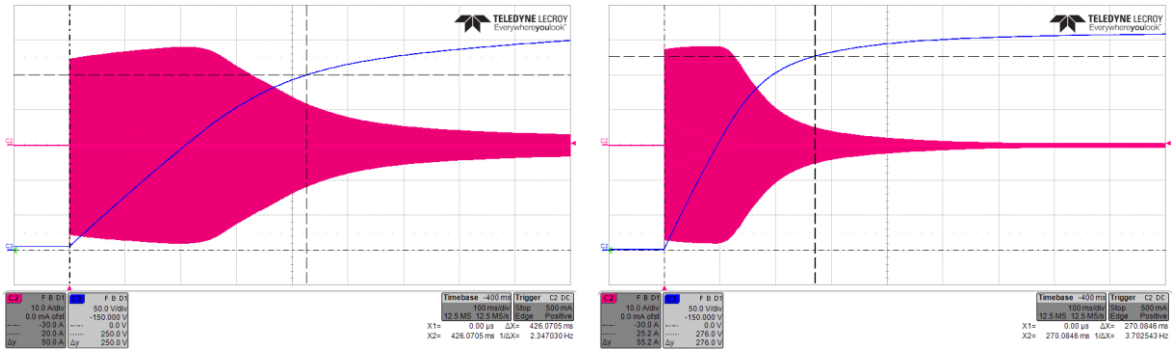
The voltage stress across the switch Q_5 (see section 3.2.1) is presented in Fig. 3.10. Simulation results are shown in Fig. 3.10a, and experimental results are shown in Fig. 3.10b. A good agreement is shown between simulation and experimental results. Full charging process experimental results were carried out with a prototype board as shown in Fig. 3.13. A storage electrolytic output capacitor of C_{out}=330μF is charged to V_T=300V off an input voltage source of V_{in}=12V with an average charging power of 25W and peak instantaneous power of approximately 70W. The charging current and output voltage are shown in Fig. 3.11a. A charge with an average charging power of 45W and peak instantaneous power of approximately 140W is demonstrated in Fig. 3.11b. A shorter charging time can be observed in Fig. 3.11b. Validation of charging time (3.9) using cycle-by-cycle simulation is shown in Fig. 3.12. Blue trace presents the target charge voltage and the time required to reach it as calculated by equation (3.9), while the stars represent cycle-by-cycle simulation results as

were aquired in PSIM simulator. The minor discrepancy between the theoretical trace and simulation results is due to the assumption that the balancers are lossless.



(a) (b)

Fig. 3.10 Switch Q_5 (keeping DCM operation) drain-source voltage. Experimental vs. simulation results. (a) Simulation results. From top to bottom: transformer primary resonant current 50A/div., V_{DS_Q5} 10V/div., gate signal. (b) Experimental results: transformer primary resonant current (pink) 10A/div., V_{DS_Q5} (green) 10V/div., gate signal (Q_2) (yellow) 5V/div.



(a) (b)

Fig. 3.11 Experimental results: full charge of output capacitor with C_{out}=330µF, V_{in}=12V, Transformer primary resonant current (pink) 10A/div., V_{out} on C_{out} (blue) 50V/div. with time scale: 100ms/div. (a) D=0.3, P_{out_avg}=25W, P_{out_max}=70W , (b) D=0.6, P_{out_avg}=45W, P_{out_max}=140W

3.5. Conclusion

In this study a new architecture of multilevel high voltage modular capacitor charger is presented. The architecture is based on a double bridge resonant converter operated in DCM as a charger that is connected to a series of energy storage cells equalized with switched capacitor balancers. The unique architecture enables the designer to spread the stresses across several components and select optimal components as dictated by the industry, i.e. carry out an industry inclined optimization, and to avoid the common solution where full rating bulk components are chosen. Industry inclined optimization is discussed along with design considerations such as regulation, charging time and charging efficiency. An experimental prototype has been built and evaluated experimentally. The validation of

system operation has been carried out using PSIM numerical simulation and experimental trials and found to be in an excellent agreement with theoretical premises.

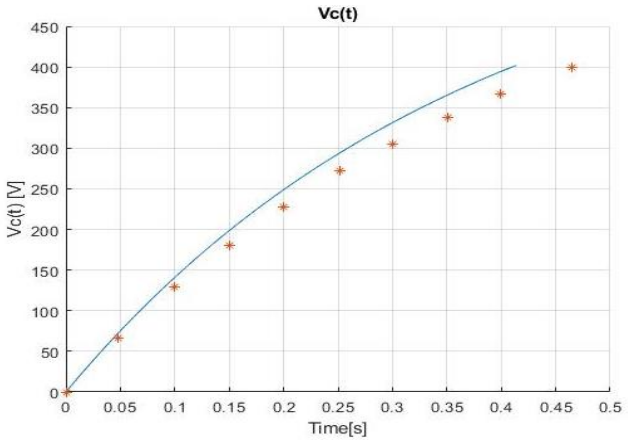


Fig. 3.12 Theoretical results of a single module charging times versus targeted output voltage with 3 capacitors in series, 330µF each. Blue trace is a model calculation, and discrete stars in red are the PSIM numerical simulation. Parameters are: V_{in}=12V, N=50, D=0.9, C_{out}=990µF, R=96mΩ

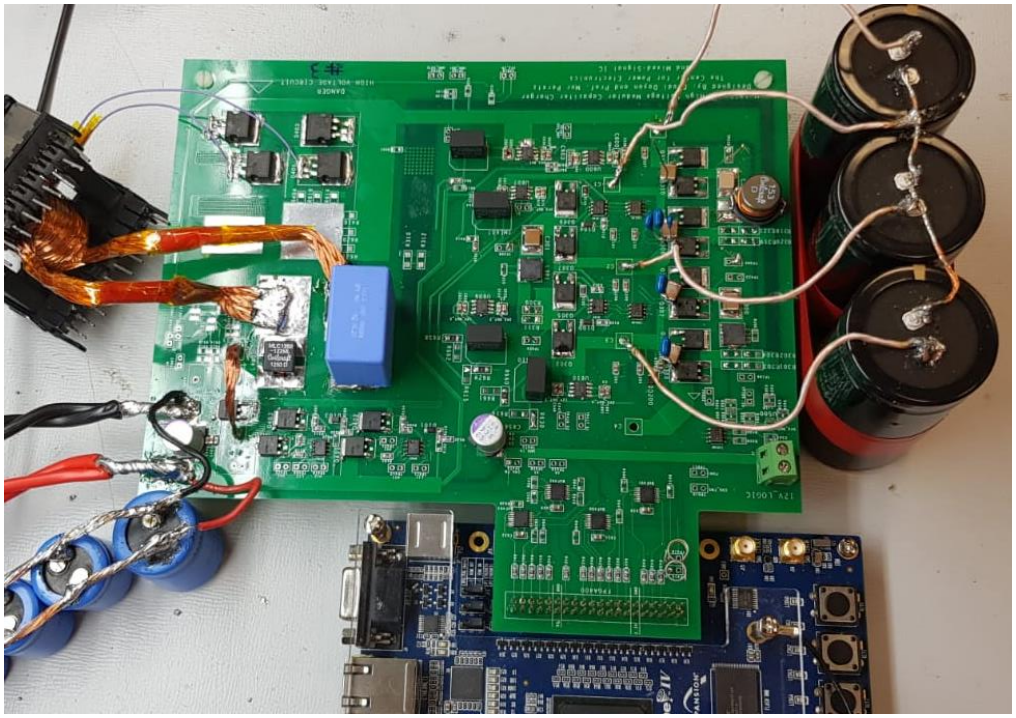


Fig. 3.13 Prototype board, including charger and balancer.

4. High-Performance Compact Electromagnetic Coilgun Propulsion System with Low-Voltage Modular Rapid Capacitor Charger

Magnetic propulsion systems utilize electromagnetic actuators to convert electrical energy into kinetic energy. A potential candidate to be mobile and compact payload launcher is a coilgun magnetic accelerator in which propulsion is inherently generated without contact and with no friction. A fundamental obstacle of the existing solutions is the low energy conversion efficiency that primarily stems from saturation of the propelled object by the excessive force of the actuator. This study introduces a partition methodology for the coilgun structure which enhances power and energy utilization along the propulsion track. It is enabled by a low voltage modular rapid capacitor charger with multilevel voltage bus and peripheral circuits, to achieve accurate timing sequencing. The resultant system is of significantly higher power density and potentially capable of producing higher velocity propulsion per unit volume. The concept and circuitries are described in detail. Experimental validation is provided for a 1KW rated rapid capacitor charger prototype, that charges 3x1mF serially connected capacitors to 1,200V from a 12V input source.

4.1. Overview

Using magnetic fields to create mechanical forces has a large number of applications ranging from magnetic bearings for high speed flywheels, through levitation and stabilization devices, and to acceleration devices or propulsion systems. Electromagnetic propulsion systems are used in everyday life to shuttle payloads, converting effectively readily available and convenient electrical energy into magnetic field and into acceleration force. The most recognizable civilian magnetic propulsion system is very high-speed train, the MAGLEV [46], where magnetic forces are used for both: levitation - to reduce the wheels friction, and propulsion. In the case of MAGLEV, acceleration is achieved by using the basic attraction and repulsion of magnetic poles. There are however at least two more kinetic acceleration system methods used to convert electric energy into magnetic field and into acceleration force. First is the concept of railgun payload acceleration [47], [48], where a current is passed through an increasing loop formed by the launch object and the launching rails, and interacts with the field it has created, resulting in a Lorenz force to accelerate the payload. Second is the concept of a gauss, or coilgun acceleration [49]-[56], where a ferromagnetic object is passed through a coil with magnetic field that creates a Lorentz force

to accelerate the payload. Although railgun concept has demonstrated successfully generation of high velocities, its primary drawback is the large friction between the rail and the launched object. In both the MAGLEV and railgun cases the payload is actively participating in creating acceleration force. High power electrical magnet is carried on board the MAGLEV, and a huge current is passed through the launched object of the railgun, which requires intensive thermal management as well as mechanical maintenance. Coilgun concept however, is preferable in the cases where the payload needs to remain passive, and to avoid friction between the actuator and the projectile. As a result, coilgun concept would be friendlier for potential miniaturization and mobile applications.

The basic coilgun structure is a single launching coil powered by a high voltage pulsed source to generate current pulses and convert them into magnetic field. Coilgun based acceleration system requires high power density, and the energy transferred is low, since most of the energy is wasted in the process as a result of the limited tangential range between the force generating coil and the fast-moving core. In addition, the magnetic field induced on the ferromagnetic core forces it into the saturation region, which from then on, the improvement in the acceleration force is negligible. The current needed to achieve some usable acceleration lays in the range of tens of kiloamperes, as a result the voltage required needs to be in the range of tens of kilovolts. Very high current pulses result in destructive effect on the system, reducing system reliability, and very high voltages require bulky components to be used, making the system occupy a lot of space.

In order to improve the system in terms of size, power and energy density the amount of electrical energy that converted into kinetic energy needs to be maximized [51]. To achieve that three major development directions are identified in this study. First is to increase the efficiency of energy conversion and waste less energy in the process. This implies usage of lower voltage pulsed sources and avoiding deep saturation regions to achieve comparable accelerations, reducing the loss and increasing the efficiency of the overall energy conversion. Second is to utilize best available location and timing sensors. Precise timing in coilgun is crucial to avoid any reminders of the current pulse to brake the payload instead of accelerating it, reducing the kinetic energy of the payload in the desired direction. Third, to modularize the system to reduce size. A more advanced coilgun design consists of multiple coils, where the payload is accelerated in several, smaller consecutive acceleration steps.

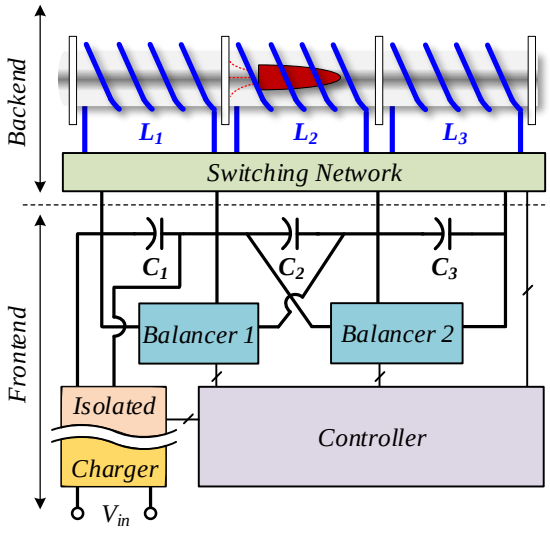


Fig. 4.1 Schematic diagram of a magnetic propulsion system module.

A modular distributed coilgun system concept diagram is schematically shown in Fig. 4.1. The power management and energy distribution system are modularized, to increase power density, and avoid potential redundancy of similar units to cut on volume and weight of the system. Partition of acceleration coil into multiple coils with lower inductance, enables lower voltages to be applied per unit coil, but retain comparable acceleration force. Power distribution source division, enables lower voltage components to be used, reducing the voltage stress and high voltage isolation requirements. Charging power converter partition enables to omit some redundant parts that are common to many of the multiple coils.

The objective of this study is therefore to introduce a system level methodology to enhance the electrical to kinetic energy conversion efficiency, reduce the volume of the magnetic actuators, and significantly increase the power density of the electrical drive generation system. By doing so, higher velocity propulsion is enabled per volume of the coilgun system. This is enabled by partition of the magnetic actuators along with modular multilevel construction of the power driver which exploits the higher power density components at low-medium voltage ratings. It is a further objective of this study to present the details of the primary building blocks associated to the enabling technology such as modular rapid capacitor charger, magneto-mechanical displacement and velocity sensors, and activation circuitry to successfully implement coilgun operated from a low voltage source.

The rest of the paper is organized as follows: section II surveys the basics in coilgun operation and designs, and presents an advanced distributed coilgun concept. Section III introduces a multilevel rapid capacitor charger configuration with multilevel voltage bus.

The backend periphery and supporting circuitry and sensors are described in Section IV. Section V presents experimental validation of distributed structure, rapid capacitor charger with multilevel voltage bus. Section VI concludes the paper.

4.2. Coilgun operation

Coilgun operation is based on a physical phenomenon, where a ferromagnetic element experiences force in the presence of magnetic field. The name of the phenomenon is Lorenz Force, and it is summarized in a law stating that the force is proportional to the coil and ferromagnetic object properties *M*, and is a function of magnetic field gradient dB_z, applied to the ferromagnetic object:

$$F_z = M\frac{dB_z}{dz}. \tag{4.1}$$

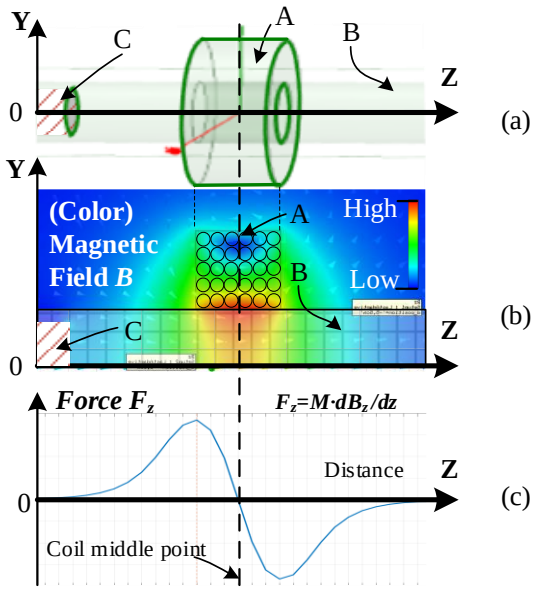


Fig. 4.2 Schematic diagram (a), magnetic field (b), and acceleration Lorenz force (c) on a ferromagnetic projectile in a single coil magnetic propulsion system

4.2.1. Single coil propulsion

The simplest electromagnetic propulsion system or coilgun is based on a single coil wrapped around an acceleration path. A current is passed through the coil, which excites a magnetic field in the coil and along the acceleration path, which in turn creates a force, Lorenz force, which pushes a ferromagnetic payload in the direction of the force, Z axis in Fig. 4.2. A basic coilgun structure is shown in Fig. 4.2a, where part A is the coil, part B is the acceleration path, and part C is the payload. The distribution of the magnetic field along Z axis as calculated by a FEM software simulation package, ANSYS-Maxwell is shown in

Fig. 4.2b. The Lorenz Force along the Z axis that is applied to the payload as a result of the magnetic field is shown in Fig. 4.2c. The unique shape of the force indicates that the payload experiences positive force in the direction of the launch only up to the middle of evenly winded excitation coil. This is well highlighted in Fig. 4.2b, where the maximum magnetic field is developed in the middle of the coil, the red area, and the field is diminishes towards both external sides of the inductor. It creates positive gradient of the field as the payload enters the coil, and negative gradient as the payload passes the middle point. In this way, passing the middle point, the payload experiences a negative force, i.e. braking of the payload is taking place. For best launching performance breaking needs to be avoided. There are two major solutions to avoid breaking. First is to force the coil excitation current to zero, once the payload reaches the middle point of the coil. Another solution is to design the excitation circuitry so that the length of the excitation pulse is shorter than the time that the payload reaches the middle point, and the current has enough time to fall back to zero before generating the braking action.

4.2.2. Cascaded coil propulsion

Magnetic fields required to create a significant Lorenz force, demand a very high current to be circulated through the acceleration coil. Extremely high voltages are required to achieve these currents. To sustain very high voltages, bulky components such as large very HV capacitors are used, and inefficient scalable converters capable to reach extremely high voltages are employed such as Cockcroft-Walton converter. This results in a system with poor power density and bulky. However, the amplitude of the pulse doesn't scale endlessly. At a certain point, current pulses become extremely high, creating huge mechanical forces that cause deformation of the inductor, move the conductors relative to one another, and become hard to counteract. In addition, high voltages that are applied to the inductor along with its mechanical deformation bring to an often shoot through and failure of the acceleration coil altogether.

A common solution to remedy some of the disadvantages of a single coil propulsion systems is to cascade several acceleration coils along the acceleration path, and to activate them one after another as the payload moves through. This solution allows to limit the peak current to a certain, tolerable maximum that maintains the integrity of the system. Several coils, each contributing lower acceleration, activated consecutively contribute to reaching high final velocity. Cascaded structure has the ability to partially cancel the unwanted

braking action of the previous coil by the next coil, and one of the major challenges of a single coil propulsion system, the residual tail of the current, needs to be solved at the last coil only, where it could be taken care by a different shape of the current pulse.

Cascaded coil configuration is generally activated by either of the two methods. First, the same very HV capacitor is reused for all of the coils. It is charged to its maximum voltage, and then connected to each of the coils, with lower and lower voltage applied to each subsequent coil. Another approach, is having a separate very HV capacitor for each of the coils. In the first case, the system suffers from huge voltage spikes resulting from high current turn off, but it could have lower volume. In the case of multiple very HV capacitors, the system occupies much larger volume, but it is capable to achieve the maximum acceleration possible within the maximum tolerable peak current limitation. Yet, in both cases the voltage of choice is around 10kV, and high power very HV capacitors are rather bulky, rendering these systems to be extremely large and heavy.

4.2.3. Advanced segmentation propulsion

As outlined above, HV isolation requirements and high mechanical stresses caused by large currents are among the major, indirect contributors to the size and weight of the launching system. Further reduction in the voltage and current stresses over the cascaded design are needed in order to increase power density and reduce the volume of the system. The approach demonstrated in this study is based on system partition beyond the concept of basic cascaded coil propulsion.

Each cascade is further subdivided into a lower inductance coil units so that the voltages required for each unit are reasonably low, while the currents are maintained high enough as in the cascaded case, but within a tolerable maximum for system integrity. Coil units could be similar to that in cascaded case, but each unit has lower inductance and parasitic resistance allowing to develop the same peak current pulse out of a lower voltage source. This can significantly reduce the volume of the system and increase power density [55]. Moreover, having a large number of coil units enables force gradient and acceleration along most of the acceleration path. Comparing to a single coil, where the acceleration takes place only to the middle of the coil, partitioned coilgun case is superior in creating longer acceleration path. Comparing to the cascaded case, where the last coil is used to take care of the braking part of the current, in partitioned coilgun case only the final coil unit of the last cascade module needs to take care of the braking current, which is again a better alternative.

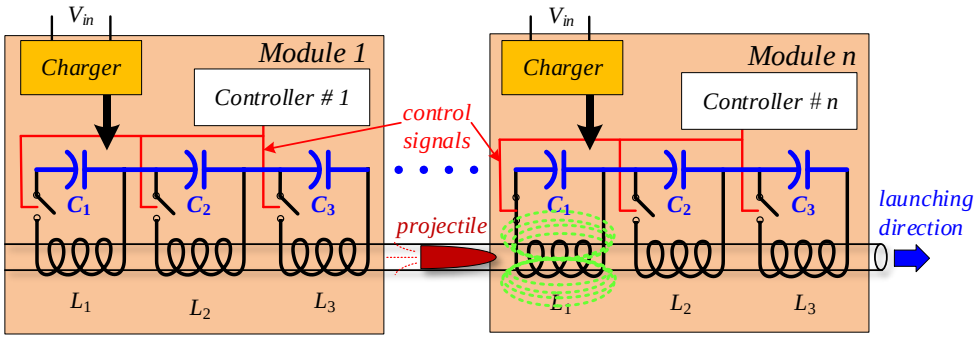


Fig. 4.3 Schematic diagram of advanced partitioning magnetic propulsion system.

4.2.4. Conceptual architecture of segmented propulsion system

Large number of coil units pose several implementation challenges. Fine division of each cascade in the propulsion system requires a large number of power capacitors to be used as the pulsed voltage sources for each coil unit, and each of these capacitors needs a charging and control circuitry. One possible way to implement the system is to build an isolated charger for each capacitor, and independently charge them. This approach however, requires very large number of similar systems operated in parallel, creating huge redundancy, a system with large number of components that results in increased potential failure rate and large volume. An alternative approach explored in this study is to divide the system into independent modules where each module has a single capacitor charger, serves several coil units, and covers approximately the number of coil units that would be used for a single cascade in an equivalent cascaded system.

A conceptual structure of the launching part of a partitioned coilgun magnetic propulsion system is shown in Fig. 4.3. Each module is designed to maintain kV range voltage that is high enough to achieve the maximum allowed pulse current in the cascaded system, but most of the module components, such as the switches and capacitors are exposed to much lower voltage, in the range of several hundred volts. In the basic version, each capacitor serves a single coil unit, while in the more advanced case, as described in section IV, a combination of several capacitors within the module could activate a single coil unit or a combination of coil units based on the system requirements and switching network (Fig. 4.1) complexity.

4.3. Rapid capacitor charger with segmented balanced high voltage rail

In order to support a large number of coils in a coilgun, a unique power and energy management system is needed. The challenges described in previous section call for a large number of charging and managing systems. The system developed in this research

overcomes the redundancy of multiple chargers, and is built around multiple number of self-sustained modules, comprised of several energy storage capacitors each that enable on one hand fine distribution of the acceleration coils and associated benefits, while on the other hand, keep relatively low the overall number of components and overcome some of the deficiencies of traditional implementations.

The basic architecture of a single charging and energy management module is arranged in two stages (Fig. 4.4): an isolated charger [23], [40]-[41], [57] followed by a voltage multiplying and active capacitor equalization circuits [27], [58]-[59]. The charger utilizes high voltage isolation transformer T_1 that makes each of the modules independent, self-sustained and floating at their secondary. High voltage isolation enables the modules to be stacked on top of each other to create very high voltages. The charger output connects to the bottom capacitor C_1, via rectifier. In this study, each module comprises a stack of three capacitors. Capacitors C_2 and C_3 receive the charge from capacitor C_1 through equalization circuits that are responsible to charge the capacitors in the stack and redistribute the charge evenly. The number of voltage multiplier circuits is as the number of energy storage capacitors. The topmost multiplier, that is omitted from Fig. 4.4, is responsible to maintain charge equalization between the current module and the next one. In this manner the energy from the charger is equally redistributed across the capacitors in the module, and a reference to both previous and the next modules is maintained.

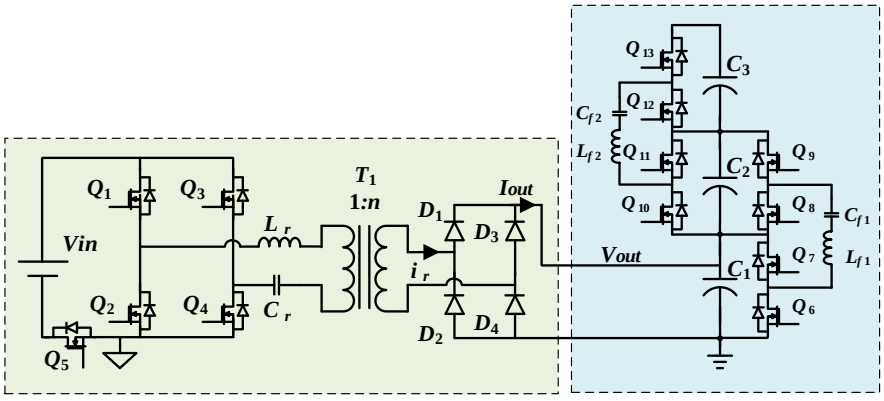


Fig. 4.4 Schematic of a rapid capacitor charger for magnetic propulsion system with advanced partitioning.

Capacitor charger is built around a dual bridge resonant converter [38], [55]. The converter is configured in a series resonant mode, where the input bridge is an active bridge, and the output bridge is passive (Fig. 4.4). The converter is operated in DCM, slightly below its resonance frequency to maintain ZCS, regulate the amount of charge transferred to the output, and present a current source type, high impedance to the output capacitor. To

maintain a DCM operation an extra unidirectional switch is required to block the voltages developed at the resonant capacitor during the first phase of charging operation. An active switch Q_5 is used to reduce the losses associated with forward voltage drop of the diode in the presence of high currents of the primary side. In addition to isolation, transformer T_1 is used to step up the voltage, and its leakage is used as a resonant inductor to resonate with resonant capacitor.

To reduce the number of chargers per module, a charge redistribution by voltage multipliers from C_1 to the rest of the capacitors in the chain is used. Voltage multipliers are built around two half bridges in parallel to two storage capacitors, and a resonant tank C_{fx} and L_{fx}, constituting a resonant switched capacitor converter. Each voltage multiplier serves two adjacent energy storage capacitors. The half bridges connect the resonant tank to each of the storage capacitors with 50% duty cycle and running at the resonant frequency, enabling the resonant tank to charge from the capacitor with higher voltage and provide the excessive charge to the capacitor with the lower voltage. In this manner the voltages of both adjacent capacitors are maintained in a close vicinity to each other. This operation ensures that no high currents are developed in the voltage multiplier components, enabling selection of smaller, lower stress rated components. In the faulty case of uneven storage capacitor discharge, a slow discharge and recovery algorithm is implemented to restore capacitor voltages to be close to each other.

4.4. Backend electrical systems

Several backend systems are required for timely activation of a large number of units with suitable voltage and current amplitudes.

4.4.1. Positioning and velocity sensing

There are three common practices to activate cascaded coils. One is by experimentally timing the periods it takes for the projectile to pass each of the subsequent coils. The second one uses trial and error tune up procedure, where the activation of each coil is trimmed up, and projectile exit velocity is used as an indicator. The third method is using active projectile positioning system. One of the active positioning system implementations is using optical sensors [60]. To achieve high positioning precision with optical sensors expensive optical components and high-quality expensive machining of the parts are required. Positioning method used in this study requires neither expensive components nor special machining. The method is based on inductance change of a winding while a ferromagnetic element is passing

through it. A basic relationship of inductance, L as a function of permeability of the coil core is summarized in (4.2):

$$L = \mu \frac{n^2 A_e}{l_e}, \tag{4.2}$$

where μ is the permeability of the coil core, n is the number of turns, A_e is the cross section of the core, and l_e is an average core length. An electrical scheme of positioning system is shown in Fig. 4.5. A sensing winding of several turns is added to the projectile acceleration path located in the vicinity of each acceleration coil. A power converter such as a simple DC-DC buck converter is used as a driver for all of the coils, driving the sensing coils at high frequency to allow high sensor bandwidth. A DC blocking capacitor is used to avoid saturation of the sensing coil. The readings of the inductor current are taken off a resistor connected in series with the sensing coil. The waveform is then passed through a peak detector with lower time constant than the driver switching period. A typical resulting output of the peak detector is shown in the photo of Fig. 6, where a projectile is shown next to the oscilloscope reading of the peak detector output. Based on the voltage amplitude of the peak detector output, positioning processing algorithm within the controller evaluates position and velocity of the projectile, and issues real time commands to the switching network and coils activation system. The method developed in this study enables location, speed and acceleration readings to be fed into the launching controller in real time. This is a continuous reading sensing approach, which provides more information and higher precision than optical based single spot detection at a fraction of a cost. It is superior to tuning and preset timing methods as well, where any change in electrical or mechanical parameters, or properties of the system and projectile could result in sub-optimal performance [61], [62].

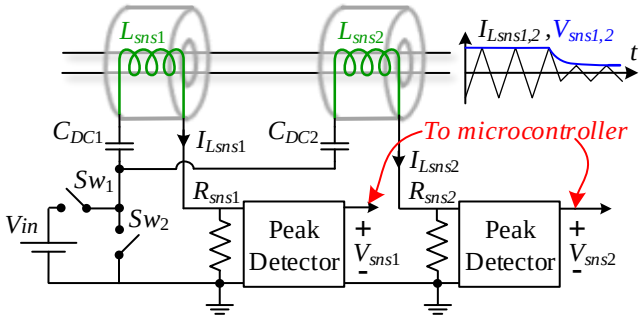


Fig. 4.5 Electrical scheme of inductance-based positioning sensor

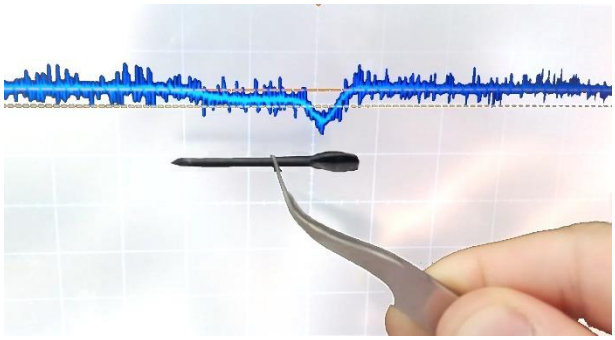


Fig. 4.6 Photograph of a projectile next to the oscilloscope reading of the peak detector output of positioning sensor.

4.4.2. Switch array and excitation modularity

A network of pulse activation switches, or switch array could grow very large if connections flexibility is a priority. Moreover, the higher the flexibility the higher voltage rating of the switches is required. To reduce the complexity and showcase a simple connectivity network suitable for coilgun application, possible voltage amplitudes applied to an acceleration coil are set to be as the number of storage capacitors in a module.

The connection between the energy storage capacitors and acceleration coils can be divided into two types: first is made at the design stage, and second are the connections made during operation of the coilgun. As an example, the modules used in this study consist of three capacitors each, and for this purpose, a simple network of three high voltage switches is required as shown in Fig. 4.7. Permanent connections are laid out based on expected excitation requirements. Drive of three coils using a single module is shown in Fig. 4.7a, where three switches S_1, S_2 and S_3 are used each to excite its own coil. This type of excitation is dictated by less and less time that the payload spends in each subsequent acceleration stage due to the speed acquired at the previous stages. To adjust the pulse width accordingly the inductance of the acceleration stage coil needs to be decreased, enabling shorter pulses.

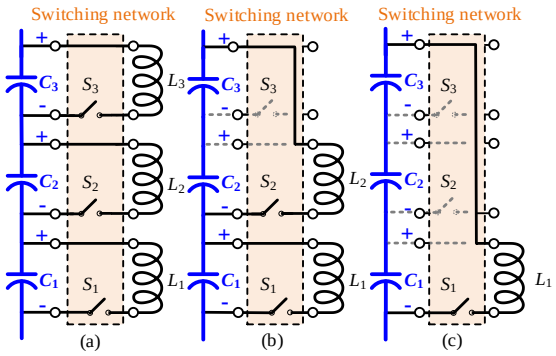


Fig. 4.7 Conceptual diagram of switching network.

An alternative activation approach shown in Fig. 4.7b takes again into account shorter time periods that the payload spends in each subsequent stage, but acceleration coils have equal inductance in this case and pulse width is adjusted decreasing the capacitance. In addition, in this case the amplitude of excitation voltage is increased to provide the same amount of energy at every stage. In this case switch S_3 is phased out in a permanent routing stage, and switches S_1 and S_2 are used to activate two acceleration coils, with double the voltage at the second acceleration coil. In this case switch S_2 needs to withstand double the maximum storage capacitor voltage.

The connection in Fig. 4.7c demonstrates a utilization of the total module high voltage. A single acceleration coil is activated using the full module voltage and a fraction of the capacitance, divided by three in this example. So, the switch S_1 needs to be rated for the full module voltage. It is important to highlight here that switching network is an independent unit, and could accommodate several modules with similar activation scheme as described in Fig. 4.7, where the number of connected capacitors is doubled each acceleration coil, and the voltage rating of activation switch needs to be doubled to prevent its breakdown.

4.4.3. Protection and monitoring

During the operation of the system, large voltage differences may develop between the capacitors within a single module. For example, the scenario of activating first and third coil units in the switching network of Fig. 4.7a., second capacitor remains fully charged next to fully discharged neighbors. This scenario imposes a very high voltage difference across the resonant tanks (C_{f1}, L_{f1} and C_{f2}, L_{f2}) of the voltage multipliers responsible to shuttle the charge between the stacked capacitors (Fig. 4.4), and as a result a very high resonant current will develop through the multiplier switches.

There are two possible ways to overcome this challenge. One is to design voltage multipliers with switches large enough to withstand the maximum possible current in every extreme condition. This option is impractical, since it involves an extreme overdesign of the voltage multiplier switches, resulting in unnecessary and unproportional volume and budget requirements. A more practical solution is to monitor capacitor voltages, and bring voltage differences actively or passively to some lower levels, acceptable by design for the voltage multiplier components. For the module containing 3 capacitors as in Fig. 4.4. the following relationships need to hold:

$$-V_{th} < \Delta V_1 = V_{C1} - V_{C2} < V_{th} \quad (4.3)$$

$$-V_{th} < \Delta V_2 = V_{C2} - V_{C3} < V_{th} \quad (4.4)$$

where V_{C1}, V_{C2}, and V_{C3} are the voltages across C_1, C_2 and C_3 capacitors (Fig. 4.4), ΔV_1 and ΔV_2 are the voltage differences between the capacitors that need to be monitored, and V_{th} is the threshold voltage that develops the maximum rated current allowable for the voltage multiplier switches. To maintain the integrity of the multilevel rapid capacitor charger, the following algorithm is developed:

In the case of $\Delta V_1 > V_{th}$ disable the main charger and stop balancer #1 (Fig. 4.1). Next, discharge C_1 (either a bleeder could be used, or if a bidirectional charger is implemented, the energy could be pumped back to the source).

In the case of $\Delta V_1 < -V_{th}$: disable balancer #1 (Fig. 4.1). Next continue to charge $C_1$with the main charger until the voltage difference is within the threshold.

In the case of $\Delta V_2 > V_{th}$: disable both charging and balancer #2 (Fig. 4.1). Next activate balancer #1 to discharge C_2 to within the threshold voltage of C_3.

In the case of $\Delta V_2 < -V_{th}$ disable balancer #2 (Fig. 4.1). Next assuming (4.3) holds continue charging C_1 by the main charger and run balancer #1 to charge up C_2 to within the threshold of C_3.

If (4.3) and (4.4) are both invalid the system should proceed eliminating one fault at a time beginning with the capacitor connected to the main charger, C_1, following with C_2, and finally C_3.

Capacitor voltage monitoring can be implemented using ADC and the differences further calculated by the microcontroller, or series of comparators could be used and a comparison result fed as a digital signal to the controller.

In addition to the voltage multiplier voltage monitoring, a faulty condition of over voltage at each capacitor needs to be monitored. This is done by using a series of comparators that invoke a fault condition once any of the capacitors exceeds maximum voltage rating, and the charging and balancing operations are immediately disabled.

4.5. Experimental validation

In order to validate the theoretical concepts and operation of the system introduced in this study, a low-voltage modular rapid capacitor charger module has been designed, fabricated and tested by simulations and experimentally. The validation of the concepts using numerical simulation has been carried out using PSIM. The schematic of the system follows the structure of Fig. 4.4. TABLE I summarizes the main parameters of the system including the storage capacitors. It should be noticed here that the storage capacitor value used in the simulation is C_{out}=1µF instead of C_{out}=1*m*F as in the experimental, that in order to make the simulation converge in a reasonable time. Therefore, to compare the convergence results of the experiments to the simulation, time in simulation should be multiplied by a factor of 10^3.

Transformer resonant currents during charging operation are shown in Fig. 3.6. Simulation results are presented in Fig. 3.6a, and experimental results are shown in Fig. 3.6b. The converter operation includes a main high peak sinusoidal current followed by a smaller resonant shape immediately after it. The second resonant shape is induced due to the high-quality factor resonant tank that results in resonant capacitor voltage exceeding the input voltage during some time at the beginning of the charging process when the difference between the input and the output voltages is high. Since the gating of the charger allows some extra time to ensure zero voltage switching in the presence of resonant tank component variation, a reverse current flow from the capacitor is developed and creates a lower amplitude sinusoidal follow up. This follow up however, doesn't impact efficiency, since it is rectified by the passive rectifier at the secondary side, and adds to the total converter energy transfer to the output.

Full charging operation of the low-voltage modular rapid capacitor charger with a single storage capacitor is demonstrated in Fig. 4.8. Simulation results are shown in Fig. 4.8a, the current in the resonant tank is shown on top and the voltage of the storage capacitor being charged is shown on the bottom. Experimental results are presented in Fig. 4.8b. The waveform in both simulation and experimental evaluations are within close fit to each other. It can be seen from simulation that the capacitor was charged from 0V to 400V at approximately 0.65ms while at experiment the storage capacitor charged from 0V to 400V at slightly more than 650ms (as mentioned above there is a factor of 10^3 due to the lower capacitors used in the simulation setup).

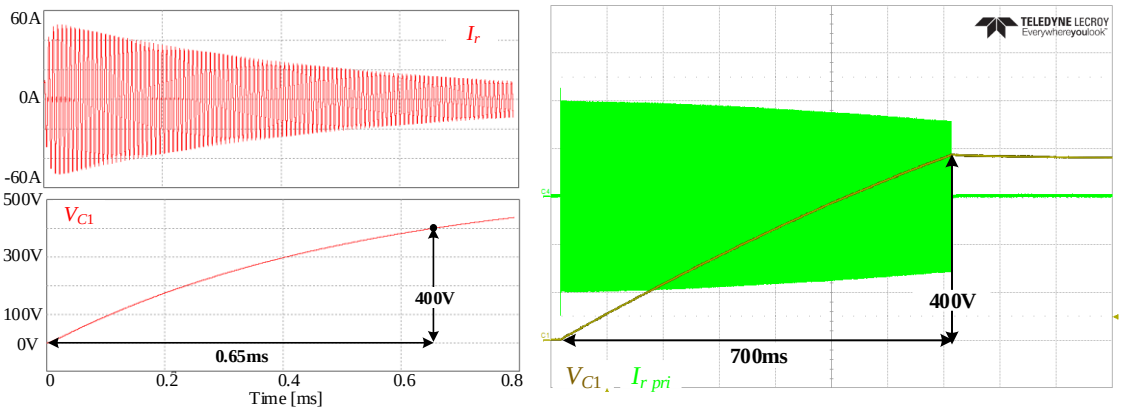


Fig. 4.8 Full charging operation of one module with a single storage capacitor at the output. Experimental vs. simulation results. (a) Simulation: Top trace - transformer primary resonant current $I_{r\ pri}$ (20A/div). Bottom trace - storage capacitor's voltage V_{C1} (100V/div). (b) Experimental: Yellow trace – storage capacitor voltage V_{C1} (100V/div). Green trace – transformer primary current I_{r_pri} (45A/div).

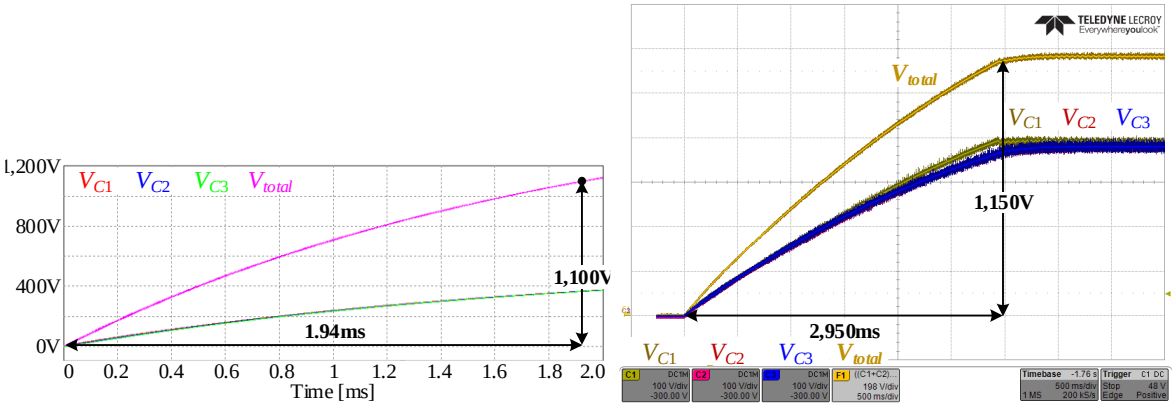


Fig. 4.9 Full charging and balancing operation with three output storage capacitors voltages: (a) Simulation: V_{C1} (red), V_{C2} (blue), V_{C3} (green), V_{total} (magenta) 200V/div. (b) Experimental: V_{C1} (brown), V_{C2} (red), V_{C3} (blue) 100V/div, V_{total} (yellow) 200V/div.

Fig. 4.9 demonstrates full charging and balancing operation of the low-voltage modular rapid capacitor charger with three serially connected capacitors at the output. Simulation results are shown in Fig. 4.9a and experimental results are shown in Fig. 4.9b. It can be seen, both in simulation and experimental results, that the storage capacitor voltages charged equally during the charging process. Total voltage of the module, $V_{total} = V_{c1}+V_{c2}+V_{c3}$ (Fig. 4.9a magenta trace), charged up to 1,100V at 1.94ms, which is in the vicinity of the experimental result charged up to 1,150V in 2,950ms (Fig. 4.9b yellow trace). The difference in charging time is due to lossless setup used in simulation. A photograph of the PCBs of the modular rapid capacitor charger module used for the experiments is shown in Fig. 4.10.

4.6. Conclusion

In this study a high performance compact electromagnetic coilgun propulsion system with low voltage modular rapid capacitor charger is presented. It has been shown that modular

approach and partition concept applied to a coilgun propulsion system are advantageous in terms of size and energy conversion efficiency. Three development directions have been examined to improve the volume and efficiency of the coilgun system: 1. modular approach, 2. operation under lower overall stress on the components, and 3. application of precise positioning sensors. Backend supporting circuits such as positioning sensor and switching network have been discussed. It has been shown that inductive based location sensing approach is advantageous to the commonly used optical and manually timed methods, resulting in real-time precise position and velocity information flow, contributing to higher energy utilization.

A hardware prototype of a rapid capacitor charger with multilevel balanced high voltage rail has been built and tested to validate the theoretical predictions and simulation trials. The results demonstrate great flexibility of multilevel capacitor charging system, and indicate great potential in supplying partitioned magnetic propulsion coilgun systems.

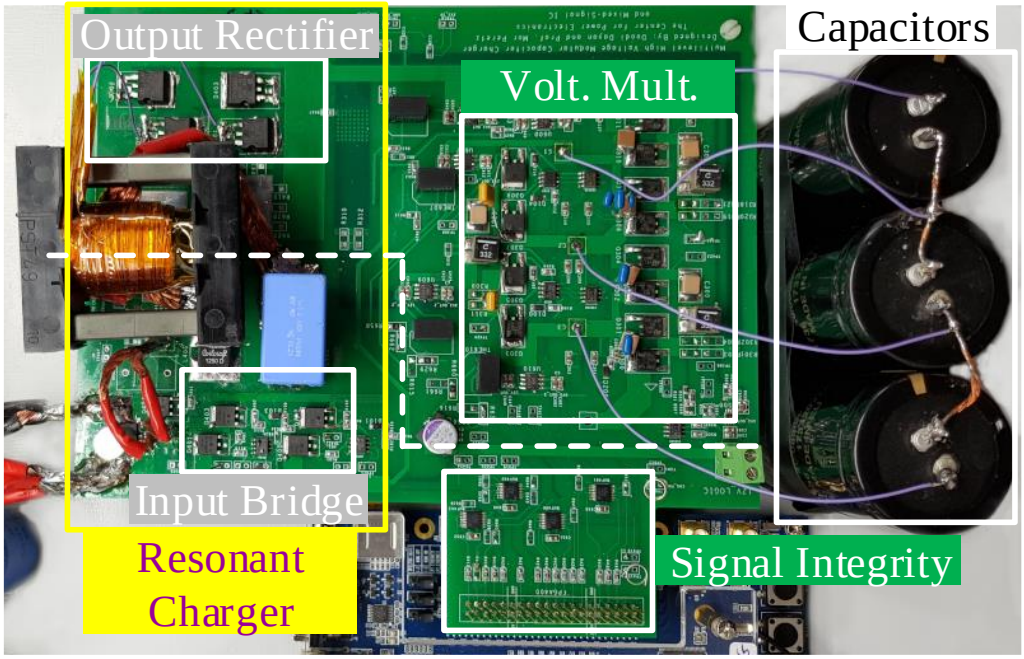


Fig. 4.10 Photograph of low-voltage modular rapid capacitor charger module as part of the lab setup

5. Discussion

5.1. Contribution of the research

High system power density- A multilevel approach was used to increase the power density of the whole system. Also, a modular architecture facilitates varying number of magnetic actuators. The structure of independent, self-sustained modules enables them to be stacked on top of each other to create very high voltages. It also enables scalability and building a system for any desired voltage and power.

Low volume of magnetic actuators – conceptual architecture of partitioned propulsion system replaces bulky and huge inductors or magnetic actuators. Each capacitor can serves a single coil unit or several capacitor within the module could activate a single coil unit or a combination of coil units based on the system requirements and switching network complexity.

Industry optimized elements – In this research, one of the presented approaches is selection of optimized energy storage components in terms of energy per volume (Joule/m^3). This approach prefers many small components on few bulky ones. The result concludes to much higher energy density system.

Positioning and velocity sensing – An active inexpensive positioning and velocity high sensing method, without any special machining used in this study. The method is based on real-time inductance change which provide more information and higher precision than optical based single spot detection at a fraction of a cost.

5.2. Suggestions for future research

Full optimization – All the components in the design can be optimized in terms of energy density because the same industry inclined optimization is true in regards to other elements.

Governor for multiple modules – Define a “master” module to control and monitor the operation of the module together. Information will be sent throughout the module down to the master module. A visual component can be connected in order to display live status. Also, protection against overcurrent, overvoltage, overtemperature, etc. should be added to the module.

Integration – Integration of the capacitor charger with the backend electrical systems can be done to create a single automatic close module. The frontend and backend systems will can design to be manufacturer on a new single small PCB.

6. Appendix

6.1. Appendix A – Capacitor charging time - mathematical derivation

Calculation of the charging time is presented in this section. The voltage across the output capacitor, V_{out}, is calculated in each half-switching cycle based by accumulating the previous voltage and the delta voltage added in the current half-switching cycle. The equation is presented as follows:

$$V_{out_n} = V_{out_{n-1}} + \Delta V_n. \tag{6.1}$$

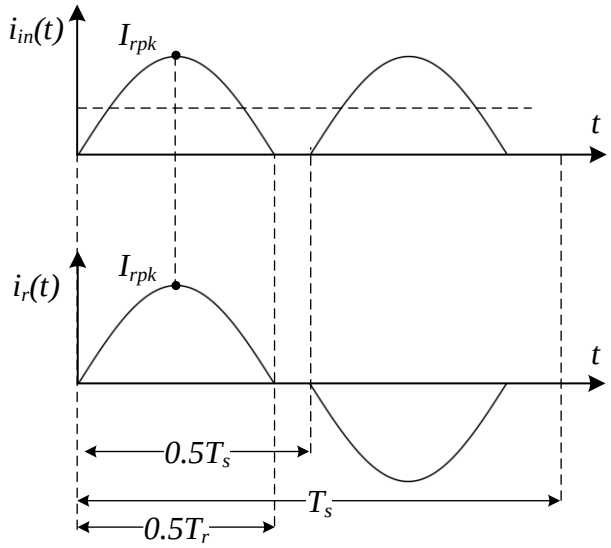


Fig. 6.1 Tpical waveforms in cpacitor charger with switching cycle time T_s and resonant time T_r. Top trace: current flows out from the input power supply i_{in}. Bottom: resonator's current i_r.

Let's find ΔV_n, using the differential equation of a capacitor charged with I_{avg}:

$$\Delta V = \frac{1}{C_{out}} I_{avg}\, \Delta T. \tag{6.2}$$

From Fig. 6.1 we can substitute the average current, I_{avg} and it gives us:

$$\Delta V = \frac{1}{C_{out}} \left(\frac{2}{\pi} I_{r_{pk}} D\right) \frac{T_s}{2}, \tag{6.3}$$

where $D = \frac{\frac{T_r}{2}}{\frac{T_s}{2}}$ is the ratio between the resonance time, T_r, and the switching cycle, T_s, and I_{rpk} is the peak current in the resonator (resonant circuit of charger, see Fig. 6.1). Since the output capacitor is isolated with N turns ratio transformer and because the charger operates in resonance, the value of I_{rpk} dependent in the input and output voltage. It leads to:

$$\Delta V = \frac{1}{C_{out}} \frac{2}{\pi} \left(\frac{V_{in} - \frac{V_{out}}{N}}{R} \frac{1}{N} \right) D \frac{\mathrm{T_s}}{2}, \tag{6.4}$$

where the expression inside the bracket is the transformer primary peak current, I_{rpk}, dependent in the output capacitor voltage, V_{out}, and the total loop resistance (including stray resistance, capacitor ESR, MOSFETs R_{ds_on} and inductor resistance). Rearranging the last equation leads to:

$$\Delta V_n = K(V_{in} - \frac{V_{out_{n-1}}}{N}), \tag{6.5}$$

where $K = \frac{DT_S}{NRC_{out}\pi}$ and now ΔV_n is a function of the output voltage in the *n*-th half-switching-cycle.

Now, substitute (6.4) in (6.1) leads to:

$$V_{out_n} = V_{out_{n-1}} + K(V_{in} - \frac{V_{out_{n-1}}}{N}), \tag{6.6}$$

$$V_{out_n} = V_{out_{n-1}} + KV_{in} - \frac{K}{N} V_{out_{n-1}} = KV_{in} + \left(1 - \frac{K}{N}\right) V_{out_{n-1}}. \tag{6.7}$$

Now substitute $V_{out_{n-1}}$ and we get:

$$V_{out_n} = KV_{in} + \left(1 - \frac{K}{N}\right) \left[V_{out_{n-2}} + k \left(V_{in} - \frac{V_{out_{n-2}}}{N} \right) \right], \tag{6.8}$$

$$V_{out_n} = KV_{in} + \left(1 - \frac{K}{N}\right) KV_{in} + \left(1 - \frac{K}{N}\right)^2 V_{out_{n-2}} \tag{6.9}$$

For *n=M* we get the following equation:

$$V_{out_n} = KV_{in} \left[1 + \left(1 - \frac{K}{N}\right) + \left(1 - \frac{K}{N}\right)^2 + \cdots + \left(1 - \frac{K}{N}\right)^{M-1} \right] + \left(1 - \frac{K}{N}\right) V_{out_0}. \tag{6.10}$$

Assuming charging start from fully discharged capacitor, i.e. $V_{out_0} = 0$:

$$V_{out_n} = KV_{in} \sum_{n=1}^{M} \left(1 - \frac{K}{N}\right)^n = KV_{in} S_M, \tag{6.11}$$

Where S_M is sum of a geometric progression. The last equation converges to:

$$V_{out_n} = KV_{in} \frac{1 - \left(1 - \frac{K}{N}\right)^M}{1 - \left(1 - \frac{K}{N}\right)} = NV_{in} \left[1 - \left(1 - \frac{K}{N}\right)^M \right]. \tag{6.12}$$

Comparing the last equation to a target charging voltage, V_T leads to:

$$V_{out_n} = V_T = NV_{in} \left[1 - \left(1 - \frac{K}{N}\right)^M \right], \tag{6.13}$$

Now, taking *M* out of the last equation and remember that it represents the number of half-switching cycles with duty ratio *D* gives us:

$$M = \frac{\log(1-\frac{V_T}{NV_{in}})}{\log(1-\frac{K}{N})}. \tag{6.14}$$

Therefore, charging time of a capacitor with capacitance *C* to a target voltage, V_T, is equal to:

$$T_{CHG}(V_T) = M\frac{T_s}{2} = \frac{\log(1-\frac{V_T}{NV_{in}})}{\log(1-\frac{K}{N})}\frac{T_s}{2}, \tag{6.15}$$

where:

$K = \frac{DT_s}{NRC_{out}\pi}$,

$D = \frac{T_r}{T_s}$

and, *N* is the transformer turns ratio.

6.2. Appendix B – Efficiency in capacitor charging process - mathematical derivation

The following mathematical derivation calculates the efficiency of the capacitor charger during *M* cycle of charging. The method calculates the average power dissipated in each half of a switching cycle and also the power delivered from the power supply in each half of a switching cycle. Then, it sums all power dissipated, and all input power deliver during charging and divide the results to get the efficiency of the charger during *M* half-cycles of charging.

V_{out} is the output capacitor voltage (after *N* turns ratio transformer) and *R* is the total loop resistance including stray resistance, capacitor ESR, MOSFETs R_{ds_on} and inductor resistance.

$$P_{loss_n} = P_{loss_{n-1}} + R \cdot I^2_{RMS,\ n} = P_{loss_{n-1}} + R \cdot \left(\left(\frac{V_{in}-\frac{V_{out_n}}{N}}{R}\right)\frac{1}{\sqrt{2}}\right)^2 \tag{6.16}$$

$$P_{loss_n} = P_{loss_{n-1}} + \left(V_{in} - \frac{V_{out_n}}{N}\right)^2 \frac{1}{2R} \tag{6.17}$$

Appendix

$$P_{loss_{n+1}} = P_{loss_{n-1}} + \left(V_{in} - \frac{V_{out_n}}{N}\right)^2 \frac{1}{2R} + \left(V_{in} - \frac{V_{out_{n+1}}}{N}\right)^2 \frac{1}{2R}. \quad (6.18)$$

For $n = M$ we get:

$$P_{loss_M} = P_{loss_1} + \frac{1}{2R}\sum_{n=1}^{M}\left(V_{in} - \frac{V_{out_n}}{N}\right)^2, \quad (6.19)$$

Substitute V_{out_n} with (6.6) and remembering that $P_{loss(n=0)}$= 0, gives us:

$$P_{loss_M} = \frac{1}{2R}\sum_{n=1}^{M}\left(V_{in} - \frac{1}{N}NV_{in}\left[1 - \left(1 - \frac{K}{N}\right)^n\right]\right)^2 = \frac{V_{in}^2}{2R}\sum_{n=0}^{M}\left(1 - \frac{K}{N}\right)^{2n}. \quad (6.20)$$

In the same way, let's find P_{in_n};

$$P_{in_M} = \sum_{n=1}^{M} V_{in} \cdot I_{in-avg} = \sum_{n=1}^{M} V_{in} \cdot \left(\frac{2}{\pi} I_{in-pk}\right) = \sum_{n=1}^{M} V_{in} \cdot \left(\frac{2}{\pi}\left(V_{in} - \frac{V_{out_n}}{N}\right)\frac{1}{R}\right), \quad (6.21)$$

$$P_{in_M} = \sum_{n=1}^{M} \frac{2V_{in}}{\pi R}\left(V_{in} - \frac{V_{out_n}}{N}\right), \quad (6.22)$$

Substitute V_{out_n} with (6.6), gives:

$$P_{in_M} = \frac{2V_{in}}{\pi R}\sum_{n=1}^{M}\left(V_{in} - \frac{1}{\mathrm{N}}NV_{in}[1 - \left(1 - \frac{K}{N}\right)^n]\right) = \frac{2V_{in}^2}{\pi R}\sum_{n=1}^{M}\left(1 - \frac{K}{N}\right)^n. \quad (6.23)$$

Dividing (6.20) by (6.23) gives the efficiency after M half switching cycles:

$$\eta_M = 1 - \frac{P_{loss_M}}{P_{in_M}} = 1 - \frac{\frac{V_{in}^2}{2R}\sum_{n=1}^{M}\left(1-\frac{K}{N}\right)^{2n}}{\frac{2V_{in}^2}{\pi R}\sum_{n=1}^{M}\left(1-\frac{K}{N}\right)^{n}} = 1 - \frac{\pi}{4}\frac{\sum_{n=1}^{M}\left(1-\frac{K}{N}\right)^{2n}}{\sum_{n=1}^{M}\left(1-\frac{K}{N}\right)^{n}}. \quad (6.24)$$

Letting q be defined as $q = 1 - \frac{K}{N}$, using sum of a geometric progression gives us the wanted result which is the charging efficiency after M/2 cycles:

$$\eta_M = 1 - \frac{\pi}{4}\frac{\frac{1-q^{2\mathrm{M}}}{1-q^2}}{\frac{1-q^M}{1-\mathrm{q}}} = 1 - \frac{\pi}{4}\frac{1-q^{2\mathrm{M}}}{1-q^2}\frac{1-\mathrm{q}}{1-q^M} = 1 - \frac{\pi}{4}\frac{1+q^M}{1+q}. \quad (6.25)$$

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נמוכים בצורה משמעותית מהמתח הכולל הנבנה במערכת וכך גם הזרמים. בנוסף, הסגמנטים אינם תלויים זה בזה ויכולים לעבוד בצורה עצמאית לחלוטין.

המחקר כולל את כל השלבים הנדרשים: סקר ספרות לטופולוגיות האפשריות למטען, בחירת הטופולוגיה על סמך התאמה לאפליקציה הנדרשת ואנליזה של המערכת על ידי שימוש בתוכנות סימולציה למעגלים חשמליים. מעבר לכך, המחקר כולל את שלב ההוצאה לפועל של המערכת, קרי העברה מתכנון לייצור אב-טיפוס. שלב זה כולל: בחירת רכיבים מתאימים, בחירת רכיב לאגירת האנרגיה החשמלית ותכנון כרטיס PCB. כמו כן, המחקר כולל תוצאות מעשיות שפורסמו כמאמר והרצאה בכנס – IEEE Workshop on Control and Modeling for Power Electronics [55] וכן כמאמר והרצאה בכנס – IEEE Applied Power Electronics Conference and Exposition (APEC).

תקציר

עבודה זו מביאה גישה מקורית וחדשה המאפשרת לתכנן וליישם מערכת לאגירה ופריקה של אנרגיה חשמלית תוך מזעור הנפח הכולל של המערכת (בסנטימטרים מעוקבים). מערכת מסוג זה כוללת מטען ומערך תאים לאגירת מטען חשמלי. המערכת מחוברת למקור מתח נמוך כמקור האנרגיה. המטרה המרכזית בעבודה זו היא לנהל את תהליך העברת האנרגיה דרך כל השלבים בשרשרת תוך הקטנת ממדי המערכת לערכים מינימליים. העבודה מתמקדת בדרישות לכמות אנרגיה מספקת וקצב הטעינה הנדרשים עבור אפליקציה מסוימת. פרמטרים אלו ועוד מהווים את השיקולים בבחירת הטופולוגיה החשמלית, הרכיבים השונים, שיטת הבקרה ועוד. השיטה להקטנת ממדי המערכת שמתוארת בעבודה זו מבוססת על בחירת רכיבים למתח נמוך וזאת על אף שהמתחים במערכת הם מתחים גבוהים. רכיבים אלו הם מעיין אבני בניין קטנות המשמשות לבניית מערכת גדולה מהם מספר מונים. הייחוד הוא בבחירת אבני הבניין האלו: רכיבים אלקטרוניים בעלי יחס גבוה ביותר של צפיפות אנרגיה ו/או הספק ליחידת נפח. מתוך כך, על ידי שימוש ברכיבים כאלו בלבד, ניתן להגיע, בסופו של דבר, למערכת עם ממדי נפח קטנים בהרבה בהשוואה למערכת הבנויה בגישה הקונבנציונלית המשתמשת ברכיבים גדולים המיועדים למתח וזרם הסופיים.

אחת המטרות של עבודה זו מתמקדת במטען. המטען הוא למעשה ממיר חשמלי DC-DC בעל יחס המרה גבוה. הוא מחובר ישירות אל מתח הכניסה הנמוך (מקור האנרגיה) וביציאתו מייצר מתח גבוה לטעינת תא אנרגיה. תא אנרגיה כזה יכול להיות קבל, סופר-קבל, מצבר, סוללה וכולי. ממטען כזה נדרשת היכולת למשוך כמות אנרגיה גדולה בתוך פרק זמן קצר. אלמנט נוסף הוא שליטה בהספק הרגעי המרבי הנצרך לטעינה. מעבר לכך, שיטת העברת האנרגיה צריכה להבטיח את היכולת לעצור את הטעינה ולנתק את המטען במינימום זמן ובמינימום מאמצים על הרכיבים וזאת בכל רגע נתון. בבחירת הטופולוגיה למטען יש לקחת בחשבון דרישה זו ולכן באופן טבעי שיטת העבודה להעברת האנרגיה היא Discontinuous Conduction Mode – DCM. ממיר DCM הוא ממיר שבו לא זורם זרם לכל אורך מחזור המיתוג, כלומר ישנו פרק זמן בכל מחזור מיתוג שבו הזרם העיקרי במערכת הוא אפס. בשיטת עבודה כזו, ניתן יהיה לנתק את המטען בקלות ולכל היותר בזמן מחזור מיתוג אחד.

מטרה נוספת וחשובה לא פחות מתמקדת ביכולת של המערכת לצבור מקסימום אנרגיה. לכן, באופן טבעי, נשתמש במספר תאי אגירת אנרגיה כנדרש עבור אפליקציה מסוימת. כלומר, כל התאים אמורים להיטען. בנוסף, נרצה לטעון אותם בצורה שווה ומאוזנת. הסיבה לכך נעוצה במספר גורמים ומשתנה בהתאם לסוג התא, בין אם זה קבל או סוללה. למשל, בבחירת סוללות ליתיום, נדרוש טעינה מאוזנת של כל הסוללות כדי: (1) להבטיח יכולת טעינה ופריקה של כל האנרגיה הפוטנציאלית הקיימת ו (2) כדי לשמור על דגרדציה זהה בזמן החיים (SoH) של כל הסוללות יחד. טעינה מאוזנת אם כן, מחייבת שימוש בשיטת טעינה ואיזון שתבטיח זאת ועל כך ארחיב בעובדתי זו.

מתוקף היכולת של המערכת לשרת מבחר מגוון של אפליקציות, נרצה לאפשר גמישות בכמות האנרגיה הניתנת לאגירה אך עדיין לשמור על ממדים זעירים ככל הניתן. במלים אחרות, יש להבטיח כי המערכת יכולה להיטען בכל כמות אנרגיה נדרשת ושאין מגבלה בנושא זה. לכן, הגישה להתמודדות עם הבעיה היא שימוש בשיטת הסגמנטים: מערכת-על המורכבת ממספר מערכות. כל מערכת תיקרא סיגמנט. כל הסיגמנטים מחוברים לאותו מקור מתח בכניסה (בצורה מקבילית) אך מוצאיהם מחוברים בטור. בצורה כזו ניתן להגיע למתחים גבוהים מאוד ולטעון לאנרגיות גבוהות מאוד כנדרש. בנוסף, כמות ההספק הנצרכת ממקור הכניסה מוכפלת עם כל הוספה של סיגמנט, אך הזרם הזורם בכל סיגמנט הוא מוגבל ליכולת שלו ובכך מקטינים את התנגדות הכניסה. כל זאת מתבצע כך שכל סיגמנט רואה מתחים

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חיבור זה מהווה חלק מהדרישות לקבלת תואר מגיסטר בהנדסה

מאת: דודי דיין

מנחה:

פרופ' מור מרדכי פרץ

המחבר: דודי דיין ..... תאריך: .....

מנחה: פרופ' מור מרדכי פרץ ..... תאריך: .....

יו"ר ועדת הוראה לתואר שני:

שם: .... תאריך: .....

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