BEN-GURION UNIVERSITY OF THE NEGEV
FACULTY OF ENGINEERING SCIENCES
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

DEVELOPMENT AND IC IMPLEMENTATION OF MULTI-MODE CONTROLLERS FOR HIGH-PERFORMANCE VOLTAGE REGULATION

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE MSc. DEGREE

By: Tom Urkin

Supervised by:
Prof. Mor Mordechai Peretz

September 2019

BEN-GURION UNIVERSITY OF THE NEGEV
FACULTY OF ENGINEERING SCIENCES
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

DEVELOPMENT AND IC IMPLEMENTATION OF MULTI-MODE CONTROLLERS FOR HIGH-PERFORMANCE VOLTAGE REGULATION

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE MSc. DEGREE

By: Tom Urkin

Supervised by:
Prof. Mor Mordechai Peretz

Author:	Tom Urkin	Tom Urkin ……	Date: ……
Supervisor:	Prof. Mor Mordechai Peretz	Mor M. Peretz ……	Date: ……

Chairman of graduate studies committee:

Name:	……	……	Date: ……

September 2019

אוניברסיטת בן-גוריון בנגב
הפקולטה למדעי ההנדסה
המחלקה להנדסת חשמל ומחשבים

תכנון ומימוש של בקרים מרובי מצבים לבקרת מתח מתקדמת של ממירים מתמתגים על גבי שבב

חיבור זה מהווה חלק מהדרישות לקבלת תואר מגיסטר בהנדסה

מאת: תום אורקין

מנחה:

פרופ' מור מרדכי פרץ

September 2019

אוניברסיטת בן-גוריון בנגב
הפקולטה למדעי ההנדסה
המחלקה להנדסת חשמל ומחשבים

תכנון ומימוש של בקרים מרובי מצבים לבקרת מתח מתקדמת של ממירים מתמתגים על גבי שבב

חיבור זה מהווה חלק מהדרישות לקבלת תואר מגיסטר בהנדסה

מאת: תום אורקין

מנחה:
פרופ' מור מרדכי פרץ

המחבר: תום אורקין ..... תאריך: .....

מנחה: פרופ' מור מרדכי פרץ ..... תאריך: .....

יו"ר ועדת הוראה לתואר שני:

שם: .... תאריך: .....

September 2019

Dedicated to my parents, for their love, endless support and encouragement in the journey that started at the launch site and ended with the submission of this thesis.

September 2019

תקציר

עבודה זו מציגה אתגרים בהתקדמות של ממירי הספק ממותגים לכיוון זמני תגובה קצרים עבור שינויים בעומס ונצילות מקסימלית בהתאם לחומרת דרגת ההספק. העבודה מתמקדת בעיקר בבעיית תופעת המעבר בעומס של ממירים ממותגים, אשר מגבילה את מזעור מערכות אלו. המטרה העיקרית של עבודה זו היא הקטנת הממדים של ממירים ממותגים ושיפור יעילות עיבוד האנרגיה של ממירים אלו. לצורך כך נוהל מחקר בשני אפיקים: 1) השוואת כל מצבי העבודה של הממיר במצב יציב ובחינת יכולת עיבוד האנרגיה עבור יחסי המרה שונים. הבאת יכולת זו למקסימום בוצעה על ידי הפעלת הממיר במצבים שונים עבור יחסי המרה שונים בהתאם לתוצאות הניתוח האנליטי. 2) שימוש בשיטות בקרה לא לינאריות מתקדמות המבוססות על מרחב המצב.

כמו כן, עבודה זו מציגה את האתגרים במימוש ואינטגרציה של בקרה דיגיטלית על גבי שבב. תכנון בקר על גבי שבב המסוגל להתאים את פעולתו עבור מגוון רחב של דרגות הספק היא משימה מאתגרת. מימושו של הבקר בתהליכים אוטומטיים מצריך שימוש בכלים מתקדמים ודורש עבודת הכנה רבה, אך התוצאה המתקבלת מאפשרת מימוש על פלטפורמות ייצור שונות כמו גם שטח קטן יותר וצריכת הספק נמוכה יותר בהשוואה לבקרים הממומשים עם רכיבים אנלוגיים. לצורך כך נוהל מחקר בשני אפיקים: 1) תיאור הבקר על ידי שפת תיאור חומרה. 2) מימוש המודולים התומכים, כמו ממיר אנלוגי לדיגיטלי, בכלים אוטומטיים המבוססים על ספריות תאים סטנדרטיים.

אחת המטרות של עבודה זו היא לשפר את התגובה לתופעת מעבר בעומס של ממירים מייצבי מתח. גודלם של הרכיבים הריאקטיביים בממירים אלה נקבע לפי דרישות תגובת המעבר בשינויי עומס, לכן על ידי שיפור תגובה זו ניתן להקטין משמעותית את גודלם של ממירים אלה. המחקר התמקד בממיר מסוג non-inverting buck-boost אשר מהווה מעין הכלאה בין ממיר ה-buck וממיר ה-boost. בקר היברידי, המשלב בקר לינארי עבור מצב יציב ובקר לא לינארי עבור שינויים בעומס, מומש על מנת לשפר את נצילות הממיר במצב יציב ואת תפקודו עבור שינויים בעומס. פרק זה במחקר פורסם כמאמר בכנס IEEE Applied Power Electronics Conference and Exposition (APEC) 2018 [1] וכחלק מעבודה נרחבת יותר בג'ורנל IEEE Transactions on Power Electronics [2].

תפקודו של בקר לא לינארי המבוסס על מרחב המצב תלוי במידה רבה ביכולת לשערך את העומס אותו מזין הממיר. על מנת לספק קריאה מדויקת של זרם העומס מבלי להוסיף חומרה נוספת פותחה במחקר זה שיטה חדשה לשערוך זרם העומס תוך שימוש בחומרה הקיימת בבקרים סטנדרטיים. שיטה זו יושמה ונבדקה עבור טווח רחב של שינויים בעומס בסימולציה ובמעבדה. תהליך שערוך זרם זה פורסם כמאמר בכנס IEEE Workshop on Control and Modelling for Power Electronics 2019 [3].

מטרה נוספת של עבודה זו היא החלפה מבנים אנלוגיים במבנים דיגיטליים הממומשים בכלים אוטומטיים בעבור אפליקציות של ניהול הספק על גבי שבב. בעבודה זו אחד המבנים הנפוצים ביותר, ממיר אנלוגי לדיגיטלי, מומש בצורה דיגיטלית על ידי שפת תיאור חומרה. ממיר זה מומש כחלק מבקר לינארי עבור ממיר buck והציג ביצועים מעולים תוך שימוש בתאים סטנדרטיים בלבד. ממיר זה פורסם כמאמר בכנס IEEE Workshop on Control and Modelling for Power Electronics 2018 [4].

מטרה רביעית ואחרונה של עבודה זו, היא פיתוח בקר דיגיטלי על גבי שבב בתהליך דיגיטלי מלא. במחקר זה פותח בקר עבור ממירי קבלים מתמתגים רזוננטים. בקר זה תוכנן לתמוך במגוון רחב של דרגות הספק ואינו דורש ידע מקדים

על ערכי הרכיבים הפסיביים. בקר זה מומש על גבי שבב, הכלל את כל הפריפריות הדרושות לפעילותו המלאה, כולל מעגלי דרייב לדרגת ההספק, שעון פנימי, לוגיקת בחירת מצב עבודה יעילה וכו'. פרק זה במחקר הוא חלק ממחקר נרחב יותר המציג שיטת בקרה מתקדמת לממירים עבור חוות שרתים, אשר נשלח לפרסום בשני מאמרים שונים בכנס IEEE Applied Power Electronics Conference and Exposition (APEC) 2019 [5]-[6].

נכון להיום, תוצאות עבודת המחקר מסתכמות ב: שלושה פרסומים בכנסים יוקרתיים בתחום אלקטרוניקת הספק, פרסום מאמר ז'ורנל ב-Transaction on Power Electronics שכרגע נמצא בסקירה מתקדמת, ושני מאמרים נוספים שנשלחו לכנס וכרגע נמצאים בסקירה.

Abstract

This thesis addresses present-day challenges in the advancement of switched-mode converters towards fast response times to load changes and maximum efficiency of a given power stage. The work mainly covers the load transient problem of switched-mode power supplies, a problem that limits the miniaturization of these systems. The primary aim of this thesis is to reduce the overall volume of switched-mode converters and to improve the energy processing capabilities of these systems. Two methods are studied for this purpose: 1) Comparing all possible operation modes of the converter in steady-state for various conversion ratios. The result of this comparison was the foundations for a highly efficient control scheme. 2) Advanced state-space based nonlinear control methods for high performance load transients.

In addition, this thesis addresses the challenges in the integration of digital controllers of switched-mode converters. Controller IC design which can be used for a variety of power-stages is a challenging task. Its realization by pure digital means requires the use of advanced design tools and extensive ground work. Two methods are studied for this purpose: 1) The controller has been fully described in hardware description language (HDL). 2) All supporting modules, such as ADC, were also realized in a digital manner by pure digital means and are based on standard-cell libraries.

One objective of this thesis is to improve the load transient response of voltage regulator modules (VRMs). The size of the reactive components of VRMs is determined by the load transient response, therefore by improving this response a significant reduction of the reactive components' size and volume can be achieved. The focus was on a non-inverting buck-boost converter which is a hybridization of a buck and boost converters. A hybrid controller, which incorporates a linear controller for steady-state and a non-linear controller for load transients has been realized to maximize the steady-state efficiency and minimize the overall volume the converter. This part of the research has been published in the proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC) 2019 [1], and within a larger study that has been published in the IEEE Transactions on Power Electronics [2].

The operation of a state-space based non-linear controller highly depends on the controller's ability to extract the information of the load current. To provide accurate reading of the load status, a new method has been developed, based on the existing hardware of a conventional steady-state controller. This method has been implemented and verified for a wide range of loading conditions. This part of the research has been published in the proceedings of the IEEE Workshop on Control and Modeling for Power Electronics 2019 [3].

Another objective of this thesis is to develop fully-synthesizable digital structure that perform tasks usually carried out by analog modules. In this study, one of the most frequency used analog

structure in dc-dc controllers, analog-to-digital converter (ADC), has been realized by pure digital means and based on standard-cell libraries. The module has been implemented as the main ADC of a buck converter voltage mode control loop. This part of the research has been published in the proceedings of the IEEE Workshop on Control and Modeling for Power Electronics 2018 [4].

The fourth objective of this thesis is to develop a fully-synthesizable digital controller IC for resonant switched-capacitor converters. The controller has been developed to support a wide range of power-stages, and does not require any knowledge of the passive components. The controller has been realized as IC, with all peripheral units including the drive circuitry, internal clock, configuration logic, etc. This part of the research is a part of a larger study that has been submitted to the IEEE Applied Power Electronics Conference and Exposition (APEC) 2020 [5]-[6], and currently in peer review process.

As of today, the thesis sum to: three conference publications in the most prestigious conferences in the field of power electronics, one journal publication that is in advanced review process, and two more conference papers that have been recently submitted.

Acknowledgments

I would like to thank my supervisor Prof. Mor Mordechai Peretz for his invaluable guidance and support for the past three years. Through an invaluable and rare combination of professional expertise and managerial guidance, Prof. Peretz has impelled me to excellence, all the while being a true friend providing me with the opportunities for enjoyment and for the self-fulfillment of achieving my goals. I also thank him for encouraging me to think outside of the box, to be persistent and to bring any achievement to perfection.

I want to thank Mr. Eli Abramov for being a true and supportive friend that always offers his unconditional help. I thank him for his collaboration, research work, and ideas. I wish him all the best in his further professional career, and his personal life.

I must not forget all my colleagues here at the Center for Power Electronics and Mixed-Signal IC, whose support and friendship meant so much: Mr. Guy Sovik, Mr. Erez Masandilov, Mrs. Hagit Peretz, Mr. Bar Halivni, Mr. Doodi Dayan, Ms. Heena Khand and anyone that I have forgotten to mention by name.

I want to thank PEMIC's alumni, Mr. Timur Vekslender and Mr. Yevgeny Lazarev for their support and ideas that enabled me to conduct my research in the best way possible.

Of the technical staff, I would like to thank Mr. Azrikam Yehieli and Dr. Michael Evzelman, who are responsible for the excellent working and social conditions of the laboratory.

With great appreciation, I would like to express my profound gratitude to my parents and brother, who have always supported and cheered me along this wonderful path.

Table of Contents

Figures List

Tables List

Acronyms and Abbreviations

IC – Integrated circuit
RSCC – Resonant switched-capacitor converter
CMOS – Complementary metal oxide semiconductor
PWM – Pulse width modulation
SCC – Switched-capacitor converter
ZCS – Zero current switching
PM – Power management
PDK – Process design kit
FPGA – Field programable grate array
ADC – Analog to digital converter
HDL – Hardware description language
SMPS – Switched-mode power supply
ZCS – Zero current switching
RL – Resistive load
VMC – Voltage mode control
TOC – Time-optimal control
PDK – Process design kit
PI – Proportional-integral
PID – Proportional-integral-derivative
MOSFET – Metal oxide semiconductor field effect transistor

Inline References Legend

X.XX – Chapter / Section number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure

1. Introduction

1.1. Overview of Power converters

Power supplies and power converters are essential building blocks in almost every electronic system, ranging from mobile applications and renewable energy sources to any grid-connected system. Power supplies convert the electrical energy provided by an electrical source into the desired form optimized for the target application. They can be described as a link or the transforming stage between the power source and the power supply output. This chapter will focus on switched-mode power converters, which are widely used for power processing of more than a few watts.

1.1.1. Switched-mode converters

The common components of the switched-mode power supplies (SMPS) traditionally comprise a switched reactive element and an input and output capacitors [7]-[11]. Another possible configuration is the switched-capacitor converter (SCC), which consists only of capacitive components, where at least one of them is a flying capacitor that connects to different nodes as a function of the operating state of the converter. In addition, these circuits employ solid-state devices that operate as electronic switches. Switched-mode converters are widely used for their high efficiency while fulfilling the systems' requirements such as operating under various voltage levels, output power and fast response time [7]-[11].

The operation principle of employing a switch to create a dc voltage is illustrated in Fig. 1.1. A simplified realization of a switched mode converter is shown in Fig. 1.1a with the periodic operation of the switch illustrated in Fig. 1.1b. Assuming the switch is ideal, the voltage at the output equals the input source when the switch is on, and zero when the switch is in off-state.

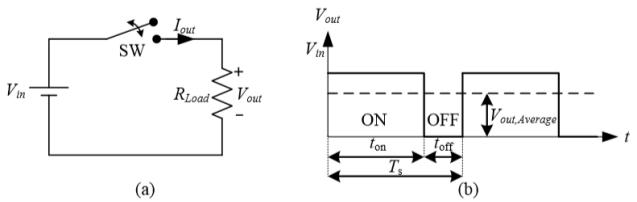


Fig. 1.1 Simplified dc-dc switching converter. (a) Equivalent circuit. (b) Output voltage.

Based on the above, the average output dc voltage can be derived by integrating the output voltage over time and divide by the switching period, as follows:

$$V_{out} = \frac{1}{T_s}\int_0^{T_S} V_{out}(t)dt = \frac{1}{T_s}\int_0^{t_{on}} Vindt = \frac{t_{on}}{T_s}V_{in} = DV_{in}\,, \tag{1.1}$$

where D indicates the ratio between the on and off times of the power switch with respect to the full switching cycle, T_s. As can be seen from (1.1), the output voltage can be controlled by adjusting the duty ratio, referred to as D. It should be noted that power converters can also process the energy to achieve output voltage that is higher than the input dc source, it will be addressed in the next section.

The linear reactive elements are used for intermediate energy storage and filtering purposes are, in many cases, the bottleneck for a cost-effective design in terms of size, weight and cost [7],[48],[51]. To overcome these limitations, switched-mode converters aim to use high-frequency switching in order to reduce component size. These reactive elements are switched in between various nodes, charging and discharging their energy. The reactive element can be an inductor, capacitor or a combination of the two.

Most converters are based on a combination of basic topologies which include buck (step-down), boost (step-up) and buck-boost (step-up or down) [38],[46]. These topologies are classified into two groups – direct energy transfer converters and indirect energy transfer converter, it will be addressed in the next section.

1.1.2. Direct energy transfer topologies

Direct energy transfer conversion is achieved when the conversion is accomplished without an energy storage stage, meaning, the converter transfers energy from the input source to the load during the on-time of the converter's switches [51],[58].

A widely used topology to perform step-down conversion is the buck topology [7]. The buck configuration is used to reduce the input voltage to a lower voltage by periodically turning the switch on and off. The operation of the buck converter can be described by separating it into two stages, as shown in Fig. 1.2. In steady-state operation, during the on-time of the switch, the input source is connected to the inductor, causing the current to ramp up with a slope of (V_{in}-Vout)/L, this current flows into both the output capacitor and the load. Once the switch is turned-off, the inductor current ramps down with a slope of V_{out}/L and the load current is supplied solely by the output capacitor. The output of this converter is a function of the duty-ratio according to (1.1).

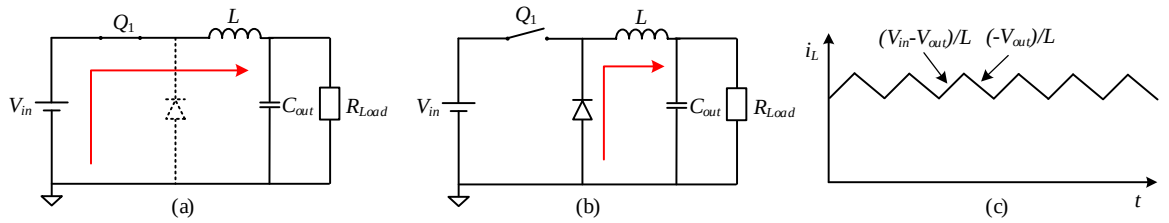


Fig. 1.2 Buck converter's operating modes and corresponding waveform. (a) On-state. (b) Off-state. (c) Inductor current under CCM operation.

1.1.3. Indirect energy transfer topologies

In contrast to the case of direct energy transfer conversion, an indirect energy conversion method uses one or more stages to store energy temporarily. Here, energy is transferred to the load only during the off-state of the switches.

Voltage step-up conversion can be achieved by a boost configuration, shown in Fig. 1.3. In steady-state operation, during the on-time of the switch, the inductor is connected to the ground, causing the current to ramp up with a slope of $(V_{in})/L$ while the load is being supplied solely by the output capacitor. During the off-state of the converter, the switch is not conducting the energy stored in the inductor is transferred to the load as well as the output capacitor.

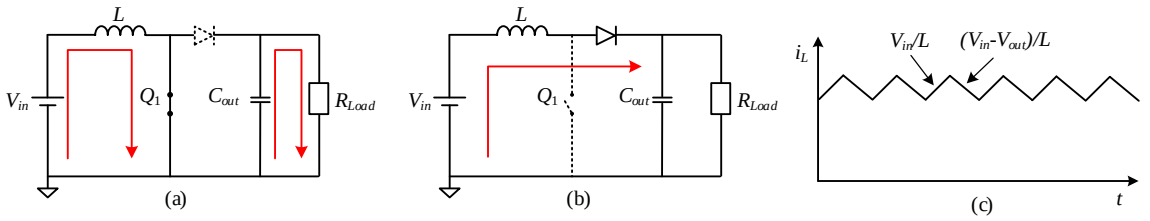


Fig. 1.3 Boost converter's operating modes and corresponding waveform. (a) On-state. (b) Off-state. (c) Inductor current under CCM operation.

The boost configuration and the buck setup have been combined into a single converter referred to as non-inverting buck-boost which is classified as an indirect energy transfer converter [7],[38], as shown in Fig. 1.4. As can be seen, the diodes have been replaced with switches, which allow continuous voltage regulation for a wide range of input and output voltages. Further discussion is provided in the next chapter.

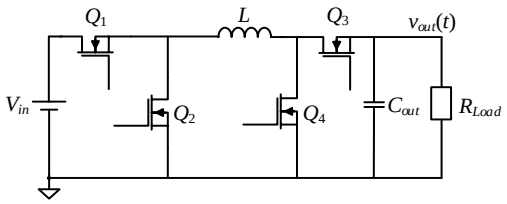


Fig. 1.4 Non-inverting buck-coost converter.

1.1.4. Switched-capacitor converters

Conventional switched-capacitor converters (SCC) do not have any inductors or transformers that dictate the flow of current in the converter. The steady-state behavior of switched-capacitor converters must be derived entirely from the charge balance of the systems' capacitors [12]-[15]. SCCs can be used to perform voltage step-up or step-down conversion. Here, a simple step-down configuration is discussed, as shown in Fig. 1.5. The switching operation of the converter's switches result in two operating stages, in which the flying capacitor is connected to the input or the output. Once the flying capacitor is connected to the input source, it accumulates charge which is transferred to the load once the capacitor is discharged to the output. To reduce the size of the converter's capacitors, the switching frequency can be increased. However, increasing the switching frequency also increases the switching losses, since SCCs are operating with hard-switching.

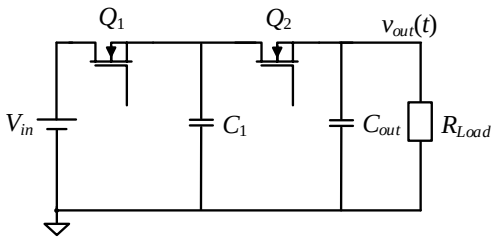


Fig. 1.5 Simple SCC.

To minimize the losses related to the hard-switching operation of conventional SCCs, inductive elements have been integrated in the converter to enable soft-switching operation [16]-[18], as shown in Fig. 1.6. Resonant switched-capacitor converters (RSCC) facilitate resonant energy transfer to achieve high efficiencies by switching according to the resonant frequency of the *L*-*C* branch. Switching at exact half-resonance period, when the current reaches zero, creates a sinusoidal shaped current, resulting in zero-current switching operation (ZCS), eliminating the switching losses. A major challenge is to determine the exact resonant period for such converters, especially in multi-stage RSCC topologies, this is addressed in chapter 4.

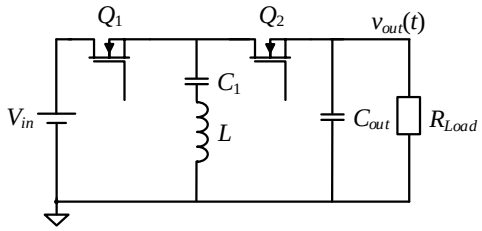


Fig. 1.6 Simple RSCC.

1.2. Control of switched-mode converters

The vast majority of switched-mode converters operate in close-loop to ensure that the output voltage is well regulated and the dynamic requirements of the system are fulfilled under both steady-state and transient conditions. Therefore, a control loop is realized which may include analog or digital controllers [23]. Modern controllers of SMPS are required to minimize steady-state error under various load conditions. In addition, recovery from loading or unloading events to the new steady-state operating point is required to support modern applications.

Modern control of SMPS is usually carried out by a digital controller, which has high immunity to component variations and can be programmed on-the-fly, thus ensuring easy integration for a variety of applications. Digital realization of the control law can be divided into two: linear control and non-linear control. Linear controller design is straightforward and its simplicity and reasonable hardware resources have made this method the preferred one for a variety of applications. A widely used implementation of such controller is PWM controller. This controller realization consists of three main building blocks: analog-to-digital converter (ADC), digital compensation unit and a digital pulse-width-modulator (DPWM) to generate the gating signals to the converters' switches.

Modern applications such as portable electronics and data centers have brought new requirements for SMPS. Among them is tighter voltage regulation, higher efficiency and accommodating load transients. As a result, a new family of controllers has emerged, referred to as non-linear controllers or state-space based controllers. Non-linear control methods provide recovery patterns for transient events, which cannot be achieved by linear controllers. The control law is designed based on the state-variables and state-equations of the converter and is chosen to accommodate the system's requirements of both transient time and state-variable's variations from the steady-state value.

1.2.1. Linear control methods

1.2.1.1. Analog voltage-mode control

Voltage mode control, carried out by pure analog means, is used in many power systems to regulate to output voltage of a given converter. Maintaining the output voltage around a reference value is achieved by adjusting a pulse-width modulated control signal, $c(t)$, as shown in Fig. 1.7. In this section, a buck topology is considered for the power stage, as shown in Fig. 1.7. The control signal, $c(t)$, is generated based on the error signal which is

produced by comparing the output voltage to a predefined reference voltage. The output voltage is usually scaled down by a voltage divider with a gain of K_v, as shown in Fig. 1.7. A conventional analog controller comprises a compensation network, referred to as *compensator*, and a modulator. These units translate the generated error signal to a pwm signal for the power stage transistors.

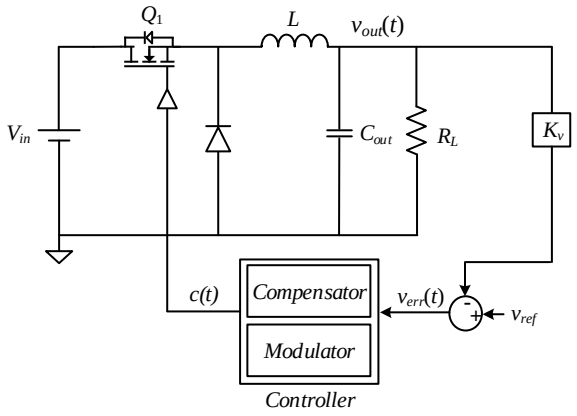


Fig. 1.7 Block diagram of voltage-mode controlled buck converter.

A more detailed implementation of an analog pwm controller is shown in Fig. 1.8. The modulator comprises a comparator and a sawtooth wave generator which produces a triangular waveform with constant frequency, referred to as the converter's *switching frequency*. A pulse-width modulated signal, $c(t)$, is generated by comparing the output of the compensator and the sawtooth waveform. The duty-cycle of this signal is proportional to the output of the compensator's output and varies to achieve zero steady-state error.

The design of the compensation network is based on the small-signal control-to-output transfer function of the power-stage and aims to achieve the highest loop bandwidth possible while ensuring zero dc error. Common compensators are proportional-integral (PI) and proportional-integral-derivative (PID). These compensators offer tight voltage regulation and relatively fast dynamic response. However, variations or drifts of the passive components' values due to tolerances and change in temperature may increase the complexity of the design procedure. A PI compensation network is shown in Fig. 1.8 along with the voltage divider which scales down the output voltage.

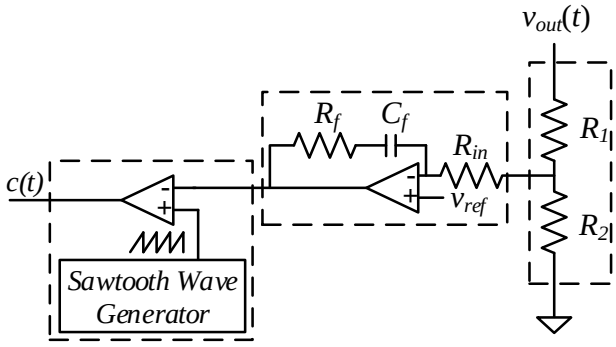


Fig. 1.8 Simplified realization of an alalog PWM controller with PI compensation network.

1.2.1.2. Digital voltage-mode control

Digital voltage-mode control is a control technique that adjusts the duty-cycle of the converter's switches based on the error signal generated by the sampled output voltage and the reference value. The converter will operate in steady-state when the error signal equals zero. Of course, in practical applications zero steady-state error cannot be achieved as a result of the digitation process and other hardware limitations, therefore a tolerance band is usually employed.

A generalized structure of voltage-mode control loop contains three main building blocks: analog-to-digital converter, digital-pulse-width-modulator and a voltage compensator, as shown in Fig. 1.9. The power stage of Fig. 1.9 is a synchronous-buck converter which performs voltage step-down conversion as discussed in 1.1. The output voltage is first sampled to generate a digital representation of the output voltage. The digital representation of the output voltage is then compared with a reference digital signal to generate the error signal. The duty-cycle command, *d*[n], is passed to the DPWM unit from the compensator block to modify the duty-cycle according to the error signal.

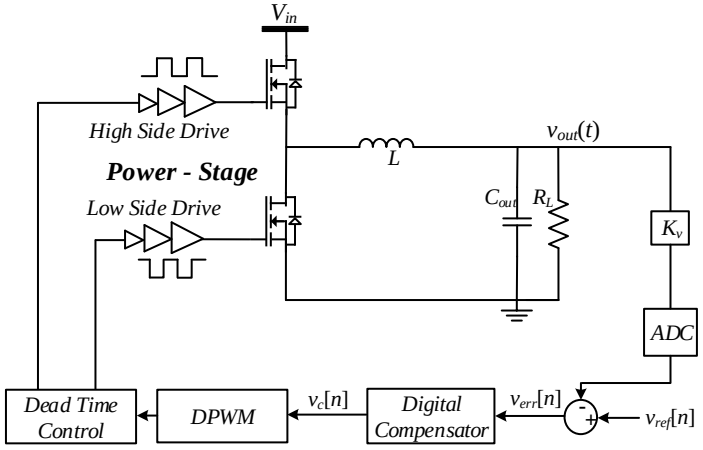


Fig. 1.9 Simplified block diagram of a digital voltage-mode controlled buck converter.

The design of voltage-mode controller aims to produce the highest loop bandwidth possible, only limited by the switching frequency [1]. The design process requires the knowledge of the plant's transfer function in order to design the feedback loop. Here, an example of a buck converter is considered, with its transfer function expressed as [55]:

$$G_{vd}(s) = \frac{V_{in}}{\frac{s^2}{\omega_0^2} + \frac{s}{\omega_0 Q} + 1} \; ; \; \omega_0 = \sqrt{\frac{1}{LC_{out}}}, \; Q = \sqrt{\frac{C_{out}}{L}} R_L \, . \tag{1.2}$$

The design procedure must also take into consideration the gain of all units in the control loop, as indicated in Fig. 1.10.

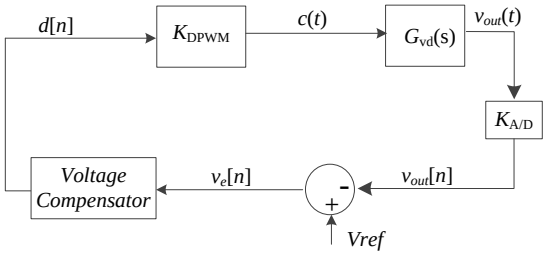


Fig. 1.10 Block diagram of the digital VM control system.

Conventional structures for digital compensators are the discrete-time equivalent of the PI and PID compensators discussed in 1.2.1.1. Their general form can be expressed as:

$$d[n] = d[n-1] = a \cdot e[n] + b \cdot e[n-1] + c \cdot e[n-2], \tag{1.3}$$

where $d[n]$ is the duty ratio control signal and $e[n]$ is the error signal. The coefficients, a-c, are found to accommodate the dynamic requirements of the system and must comply with the stability criterions to ensure proper operation of the converter.

1.2.1.3. Peak Current-mode control

The output voltage can be regulated indirectly by controlling the peak inductor current. This approach is referred to as *peak-current mode control* and its realization is shown in Fig. 1.11. Such control method provides inherent current protection and reduces the compensator's complexity. Here, a voltage compensator is used for the output voltage regulation with its output feeding the negative input of the comparator, setting the peak inductor current. This reference value, $Ic(t)$, is modified by the compensator to achieve zero steady-state error. At the beginning of each switching cycle, the inductor current ramps up with a slope of $(V_{in}\text{-}V_{out})$/L until the scaled inductor current reaches the assigned peak value.

Once this reference is achieved, the inductor current is ramped-down with a slope of V_{out}/L by conducting the power-stage's diode until the end of the converter's switching cycle.

The current regulation is usually achieved within a single switching cycle, by the *current loop*. Since this loop is much faster than the output voltage loop, it can be considered as a constant gain in the time-averaged model. It means that the inductor current behaves as a current source, which simplifies the controller design by reducing its order to a first-order system. Therefore, this system can be regulated with a PI compensator and still achieve fast dynamic response, usually accomplished by a PID compensator in a single-loop controller configuration. It should be noted that such controller realization often requires additional hardware for slope-compensation to eliminate the effects of sub-harmonic oscillations which are present in practical systems.

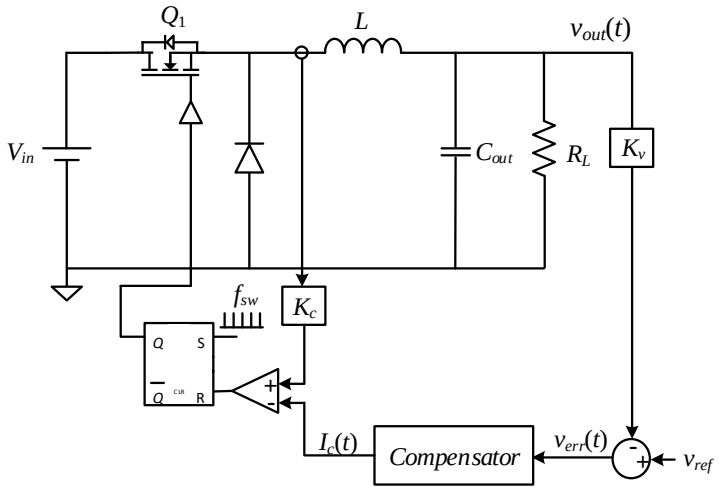


Fig. 1.11 Peak-current mode controller for buck converter.

1.2.2. Non-linear control methods

1.2.2.1. State-space representation of switched-mode convreters

Classical control theory of power converters is based on linearization of the plant expressed as a transfer function. This results in limited control of the closed-loop system by applying a linear controller such as PI or PID [19]. The state-space description of the system can provide a richer description of the plant dynamics, that may lead to enhanced switching operation of the converters switches which cannot be derived from the conventional approach mentioned earlier.

Analyzing the converter's behavior during transient can't be carried out by the linear small-signal model, since the switched-mode converter becomes nonlinear. However, analyzing the converter's behavior during transient using the state-space representation,

which does not assume linearity and takes into consideration the dynamic properties of the system, leads to a much more accurate result. The analysis is aided by the state trajectories, which are the graphical representation of the state variables movement across the stat-plane, which axis are the values of the state-variables. Modern SPMS are required to support transient based operation, and therefore state-space base representation is extensively studied and employed in modern control of SMPS.

There are some key advantages for the use of state-space based representation of SMPS compared to conventional description of a transfer function, listed below are some of them:

1. It allows accurate representation of non-linear systems
2. It can be applied on time invariant systems
3. The operation of the converter can be visually detailed on the state-plane
4. It enables the design of advanced mitigation sequences which can only be extracted from the graphical output of this representation method
5. It can be applied on systems with more than one input or one output
6. The effect of initial conditions can be easily taken into account as opposed to a transfer function description of the system

1.2.2.2. State-variables

State-variables do not change their values instantaneously and hold the information regarding the system's state at any given moment. In the simplistic case of conventional buck or boost converters, the inductor current and the output capacitor's voltage are the obvious candidates for such rule. All energy relations can be expressed in full in terms of differential equations of the state variables, referred to as state-equations.

1.2.2.3. State equavations of switched-mode converters

A switched-mode converter is a system with at least two possible operation states: when the switch conducts (on-state) and when the switch doesn't (off-state). The number of state equations will be equal to two times the number of possible converter states. Derivation of the state equation is carried out by analyzing its operation as linear circuits, in correlation to the possible converter states [20]-[21].

An example of deriving the state equations is given for a non-inverting buck-boost converter loaded by a resistive load. As previously mentioned, this converter has three operating states, which results in six state equations. The equivalent circuits for each state

are shown in Fig. 1.12 with the relationship between the state variables for each case described as differential equations.

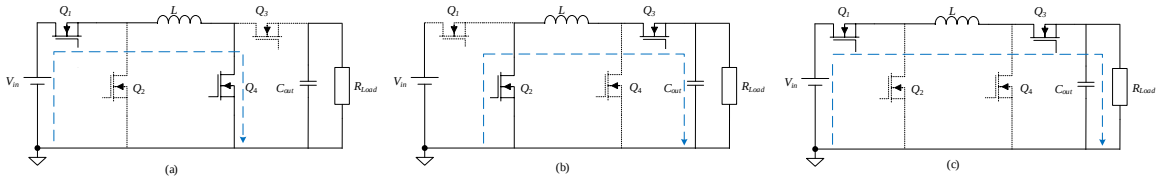


Fig. 1.12 Non-inverting buck-boost converter equivalent circuits.

$$a: \frac{dv_C}{dt} = \frac{v_C}{RC}, \quad \frac{di_L}{dt} = \frac{V_{in}}{L}. \tag{1.4}$$

$$b: \frac{dv_C}{dt} = \frac{i_L}{C} - \frac{v_C}{CR}, \quad \frac{di_L}{dt} = \frac{-v_C}{L}. \tag{1.5}$$

$$c: \frac{dv_C}{dt} = \frac{1}{C}\left(i_L - \frac{v_C}{R}\right), \quad \frac{di_L}{dt} = \frac{v_{in} - v_C}{L}. \tag{1.6}$$

1.2.2.4. State trajectories construction

State-trajectories are the visual representation of the movement of the state-variables across the state-plane. When constructing the trajectories, the time parameter is implicit, i.e. the speed of movement cannot be extracted from the trajectories. The state trajectories for each possible state are written in the following template:

$$g(v_C, i_L, v_{C0}, i_{L0}) = 0, \tag{1.7}$$

where v_{C0} and i_{L0} are the initial conditions for the output capacitor's voltage or inductor current, which are the most common state variables in control schemes of SMPS. The number of state trajectories equals the number of sub-circuits, three for the case of the NIBB converter. There are three methods for drawing the state trajectories [22]. The method used in this study is integrating the differential equations (state-equations) derived in previous section in the following manner:

$$\int f_1(v_C, i_L)\, di_L = \int f_2(v_C, i_L)\, dv_C. \tag{1.8}$$

Solving (1.8) for all three sub-circuits, (1.4)-(1.6) yields the following:

$$\frac{1}{L} V_{in}(v_C - v_{C0}) + \frac{1}{RC} v_C(i_L - i_{L0}) = 0. \tag{1.9}$$

$$\frac{1}{2C}(i_L^2 - i_{L0}^2) - \frac{v_C}{RC}(i_L - i_{L0}) + \frac{1}{2L}(v_C^2 - v_{C0}^2) = 0\,. \qquad (1.10)$$

$$\frac{1}{2C}(i_L^2 - i_{L0}^2) - \frac{v_C}{RC}(i_L - i_{L0}) - \frac{V_{in}}{L}(v_C - v_{C0}) + \frac{1}{2L}(v_C^2 - v_{C0}^2) = 0\,. \qquad (1.11)$$

Based on the state-trajectories of (1.9)-(1.11) and for different initial conditions, the graphical representation of the trajectories can be constructed, which for the case of NIBB converter yields the following:

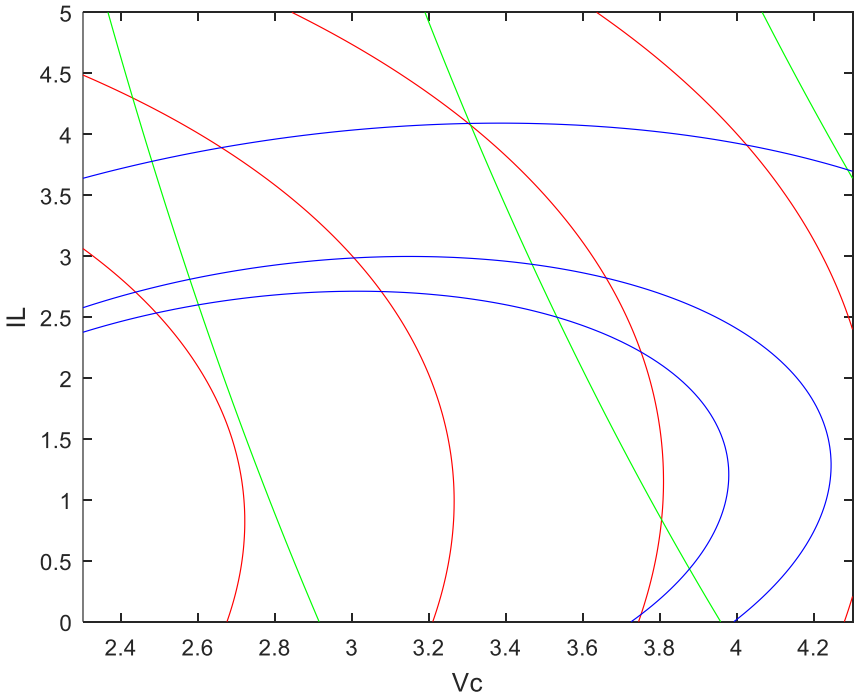


Fig. 1.13 State-plane and trajectories if a non-inverting buck-boost converter.

1.2.2.5. Time-optimal control

Time-optimal control (TOC) is a control method which results in the fastest dynamic response possible for a load transient [25]-[30]. In conventional converters with two operating states, TOC consists of two switching actions of the converter's switches. For a case of a loading event, the first trajectory will increase the energy stored in the inductor while the second one will bring the systems' variables to the new operating point. For a case of unloading transient event, the amount of energy in the system must be reduced, therefore the first trajectory will be the off one, followed by an on state to converge to the new steady-state point.

Shown in Fig. 1.14-Fig. 1.15 is TOC recovery pattern of a NIBB converter operating in step-down mode for a loading transient. Here, the switching actions utilize the conventional trajectories of a buck setup to recover from the loading event. Fig. 1.14 illustrates the state-plane and the trajectories which are used for conventional TOC of a buck converter. The timing diagrams of the recovery is shown in Fig. 1.15.

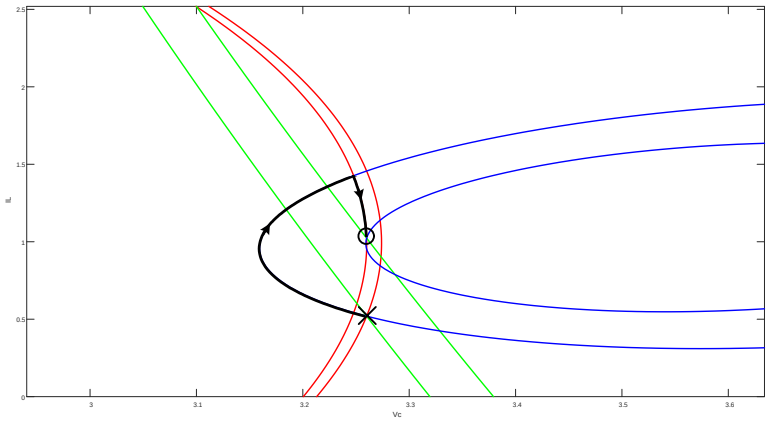


Fig. 1.14 TOC for a NIBB converter operating in step-down mode.

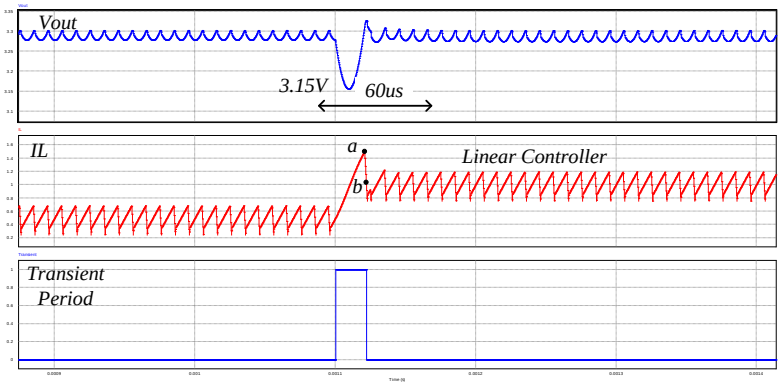


Fig. 1.15 TOC for a NIBB converter operating in step-down mode.

It should be noted that for converters with more that two operating states, such as the non-inverting buck-boost converter, TOC may require more than just two switching actions, which increases the complexity of its implementation in practical applications. Shown in Fig. 1.16 is the recovery trajectories of the same loading event, which use the additional trajectory of the boost configuration (green) available in this specific converter to further enhance the recovery pattern. As can be seen in Fig. 1.17, the additional trajectory leads to a better transient response.

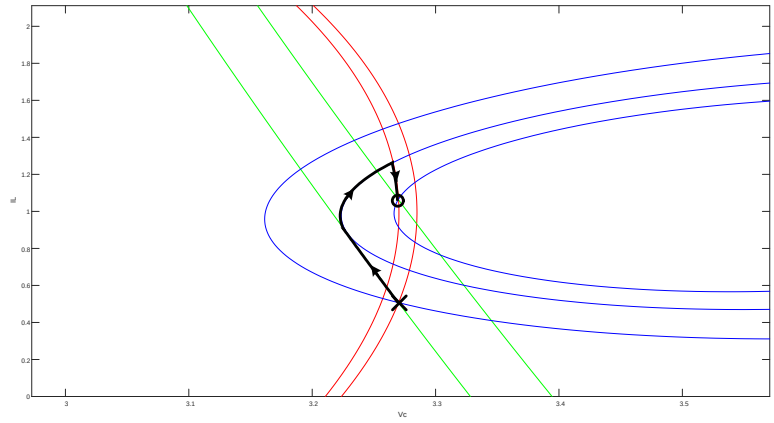


Fig. 1.16 TOC for a NIBB converter operating in step-down mode with an additional trajectory.

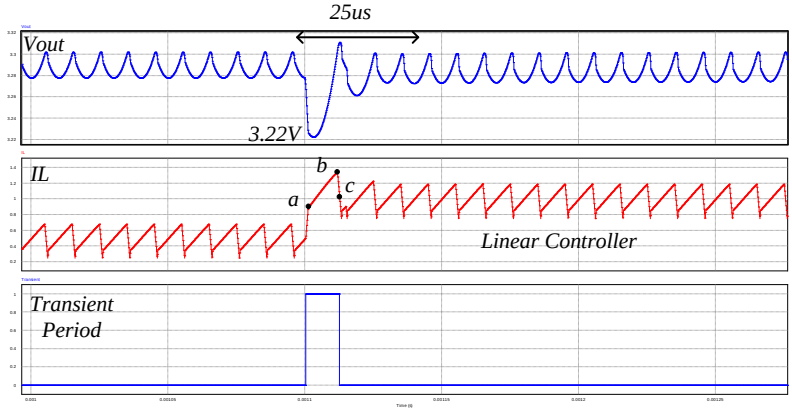


Fig. 1.17 Timing diagram of TOC for a NIBB converter operating in step-down mode with an additional trajectory.

Ideal TOC may be impractical for a wide range of applications due to complex calculations of the switching moments on-the-fly which require significant hardware to be added. In addition, TOC is sensitive to operating conditions, parameter tolerances and parasitics. To address these issues, more sophisticated mitigation algorithms have been recently investigated.

1.2.3. Multi-mode controller design

1.2.3.1. Hybrid controllers

The control objectives of modern SMPS controllers cannot be fulfilled by a single control method to achieve both steady-state and transient requirements. It has been shown that combining two control laws, one for steady-state and one for transient operation, yields significant improvement of the overall system performance [24]. Within the context of switched-mode applications, a hybrid controller merges a small-signal based controlled such as PID, to allow constant switching frequency during steady-state operation and a transient mode controller, to enable fast response to transient events with minimum voltage and

current overshoots. As can be seen in Fig. 1.18, a dedicated multiplexer sets the final gating signals to the converter's switches as a function of the operation state of the system, i.e. steady-state or transient conditions.

As in any feedback system, the controller's stability must be addressed during the design procedure. Stability criterions for the linear controller are straightforward and widely discussed in the literature [48],[58]. For the case of the non-linear controller, large signal stability is not a necessity for this controller's operation is to bring the converter around the new steady-state point. The small-signal linear controller is in charge of maintaining zero steady-state error and is used when small perturbations occur or after the transient-oriented controller has brought the converter around the new operating point. The switching operation of any large-signal based controller must bring the system around the new operating point regardless of the initial conditions. The design of such control scheme is based on the state-plane as detailed in 1.2. Further discussion is given in chapter 2.

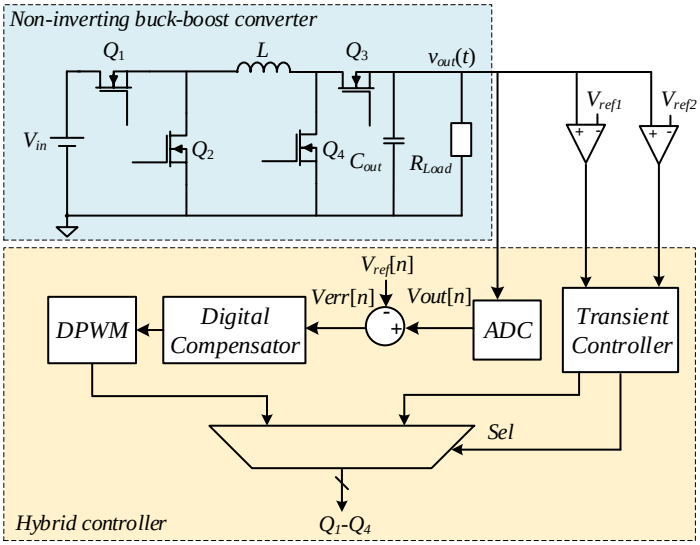


Fig. 1.18 Simplified block diagram of a NIBB converter with digital hybrid controller.

1.2.3.2. Controllers for RSCC

Single or multi-stage RSCC's high efficiency characteristics highly depend on the ability to perform the switching action when the resonant current equals zero, i.e. operating at zero-current switching (ZCS). The simplest approach is to dictate the switching actions based on the nominal values of the resonator's passive components, which determine the resonant frequency. Tolerances of the component values and drifts due to temperature and ageing are not taken into consideration in such realization, which result in poor overall efficiency. To achieve precise soft-switching operation current sensing is required. However, direct measurement of the resonant current is not a viable solution for converters operating in the

MHz range, which will require ultra-high gain-bandwidth current sensors. To avoid the design of such complex sensors, solutions that observe the zero-crossing point have been employed in RSCC controllers as shown in Fig. 1.19. Although this approach significantly increases the converter's efficiency, full ZCS operation cannot be achieved due to latencies of the sensor and the driving circuitry present in practical systems.

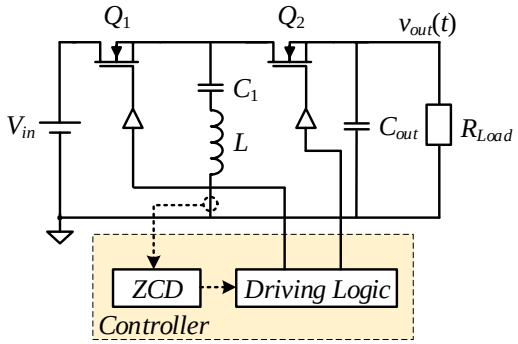


Fig. 1.19 Simplified block diagram of a zero-crossing detection based RSCC controller.

In this study, a different approach has been perused which incorporates a compensation logic that tunes into the resonant frequency of the resonant tank. The controller's operation is based on the concept of sampling at turn-off, which provides the controller with the information of the resonant current at the switching instance. Further discussion is given in chapter 4.

1.2.3.3. Peripheral units

1.2.3.3.1. Digital Pulse width modulator

The pulse-width modulator serves as a digital-to-analog converter which translates the compensator's output to the gating signals of the power stage transistors. Each digital pulse-width modulator (DPWM) has a finite set of conversion values, which results in discrete set of regulated output voltages.

The conventional approach to implement high-resolution, high-frequency DPWM is by a fast-clocked counter-comparator scheme [107]-[109]. This way, for a converter operating at switching frequency *fsw*, *n*-bit resolution DPWM requires a reference clock frequency of $2^n \cdot fsw$. For example, an 8-bit resolution DPWM for a SMPS operating at 1MHz will require a reference clock with frequency of 256MHz. Power consumption as well as design complexity are increased when fast reference clock is used.

Another approach is to implement a high-resolution DPWM which uses a relatively slow reference clock combined with digital-logic to produce the pwm signal with a resolution of

a single delay-element. A simple realization of such modulator is shown in Fig. 1.20. A counter, referred to as *master-counter*, is used to produce the coarse section of the pwm signal. Once the counter's result equals its assigned value, a digital logic block is used to produce the additional section of the pwm signal, which is shorter that the duration of the reference clock.

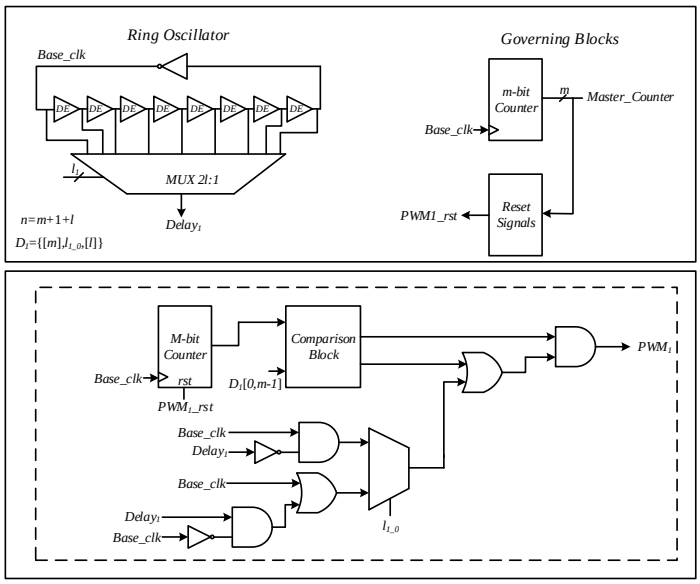


Fig. 1.20 Simplified block diagram of a high-resolution DPWM based delay-line.

An example is shown in Fig. 1.21, in which a relatively slow reference clock is used to produce a pwm signal with high-resolution without increasing power consumption or design complexity. It should be noted that this DPWM architecture can be easily modified to produce multiple pwm signals, thus making it a promising candidate for multiphase applications.

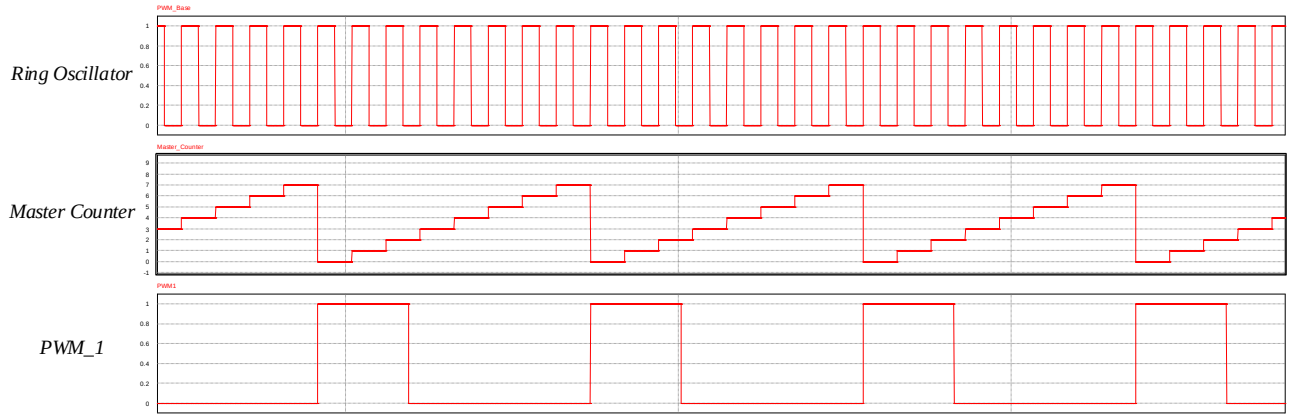


Fig. 1.21 DPWM with resolution of a single delay-element.

1.2.3.3.2. Load-estimation units

Direct measurement of the load current is prohibitive for most applications, therefore load-estimation units are incorporated in the controller design, especially for indirect-energy transfer converters [51]. The ability to execute complex mitigation patterns for fast and accurate recovery from a loading transient is correlated to the information available to the controller. There are various load estimation procedures which are based on prior knowledge of the converter's passive components [27] or information of past load-estimation results [25]. Self-tuning estimators have also been presented in the literature [51] which provide accurate readings of the load status regardless of components' variations and require no prior knowledge of the components' values or past estimation results.

The implementation of the self-tuning estimator is described in Fig. 1.22. It is based on a look-up-table (LUT) and on estimation of the load current through a comparison with a measurement of the known current value, named unity current. The LUT of the estimator is populated during the converter start-up. Over that period, the LUT's entries are stored, i.e. current and voltage threshold values are created, from measurement of the output voltage. After the writing of the values in the tables is completed, the output voltage deviation is used as an address (input of Fig. 1.22) to determine the LUT's outputs, i.e., V_{th} and I_{th} values. Upon the converter power-up a generic LUT is assigned. The known current of the protective resistor R_{bld} (also known as bleeding resistor), named unit current I_{unit}, is used for the system calibration. During this time, the load is disconnected from the output of the converter, i.e., switch M_{out} is turned off, and in addition, switches Q_1, Q_3 are off while Q_2, Q_4 are on. This assures that the current path to R_{bld} is via the output capacitor alone. The value ΔV_1 is a function of I_{unit} and is measured as:

$$\Delta V_1 = v_{ADC}[n] - v_{ADC}[n-1] = \frac{V_{ref}}{R_{bld}} \frac{\Delta t}{C} = I_{unit} \frac{\Delta t}{C} . \quad (1.12)$$

where Δt is the sampling interval, v_{ADC}[n] is the current value of the ADC output and v_{ADC}[n-1] is the ADC value from the previous sampling cycle. The value ΔV_1 is used to populate the LUT with I_{th} and V_{th} values for the full range of allowable output voltage deviations.

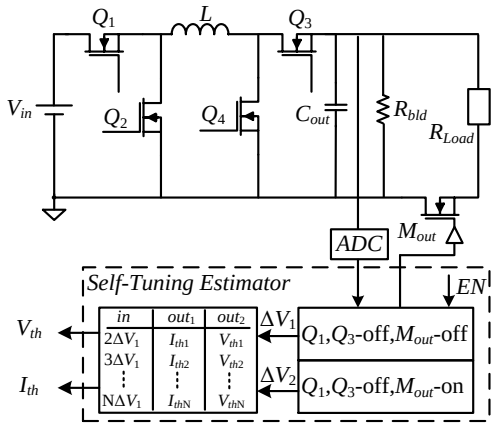


Fig. 1.22 Block diagram of a self-tuning estimator for a NIBB converter.

Upon power up of the converter and population of the LUT is completed, the switch M_{out}, usually existing in the applications of interest is turned on. During the remaining portion of the converter operation, the LUT is used to produce I_{th} and V_{th} during transient events. The input to the LUT is now the voltage deviation ΔV_2 measured during the on time of Q_1 and Q_4. During a transient event, the load current $I_{out_}$new is estimated as:

$$I_{out\_new} = \frac{\Delta V_2}{\Delta V_1} I_{unit} \,. \tag{1.13}$$

1.3. ASIC integration of controllers for DC-DC converters

1.3.1. Introduction and motivation for IC integration

Modern power management controllers rely on the integration of the power stage driving circuitry, conversion blocks and digital logic [31]-[34]. The digital logic can be written in a way that enables the compensation scheme to be re-programed on-the-fly based on the specifications of the power-stage. This also applies for other supporting blocks which perform house-keeping and monitoring tasks. Digital controllers have inherently lower sensitivity to process and parameter variations [81][80]-[81]. Moreover, some modern control schemes or periphery modules cannot be realized with pure analog means. For example, all digital-cells based driving circuitry has been realized in [55] and achieved timing resolution of a single delay-cell. The digital realization of this module can be easily modified to support multi-phase converters and to achieve precise phase-shifter duty ratios, a task that is considered highly challenging if the modules are not highly-matched.

An application-specific integrated circuit (ASIC) is an integrated-circuit customized for a particular use. For example, control of multi-phase switched-tank converters, as

investigated in this study and discussed in 4. As standard cells' sizes have shrunk and digital design tools improved over the years, the integration density significantly increased. This directly translates to reduced costs of controller ICs of dc-dc converters. From the system perspective, the viability of a controller IC depends on the operating frequency, power consumption and the system flexibility. Full custom design, which tailored to a specific application has the potential to be more efficient and precise. However, the lack of flexibility may result in un-fixable mistakes and will have a significant delay in the time-to-market (TTM).

Standard-cell based design is a common methodology for the design of digital ICs, it is also known as "top-down" approach. This design flow is based on the standard-cell libraries the FAB provides, which may include basic logic elements such as multiplexers, adders, etc. It should be mentioned that the standard-cell libraries of different FABs may include different cells. Based on the provided cells, this design flow aims to realize the digital logic with the minimum silicon area while complying with all timing requirements set by the designer. The design in described at the functional level using a hardware-description language. This is followed by synthesis, compilation and place-and-route processes. Dedicated simulation and verification tools are used to verify the operation of the IC prior to fabrication process. In contrast to analog-based controllers, digital controller ICs scale well with technology which plays a major rule in the integration of such controllers in almost every electronic device.

1.3.2. Digital design flow

Prior to silicon realization of the controller IC, it is described in pseudo-code and all interior blocks are specified, along with the timing specifications. For example, the error calculation of the output voltage in voltage-mode must be executed only after the new reading from the ADC has been acquired [55].

The digital design flow can be divided into two main phases, as shown in Fig. 1.23. Each sub-module of the controller is described in HDL, and verified by behavioral and functional simulations prior to synthesis process. Then, each sub-module is synthesized using automatic tools into optimized gate-level representation, taking into account the design and timing constraints. Synthesis reports, such as area, power and timing reports are extracted at the end of this phase, to verify the correctness of the vendor's standard-cell based description of the IC. The output of the first phase is an HDL code, which describes the logic with the available

cells from the vendor's libraries. This HDL code includes all sub-modules as hard-IPs which are the building blocks of the highest hierarchy. It is worth mentioning that this representation does not implicate on the physical design, for the second phase of this flow optimizes the physical design based on the gate-level. In synchronous design, additional constraints on the distribution of the clock are added.

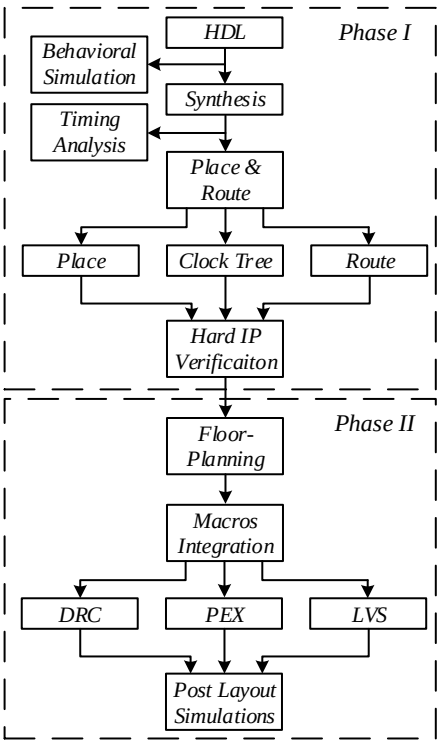


Fig. 1.23 Block diagram of the digital design flow.

The second phase of the digital design flow starts with definition of the IC's size, density and shape, referred to as "floor-planning". During this phase, all hard macros are placed, taking into consideration the IOs arraignment and the relationship between them to avoid unnecessary delays due to extensive routing. The power planning of the IC is defined after all macros have been placed, to ensure sufficient current paths throughout the chip. Logic low and high rings and stripes are added around the macros and throughout the chip. Then, all logic which is not already implemented in one of the sub-modules is added and routing is performed by automatic tools. In this thesis, the Cadence "Encounter" tool was used, which has been found very reliable and user friendly. The last step of this phase is to perform final verifications of the IC.

Design-Rules-Check (DRC) is performed to verify that the generated silicon realization does not violate any fabrication limitation. In case a violation has been detected, the routing step must be executed again. Then, a Layout-versus-Schematic (LVS) check is performed, to ensure that all logic described by the designer is indeed realized in the final IC. Once DRC

and LVS tests have passed with no errors, the final verification of the IC's operation can be performed. Parasitic extraction (PEX) is performed based on the verification purposes. During this step, parasitic capacitances, resistances and inductances can be extracted and used for the post-layout simulations which are the final step before tape-out. All DRC and LVS checks as well as parasitic extraction have been executed on the Cadence "Virtuoso" tool. This tool enables the designer to further enhance the design by manually apply changes, add structures or combine many blocks to form a large-scale IC.

1.3.3. IC realization of analog to digital converters

Power system-on-chip (SOC) which include both the power stage and the controller are complex systems that are becoming more common as the requirements for efficient power delivery are increased [31]-[34]. Analog IPs are a part of every control loop, which must use the continuous-time domain information of the converter's output voltage and inductor current to accurately fulfill its tasks. However, the nature of analog circuit design makes reusable IP a somewhat different issue than in the digital case. To overcome this limitation, and to allow the design of analog IPs that can be reused without any major modifications on various fabrication processes and applications, digital realization methods of conventionally analog circuits is perused. The use of hardware description language (HDL) is used in this study to design digital IPs that execute tasks that are usually carried out by analog circuits such as ADCs, DACs and Comparators. Reducing the amount of analog circuits in the system results in a much easier design procedure that is in many cases smaller in size and has lower power.

An ADC that uses analog circuits for the digitation process is the Flash-ADC [35]-[36], which is the fastest and one of the most accurate and reliable topologies. However, this method requires a non-negligible number of comparators and resistors in addition to digital logic at the output stage. A 2-bit flash ADC realization is shown in Fig. 1.24. As can be seen, four resistors and comparators are implemented. For most power processing applications, this architecture provides the information much faster than required on the expense of extremely large silicon area and power dissipation.

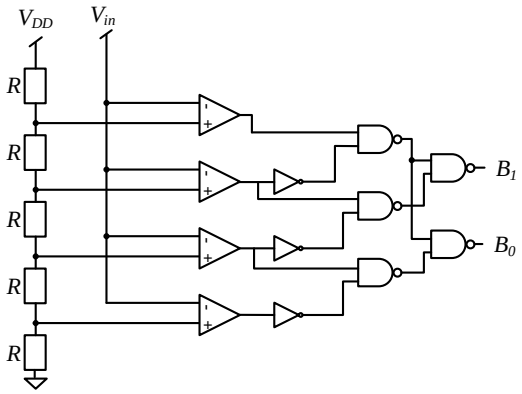


Fig. 1.24 2-bit flash ADC architecture.

To address these issues, topologies that are lean on hardware have emerged as the sigma-delta (SD) ADC which is described next.

1.3.3.2. ∑-Δ analog to digial converter

Sigma-delta ADCs are ideal candidates for power processing applications in terms of complexity and area which can produce digital representation of analog signals with frequencies varying from DC to a few MHz [80]-[81]. A conventional sigma-delta ADC (SDADC) is shown in Fig. 1.25. It consists of a summing junction, an integrator, a comparator and a 1-bit DAC.

The analog signal to be converted into a digital word has to be relatively slow compared to the internal clock, so the converter will be able to sample it multiple times on the course of a single digitation stage. This method is called oversampling. Here, the sampling rate is much higher than the SDADC output rate. The sensed signal is compared to the feedback signal, X_5, to produce the error signal, X_2. The output of the integrator block is the summation of the last two over-sampling cycles error signals. The output of the 1-bit ADC, implemented by a comparator, is the input to the LPF which accumulates the modulator's results and produces a digital representation of the sensed signal every clock cycle. In most applications, the oversampling frequency is very high, on the range on 10s of MHz, therefore a decimation filter is usually employed as the final stage of this ADC.

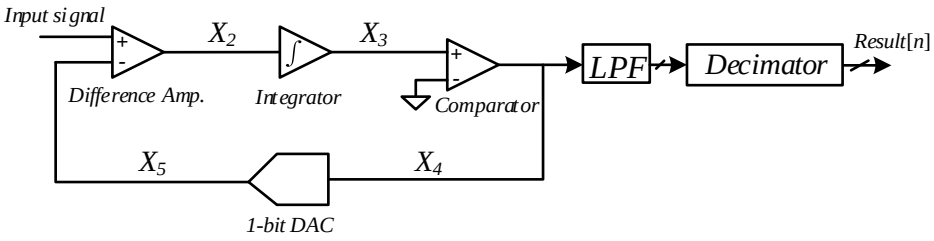


Fig. 1.25 Conventional implementation of a sigma-delta ADC.

1.4. Motivation, objectives and significance of the research program

The volume and size of switched-mode converters dictate their load transient response. Tighter output voltage regulation, faster response time to load transients and smaller volume are major concerns in the design of modern SMPS.

Integration of digital controllers as ICs for power applications, especially with uncertainties in the system parameters, is a challenging task, widely perused by both academia and industry. It would be extremely efficient if a controller can be self-tuned according to the power stage, with minimum intervention from the user.

The primary objective of this research program is to devise a new control scheme for non-inverting buck-boost converter for portable applications. The controller will combine advanced digital control methods taking advantage of this converter's unique structure, to dramatically minimize the overall volume and significantly improve efficiency during steady-state operation. It is expected that a transient controller which uses all possible converter trajectories, will achieve near optimal load transient recovery patters.

Another objective of this research program is the development of on-chip, auto-tuning fully-digital controller for dc-dc converters alongside its periphery units, such as an ADC.

More specifically, the objectives of the research program are:

1. To improve the load transient response of NIBB converter in order to reduce the overall volume and to improve its power processing efficiency.
2. To develop a new load-estimation process for indirect energy transfer converters with minimum hardware modifications.
3. Development of a new hybrid-type controller for NIBB converter that supports operation for a wide range of input voltages with improved efficiency around unity conversion ratio. In addition, Near-optimal load transient recovery profile for both loading and unloading conditions is also pursued.
4. To develop a fully-synthesizable ADC for power processing applications that performs the digitation task with low power dissipation without sacrificing accuracy.
5. Development of a new lock-in integrated controller for resonant SCC. The controller will support a wide range of single or multi-stage RSCC topologies.

2. Digital CPM Controller for Non-Inverting Buck-Boost Converter with Unified Hardware for Steady-State and Optimal Transient Conditions

This chapter introduces a new controller architecture and implementation for non-inverting buck-boost (NIBB) converter. An overview of the NIBB converter is presented, followed by steady-state analysis of the inductor current for all conventional operating modes as well as for new modes developed in this study. Near-optimal load transient recovery profile, with programmable constraints of the state variables is detailed. Then, a new load estimation procedure, which is the enabler for the non-linear control scheme, is discussed. The new controller operation is verified by simulations and experimental results of a 2-15V to 3.3V prototype.

2.1. Overview

Following the rapid growth in computing power and in particular for portable electronics, the specifications and restrictions on efficient usage of battery-powered applications have been significantly tighten to assure compact and light devices with long operation cycles. In variety of such applications, in particular as those prone to wide range of ambient temperature swing, or for cells with wide voltage range [38]-[41], the source voltage can be higher or lower than the target regulated output. Another case that requires front-end conversion flexibility is for high-performance programmable-gate arrays (PGAs) that may be fed by multiple sources [42].

It is apparent that a flexible SMPS capable of stepping down, up, or operating around unity is essential. In addition, since direct conversion as point-of-load is preferred due to efficiency considerations, then the SMPS is also required to satisfy transient requirements and comply with the system dynamic characteristics [43]-[45]. Non-Inverting Buck-Boost (NIBB) converter configuration has a long track-record of carrying out the above-mentioned prerequisites. Although it comprises of four switches with two devices in the conduction path, its efficiency characteristics and ripple efforts have demonstrated superiority in comparison to a conventional buck-boost arrangement. One of the more attractive features of NIBB converters is the capability of operating as a buck converter when step-down operation is needed and as a boost for step-up. Remaining is the region around unity in which, apparently, this converter lacks advantages than its precursor. Fortunately, several fundamental studies in the recent years [45]-[47], have been conducted around the unity region and demonstrated ripple and efficiency enhanced modes of operations. A key

challenge would be to embed all required features as well as superior transient capabilities in a simple and unified controller.

Load transient recovery is a critical factor in the design of modern switch-mode power supplies. In particular, sizing of the passive components predominantly depends on the recovery pattern of the system, since largest deviations occur during transient events. To reduce the requirements of the converter's passives and as a result, the overall volume of the SMPS, high-performance voltage regulators typically employ transient-oriented controllers, which can be either boundary or hybrid. Boundary controllers [48]-[49], among them hysteretic and sliding-mode controllers, are geometry-based methods that split the state-plane such that in one side of the boundary the operation is governed by the on state and by the off state at the other side of the boundary. Hybrid controllers [50][50]-[51] switch between two or more control laws based on the system state variables in order to obtain the performance goals. Within the context of switch-mode applications, the hybrid control law typically incorporates a steady-state linear controller (i.e., PI or PID), to allow constant operating frequency, which simplifies the design of the power converter.

As opposed to buck-type conversion, which is classified as direct-energy transfer and characterized with closed-form optimal solution for the load transient recovery and deviation, in boost-type circuits general optimization of the recovery targets is significantly more complex. For example, time-optimal recovery of buck-boost converter results in extensive voltage drop, much larger than the minimum value that can be obtained [52]. However, ideal minimal voltage drop for boost-type conversion requires infinite convergence time. On the other hand, since in this study a NIBB converter configuration is used to support wide range of conversion ratios, it stands to reason that the recovery pattern may be further enhanced, beyond the conventional definition of time-optimality, benefiting from the topological flexibility of the converter. For instance, adding boosting phase to a loading step while in step-down conversion (buck mode in steady-state).

The objective of this study is to introduce a new controller architecture and implementation for NIBB converter as shown in Fig. 2.1. It employs a simple current-programmed configuration to realize a hybrid-type controller with tight voltage regulation and excellent transient convergence, all carried out through a classic two-loop controller hardware. A new steady-state operation mode for improved efficiency and ripple characteristics around unity conversion ratio is described and analyzed. The new controller supports operation in steady-state for the full range of conversion ratios with seamless transition between modes. It is a further objective of this study to introduce detailed transient

mitigation algorithms for all operation modes, in particular for the unity conversion ratio but also for the entire operation range, enabling optimized transient recovery and untimely volume reduction of the overall solution. In addition, a load estimation procedure is delineated and demonstrated which considerably enhances the transient performance.

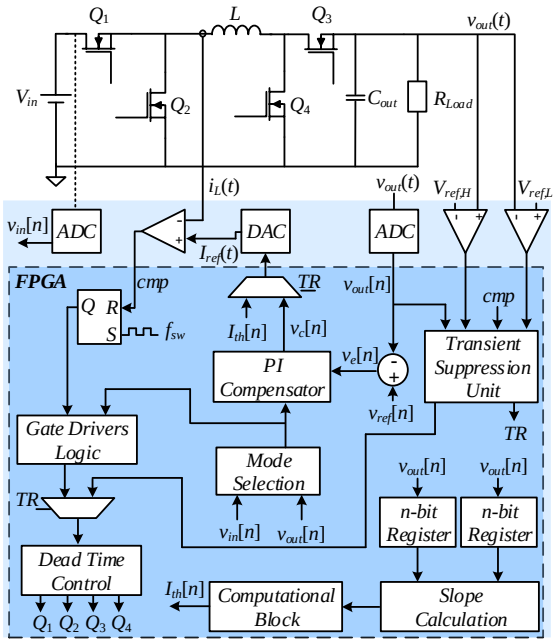


Fig. 2.1 Simplified schematic diagram of a non-inverting buck-boost converter with current-programmed controller.

2.2. Controller Architecture and Operation

The NIBB converter, shown in Fig. 2.1 has four switches, which can be divided into two pairs: Q_1 and Q_2 make up the buck pair while Q_3 and Q_4 make up the boost pair. The operation for each pair of switches is complementary. The control objective in this study is to sustain a regulated output voltage for any setting of the input voltage (within the design specifications), which may be above, below or equal to the target output, and significantly vary during operation. To this end, the system governor adjusts the switching sequence so that the converter operates at the best performing configuration for the specific voltage gain. By assignment of two duty ratio notations, d_{buck} for the pair of Q_1-Q_2 and d_{boost} for Q_3-Q_4, then the dc conversion ratio for NIBB converter can be uniformly expressed (i.e., regardless of information for the specific mode of operation) as [45]:

$$\frac{V_{out}}{V_{in}} = \frac{d_{buck}}{1 - d_{boost}} . \tag{2.1}$$

2.2.1. Controller Architecture and Operation

As can be seen in Fig. 2.1, the controller follows a two-loop current-programmed configuration with a digital outer voltage loop and inner comparator-based current loop. The voltage loop produces a digital reference, $v_c[n]$ based on the error signal, $v_e[n]$, of the voltage loop for either the peak or valley current values, depending on the operation mode. The reference current values are converted to continuous-time representation by a digital-to-analog converter (DAC) which feeds the positive input of a comparator.

To ensure proper regulation of the output voltage for all conversion ratios, a state-machine algorithm described by the flowchart of Fig. 2.2, has been incorporated. The mode of operation (i.e., step-up, step-down or unity) is determined in this study by samples of the input voltage, $v_{in}[n]$ and output voltage, $v_{out}[n]$, which are the inputs to the mode selection block (see Fig. 2.1). To prevent toggling and to ensure smooth transition between modes, the assignment of the operation mode is determined based on the steady-state value for the output voltage, $v_{ref}[n]$, and in addition, a hysteresis band is assigned around unity conversion ratio.

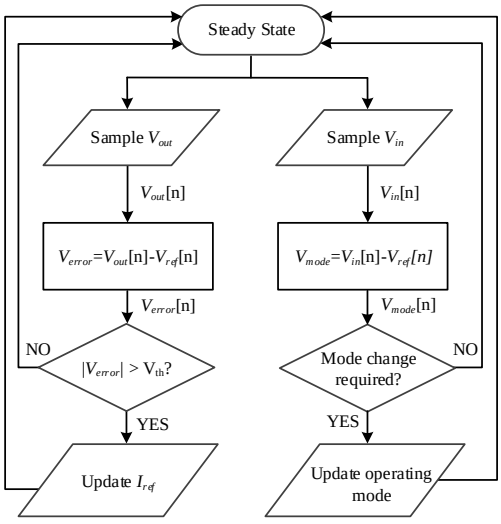


Fig. 2.2 Flowchart of the controller's operation in steady-state.

Efficient way that exploits the flexibility of this converter is to operate in the dedicated converter topology that is suitable for the conversion ratio based on the status of the input and output voltages. In this way, rather than operating in buck-boost mode for the entire range, a buck setup is preferred for step-down conversion, whereas step-up conversion is to be performed with a boost arrangement. It has been established in [53]-[54] that this approach improves the power conversion efficiency and reduces the components ripple. Still remaining however, is the region around unity conversion ratio where buck-boost operation prevails since neither buck nor boost converters can achieve pure unity conversion while

regulating the output voltage. To this end, several approaches to lower the ripple efforts have been pursued in recent years [45],[53]. This study too adopts the approach of operating in an enhanced mode around unity conversion ratio, with some unique adjustments of the enhanced modes selection and realization. To cover all conversion modes and move between them seamlessly, the operation of the steady-state controller has been segmented into four. There are two conventional cases of buck and boost, and two new modes of enhanced-buck and enhanced-boost, which are distinguished by the voltage status around the unity conversion ratio. The topology subcircuits for all operating modes are shown in Fig. 2.3 with typical current waveforms in Fig. 2.4.

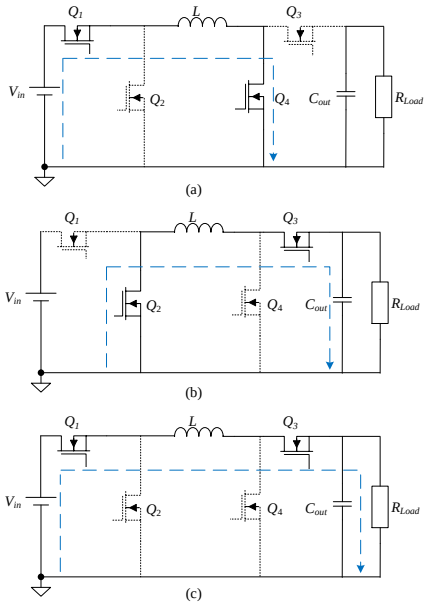


Fig. 2.3 Equivalent circuit of the non-onverting buck-boost converter in various stages of operation.

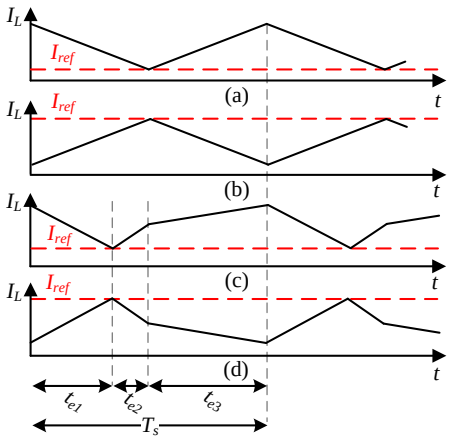


Fig. 2.4 Inductor current waveforms in various modes (a) conventional-buck. (b) conventional-boost. (c) enhanced-buck. (d) enhanced-boost.

For the case that $V_{in}>V_{out}$, the controller operates in a conventional buck mode. Here, Q_3 is kept on, Q_4 is off and the pair Q_1 and Q_2 toggles complementary. Voltage regulation is facilitated through valley current control, which determines the duty ratio of the toggling

transistor pair. Equivalent subcircuits for this operation mode are shown in Fig. 2.3b-c with inductor current shown in Fig. 2.4a.

For the case that $V_{in}<V_{out}$, the controller operates in a conventional boost mode. The passive pair here is Q_1-Q_2 while Q_3-Q_4 switching complementary (Fig. 2.3a-b). To utilize the same control hardware without modification, peak current control now determines the duty ratio for output voltage regulation (see Fig. 2.4b).

The enhanced-buck mode is engaged where the input voltage is slightly higher than the output voltage. In this case, the conventional valley current control, employed for the pure buck mode, is modified to a three-phase sequence for a switching period, resulting in inductor current waveform as shown in Fig. 2.4c. In the first interval t_{e1}, Q_2 and Q_3 are on (subcircuit Fig. 2.3b) and the inductor current ramps down with a slope of $(-V_{out})/L$ to the valley value assigned by the current reference. The second interval t_{e2} is a short boosting phase (subcircuit Fig. 2.3a) where the inductor current ramps up with a slope of V_{in}/L. The duration of the second time interval, t_{e2}, is chosen according the minimum conduction time of the power stage transistors and drivers, $t_{min,}$ so that the following holds: $t_{e2}>t_{min}$. In the third interval t_{e3} (subcircuit Fig. 2.3c) the inductor current continues to ramp up, but with a moderate slope of $(V_{in}-V_{out})/L$, until the end of the cycle. The boosting phase timing can be realized by either assignment of a fixed duty ratio d_{boost} as employed in [45]-[46], or as carried out in this study by changing the reference value to the comparator. Using the latter, cycle-by-cycle protection merit is maintained continuously along the entire range of conversion ratios.

Enhanced-boost mode is used for the case that the input voltage is slightly lower than the output voltage. In a similar way as the previous mode, a three-phase sequence is utilized, now with the difference that peak current value is initially obtained. A typical inductor current waveform for this case is depicted in Fig. 2.4d. Here, in the first interval t_{e1}, the current ramps up with a slope of V_{in}/L (subcircuit Fig. 2.3a). Then, in t_{e2}, the inductor discharges onto the load with a slope of $(-V_{out})/L$. Finally, in t_{e3}, the inductor current ramps down in buck-mode with a moderate slope of V_{out}/L. To facilitate the second phase, here too there are two options; One with a fixed duty ratio [45]-[46] , now d_{buck}. The second alternative, which has been carried out in this study, is by the current comparator.

From the above description, it implies that a single-comparator current-mode architecture is sufficient to all four modes, covering the full range of conversion ratios with enhanced conversion efficiency and lower ripple effort around unity ratio. These are achieved while retaining cycle-by-cycle current protection and simplifying the voltage-loop compensator by

reducing the system order, because of the tight current-programmed control [55]-[56]. A simple slope compensation configuration is also employed which supports all operating modes [57].

2.2.2. Impact of the Operation Mode on the Inductor's Current rms Value

Conduction losses are a primary contributor to the efficiency of buck-boost converters, in particular around unity conversion ratio. Since this study presents a modified operating sequence, it is essential to explore the effect of the new current waveform on the rms value. The analysis in this subsection is carried out in the context of the presented control method, i.e. it is generalized for wider range of conversion ratio, considering the operating mode per the status of input and output voltages.

The inductor's current in enhanced-boost and enhanced-buck modes can be divided into three sections, as can be seen in Fig. 2.5a and Fig. 2.5b. The rms value of the inductor current can be derived using the sum of the squares as follows [7]:

$$I_{Lrms} = \sqrt{I_{Lrms(1)}{}^2 + I_{Lrms(2)}{}^2 + I_{Lrms(3)}{}^2}\,, \tag{2.2}$$

where $I_{Lrms(1)}$, $I_{Lrms(2)}$, $I_{Lrms(3)}$ are the rms values of the three parts of the inductor current waveform.

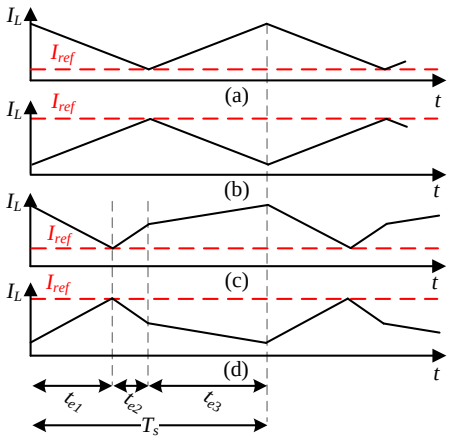


Fig. 2.5 Current waveforms around unity conversion ratio. (a) enhanced-boost mode. (b) enhanced-buck mode.

The rms value of the inductor's current when operating in conventional buck, conventional boost and conventional buck-boost modes can be expressed as [46]:

$$I_{Lrms\_buck} = \sqrt{I_{out}{}^2 + (\frac{\Delta I_L}{2\sqrt{3}})^2}\,. \tag{2.3}$$

$$I_{Lrms\_boost} = \sqrt{\left(\frac{I_{out}}{1-\frac{V_{out}-V_{in}}{V_{out}}}\right)^2 + \left(\frac{\Delta I_L}{2\sqrt{3}}\right)^2}\ . \tag{2.4}$$

$$I_{Lrms\_buck-boost} = \sqrt{\left(\frac{V_{out}+V_{in}}{V_{in}} I_{out}\right)^2 + \frac{1}{12}\left(\frac{V_{out}V_{in}T_s}{(V_{out}+V_{in})L}\right)^2}\ . \tag{2.5}$$

To facilitate comparison benchmark, the inductor's current rms value has been normalized with respect to the highest rms value of a conventional buck-boost mode, as can be seen in Fig. 2.6. Also added are independent simulation results, that validate the correctness of the expression in (2.2), as shown in Fig. 2.6. The result implies that when feasible, operation in either pure buck or boost is preferred. However, around unity conversion, the new shape for the current as obtained by the enhanced modes, results in lower conduction losses in steady-state compared to conventional approaches.

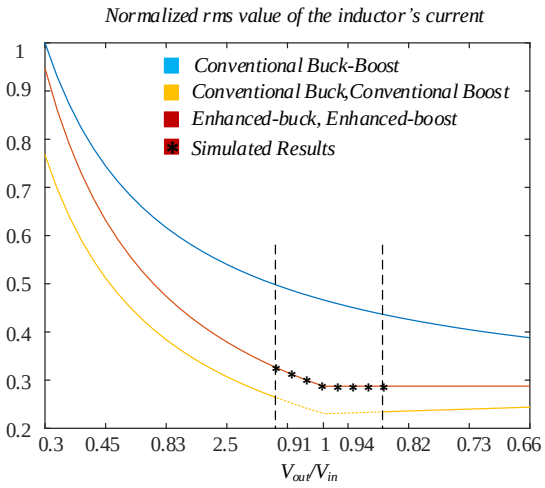


Fig. 2.6 Normalized rms values of the inductor current under various operating modes.

2.2.1. Variable Frequency Operation

To further improve the conversion efficiency, frequency scaling is employed. Operation at high conversion ratio calls for higher frequency operation to lower the ripple efforts and by doing so, reduce the size of the passive components. When operating around unity conversion ratio however, it is possible to lower the operating frequency and by that reduce the switching losses, and more importantly, drive losses. In the enhanced modes, the second time-interval (t_{e2}) with respect to the cycle duration, determines the average value of the inductor current, which is expressed as:

$$I_{L(\text{avg})\_\text{enhanced}-buck} = I_{out}\frac{1}{1-\frac{t_{e2}}{T_s}}\ . \tag{2.6}$$

$$I_{L(\text{avg})\_\text{enhanced}-boost} = I_{out} \frac{1}{1 - \frac{t_{e2} + \frac{V_{out} - V_{in}}{V_{out}}(T_s - t_{e2})}{T_s}} . \quad (2.7)$$

As can be seen from these expressions, keeping the correct ratio between the second interval to the switching period assures that the average current, and hence the load current, are satisfied. This implies that lowering the switching frequency is allowed without jeopardizing the performance, and even improving it. It should be noted however, that a secondary constraint of the maximum allowed ripple sets a lower limit on the frequency. The controller in this study has been designed so that the constraints are met while the switching frequency is adjusted according to the difference (or ratio) between V_{out} and V_{in}.

2.3. Transient Control

In this section, two recovery patterns are presented within the context of indirect energy transfer conversion (as NIBB) that, compared to the time-optimal solutions, constrain the output voltage deviation or peak inductor current (or both) while maintaining fast convergence in response to load transients. A primary objective in the controller design is to maintain the same hardware for all cases in the steady-state as well as for transients. Therefore, the hybrid controller incorporates the steady-state peak current programmed mode (CPM) arrangement and adds a transient-mode controller. For the transient-mode, two additional logic blocks have been developed, namely the *transient suppression block* and *Slope Calculation* (see Fig. 2.1). Upon a load transient detection, these blocks take over the task of estimating the load current and creating the gating signals to the power switches.

2.3.1. Programmable-deviation controller

The first recovery profile that is described is current-constrained recovery as illustrated in Fig. 2.7. Upon detection of a loading transient, from I_{old} to I_{ref}, the controller recovers from the loading event in a two-step process. First, the CPM controller is bypassed and Q_1 and Q_4 are turned ON while Q_2 and Q_3 remain OFF, while the new load state is estimated. During this time and based on the new load estimation, the controller sets a threshold for the inductor current, $I_{th}=I_{ref}$. Once the inductor current reaches the assigned threshold, the controller moves along the boundary $I_L=I_{th}$ in a sliding mode operation, causing the output voltage to rise up without changing the inductor current. The definition of the controller and

its realization is quite simple and features simple current comparison with some hysteresis band. As a sliding controller, it can be defined as follows:

$$\begin{aligned} &\sigma_i(v_C, i_L) = i_L - I_{ref}, \text{ for } v_C < V_{ref} \\ &on: \ \sigma_i < 0 \quad off: \ \sigma i > 0 \end{aligned} . \tag{2.8}$$

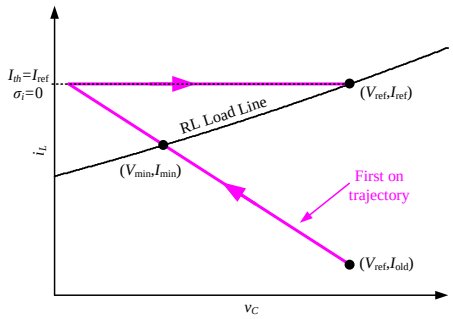


Fig. 2.7 Illustrative movement of the state plane for the current constrained mode handling a loading transient.

The second recovery profile applies constrains on both the output voltage to a desired level and on the inductor current, here the new steady-state value has been assigned. The recovery is described through a three-step process and is illustrated in Fig. 2.8. First, in a similar way as in the previous mode, the inductor current is ramped up, while the controller sets two thresholds: one for the output voltage and one for the inductor current based on the load estimation. In the second step, the controller is assisted by the voltage threshold to operate as a sliding-mode controller that is defined by:

$$\begin{aligned} &\sigma_v(v_C, i_L) = v_C - V_{th}, \text{ for } i_L < I_{th} \\ &on: \ \sigma_v > 0 \quad off: \ \sigma_v < 0 \end{aligned} . \tag{2.9}$$

During this step, the inductor current rises without changing the output voltage until it reaches the current threshold and the controller moves to the third step. During the third and final step, the controller moves along the boundary i_L=I_{th} in a sliding mode operation, this can expressed as:

$$\begin{aligned} &\sigma_i(v_C, i_L) = iL - I_{th}, \text{ for } v_C < V_{ref} \\ &on: \ \sigma_i < 0 \quad off: \ \sigma_i > 0 \end{aligned} . \tag{2.10}$$

Optimized boundary control scheme covering the entire range of conversion ratios has been designed based on the above-mentioned recovery profiles for loading events and conventional time-optimal solutions for unloading events. The design approach is aided by the analytical derivation of the converter's state trajectories and load-line combined with graphical illustrations of the state-plane for various voltage gains.

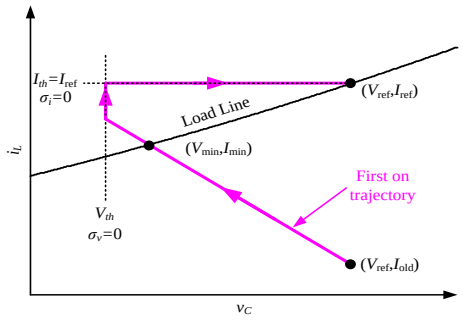


Fig. 2.8 Illustrative movement of the state plane for the voltage-deviation and current-constrained mode handling a loading transient.

In both recovery profiles, the switching frequency of the power devices during sliding-mode operation is determined by a hysteresis band around the reference value. It is set according to the maximum allowed ripple and takes into account the frequency limitations of the power-devices and drivers used in the design.

The selection of the specific recovery pattern relates to the sensitivity of the design to specific components. For example, should the inductor current in the design must not exceed a certain limit then the current-constrained controller is to be employed. This controller realization provides flexibility in the selection of the hardware by choosing the recovery pattern based on the available sensors per specific design.

The controller recovery pattern for loading events in enhanced-buck mode is an example of exploiting the topological flexibility of the NIBB converter to further improve the transient response while reducing output voltage deviation as well as lowering the peak inductor current that is required for recovering to the new steady-state. Illustrations of the state-plane as well as the specific recovery trajectories for loading transient, in enhanced-buck mode are depicted in Fig. 2.9. The two constrained recovery profiles (Fig. 2.9b-c) presented earlier in this section are compared with time-optimal pattern (Fig. 2.9a) as a benchmark case. It can be seen that while a conventional buck time-optimal recovery ramps the inductor current up by with a slope of $(v_{in}\text{-}v_{out})/L \approx 0$, here the addition of a boosting phase ramps up the inductor current with a slope of v_{in}/L. This improvement alone significantly enhances the recovery performance on both deviation and time properties since it increases the applied voltage on the inductor. In a similar manner, recovery of enhanced-boost mode for the NIBB converter is found to superior over the one of a conventional boost. This has been widely detailed in [51].

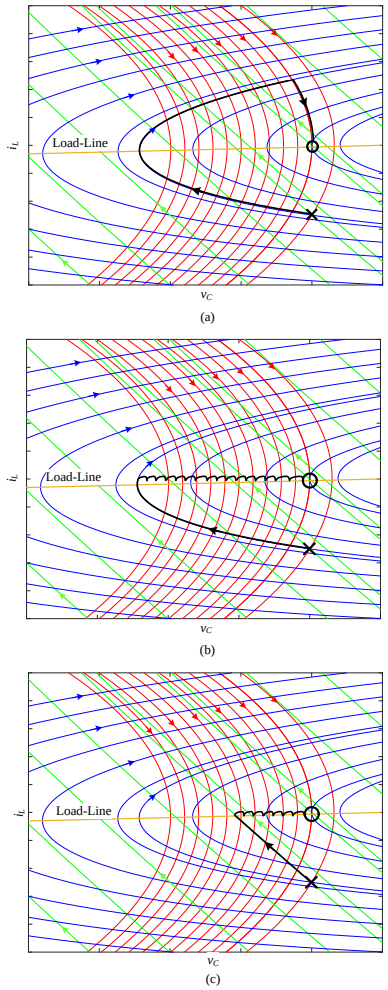


Fig. 2.9 State plane representation of NIBB operating in enhanced-buck mode for a loading transient. (a) Recovery pattern of conventional Time-Optimal Control (TOC). (b) Recovery pattern of current-constrained mode in conventional buck mode. (c) Recovery pattern of current-constrained mode in enhanced-buck mode with a boost-phase.

To demonstrate the operation of the transient recovery pattern, simulation testbench (in PSIM) has been constructed. Fig. 2.10 shows the resultant recovery pattern for 0.8A to 3.5A loading transient, while the converter operated in enhanced-buck mode (3.8V to 3.3V). Fig. 2.10 depicts the time waveforms for the output voltage and inductor's current as well as the state-plane for better visualization of the trajectories along the recovery phase. It can be seen that the current is well confined within the hysteresis margins during the convergence. It can also be seen that resumption to steady-state is obtained smoothly without additional oscillations due to the correct estimation of the load status (location marked on the timing diagram).

Fig. 2.11 shows the resultant recovery pattern for a 3.5A to 0.8A unloading transient, while the converter operates in enhanced-buck mode (3.8V to 3.3V). Here, fast convergence is assured by employing conventional time-optimal recovery pattern. Fig. 2.11 depicts the

time waveforms for the output voltage and inductor's current as well as the state-plane representation.

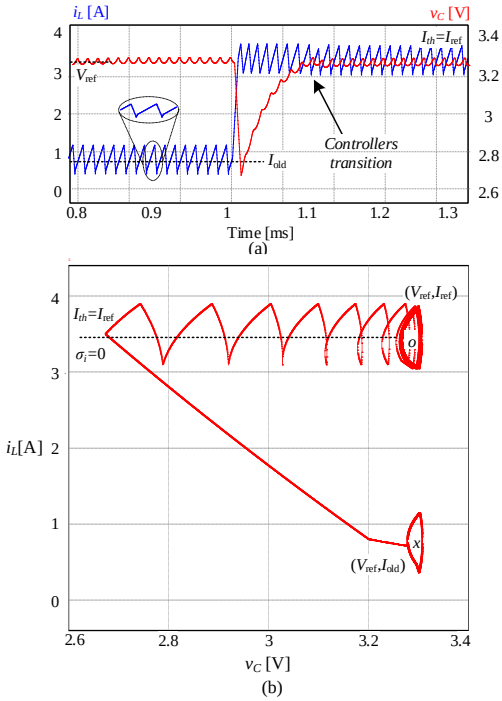


Fig. 2.10 Simulated response of the current-constrained controller to a 0.8-3.5 A loading transient ot a NIBB converter in enhanced-buck mode. (a) Inductor current (blue) and output voltage (red) (b). State-plane representation of the output voltage and inductor current.

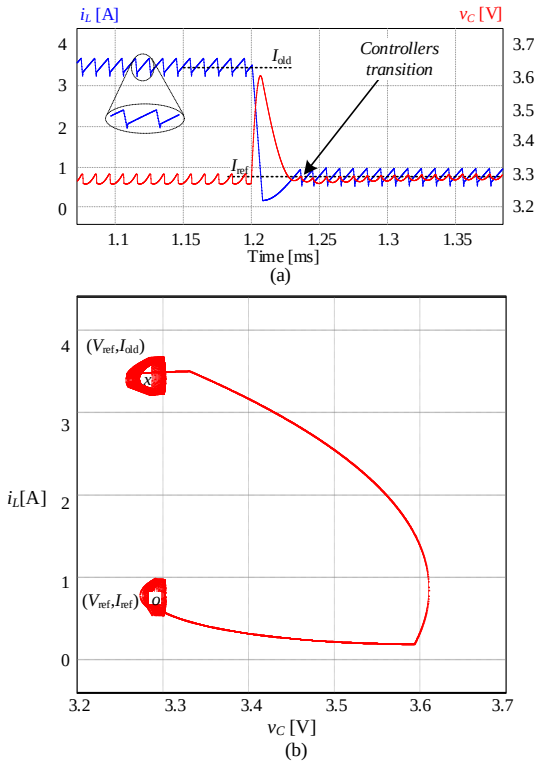


Fig. 2.11 Simulated result of time-optimal controller to a 3.5A to 0.8A unloading event of a NIBB converter operating in enhanced-buck mode. (a) Inductor current (blue) and output voltage (red). (b) State-plane representation of the output voltage and inductor current.

2.3.2. Stability analysis

The hybrid controller in this work combines large-signal and small-signal controllers. The condition for stability in such a hybrid controller is that the large-signal controller will move the converter's state to the desired steady-state operating point, regardless of its initial conditions. Derivation of the large-signal region of convergence (ROC) is carried out in this section for the sliding-mode controller used in case of a loading event in step-down mode.

The template of the sliding-mode controller is chosen according to the converter's load-line. The load line of a NIBB converter operating in step-down configuration loaded by a resistive load (RL) can be expressed as:

$$LL_{\mathrm{RL}}(\mathrm{v_C},\mathrm{i_L}) = \left\{ v_L, i_L : i_L = \frac{v_C}{R} \right\}. \tag{2.11}$$

The load-line is linear and thus a linear switching surface, σ_{RL}, is selected:

$$\sigma_{RL} = i_L - I_{ref} - \lambda_{RL}(\mathrm{v_C} - \mathrm{V_{ref}}). \tag{2.12}$$

The converter's average model can be expressed as:

$$\begin{cases} \dfrac{dv_C}{dt} = \dfrac{1}{RC} v_C + \dfrac{1}{C} i_L \\ \dfrac{di_L}{dt} = \dfrac{1}{L} V_{in} u - \dfrac{1}{L} v_C \end{cases}, \tag{2.13}$$

where *u* is the control input. To examine whether the trajectories along the switching surface lead to a unique steady-state operating point, current and voltage errors, $\tilde{i}_L$ and $\tilde{v}_C$, are defined as follows:

$$\begin{cases} \tilde{v}_C = v_C - V\mathrm{ref} \\ \tilde{i}_L = i_L - I\mathrm{ref} \end{cases}. \tag{2.14}$$

Substituting (2.13) into (2.14) yields:

$$\tilde{i}_L + I_{\mathrm{ref}} = C \frac{d(\mathrm{v_C} + \mathrm{V_{ref}})}{dt} + \frac{1}{R}(\mathrm{v_C} + \mathrm{V_{ref}}). \tag{2.15}$$

The expression in (2.15) can be separated into two parts which represent the dc component and the time-dependent component:

$$\begin{cases} i_{DC} = \dfrac{V\text{ref}}{R} \\ i_{AC} = \tilde{i}_L = C\dfrac{d(\tilde{v}_C + \mathrm{V}_{\text{ref}})}{dt} + \dfrac{1}{R}\tilde{v}_C \end{cases}. \tag{2.16}$$

If $i_{AC} \underset{t\to\infty}{\to} 0$ along the switching surface, the system is asymptotically stable and converges to the dc steady-state point. By substituting (2.14) and (2.16) into the switching surface, the following differential equation is obtained:

$$C\frac{d\tilde{v}_C}{dt} + \frac{1}{R}\tilde{v}_C - \lambda_{RL} v_C = 0. \tag{2.17}$$

Using (2.17), the stability condition of the switching surface can be obtained as:

$$\lambda_{RL} < \frac{1}{R} = \lambda_{RL,\max}. \tag{2.18}$$

Choosing λ_{RL} that satisfies (2.18) results in assured convergence of the state variables to (V_{ref},I_{ref}). In addition, the ROC is bounded by the load-line to guarantee that the switching surface does not pass in a rejective region [58]. The ROC can be depicted on the state-plane as shown in Fig. 2.12, bounded by the load-line and the curve $\sigma_{RL,\max}$. The switching surfaces where chosen to comply with the above constraints and thus large-signal stability is assured.

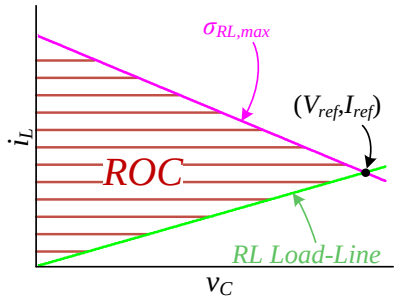


Fig. 2.12 Illustrative ROC for NIBB in step-down configuration loaded by a resistive load.

Analysis for voltage step-up configurations has been studied in detail in previous studies [58]. Here, to assure convergence of the state variables λ_{RL} should be chosen to satisfy the following:

$$\lambda_{RL} < \frac{1}{RV_{in}} = \lambda_{RL,\max}. \tag{2.19}$$

2.4. Load Estimation Procedure

The enabler of accurate reading of the load status is the capability to control the converter's output current, and by doing so, reducing the order of complexity to extract the charge balance at the output capacitor. Assuming that the output current is regulated during transient, then the output voltage is a direct, and single, indicator to whether the load current is supplied by the converter. Toggling between subcircuits of Fig. 2.3a and Fig. 2.3c, under CPM operation, the average inductor current can be regulated to any value, regardless of the voltage conversion ratio.

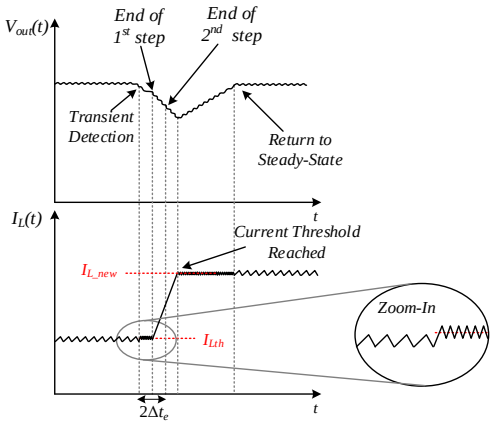


Fig. 2.13 Illustrative load estimation process for a loading transient when operating in current-constrained mode.

2.4.1. Principle of operation

Upon detection of a loading transient, the controller estimates the new load current in a two-step process, each with a time duration equals to Δt_e. First, the output voltage is sampled at the beginning of the load estimation process and its value, $V_{out}^{(1)}[n]$, is stored in a dedicated n-bit register. For that pre-defined time interval, Δt_e, the converter operates in the configuration shown in Fig. 2.14a, referred to as "*step 1 operation*". During this step, the load is fed by the the output capacitor, C_{out}, and the constant output current of the converter, I_1. During this step, to assure tight current regulation that outputs I_1, the controller operates as a sliding mode controller defined by the following set of equations:

$$\begin{aligned} &\sigma_i(v_C, i_L) = i_L - i_{Lth} \\ &on: \ \sigma_i < 0 \\ &off: \ \sigma_i > 0 \end{aligned} \quad , \tag{2.20}$$

where i_L is the inductor current and i_{Lth} is assigned so that constant current of I_1 is outputted as shown in the time diagram of Fig. 2.13. At the end of first step, the output voltage is sensed again to produce a digital representation of the output voltage value $V_{out}^{(2)}[n]$.

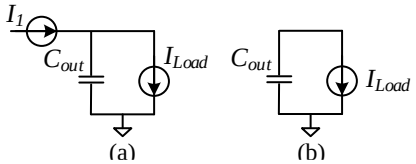


Fig. 2.14 Equivalent circuits of the converter. (a) step 1 operation. (b) step 2 operation.

The output voltage deviation, $\Delta V_{out}^{(1)}[n]$, is obtained by the following:

$$\Delta Vout^{(1)}[n] = Vout^{(1)}[n] - Vout^{(2)}[n], \tag{2.21}$$

which is the discrete-time equivalent of the output voltage deviation, and can be expressed as:

$$\Delta Vout^{(1)} = \frac{ILoad^{new} - I1}{Cout}\Delta te, \tag{2.22}$$

During the second step, Q_1 and Q_4 are kept on and the pair Q_2-Q_3 remains off, as shown in Fig. 2a. The load is fed solely by the output capacitor, C_{out} (Fig. 2.14b). At the end of the second step, the output voltage is sampled once again and the output voltage deviation can be expressed as:

$$\Delta Vout^{(2)}[n] = Vout^{(2)}[n] - Vout^{(3)}[n]. \tag{2.23}$$

Similarly, this correlates to the output voltage deviation during the second step, expressed by:

$$\Delta Vout^{(2)} = \frac{ILoad^{new}}{Cout}\Delta te. \tag{2.24}$$

The new load current can be extracted from (2.22) and (2.24) without prior knowledge of the output capacitor value, C_{out}, or the duration of each step, Δt_e. This can be obtained by simple arithmetic operations in continuous-time or discrete-time expressions, as follows:

$$ILoad^{new} = \frac{\Delta Vout^{(1)}}{\Delta Vout^{(2)} - \Delta Vout^{(1)}} I1. \tag{2.25}$$

$$ILoad^{new}[n] = \frac{\Delta Vout^{(1)}[n]}{\Delta Vout^{(2)}[n] - \Delta Vout^{(1)}[n]} I1[n]. \tag{2.26}$$

2.4.2. Relationship between I_{LOAD_new} and i_{L_new}

The post-transient inductor current reference assigned by the DAC is a function of the load estimation result and the operating mode of the NIBB, i.e. step-up or step-down. In direct energy transfer configuration, the average output current is equal to the average inductor current. Therefore, the new steady-state average current can be expressed as follows:

$$i_{L\_new} = i_{Load\_new}. \tag{2.27}$$

However, for indirect energy transfer the average inductor current is higher than the load current by factor of the duty ratio. For example, in a boost configuration, the new inductor current setting will be:

$$i_{L\_new} = i_{Load\_new}\frac{1}{1-D_{boost}}, D_{boost} = \frac{V_{out}-V_{in}}{V_{out}}. \tag{2.28}$$

Following the same load estimation procedure as prescribed above, it can support both step-up and step-down configurations with a minor modification of the final inductor current reference assignment.

2.4.3. Estimation of the effective output capacitance value

The performance of the steady-state controller might deviate from its optimal compensation goals due to variations of the passive components, in particular the output capacitance may significantly vary under different bias voltages, which further intensifies as the voltages are higher. There are several cases that the steady-state controller, and the compensator design can benefit from accurate knowledge of the effective output capacitance value. This can assist in improving the performance of the compensation by covering stability for wider operation range as well as to minimize the steady-state error. Utilizing the load estimation process described earlier, the output capacitance value can be extracted as follows:

$$C_{out} = \frac{I_{Load\_new}}{\Delta Vout^{(2)}}\Delta t_e. \tag{2.29}$$

The information obtained can also be used to enhance the overall performance of the current estimation process by reducing calculation efforts. Based on the extracted output capacitor value, the new load current can be estimated through a single step, reducing the total estimation period to Δt_e. Here, once a load transient is detected, the converter operates

in the configuration shown in Fig. 2.14b for a pre-defined time interval of Δt_e. Two samples of the output voltage are sufficient in this case to accurately estimate the new load. The load estimation can be expressed as:

$$I_{Load\_new} = C_{out} \frac{\Delta Vout}{\Delta te}. \tag{2.30}$$

2.5. *Experimental Verification*

In order to validate the operation of the unified current-programmed digital controller, a 2-15V to 3.3V non-inverting buck-boost prototype has been built and tested, using an 8.2μH inductor, 30μF output capacitance and operating frequency of 100-200 KHz. The experimental setup is shown in Fig. 2.15. The CPM controller dictates the resolution of the ADC and DAC which also satisfy the requirements of the non-linear controller. The resolution of the ADC is 32mv with maximum conversion rate of 20MHz. The resolution of the DAC is 2.5mV with maximum conversion rate of 20.4MHz. The converter is digitally controlled by a steady-state voltage-mode compensator and a transient-mode controller as shown in Fig. 2.1. The digital controller has been entirely realized on Altera Cyclone IV FPGA, and the total number of logic elements used is 980 for the entire controller.

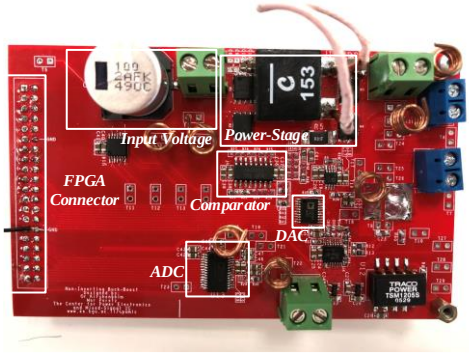


Fig. 2.15 Experimental prototype of the NIBB converter.

Steady-state operation has been verified through multiple experiments under various input voltages, as shown in Fig. 2.16-Fig. 2.18. Fig. 2.16a and Fig. 2.16b show the inductor's current in enhanced-boost mode for V_{in}=2.8V and V_{in}=3.2V, respectively. Regulated output voltage is achieved for a wide range of input voltages while significantly reducing average inductor current and rms values. Fig. 2.17a and Fig. 2.17b depict the operation in enhanced-buck mode for V_{in}=3.8V and V_{in}=3.4V, respectively. Fig. 2.18 shows a transition mode between conventional boost to enhanced-boost. It can be seen that seamless transition between the two operating modes is achieved as in all other mode transition cases. A

zoomed-in view of the inductor current and output voltage is shown in Fig. 2.18b demonstrating frequency scaling operation.

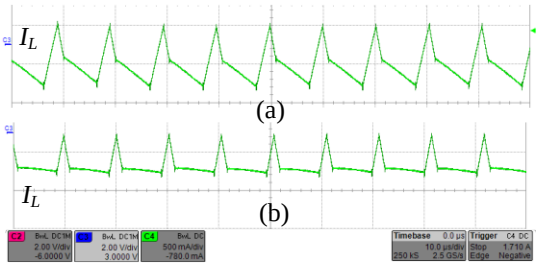


Fig. 2.16 Enhanced-boost mode, V_{out}=3.3V (a) V_{in}=2.8V (b) V_{in}=3.2V.

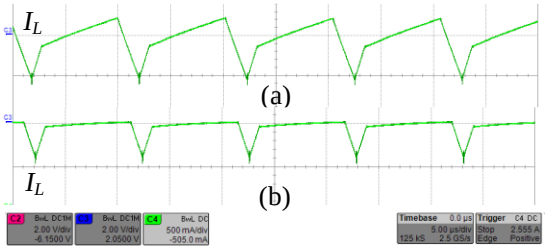


Fig. 2.17 Enhanced-buck mode, V_{out}=3.3V (a) V_{in}=3.8V (b) V_{in}=3.4V.

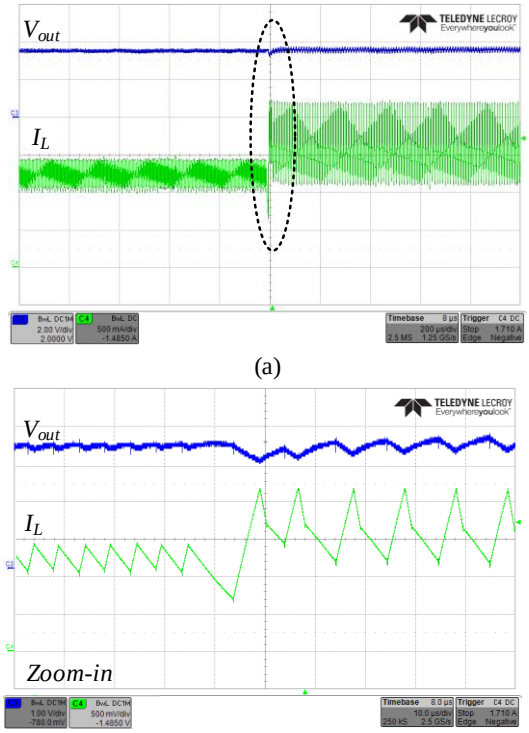


Fig. 2.18 Transition event from conventional boost to enhanced-boost operating mode, V_{in}=3V, V_{out}=3.3V. (a) Transition event. Output voltage (top-blue) 2V/div, inductor current (bottom-green) 500mA/div, time scale 200μs/div. (b) Zoom-in on the transition, Output voltage (top-blue) 1V/div, inductor current (bottom-green) 500mA/div, time scale 10μs/div .

The transient controller performance for loading transient of 0.8-3.5A is depicted in Fig. 2.19-Fig. 2.20. Fig. 2.19 shows the loading transient recovery of the current-constrained

controller while in enhanced-buck mode. I_{th} is chosen to be equal to the new steady-state peak inductor current which results in an output voltage deviation of 1V and total transient time of 60μs with no current overshoot. Fig. 2.20 shows loading transient recovery of the voltage-deviation-and-current-constrained controller while operating in pure-boost mode. The resultant recovery parameters are output voltage deviation of 1V, no current overshoot, recovery time to steady-state is 50μs.

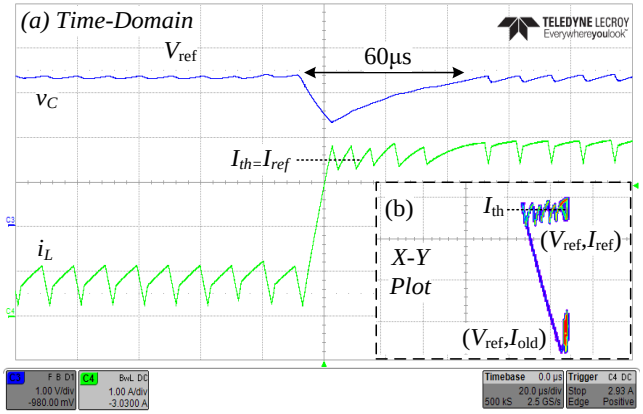


Fig. 2.19 NIBB converter's response and state-plane representation to a 0.8-3.5 A loading transient using the current-constrained controller. (a) Output voltage (top-blue) 1V/div, inductor current (bottom-green) 1A/div, time scale 20μs/div. (b) State-plane representation of inductor current (vertical axis – 1 A/div) and output voltage (horizontal axis - 1 V/div).

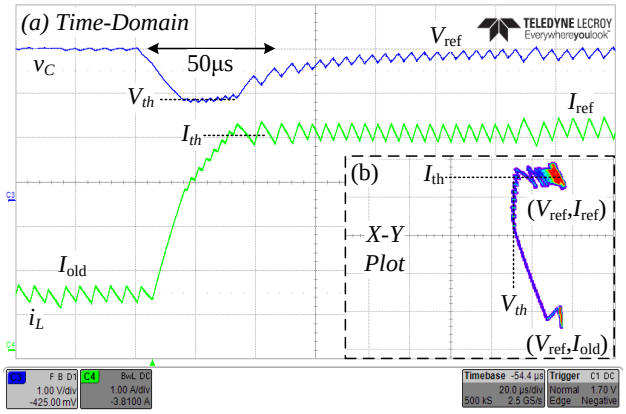


Fig. 2.20 NIBB converter's response and state plane representation to a 0.8-3.5 A loading transient using the voltage-deviation and current-constrained controller. (a) Output voltage (top-blue) 1V/div, inductor current (bottom-green) 1A/div, time scale 20μs/div. (b) State-plane representation of the inductor current (vertical axis – 1A/div) and output voltage (horizontal axis – 1A/div).

Fig. 2.21 shows the loading transient recovery of the current-constrained controller for a 0.8-2.9A loading transient while operating in step-up configuration with a zoom-in on the controlled inductor current during the first step of the load estimation procedure. The inductor current reference was chosen according to (2.28), which results in output voltage deviation of 1V and total transient time of 80μs with no current overshoot.

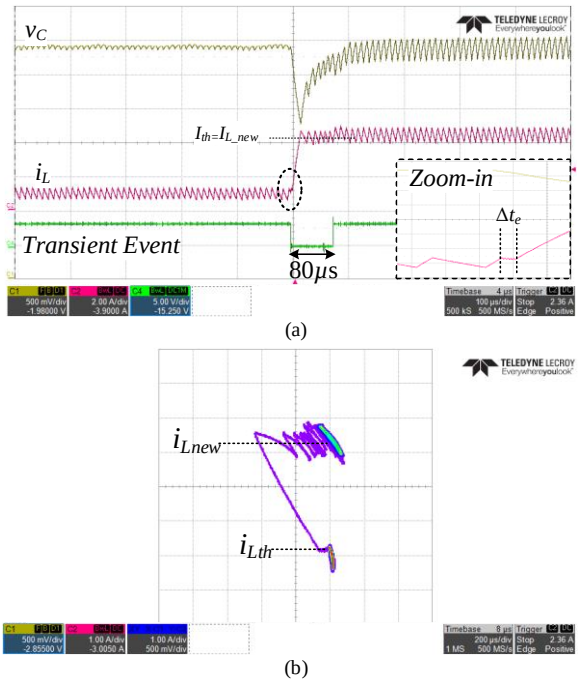


Fig. 2.21 NIBB converter's response and state-plane representation to a 0.8-2.9A loading event using current constrained controller and load estimation procedure in step-up configuration. (a) Output voltage (top-yellow) 500mv/div, inductor current (middle - red) 2A/div, transient event (bottom – green), time scale 100us/div. (b) State-plane representation of inductor current and output voltage.

2.6. Conclusion

A unified current programmed digital controller for NIBB converter have been presented in this study. The controller incorporates a steady-state CPM controller for steady-state operation and a nonlinear transient-mode controller for load transients. Detailed analysis of the enhanced-modes has been carried out, followed by steady-state control scheme design to allow seamless transition between modes and improved ripple characteristics. Load transients are supported by the same hardware of the CPM controller, with programmable constraints of the output voltage deviation and inductor current. An optimized boundary control scheme for efficient load transient convergence has been perused with assured large-signal stability.

Experimental results of a 2-15V to 3.3V NIBB converter prototype are provided. For steady-state operation around unity conversation, well regulated output voltage is achieved with significantly reduced average inductor current and rms values. The controller exploits the versatile structure of the NIBB to maintain short transient time without the penalty of increased current or voltage overshoots.

3. Enhanced Performance Fully-Synthesizable ΣΔ ADC for Efficient Digital Voltage-Mode Control

This chapter introduces a new approach for sigma-delta based analog to digital converter (SDADC) with enhanced performance suitable for digital voltage regulation. The new ADC increases the number of digital representations of the sampled signal per conversion cycle, for the same oversampling clock frequency. An all-digital fully synthesizable realization of the new architecture sets it as an attractive candidate for many digital application platforms ranging from housekeeping and monitoring and even as the main ADC for the compensation loop. An experimental closed-loop operation on a voltage-mode buck converter with the digital controller implemented on FPGA, demonstrates superior operation over a conventional SD operation. The SDADC has also been implemented as an IC by an automated synthesis process and place-and-route tools in 0.18μm 5V CMOS process.

3.1. Overview

Sigma-Delta modulators and converters are major enablers of the digital technology ramp up dating back to the late 1980s. The appearance of low-cost and reliable means to translate continuous-time signals onto the sample-data domain revolutionized the field of low and medium frequency range signal processing and in particular the audio world [59]-[62]. Nowadays, the availability of simple and efficient interface from the analog world to the digital hardware is still extremely important in all fields of electronics. In particular for power management, where fast performance with reasonable cost is critical, analog implementation of the controller core is still predominant [63],[64]. In the last decade or so there has been a significant progress in digital power management thanks to the development of dedicated hardware that is tailored to its unique needs [65]-[69]. With the integration of digital technology, the power management system transforms as well. Now comprises design flexibility, scalability, and upgrade options; communication and power quality logging; plug-and-play operation; and of course, improved performance.

Since a typical digital compensation loop must have at least comparable dynamics to its analog precursor, high-performance peripherals are essential, i.e., the digital PWM (DPWM) and ADC [65],[66], [69]. Conversion of 10bit word within 100ns is a common requirement to accommodate switching frequencies in the range of 300kHz (where the control bandwidth is approximately $1/6f_s$). As a consequence, high-performance ADCs such as pipeline or successive approximation are employed [70],[71]. Since Sigma-Delta analog to digital

converters (SDADC) are operated through oversampling concept and require very high speed clock, in the order of 100s MHz to generate comparable conversion rate, they are typically avoided for compensation purposes and mostly used for slower tasks such as housekeeping and user interfaces. On the other hand, the very simple hardware of a SDADC is an attractive feature, which should be further pursued.

A typical voltage-mode (VM) compensation loop for switch-mode power supply (SMPS), as illustrated for a buck converter in Fig. 3.1, operates on the basis of one sample per cycle to regulate the average value of the output voltage and fully utilize the correction rate (switching frequency) of the loop. For a compensator based on conventional SDADC, this calls for oversampling clock of at least 2^n time the switching frequency (where n is the number of ADC bits) with a bit stream of similar size. However, since convergence of a linear control scheme takes several switching cycles, these strict requirements are eased in this study by trading some of the accuracy with faster reading. The data of the long string, for precision, is generated out of lower resolution, shorter strings. Information of the output voltage status continuously updates the loop, and since it is of shorter duration, the potential deviation in the output voltage is lower which agrees with the momentary lower resolution reading. In this way, with minor hardware additions, a SDADC can be considered as an attractive candidate for various tasks, and even for core control in digital voltage regulation.

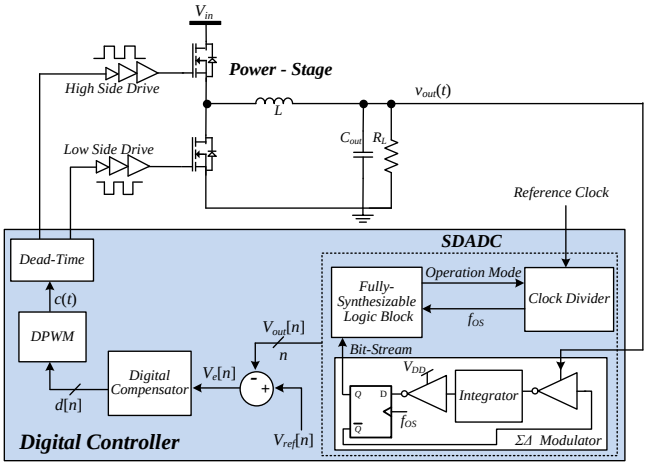


Fig. 3.1 Simplified schematic diagram of digital voltage-mode control loop for a buck converter utilizing the SDADC.

3.2. Enhanced performance SDADC principle of operation

The principle of operation of the modified SDADC is described in comparison to a conventional SDADC and with the aid of Fig. 3.2 and Fig. 3.3, which show a conceptual block diagram of the modified conversion scheme and high-level operation flowchart,

respectively. It is assumed here that a first-order SD modulator is used to generate a bit stream with average value that is proportional to the sampled signal $v_{out(t)}$. To produce an *n*-bit digital value representation of the sampled signal, the amount of 'ones' of the bit-stream is stored in a main *n*-bit counter (see Fig. 3.2). The counter acts as a sinc Low-Pass Filter (LPF), and resets at pre-determined intervals to perform decimation [59]-[61].

The sampled output voltage $v_{out}(t)$ is translated to a digital representation $v_{out}[n]$. In the SDADC of this study, the sampled signal is updated several times, with coarser resolution, during a full conversion cycle. These mid-cycle time updates are generated by a state machine combined with a digital logic block, and pre-defined according to the overall number of bits of the counter. An *n*-bit register holds the most recent digital value of the sampled signal, and is updated throughout the conversion cycle in both mid-cycle and full-cycle update points. Thus, a coarse result of the sampled signal is generated, which is refined through the conversion cycle, and after 2^n over sampling clock cycles (f_{OS}) a full resolution digital representation of $v_{out}[n]$ is obtained.

Typically SDADCs are designed to sample signals that do not vary between two reset operations of the counter [59], [61],[72]. The concept employed in this study is designed to accurately track the sampled signal variations between two or more reset events of the counter, exploiting the SDADC advantages without the penalty of slower dynamics, power consumption, or increased design efforts [59]-[62], [72]-[75]. This enables to update the result more than a single time per conversion cycle and fast digitizing of the sampled signal with high accuracy. Effectively, wider dynamic range is achieved even for fast variations without sacrificing precision.

For the modulator operation (detailed in Section IV), given 2^n clocks cycles since the latest reset operation the value of the reconstructed continuous-time equivalent for the digitization process, $V_{out}^{*}(t)$, is found with respect to the main counter's value, and can be expressed as:

$$v_{out}^{*}(t) = V_{ref}\frac{2^n}{CNTR_n}, \tag{3.1}$$

where V_{ref} is the reference value for the modulation process, and CTR_n is the counter's value for a given number of bits. For intermediate updates during the conversion cycle (referred throughout the text as *mid-cycle updates*), the effective number of bits is smaller than *n* and the reconstructed value is scaled and normalized according to the bits difference as follows:

$$\frac{2^n}{CNTR_{mid}} = \frac{2^m}{CNTR_n} \quad \Rightarrow \; CNTR_{mid} = \frac{2^n}{2^m} CNTR_n \quad , \tag{3.2}$$

where *m* is the number of bits during mid-cycle update command and CTR_{mid} is the digital representation of the sampled signal at mid-cycle update points.

One of the drawbacks of typical SDADCs is power consumption due to relatively high operating frequencies to assure Nyquist sampling criterion [59], [61], [72]. Employing the modified operation concept, power saving option is enabled. This is achieved by setting the SDADC into two operation modes: (a) transient detection, (b) steady-state. For transient event or any other sudden potential variation of the sampled signal, the system operates at high clock. The latter combined with mid-cycle updates, results in fast responses of both the SDADC and the overall control loop. However, if the system is in steady-state mode, i.e. a system governor detects minor deviations of the conversion output along a predetermined number of cycles, the clock frequency can be lowered. This reduces the power consumption without sacrificing precision of the sampled signal. The selection procedure between the modes is illustrated in the flowchart of Fig. 3.3.

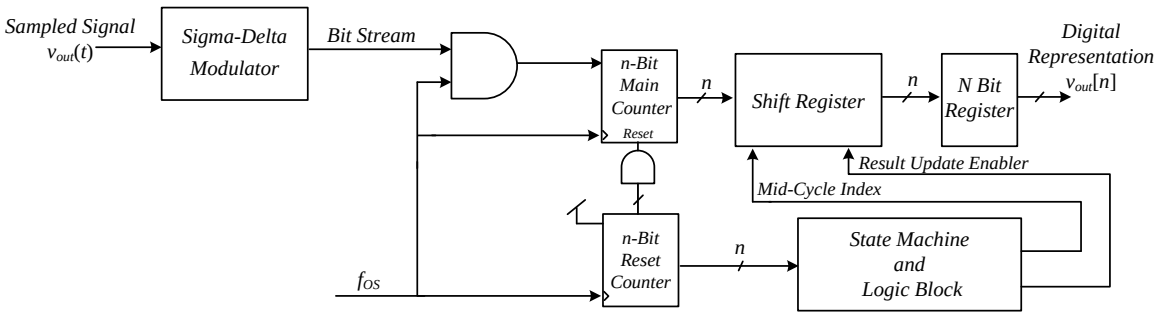


Fig. 3.2 Simplified block diagram of the new architecture for SDADC.

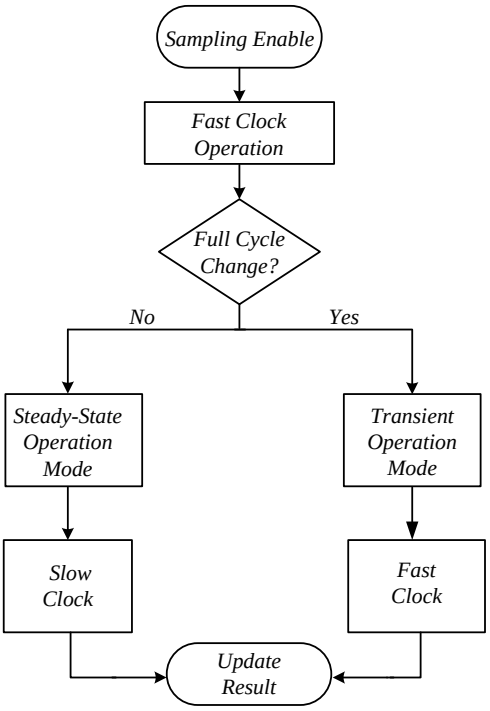


Fig. 3.3 High-level flowchart of the clock selection mode.

3.3. All digital voltage loop compensation

Digital VM compensation for SMPS is a simple and streamlined approach [69], [76], [77], to regulate the output voltage to a desired reference voltage over wide range of operating conditions. Since a single state variable (the output voltage) is controlled, it requires moderate hardware complexity. It should be noted however, that the dynamic performance of this control scheme may not suffice all applications and therefore an additional current loop is added which may be either analog [63], [78] or digital [65]-[68]. In the context of this study, which aims to introduce a new ADC architecture, a voltage feedback loop has been selected as a demonstrative tool for simplicity.

A conceptual block diagram of a typical single-loop VM control scheme is depicted in Fig. 3.4. As can be seen, the output voltage $v_{out}(t)$ (or a scaled version of it) is sensed and then sampled by the SDADC, to produce a digital representation of the output voltage value $v_{out}[n]$. Then allows, the sampled voltage is compared with a digital reference value, and results in an error signal $v_e[n]$. The error signal is passed through a digital compensator (either PI or PID), which then updates the DPWM unit to generate drive signals for the low and high side power switches of the converter. $K_{A/D}$ and K_{DPWM} are the gains of the SDADC and DPWM, respectively. The power stage that has been selected for evaluation is a buck

converter, with idealized control-to-output transfer function $G_{vd}(s)$ that can be expressed as [65], [78]:

$$G_{vd}(s) = \frac{V_{in}}{\frac{s^2}{{\omega_0}^2} + \frac{s}{\omega_0 Q} + 1} \; ; \; \omega_0 = \sqrt{\frac{1}{LC_{out}}}, \; Q = \sqrt{\frac{C_{out}}{L}} R_L \, . \tag{3.3}$$

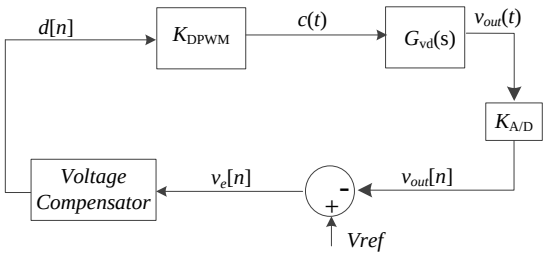


Fig. 3.4 Block diagram of the digital VM control system.

Fig. 3.5 shows a conceptual timing diagram for an output voltage variation for both a conventional SDADC and the enhanced performance SDADC developed in this study. Output voltage regulation is achieved by properly adjusting the duty-ratio command $d[n]$ as a function of the generated error signal $v_e[n]$. Fig. 5a shows that the conventional SDADC is being updated only at the end a of a full conversion cycle, resulting in relatively slow closed-loop response due to limited sampling and correction rate. For similar settings of the digital hardware (i.e., clock speed and calculation hardware), the new SDADC employs coarse corrections throughout the operation cycle at shorter intervals, which provides more information on the voltage, but with lower resolution than the end-of-cycle result. Consequently, the output voltage is corrected faster, and convergence to desired reference value V_{ref} is obtained. While information of coarser resolution apparently distorts the tracking capability of the loop, the information flows in a faster rate and as a result compensates for lower accuracy. It should be noted that, the ratio between the effective sampling rate and resolution is virtually identical for samples at mid-cycle as the one obtained at the end of the longer cycle. The faster and more accurate response of the new SDADC implies that higher effective bandwidth of the closed-loop system is achieved for the same hardware complexity and running frequency of the controller.

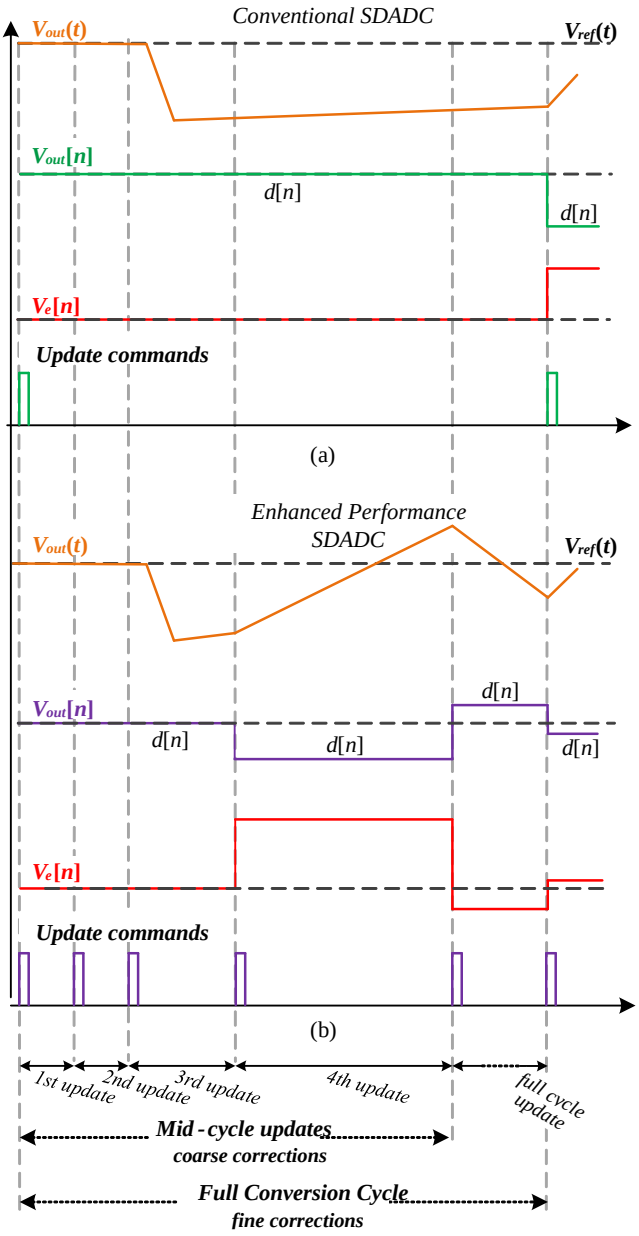


Fig. 3.5 Conceptual timing sequence of duty-ratio updates in response to voltage reference change: (a) Conventional SDADC, (b) Enhanced performance.

3.4. Practical implementation

Practical implementation and design considerations of the SDADC's main functional units are discussed in this section. Since this design is ultimately IC oriented, with automatic tools, emphasis is made to reduce the use of analog peripherals.

3.4.1. Modulator stage

Conventional SD modulators comprise difference amplifier followed by an integrator and comparator [60], [62], [72]. In this study, a digital-oriented approach is considered and is

shown in Fig. 3.6. An inverter is used as the modulator's front-end, with the sensed signal as the high logic level (supply) of the inverter. This can be implemented in variety of ways such as variable supply [79], [80], current-starved inverter [81], [82], or digital differentiator or comparator [77]. To reduce circuit complexity, the integrator is realized by a simple RC network (may be double RC for further size reduction) with a corner frequency of at least one order of magnitude lower than the clock frequency. The one-bit quantizer is also realized by another inverter, where the threshold value of the inverter is the comparison [77]. Finally, the quantized value is held for a clock cycle using a D flip-flop which also drives the first inverter data path. Utilizing this configuration of Fig. 3.6, a simple and efficient SD modulator with streamlined IC implementation is facilitated.

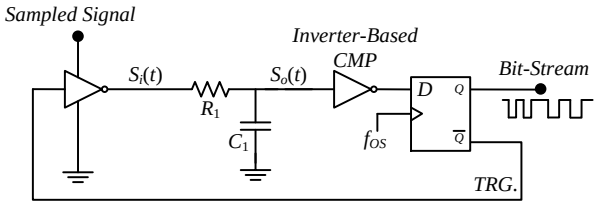


Fig. 3.6 SDADC modulator schematic circuit.

Fig. 3.7 depicts an example for steady-state operation of the SDADC's modulator. The modulator produces the bit-stream such that the voltage at node $S_o(t)$ is toggled around the threshold voltage of inverter-based comparator Vth. This is achieved by feedback link between the flip-flop and the input sampling inverter operation as can be seen in Fig. 3.7, resulting in a square signal $S_i(t)$ between 0 and the sampled voltage value, which charges/discharges the integrator's output. The relationship between the sampled signal and the generated bit-stream is according to (3.1), and it is a primary concept for the new SDADC architecture.

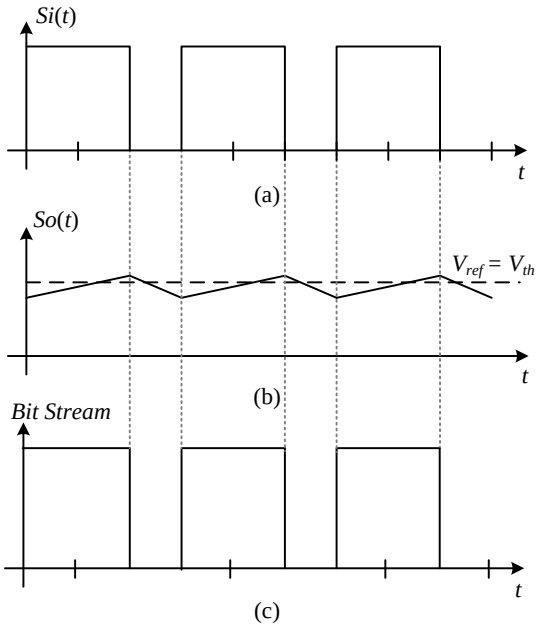


Fig. 3.7 Typical steady-state sampling operation of the SDADC. (a) Output voltage of the sampling inverter (b) Integrator's output (c) Generated bit-stream representing the sampled signal.

3.4.2. Operation mode detector

As discussed in Section II, the SDADC in this study has a clock selection mechanism to reduce the power consumption at steady-state operation. An algorithm to identify transitions is described with the aid of Fig. 3.8 and Fig. 3.9. Every four sequential full cycle results are held in the registers as shown in Fig. 3.8. The results are continuously compared and as long as they are equal, the system operates at a lower clock frequency. For a case that the comparison block detects a single change between the four sequential results, the system immediately switches to fast clock mode with rapid transitions to obtain the most accurate value of the sampled signal. It should be noted that full cycle conversion is generated when the reset counter (see Fig. 3.2) reaches 2^n-1.

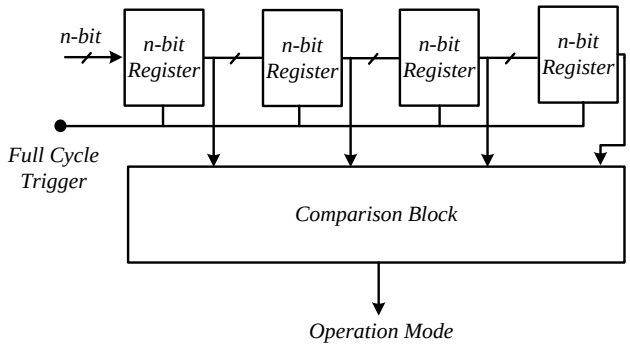


Fig. 3.8 Simplified block diagram for operation mode decision making algorithm.

Fig. 3.9 shows simulation example demonstrating the clock selection algorithm for a 10-bit SDADC to an input signal that periodically toggles between 3V to 4V. As can be seen, while the sampled voltage is constant the reset counter increases with slow clock, however, whenever transition occurs, the reset counter rapidly increases with the aid of the fast clock within in the system.

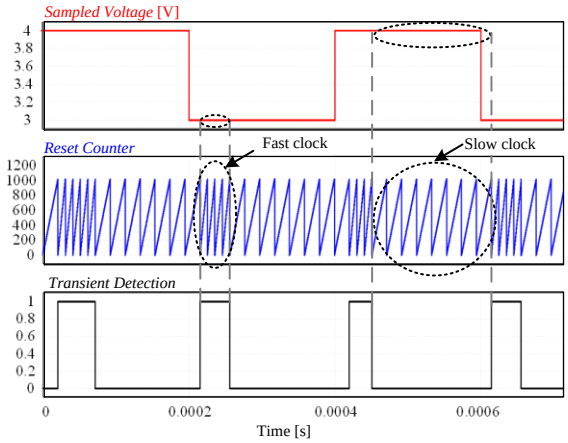


Fig. 3.9 Simulation results of clock selection entering and exiting power saving mode.

3.4.3. IC implementation

The realization of the digital control in this study primarily relies on an automated digital implementation flow, using vendor's standard cells. The IC implementation of the voltage control loop is described through three main steps. In the first step, digital custom design is carried out for SDADC's modulation stage and inverter-based comparator. Second, the controller's units including the SDADC core are described in HDL as standalone units. This is done for simplicity of the verification and functionality simulations. Then, each unit is translated to hardware using synthesis and timing verification tools into an optimized gate-level representation, given a set of design constraints. The silicon layout for each unit is generated by an automated place-and-route process. In the third step, all units are integrated together onto the higher hierarchy of the digital controller, and the resultant overall die-area is 0.07mm^2 (with 5V CMOS realization). It should be emphasized however, that for higher density assignment or scaled technology (such as deeper sub-micron process), the area and power consumption can be further reduced.

The implemented SDADC comprises of a double RC network based integrator, front-end custom designed inverter, standard cell based inverter that functions as a comparator, and a digital computation core that operates at f_{OS}=6.25MHz. Fig. 3.10 shows the SDADC layout which results in effective silicon area of 0.023mm^2, which is significantly compact in

comparison to other ADCs with similar performance. Fig. 3.11 depicts post-layout results of the SDADC for a wide range of sampled voltages to characterize and quantify the sampling accuracy. As can be seen, for sampled voltages in the range of 2.5-to-5V the obtained sampling error is less than 1.7%.

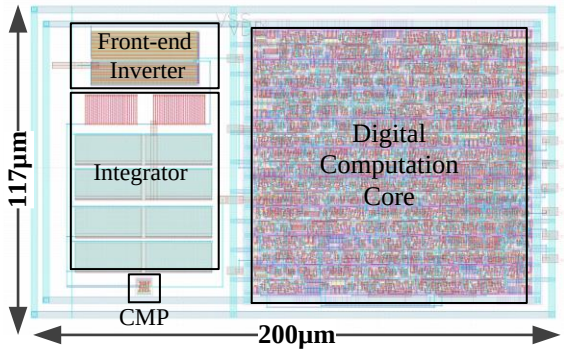


Fig. 3.10 SDADC layout 200µm x 117µm.

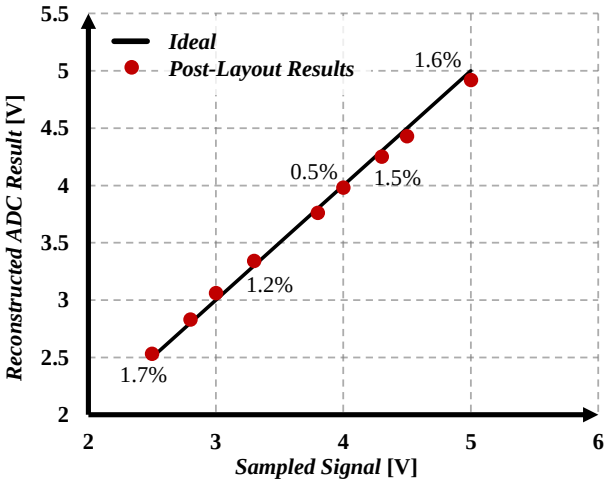


Fig. 3.11 Accuracy post-layout results of the SDADC for wide range of sampled voltages.

3.5. Simulation case study

Using the analysis and observations from the previous sections, set of simulations have been conducted in PSIM (PowerSim, Inc.) to verify the effectiveness of the new enhanced performance SDADC in a closed-loop operation of a buck converter as illustrated in Fig. 3.1.

Fig. 3.12 shows the response to reference changes of the buck converter operating in closed loop for different settings of the operating frequency, output capacitor and inductor. In the first case (Fig. 3.12a) a conventional SDADC is examined, and switching frequency f_{sw1} is as follows:

$$f_{sw1} = \frac{f_{os}}{2^n}\,, \tag{3.4}$$

where f_{os} is the oversampling clock frequency.

In the second test case (Fig. 3.12b), the new SDADC is used, demonstrating improved performance compared to the results obtained in Fig. 3.12a. It should be noted that for this evaluation, the values for inductance and capacitance in the buck converter remain the same. Since the effective sampling frequency is higher when utilizing the new approach, the switching frequency may exceed to f_{sw2}, which can be expressed as:

$$f_{sw2} = \frac{f_{os}}{\frac{m}{2}}\,, \tag{3.5}$$

and the ratio between f_{sw2} and f_{sw1}, using (3.4) can be written as:

$$\frac{f_{sw2}}{f_{sw1}} = \frac{2^n}{2^m} \;\Rightarrow\; f_{sw2} = \frac{2^n}{2^m} f_{sw1}\;. \tag{3.6}$$

As can be observed from Fig. 3.12b, the new loop settings that allowed increased switching frequency f_{sw2}, result in improved convergence of the output voltage to the new steady-state value.

The advantage of utilizing the new SDADC becomes widely apparent in response of the third test case of Fig. 3.12c. Since higher switching frequency is allowed, the inductance and capacitance values may be adjusted to satisfy similar ripple constraints as in Fig. 3.12a. This implies that effectively higher bandwidth can be achieved, resulting in better dynamic response (for the same control hardware) and lower volume of the overall solution. For the example of Fig. 3.12c, the frequency is adjusted $f_{sw2} = 4f_{sw1}$ so that same target ripples as in Fig. 3.12a. The output capacitor C_2 and inductor L_2 can be calculated as:

$$C_2 = \left(\frac{f_{sw1}}{f_{sw2}}\right)^2 C_1 \quad ; \quad L_2 = \frac{f_{sw1}}{f_{sw2}} L_1\,. \tag{3.7}$$

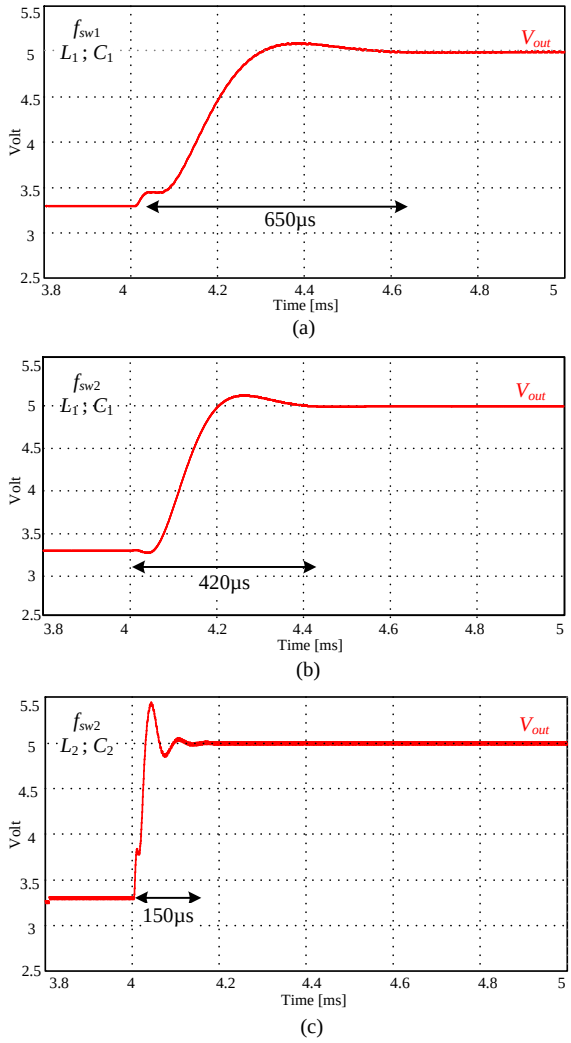


Fig. 3.12 Response to changes in the reference voltage for the digitally controlled buck converter: (a) Conventional SDADC with sampling frequency f_{sw1}, (b) New SDADC with sampling frequency f_{sw}, and same components (c) New SDADC adjusted f_{sw} and components.

Fig. 3.13 shows a simulation closed-loop VM operation of a buck converter with L=75µH and Cout=100µF at operating frequency 100kHz For a step event of the output voltage reference, Fig. 13a shows the transient response of the converter using a conventional SDADC with fOS=6.25 MHz Fig. 13b shows the transient response of the converter using the new SDADC for the same operating conditions and n=10. It can be seen that both the overshoot and settling time are significantly reduced when the sampling frequency is increased as a result of the mid-cycle updates.

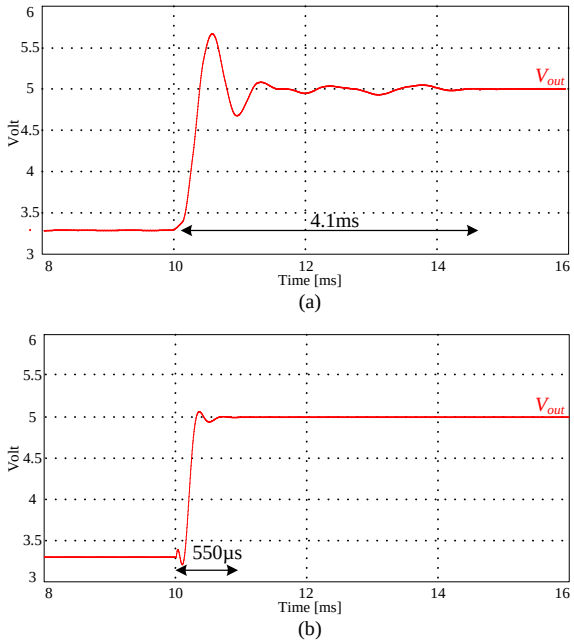


Fig. 3.13 Response to changes in the reference voltage for the digitally controlled buck converter: (a) Conventional SDADC with sampling frequency f_{sw1}, (b) New SDADC with sampling frequency f_{sw}, and same components (c) New SDADC adjusted f_{sw} and components.

3.6. Experimental system implementation and validation

To validate the operation of the new SDADC in a VM control loop, an FPGA based controller utilizing 10-bit counter based SDADC has been fully coded in Verilog and implemented on a Cyclone IV FPGA using Quartos environment, resulting in approximately 205 logic cells. The operation has been demonstrated with a buck converter prototype operating at 100 kHz for a nominal output voltage of 3.3V. TABLE I summarizes the experimental setup main characteristics. The first step of the experimental validation is to characterize and quantify the sampling accuracy of the SDADC. This is done for a wide range output voltages of the buck converter prototype. Fig. 3.14 shows the results for varying the output voltage in the range of 2.8v to 8V. It can be seen that in the range of the nominal output voltage that the error of the SDADC is less than 1%, while worst-case error of 4.6% is obtained for sampled voltage of 8V.

TABLE I. EXPERIMENTAL PROTOTYPE CHARACTERISTICS

Parameter	Value/Type
Input voltage V_{in}	10V
Output voltage V_{out}	3.3V
Switching frequency f_s	100kHz
Inductor	75µH
Capacitor	100µF, ESR=0.5Ω
Counter number of bits n	10-bit
Number of mid-cycle updates	4
Modulator's clock frequencies	3.125/6.25 MHz

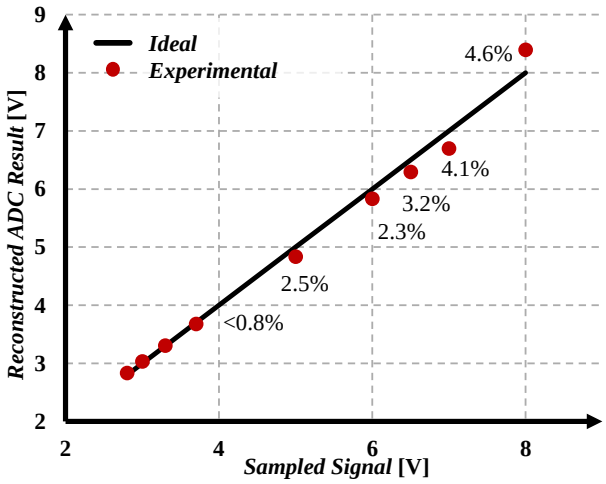
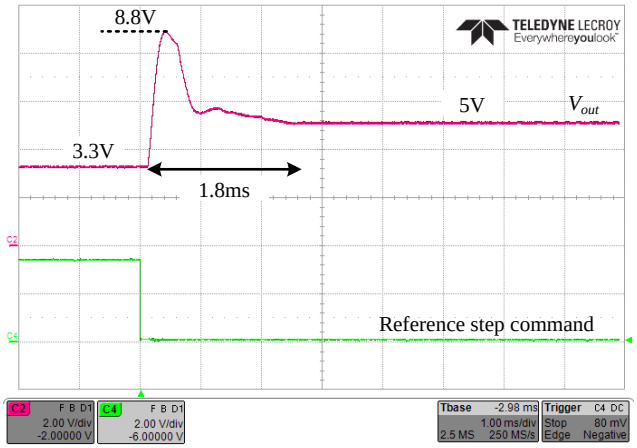
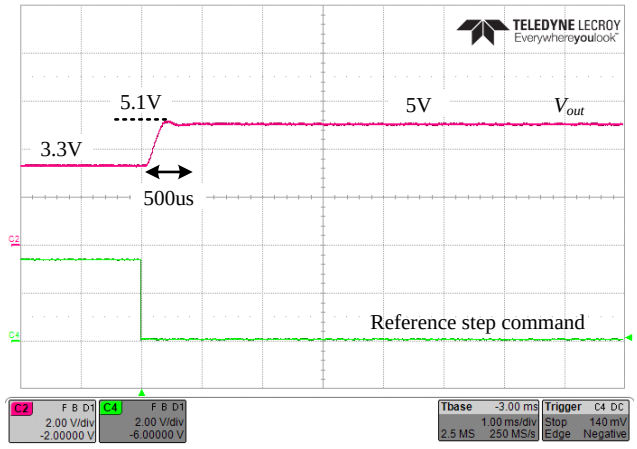


Fig. 3.14 SDADC accuracy experimental measurements for wide range sampled output voltages.

To further validate the effectiveness of the enhanced SDADC, the experimental prototype has been evaluated through a closed-loop VM operation. Fig. 3.15 shows the results for a step event of the output voltage reference, such that the output voltage varies from 3.3V to 5V, which are in good agreement with the simulation results in Fig. 3.13. Shown in Fig. 3.15a is the response of the system with the developed SDADC, it can be seen that system is well regulated validating the proper functionality of both the SDADC and digital control loop, where a 100mV overshot is obtained. Fig. 3.15b shows the response of the experimental prototype while using a conventional SDADC, it can be observed that the obtained overshot is 8.8V that is 38 times larger overshoot compared to the SDADC developed in this study. In addition, 3.6 times shorter settling time is achieved while using the new SDADC. Fig. 3.16 depicts a zoom-in on transient event of the output voltage within the system. It can be well observed that during the transition, the duty-ratio is varied according to the pre-defined mid-cycle update commands, which in this case are set in the range of 6-bits to 10-bits. The duty-ratio is increasingly growing to compensate for the variation at the output voltage, eliminate the need to wait for an update command every 2^{10} clock cycles.



(a)



(b)

Fig. 3.15 Output voltage transient response of the experimental buck prototype for 3.3V to 5V: (a) Conventional SDADC with full-cycle update (b) SDADC with mid-cycle updates. Output voltage (top – pink) 2V/div, voltage reference step (bottom – green) 2V/div. Time scale 3ms/div.

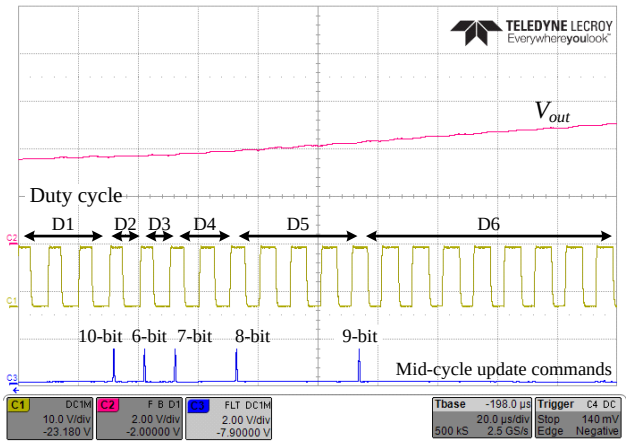


Fig. 3.16 A zoomed-in view on a transition event with increasingly growing duty-ratio based on mid-cycle time update results.

3.7. Conclusion

An enhanced performance fully-synthesizable SDADC has been presented, and verified through simulation and experimental data. The new SDADC has less hardware and silicon

requirements compared to a conventional SDADC, while presenting much better dynamics, generating fast digitizing of the sampled signal with high accuracy and wide dynamic range, even for fast variations without the penalty of sacrificing the precision. In addition, a digital VM compensation has been realized and experimentally verified with a buck converter. The accuracy of the SDADC has been experimentally characterized by measuring the output voltage over wide range operating points, demonstrating worst-case error of 4.6%, while in the vicinity of the nominal operating conditions 99% accuracy has been achieved. The VM control including the new SDADC have been designed in digitally-oriented approach without any power hungry analog blocks, and implemented in 0.18μm 5V CMOS process resulting in total effective silicon area of 0.07mm^2.

4. Digital Lock-In Controller IC for Optimized Operation of Resonant SCC

This chapter describes a lock-in integrated controller for resonant SCC. The controller identifies the resonant period of each sub-circuit on-the-fly and locks-in to the correct switching time to fully utilize the charge transfer rate for each flying capacitor. The various modules of the controller are detailed, including the auto-tuner and sequencer which accommodate any mismatch, variations or drifts of component values or circuit configuration. The IC has been designed and fabricated on a 0.18µm 5V process resulting in effective silicon area of 0.64mm2. Post-layout results of the controller IC operating in closed-loop are provided, demonstrating accurate lock-in for two resonators with individual independent resonant characteristics. A full-scale hardware prototype of 650W 4:1 switched-tank-converter is used to validate the controller's operation prior to IC fabrication, demonstrating excellent lock-in capabilities resulting in high efficiency of up to 98.6%.

4.1. Overview

Switched-Capacitor Converters (SCC) which have been rigorously explored over the last two decades ,[83]-[92] have established a dominant role in power management in datacenters and other cloud computing related applications. In light of the acceleration of the standardization of the power delivery structure that has been heavily affected by the trend-leading open-computing-project consortium (OCP) [93], the necessity to step the 48V rail down to 12V with extremely high efficiency and very high power density has established an application stand point at which SCC technology and its derivatives is highly superior over the inductor-based alternatives.

Power density and conversion efficiency are of key importance in datacenters applications (to maximize the amount of computing power per volume). This translates onto extremely strict conversion performance requirements at the 48V-to-12V level so that it would not further deteriorate the attractiveness of the overall solution. Since this application calls for a fixed conversion ratio, SCC technology renders a very attractive candidate. At medium power levels, SCCs have widely demonstrated peak efficiency over 98% [94]-[95]. Results of resonant SCC (RSCC) based power converters for datacenters applications, demonstrating peak efficiency of 98.5% around 200W have been recently presented [96]-[98].

The primary factor that facilitates efficient power conversion for the general case of RSCC is the accuracy of the switching frequency with respect to the resonant conditions of

the converter. Optimal charge transfer is achieved in the case that the conduction time of each switching state matches exactly half of the resonator's period, and that deadtime between switching states is minimized [99]-[100]. In this way, the charge of the flying capacitor is fully utilized every cycle. Converter topologies with more frequent charge transfer of the output such as [101] inherently feature lower equivalent resistance, and as a result potentially more efficient than topologies with the basic charge-discharge pattern [102].

In topologies that comprise multiple switching states to complete a charge cycle [103], or in configurations with multiple resonators, full utilization of the charge out of each flying capacitor, every cycle, introduces complexity to the circuit controller. This mandate accurate zero-crossing information of the flying capacitor current and specific timing settings per switching state (and in some applications, per individual switch). This is since the conduction path is different for every state, which changes the resonant period. The resonant parameters per sub-circuit vary as a function of the stresses on the component, loading conditions, the physical layout of the design, and drifts with temperature and over time. In addition, the timing parameters need to account for variations and the accuracy of the current zero-crossing detection circuit (ZCD). It would be extremely advantageous to utilize a controller which obtains the ZCD information, identifies on-the-fly the resonant period for each sub-circuit, locks-in to the correct switching time, and is capable of automatically compensate to any variation of the circuit – This has been pursued in this study.

The objective of this chapter is therefore to introduce a lock-in integrated controller architecture that facilitates accurate switching timing to fully utilize the charge transfer for each flying capacitor at every switching state as schematically illustrated in Fig. 4.1. The controller adjusts to accommodate any mismatch, variations or drifts at component values or the circuit configuration. It is a further objective of this study to present an all-digital IC implementation of the lock-in switching governor and detail the fundamental building blocks. Two lock-in architectures are presented and described in detail. One based on synchronized digital hardware and suitable for medium frequency range applications (in the range of several hundred kHz) whereas the second method is based on asynchronous combinatorial logic and features very high frequency resolution which qualifies to the MHz range. The control method is demonstrated for two resonators, with individual independent tuning per sub-circuit and switching state.

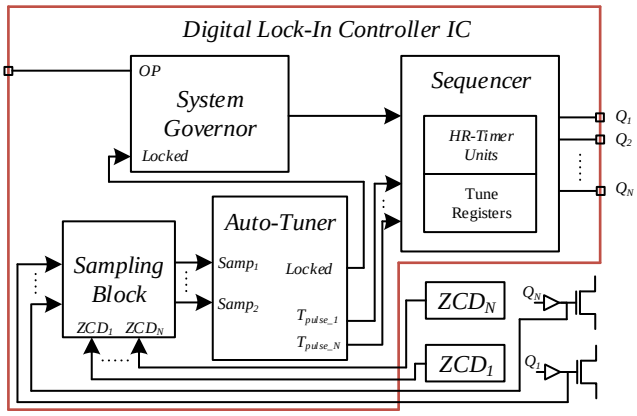


Fig. 4.1 Simplified block diagram of the digital lock-in controller IC.

4.2. Digital lock-in controller

The digital lock-in controller illustrated in Fig. 4.1 is described in this section in a general form and can be applied to various types of RSCC-based single or multi-stage converters topologies. The controller comprises the following modules as depicted in Fig. 4.1 (described in-detail in the subsections below): a) a system governor to manage, synchronize and dictate the operation mode; b) auto-tuner unit to adjust and calibrate the conduction time of the switches to achieve ZCS operation in all resonant tanks; c) switching sequencer to generate the required drive signals to the power switches; and d) a sampling block for accurate reading of the zero-current-detection (ZCD) sensors' outputs.

One possibility for tuning the drive frequency to the resonant characteristics can be performed by immediate response to the information from the zero-crossing point sensor [89]-[90]. This method may be problematic for some cases due to latencies and delays in the system. An alternative approach that is utilized for high switching frequency applications [91] performs delay-locked-loop convergence of the switching frequency to the resonant one. Such utilization, as employed in this study, locks in to the desired running frequency and compensates for any variations or mismatches in the system. This operation suits well resonant conversion, in particular at high-Q, since the response of the system to variations is rather slow and carries on over several switching cycles. In the specific case on-hand, as described in this study, the main motivation of the tuning comes from thermal considerations, to achieve optimal transfer conditions which result in the highest efficiency conditions in the system, is a relatively slow-varying objective that can be fulfilled well with a lock-in tuning architecture.

The tuning process is performed by the relatively slow internal clock of the controller IC, resulting in a simple and straightforward realization of the *Sequencer* and the *Sampling*

blocks. For converters operating at higher frequencies, the frequency detection and generation units have been realized through asynchronous combinatorial logic to enable operation with higher resolution than of the one obtained by the internal synchronous clock.

4.2.1. System governor

The *governor* module dictates the desired operation mode of the converter, based on auxiliary configuration (*OP* in Fig. 4.1). In the private case for a conventional RSCC, the governor decisions include light-load operation of the converter, start-up and turn-off sequences as well as the applied dead-time. For more complex topologies, the system governor may dictate various switching schemes to minimize on-board periphery such as ZCD sensors in multi-stage converters, and even to determine the voltage conversion ratio. In this study, all synchronization actions performed by the system governor are based on an internal clock (in the specific case is 20*MHz*). A feedback from the auto-tuner block (*Locked* in Fig. 4.1Fig. 4.1) provides the governor with the required information regarding the tuning process. To support wide range of resonant converters, start-up and turn-off sequences can be re-programmed with no hardware modifications.

4.2.2. Auto-tuner

The auto-tuning module consists of several internal units, as shown in Fig. 4.2Fig. 4.2a. A digital compensation unit evaluates the sampled ZCD signals and determines whether the resonator current is zero when the transistor turns off. Non-zero resonant current at transistor turn off will occur in case of '*early*' or '*late*' switching as illustrated in Fig. 4.3 . Based on the information of the polarity of the current at turn-off, the compensator modifies the on-time for each resonant tank separately (T_x in Fig. 4.2Fig. 4.2a). The on-time of the next switching cycle is increased in case the sampled ZCD signal indicates '*early'* switching and decreased in case of '*late'* switching indication. Once the sampled signal of the ZCD indicates ZCS, the on-time remains unchanged. The initial values that the unit start the process with can be programmed in advanced, or can be used as default, depending on the length of the start-up tuning procedure that is allowed.

The compensator block is followed by a digital LPF to smooth any noise variations, and it also functions as a possible degree of compensation network in cases where additional lagging or leading phase is required. In this study, filtering is performed by comparing a configurable number of compensator outputs, as shown in Fig. 4.2Fig. 4.2b. At the beginning

of each switching cycle a shift operation is performed on the register structure and the output of the LPF filter is calculated (T_{pulse_x} in Fig. 4.2Fig. 4.2a). The tune-registers are updated only when all registers hold the same value, which completely eliminates the effect of singular non-ZCS events or inaccurate indications of the ZCD sensors on the converter's operation.

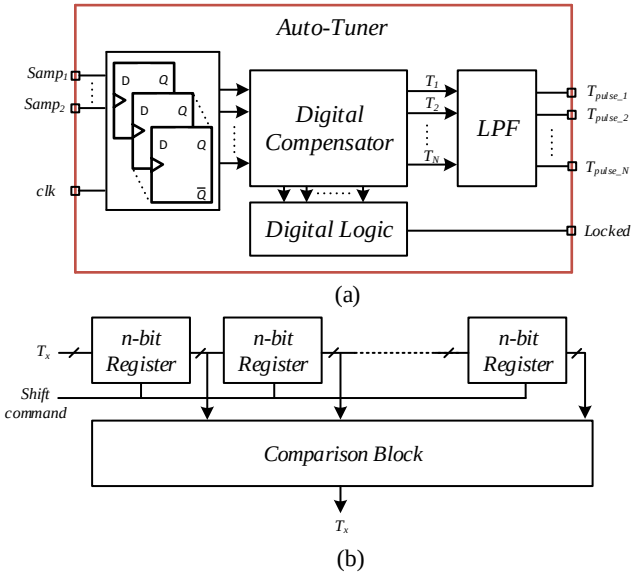


Fig. 4.2 (a) Internal block-diagram of the auto-tuner module (b) Simplified block-diagram of the LPF.

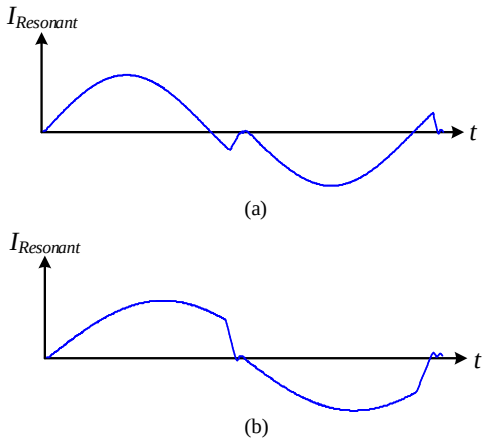


Fig. 4.3 Current waveform of a resonant circuit switched-off at (a) late switching (b) early switching.

The auto-tuning module allows flexible choice of the resonant tank values which determine the operating frequency of the converter. At power-up a lock-in routine is initiated in which the auto-tuner locates the resonance frequency of each tank. During normal running mode, the module observes the operation of the power-stage and provides fine-tuning to ensure ZCS in case the passive components drift from their values upon start-up.

4.2.3. Sequencer

The *sequencer* module executes the gating signals to the power stage based on the information from the preceding modules. It incorporates a multi-phase high-resolution timer to ensure correct and precise pulse-length for single or multi-stage converter topologies. The gating signals are set independently per resonator (or sub-circuit) of the converter so that ZCS operation can be separately realized per all resonant tanks or stages of a converter, regardless of component mismatches or variations.

The conventional approach to implement a high-resolution timer is by a fast-clock counter-comparator scheme [107]-[109]. In this way, *n*-bit resolution at a switching frequency of f_s requires a reference clock frequency of $2^n \cdot f_s$ which translates to increased power consumption. In this study, the high-resolution pulse-width drive signals for the power switches are produced by incorporating a coarse-counting block followed by a fine-tuning delay-line based module, as shown in Fig. 4.4. This allows a design that is based on standard cells, and enables direct synthesis with low power consumption. As can be seen, a counter-based signal is generated independently for each resonant tank by the information provided from the auto-tuner block. This signal is then delayed by the delay-line to achieve the exact on-time for ZCS operation of all resonant tanks by setting the input of each multiplexer unit according to its *sel* command, which is supplied by the auto-tuner. Protection logic and other gating-related features are also incorporated in this module to allow full completion of a sequence and to avoid overlapping of signals in case the resonant tanks operate with different drive sequences.

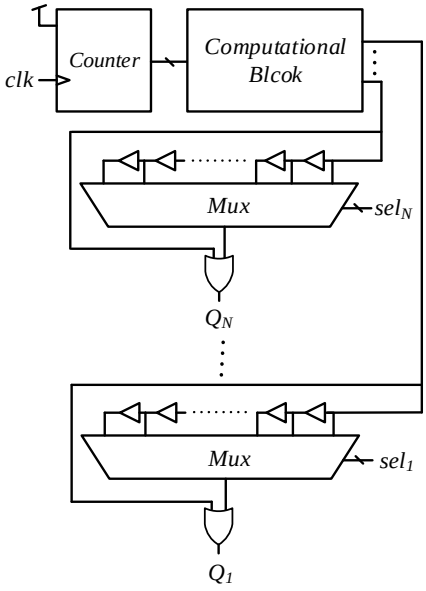


Fig. 4.4 Simplified block diagram of the sequencer module.

4.2.4. Sampling block

Inherent delay between the generated gating signals in the controller and the actual conduction of the transistors is quite common for all switch-mode applications. This delay, from a controller point of view, is generally unknown and may significantly vary as a function of the operating point or the passive components, driving circuitry and power transistors used [110]-[112]. The information regarding the polarity of the resonant current at transistor turn-off, which is the indicator for early or late switching of the transistors, is only valid in proximity to the switching event. Sampling the ZCD sensors must be able to compensate, or at least consider this inherent delay so that an accurate status information is obtained, i.e. early or late switching.

In this study, two completely synthesizable approaches have been realized to acquire the information from the ZCD sensors while accounting for the above-mentioned delay. The first is based on continuous sampling of the ZCD sensors at the internal clock's frequency from the turn-off command by the controller until the end of the applied dead-time period, as shown in Fig. 4.5. Here, the ZCD sensor is sampled at the beginning of each clock cycle and the acquired result is processed according to a state-machine algorithm to acquire the converter's switching-state. Once the dead-time period is over, the sampling block provides the auto-tuner with the valid readings for further processing and tuning operations.

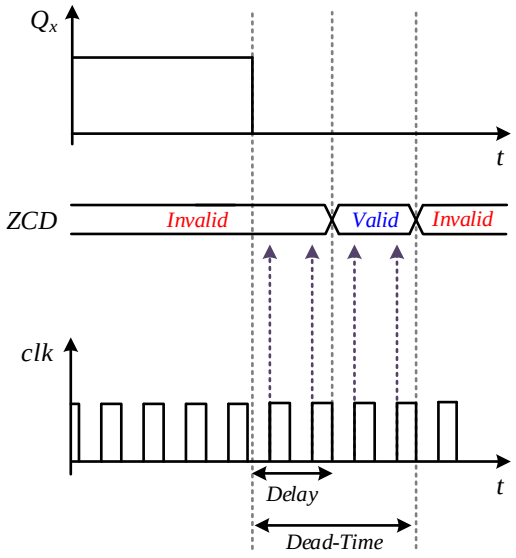


Fig. 4.5 Continuous-sampling based approach of the ZCD sensors.

The second approach requires less computational efforts during the sampling process, yet still allows sampling with greater proximity to the switching action to further minimize charge losses due to late or early switching of the transistors. This is performed by incorporating a *delay-estimation logic* (detailed in 4.5) which accurately estimates the

inherent delay upon start-up, illustrated as Δ_s in Fig. 4.6 , in addition to a delay-line based structure which generates a sampling signal with a resolution of a single delay-element. Once the ZCD sensors have been sampled, the sampling block provides the auto-tuner with the acquired readings for further processing and tuning operations.

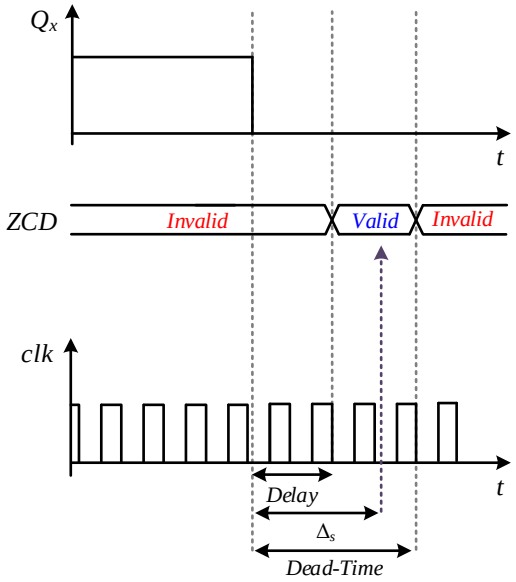


Fig. 4.6 Single-sample based approach of the ZCD sensors.

4.2.5. 4:1 STC control and simulation case-study

As described earlier, the on-time for each resonant tank is modified by the auto-tuner to achieve ZCS operation based on the polarity of the resonant current at turn-off. The operation of the controller is demonstrated for a 4:1 switched-tank-converter (STC) [96] which comprises two resonators, independently tuned to achieve full ZCS operation, as shown in Fig. 4.7. The operation of the STC can be divided into two states – charging or discharging of the resonators, as shown in Fig. 4.7a and Fig. 4.7b, respectively, with a short dead-time period between them. The flying capacitor (intermediate element in Fig. 4.7) connects to a different resonator at each active sub-circuit, resulting in charge transfer from the input to the output. Soft-charging is achieved for all capacitors in the system, and soft-switching of all switches can be achieved allowing the correct timing which is the task of the controller. For the case of 4:1conversion ratio STC illustrated in Fig. 4.7, the voltages at V_{sw1} and V_{sw2} are a direct indicator to the current polarity at turn-off. In case of early switching, the resonant current is flowing towards V_{sw1} or V_{sw2} (as shown in Fig. 4.7a) and the voltages are clamped to $V_{out} + V_F$ (where V_F is the forward voltage of the transistor diode). The same applies to the case of late switching where the current is flowing from V_{sw1} or V_{sw2} (as shown

in Fig. 4.7b), here the voltages will be equal to $-V_F$. Therefore, the ZCD inputs to the controller are obtained from V_{sw1} or V_{sw2}.

The ZCD sensor produces a *2-bit* result indicating late-switching (*2'b00*), early-switching (*2'b11*) or ZCS operation (*2'b01*) which is the input to the auto-tuner block, as shown in Fig. 4.1. The controller observes the status of the ZCD sensors after transistor turn-off and the on-time for each tank is modified accordingly by the compensator.

The verification of the controller operation has been carried out on a 48V-12V STC converter by a set of simulations conducted in PSIM (PowerSim, Inc.); the parameters of the nominal values of the passive components are: C_{r1}=2.35μF, L_{r1}=70nH, C_{r2}=2.1μF, L_{r2}=63nH, R_L=0.26Ω. Results of the lock-in tuning process are shown in Fig. 4.8a-e, demonstrating convergence onto tuned conditions from off-tune starting points of both resonators, where Fig. 4.8c,Fig. 4.8d and Fig. 4.8e are a zoom-in of the area marked C,D and E in Fig. 4.8a, respectively. It can be seen that the output voltage increases to approximately 12V, which is the no-load target voltage, indicating that in the context of optimal charge transfer, the controller adequately fulfills its task.

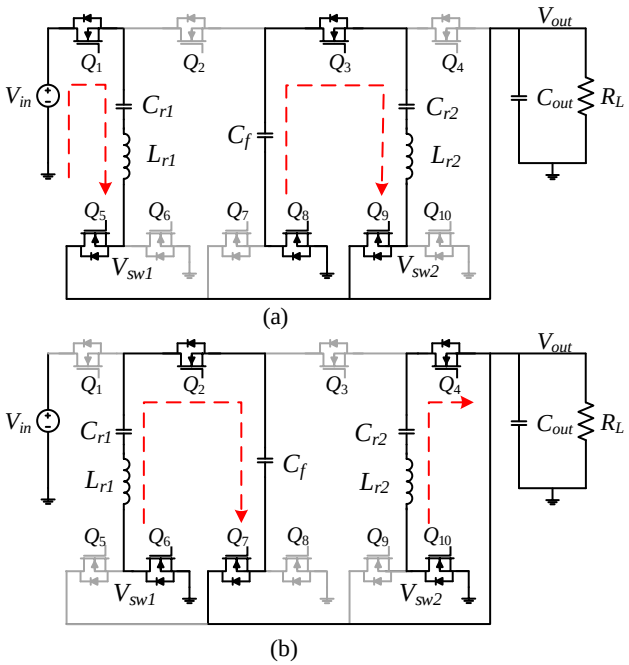


Fig. 4.7 Equivalent circuits of the 4:1 STC. (a) Charging operation of the resonant tank. (b) Discharging operation of the resonant tanks.

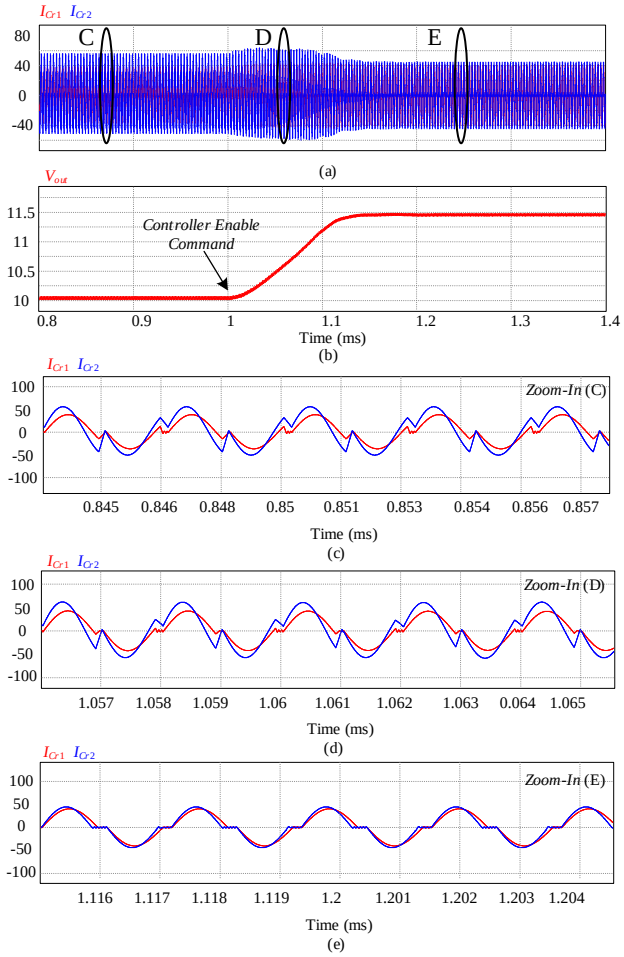


Fig. 4.8 Closed-loop operation of the controller for a 4:1 STC converter. (a) Resonant currents (b) Output voltage (c) Zoom-in on the resonant currents before controller enable command (d) Zoom-in on the resonant currents during the convergence period (e) Zoom-in on the resonant currents at steady-state.

4.3. System-level and performance challenges

4.3.1. Single-pin configuration

In complex controller ICs where pin-count is an important asset and it is required to provide access to a large number of operating modes, a single-pin setup is essential. This implies that programming, mode selection, or values setting is carried out according to the voltage level that is imposed on the input pin. The amount of levels that can be utilized in this approach depends on the voltage span allowed on the input, resolution and accuracy of the detection unit. The single-pin configuration is facilitated in this study by a Sigma-Delta (SD) modulator and digital logic as shown schematically in Fig. 4.9.

The SD modulator has been realized with simplified hardware to reduce complexity and the effective area. This may come at the cost of performance or conversion speed, but since the objective of this ADC is to acquire static, or semi-static, voltage levels, the solution fits

well within the specifications. As can be seen in Fig. 4.9, the modulator front-end is realized by a digital inverter, with V_{op} as the high logic level (supply). The integrator is realized by a simple RC network with a corner frequency of at least one order of magnitude lower than the clock frequency. Quantizer is realized by another digital inverter or buffer. The result is then held by a D-flipflop to facilitate a clocked bit-stream and to generate the oversampling frequency of the ADC. The resultant SD-based ADC is a hardware-efficient voltage level translator, the average voltage at node $S_o(t)$ can be expressed as:

$$\overline{S_o(t)} = V_{ref} = V_{op}\frac{CNTR_n}{2^n}, \tag{3.8}$$

where V_{ref} is the reference value for the modulation process (the threshold voltage of the inverter-based comparator) and $CNTR_n$ is the number of logic-high occurrences in the bit stream for 2^n clock cycles.

The bit-stream is the input to the computational logic which counts the amount of 'ones' (equals to $CNTR_n$) with a dedicated counter which acts as a sinc LPF, and resets at pre-defined intervals to perform decimation. In this study, the voltage applied on the front-end inverter is translated to a digital representation every 1024 clock cycles, which results in a 10-bit representation of the desired operating mode of the controller.

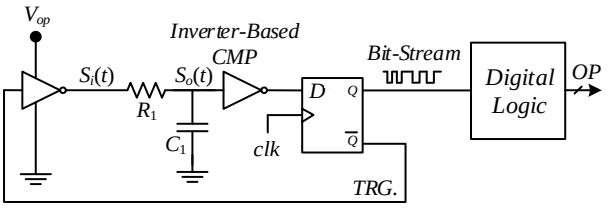


Fig. 4.9 Simplified architecture of the single-pin configuration hardware.

4.3.2. Inherent delay calculation

Estimation of the inherent delay between the gating signals of the controller and the actual turn-off of the power transistors is performed upon start-up and every N_{est} STC switching cycles to account for variations of the passive components (N_{est} is set by the configurable inputs of the controller, *OP* in Fig. 4.1). Upon initiation of the delay estimation procedure, a pre-defined switching frequency is applied on both tanks so that early-switching operation is ensured. As a result, the voltage at the switching nodes, V_{SW1} and V_{SW2}, is clamped to $V_{out} + V_F$ when the power stage transistors are turned-off, as shown in Fig. 4.10. To estimate the inherent delay, sampling the ZCD sensor is performed once every switching cycle in different locations (Δ_x in Fig. 4.10) until the early-switching reading from the ZCD sensor

is acquired (2'*b*11), as shown in Fig. 4.10b-d. The inherent delay, Δ_s, is estimated to be the minimum delay between the controller gating signals and a sampling command that acquires a valid reading from the sensor.

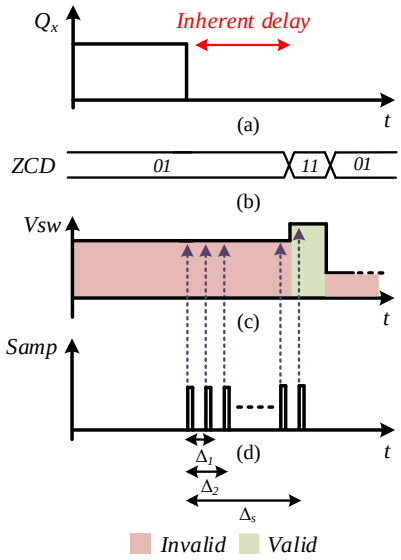


Fig. 4.10 Waveforms during the inherent delay calculation procedure (a) Controller gating signal (b) ZCD sensor (c) Switching node (d) Sampling signals.

4.4. Experimental and post-layout verification

A digital controller IC for RSCC has been designed and fabricated in 0.18μm 5V process (taped-out on June 28, 2019). The IC layout micrograph is depicted in Fig. 4.11 with overall die area that is pad-limited at 4 mm^2, while the effective silicon used is 0.64mm^2. The operation of the controller IC has been verified with post-layout simulations using Cadence Virtuoso, where the IC connects to a 4:1 STC converter with a 48V input voltage feeding a resistive load of 0.3Ω. The power stage as well as all peripheral circuitry (ZCD sensors, sigma-delta modulator, etc.) have been added to the simulation based on the components used in the experimental setup (discussed next). A transition from late-switching open-loop operation to closed-loop ZCS operation is simulated and verified as shown in Fig. 4.12. The zoomed-in view of Fig. 4.12b indicates that in the case of late-switching the voltage at the switching node, V_{sw2}, is clamped as discussed in IV and accurately indicates the polarity of the resonant current at turn-off. The zoomed-in view of Fig. 4.12c shows that once the closed-loop operation is enabled, ZCS is achieved within several cycles.

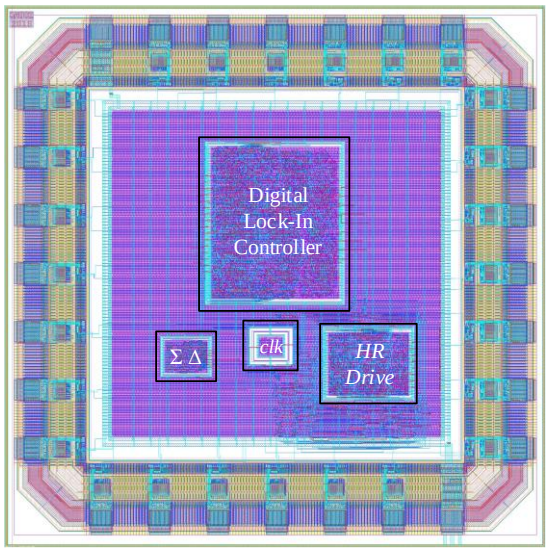


Fig. 4.11 Layout of the fabricated RSCC controller IC.

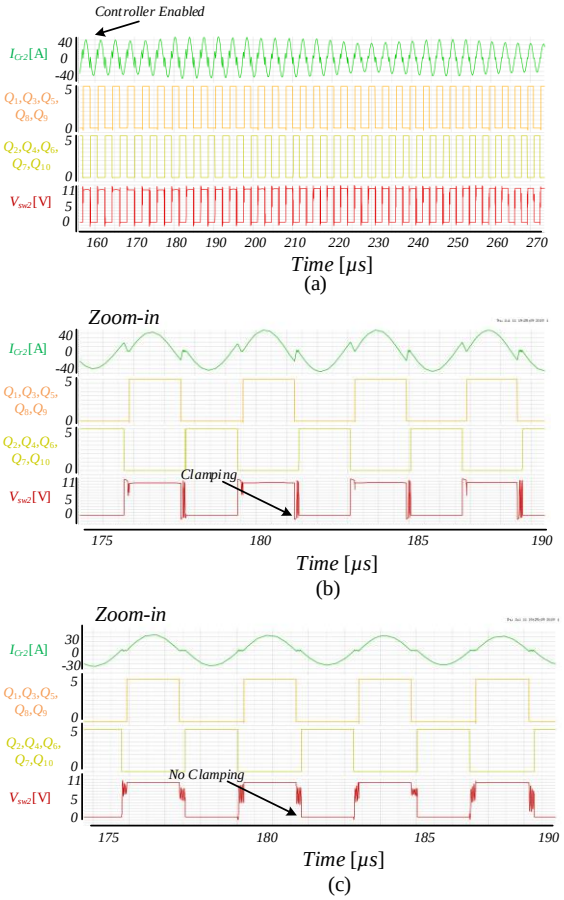


Fig. 4.12 Post-layout simulations controller IC for a 4:1 STC. (a) Transition from late-switching to ZCS. (b) Zoom-in during open-loop operation. (c) Zoom-in after convergence to ZCS operation.

To validate the core of the controller prior to IC fabrication, and to further investigate the capabilities of the main control units developed in this study in real environment, a full-scale hardware prototype of a 650W 4:1 STC (48V-12V) converter as well as all required peripherals for the controller operation have been designed, built and tested. Shown in Fig. 4.13 are the full experimental setup, PCB with the power stage and connection to FPGA

platform. The control algorithm has been fully coded in Verilog and implemented on a Cyclone IV FPGA using Quartus environment. The experimental STC hardware has been designed on a 14-layer PCB and it is rated for 650W. The effective board area of the 4:1 power stage is 5cmX2cm. The resonators have been designed symmetrically with equal resonant frequency and the following component values: C_{r1}=2.35μF, L_{r1}=70nH, C_{r2}=2.35μF, L_{r2}=70nH.

Fig. 4.14 shows the efficiency curve as a function of the load under tuned conditions that have been obtained by the controller operation. Experimental waveforms, depicted in Fig. 4.15, for closed-loop operation of the system with deliberate mismatch between the resonant tanks component values (C_{r1}=2.62μF, L_{r1}=70nH, C_{r2}=2.35μF, L_{r2}=50nH). Fig. 4.15a shows smooth transition from open-loop early-switching operation to ZCS of both resonant tanks. A zoomed-in view of the resonant currents as well as the switching nodes is shown in Fig. 4.15b-c.

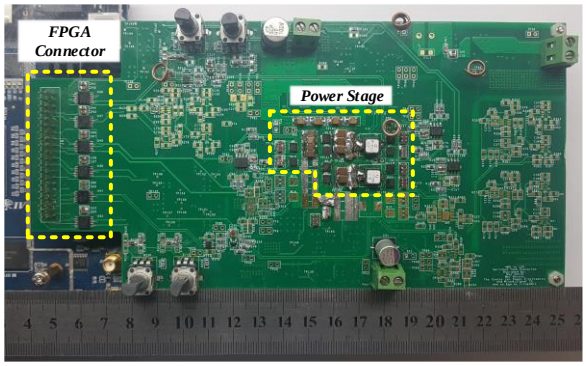


Fig. 4.13 Experimental prototype of a 4:1 STC for evaluation of the control algorithm on FPGA.

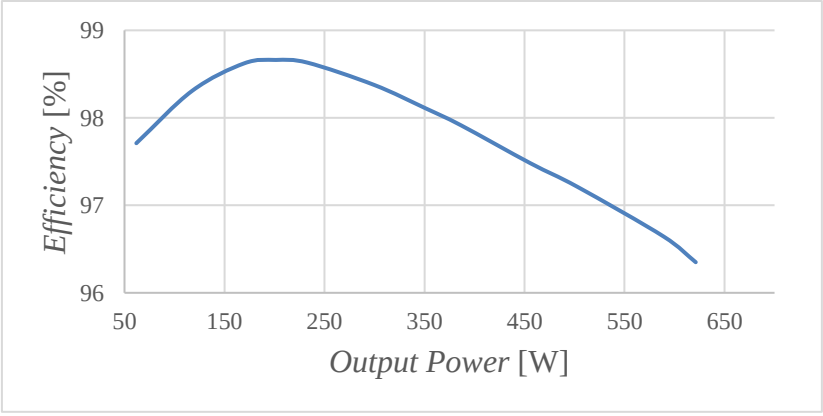
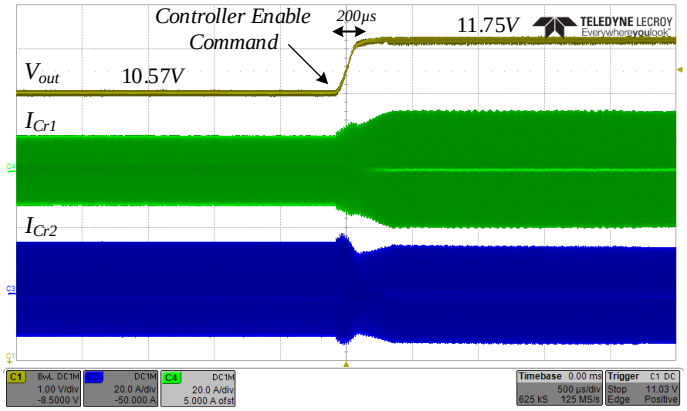
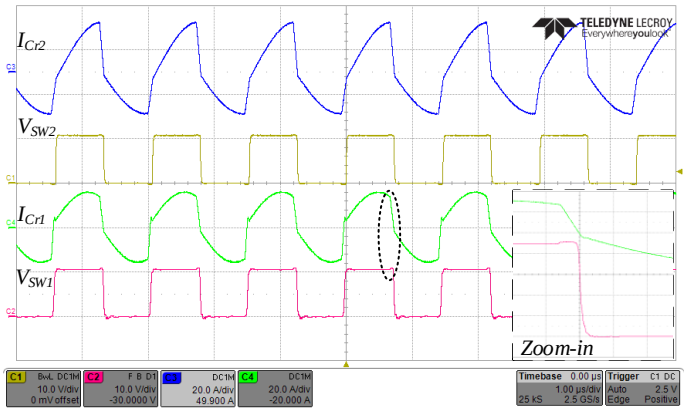


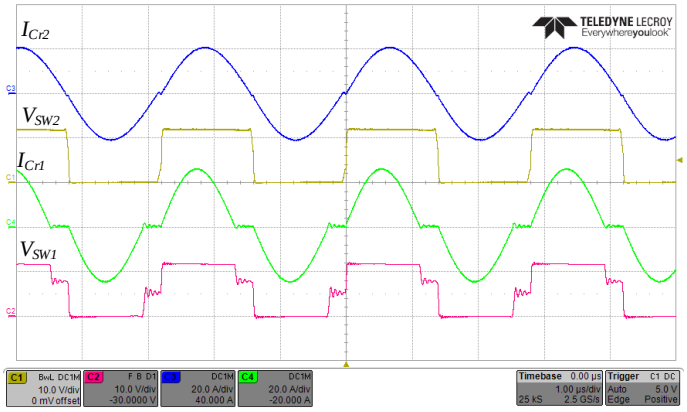
Fig. 4.14 STC efficiency under tuned conditions.



(a)



(b)



(c)

Fig. 4.15 Experimental results of a 4:1 STC's transition from open-loop early-switching to ZCS by the digital lock-in controller. (a) Full view of the tanks' currents and the output voltage. (b) Zoom-in view during open-loop operation on the tanks' currents (top-blue, middle-green) 20A/div, switching nodes (middle-yellow, bottom-red) 10V/div, time scale 1μs/div. (c) Zoom-in view during ZCS closed-loop operation on the tanks' currents (top-blue, middle-green) 20A/div, switching nodes (middle-yellow, bottom-red) 10V/div, time scale 1μs/div.

Operation of the fabricated controller IC has been verified through multiple experiments under various switching states, as shown in Fig. 4.17-Fig. 4.18. The same power-stage was used in these experiments, to enable correct comparison between the FPGA based and the fabricated IC controller. An additional PCB was designed which connects to the power stage and enables the IC to directly drive the power switches, as shown in Fig. 4.16.

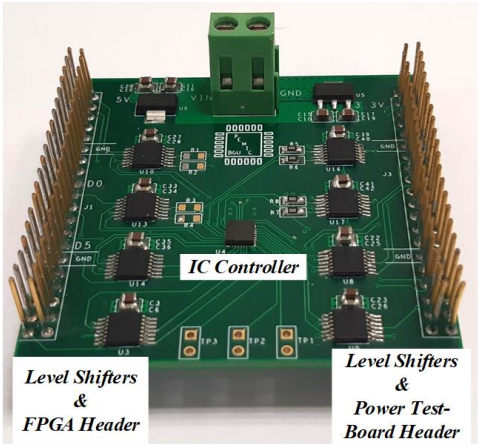


Fig. 4.16 Chip prototype on PCB.

Fig. 4.17 shows a transition from open-loop late-switching of both resonators to ZCS. Prior to the enable command of the controller IC, the converter operated with arbitrary switching times. As can be seen, once the auto-tuning capabilities of the controller are utilized, ZCS is achieved which also significantly increases the charge transfer rate.

The controller's performance for two different resonators is depicted in Fig. 4.18. Here, a transition from open-loop early-switching of both resonators to ZCS is shown. Prior to the enable command of the controller IC, the converter operated with very short on-times. As can be seen, ZCS is achieved for each resonant tank separately, which fully utilizes the charge transfer for each flying capacitor. As described in III, switching cycle is determined according to the longest required on-time, this to ensure constant operating frequency in steady-state. The clamping of the switching nodes' voltages is shown in the zoom-in of Fig. 4.18b when the converter does not operate in ZCS. As can be seen in the zoom-in of Fig. 4.18c, once ZCS is achieved the power switches' diodes are not clamped, as described in IV.

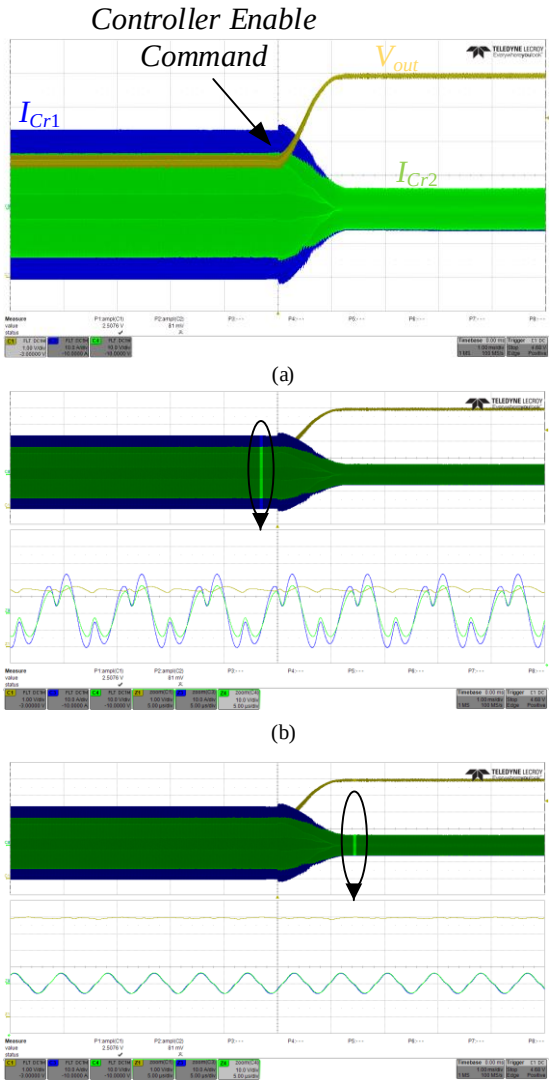


Fig. 4.17 Tansition from open-loop late-switching to ZCS (a) Tansition event from open-loop to closed-loop operation (b) Late-switching of both resonators with zoon-in on inductors currents and output voltage. (c) ZCS of both resonators with zoon-in on inductors currents and output voltage.

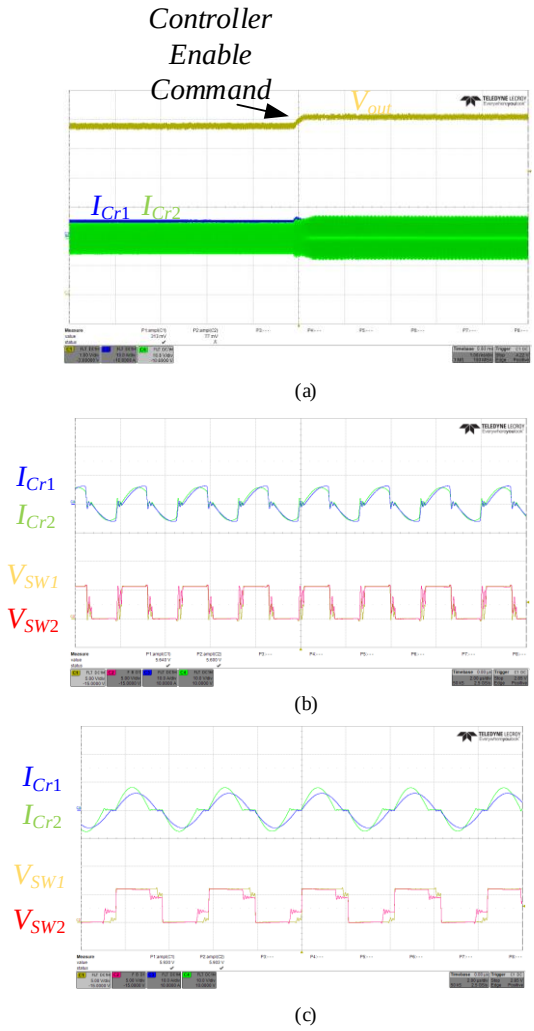


Fig. 4.18 Tansition from open-loop early-switching to ZCS for two differenct resonators (a) Tansition event from open-loop to closed-loop operation (b) Late-switching of both resonators with zoon-in on inductors currents and output voltage. (c) ZCS of both resonators with zoon-in on inductors currents and output voltage.

4.5. Conclusion

A lock-in integrated controller architecture that facilitates accurate switching timing for single or multi-stage RSCC based topologies has been presented. The controller adjusts to accommodate any mismatch, variations or drifts of component values or circuit configuration, and performs tuning for each resonator independently to fully utilize the charge transfer for each flying capacitor in the system. A full-scale hardware prototype of 650W 4:1 switched-tank-converter has been used to validate the controller's operation prior to IC fabrication, demonstrating excellent lock-in capabilities resulting in high efficiency of up to 98.6 %. The fully-digital controller IC has been designed and fabricated on a 0.18μm 5V process by pure digital means, resulting in effective silicon area of 0.64mm^2. The post-layout results of the closed-loop operation demonstrated accurate lock-in capabilities for two resonators with individual independent resonant characteristics. Experimental results of the

fabricated controller IC are in very good agreement with post-layout results as well as with the FPGA-based prototype.

5. Discussion

5.1. Contribution of the research

The key contributions of this work are summarized as follows:

Optimized control scheme for NIBB converter –A new operation mode for steady-state operation for NIBB converters around unity conversion ratio, as well as its detailed analysis and implementation details have been detailed. In addition, the study introduces detailed transient mitigation algorithms for all operation modes, in particular for the unity conversion ratio but also for the entire operation range, enabling optimized transient recovery and untimely volume reduction of the overall solution.

Single-variable load estimation procedure – A transient-event-driven load extraction method for optimal transient mitigation controllers of boost-type converters has been developed. The procedure operates on present information alone, without the need for prior knowledge of the former performance neither of the system parameters. The overall resources are equal or less to those needed for CPM operation execution, making the solution lean on hardware and extremely attractive for integration into any controller platform.

Fully-synthesizable $\Sigma\Delta$ ADC – A new approach for sigma-delta based analog to digital converter suitable for digital voltage regulation has been developed. Its all-digital fully-synthesizable realization results in less hardware and silicon requirements compared to conventional SDADC.

Digital lock-in controller IC for optimized operation of RSCC – A fully monolithic digital controller for RSCC has been designed and implemented on-chip by pure digital automated synthesis process and place-and-route tools. The controller identifies the resonant period of each sub-circuit on-the-fly and locks-in the current switching time fully utilize the charge transfer rate for each flying capacitor. It can be applied to various types of RSCC based single or multi-stage topologies.

5.2. Suggestions for future research

Some suggestions for future lines of investigation that can be developed as a result of this thesis are outlined below:

Regulated switched-tank converter – Regulating the output voltage of a switched-tank converter by integrating a DC-DC converter at its output. NIBB converter can support a wide range of input voltages, which makes it a good candidate for applications in which the input voltage may vary from its nominal value. In addition, operation around unity conversion ratio has been addressed in this study and can be implemented in the control scheme to ensure high efficiency.

HR-PWM module for multi-stage and multi-phase converters – A more precise and size-efficient multi-phase module is required to achieve better time-resolution for multi-stage or multi-phase converters. A fully-synthesizable approach, as taken in this study, will enable scaling with the fabrication process and versatility to a variety of PDKs.

6. References

[1] T. Urkin, M. M. Peretz, "Unified Current-Programmed Digital Controller for Non-Inverting Buck-Boost Converter with Optimal Steady-State and Transient Conditions", *2019 IEEE Applied Power Electronics Conference and Exposition (APEC), March 2019*.

[2] T. Urkin, M. M. Peretz, "Digital CPM Controller for Non-Inverting Buck-Boost Converter with Unified Hardware for Steady-State and Optimal Transient Conditions", *IEEE Trans. On Power Electron*.

[3] T. Urkin, M. M. Peretz, "Single-Variable Accurate Load Estimation for Optimized Transient Mitigation in Boost Type Converters", *2019 IEEE 20th Workshop on Control and Modelling for Power Electronics (COMPEL)*, June 2019.

[4] T. Urkin, E. Abramov, M. M. Peretz, "Enhanced Performance Fully-Synthesizable SD-ADC for Efficient Digital Voltage-Mode Control", *2018 IEEE 19th Workshop on Control and Modelling for Power Electronics (COMPEL)*, June 2018.

[5] T. Urkin, G. Sovik, E. E. Masandilov, M. M. Peretz, "Digital Lock-In Controller IC for Optimized Operation of Resonant SCC", *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)* -In review process.

[6] G. Sovik, T. Urkin, E. E. Masandilov, M. M. Peretz, "Optimal Self-Tuning Control for Google Data-Centers' 48V-12V ZCS-STC", *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)* – In review process.

[7] R. W. Erickson and D. Maksimović, Fundamentals of Power Electronics, 2nd ed. Norwell, MA: Kluwer, 2001.

[8] M. Rashid, Power electronics: circuits, devices & applications, New Jersey, Prentice-hall, 1993.

[9] N. Mohan, T. M. Undeland, and W. P. Robbins, Power electronics, New Jersey, Wiley, 2003.

[10] D. W. Hart, Power electronics, New York, McGraw-Hill, 2011.

[11] S. Maniktala, Switching power supplies a-z, Oxford UK, Elsevier Ltd., 2012.

[12] M. S. Makowski and D. Maksimović, "Performance limits of switched-capacitor DC-DC converters," in Proc. IEEE Power Electron. Spec. Conf., 1995, vol. 2, pp. 1215–1221.

[13] S. V. Cheong, S. H. Chung, and A. Ioinovici, "Inductorless dc-to-dc converter with high power density," IEEE Trans. Ind. Electron., vol. 41, no. 2, pp. 208–215, Apr. 1994.

[14] M. D. Seeman, S. R. Sanders, "Analysis and optimization of switched capacitor DC-DC converters," IEEE Transactions on Power Electronics, Vol. 23, No. 2, pp. 841-851, March 2008.

[15] J. M. Henry and J. W. Kimball, "Practical performance analysis of complex switched-capacitor converters," IEEE Trans. Power Electron., vol. 26, no. 1, pp. 127–136, Jan. 2011.

[16] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "Resonant switched capacitor converters for sub-module distributed photovoltaic power management," IEEE Trans. Power Electron., vol. 28, no. 3, pp. 1189–1198.

[17] J. T. Stauth, M. D. Seeman, and K. Kesarwani, "A high-voltage CMOS IC and embedded system for distributed photovoltaic energy optimization with over 99% effective conversion efficiency and below 0.1% insertion loss," in Proc. Int. Solid-State Circuits Conf., 2012, pp. 100–102. Mar. 2013.

[18] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant switched capacitor converters for chip scale power delivery: Modeling and design," in Proc. vIEEE Control Modeling Power Electron., Jun. 2013, pp. 1–7.

[19] D. Maksimovic and R. Zane. "Small-signal discrete-time modeling of digitally controlled PWM converters." IEEE Trans. On Power Electron, vol. 22, no. 6, pages 2552–2556, Nov. 2007.

[20] W. W. Burns and T. G. Wilson, "A State trajectories used to observe and control DC-to-DC converter," IEEE Trans. Aerosp. Electron. Syst., vol. 12, no. 6, pp. 706–717, Nov. 1976.

[21] W. W. Burns and T. G. Wilson, "Analytic derivation and evaluation of a state trajectory control law for dc-to-dc converters," in Proc. Power Electron. Spec. Conf., pp. 70–85, 1977.

[22] J. J. E. Slotine and W. Li, Applied Nonlinear Control. Englewood Cliffs, NJ, Prentice-Hall, 1991.

[23] Voltage regulator module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0, Intel Corp., Hillsboro, OR, USA, Sep. 2009.

[24] N. H. Mcclamroch and I. Kolmanovsky, "Performance benefits of hybrid control design for linear and nonlinear systems," IEEE Proceedings vol. 88, no. 7, pp. 1083–1096, 2000.

[25] A. Babazadeh and D. Maksimović, “Hybrid digital adaptive control for fast transient response in synchronous buck DC–DC converters,” IEEE Trans. Power Electron., vol. 24, no. 11, pp. 2625-2638, Nov. 2009.
[26] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, “Parameter-independent time-optimal digital control for point-of-load converters,” IEEE Trans. Power Electron., vol. 24, no. 10, pp. 2235-2248, Oct. 2009.
[27] A. Babazadeh, L. Corradini, and D. Maksimović, “Near time-optimal transient response in DC-DC buck converters taking into account the inductor current limit,” in Proc. IEEE Energy Convers. Conf. Expo. (ECCE), Sep. 2009, pp. 3328-3335.
[28] V. Yousefzedah, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimović, “Proximate time-optimal control for synchronous buck DC–DC converters,” IEEE Trans. Power Electron., vol. 23, no. 4, pp. 2018-2026, Jul. 2008.
[29] L. Corradini, A. Babazadeh, A. Bjeletić, and D. Maksimović, “Current-limited time-optimal response in digitally controlled dc–dc converters,” IEEE Trans. Power Electron., vol. 25, no. 11, pp. 2869-2880, Nov. 2010.
[30] G. E. Pitel, and P. T. Krein, “Minimum-Time transient recovery for DC–DC converters using raster control surfaces,” IEEE Trans. Power Electron., vol. 24, no. 12, pp. 2692-2703, Dec. 2009.
[31] G. Wei and M. Horowitz, “A low power switching power supply for self-clocked systems,” in Proc. Int. Symp. Low Power Electron. Design, ISLPED, pp. 313–317, 1996.
[32] F. Sluijs, K. Hart, W. Groeneveld, and S. Haag, “Integrated DC/DC converter with digital controller,” in Proc. Int. Symp. Low Power Electron. Design, ISLPED, pp. 88–90, 1998.
[33] A. P. Dancy and A. P. Chandrakasan, “Ultra low power control circuits for PWM converters,” in Proc. IEEE PESC Conf., pp. 21–28, 1997.
[34] A. P. Dancy, R. Amirtharajah, and A. P. Chandrakasan, “High-efficiency multiple-output DC–DC conversion for low-voltage systems,” IEEE Trans. VLSI Syst., vol. 8, pp. 252–263, June 2000.
[35] A. Abumurad and K. Choi, "Increasing the ADC precision with oversampling in a flash ADC," 2012 IEEE 11th International Conference on Solid-State and Integrated Circuit Technology, Xi'an, 2012, pp. 1-4.
[36] T. M. Ignatius, J. K. Antony and S. R. Mary, "Implementation of high performance dynamic flash ADC," 2014 Annual International Conference on Emerging Research Areas: Magnetics, Machines and Drives , Kottayam, 2014, pp. 1-5.
[37] O. Erdinc, B. Vural and M. Uzunoglu, "A dynamic lithium-ion battery model considering the effects of temperature and capacity fading," *International Conference on Clean Electrical Power*, Capri, 2009, pp. 383-386.
[38] B. Sahu and G.A. Rincon-Mora, “A low voltage, dynamic, non-inverting, synchronous buck-boost converter for portable application,” *IEEE Transactions on Power Electronics*, vol. 19, pp.443-452, 2004.
[39] C. Yao, X. Ruan, W. Cao and P. Chen, "A Two-Mode Control Scheme With Input Voltage Feed-Forward for the Two-Switch Buck-Boost DC–DC Converter," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 2037-2048, April 2014.
[40] C. H. Tsai, Y. S. Tsai and H. C. Liu, "A Stable Mode-Transition Technique for a Digitally Controlled Non-Inverting Buck–Boost DC–DC Converter," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 1, pp. 475-483, Jan. 2015.
[41] J. Ma, M. Zhu, X. Li and X. Cai, "Bumpless transfer of non-inverting buck boost converter among multiple working modes," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 1909-1914.
[42] S. M. Ahsanuzzaman, J. Blackman, M. M. Peretz and A. Prodić, "Power management architecture for universal input Ac-Dc adapter support in battery powered applications," *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, 2013, pp. 1-9.
[43] A. Babazadeh and D. Maksimovic, "Hybrid Digital Adaptive Control for Fast Transient Response in Synchronous Buck DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2625-2638, Nov. 2009.

[44] A. Babazadeh, L. Corradini and D. Maksimovic, "Near time-optimal transient response in DC-DC buck converters taking into account the inductor current limit," *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, 2009, pp. 3328-3335.

[45] Y. Zhang, I. Radović, S.M, Ahsanuzzaman, A. Prodić, G. Calabrese, G. Frattini, M. Granato ., "Low-frequency ripple-shaping controller for operation of non-inverting buck-boost converters near step-up step-down boundary," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 292-297.

[46] N. Zhang, S. Batternally, K. C. Lim, K. W. See and F. Han, "Analysis of the non-inverting buck-boost converter with four-mode control method," *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, 2017, pp. 876-881.

[47] J. Ma, M. Zhu, Guanghui Li, Xiuyi Li and X. Cai, "Concept of unified mode control for non-inverting Buck-Boost converter," *2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia (IFEEC 2017 - ECCE Asia)*, Kaohsiung, 2017, pp. 1235-1240.

[48] M. M. Peretz, B. Mahdavikhah and A. Prodić, "Hardware-Efficient Programmable-Deviation Controller for Indirect Energy Transfer DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3376-3388, June 2015.

[49] G. G. Oggier, M. Ordonez, J. M. Galvez and F. Luchino, "Fast Transient Boundary Control and Steady-State Operation of the Dual Active Bridge Converter Using the Natural Switching Surface," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 946-957, Feb. 2014..

[50] V. Yousefzadeh, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao and D. Maksimovic, "Proximate Time-Optimal Digital Control for Synchronous Buck DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 2018-2026, July 2008.

[51] O. Kirshenboim and M. M. Peretz, "Fast Response of Deviation-Constrained Hybrid Controllers for Indirect Energy Transfer Converters," in *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 2615-2629, March 2018.

[52] J. Ma, M. Zhu, G. He and X. Cai, "Breaking performance limit of asynchronous control for non-inverting buck boost converter," *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, 2017, pp. 928-933.

[53] D. C. Jones and R. W. Erickson, "Buck-Boost Converter Efficiency Maximization via a Nonlinear Digital Control Mapping for Adaptive Effective Switching Frequency," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 3, pp. 153-165, Sept. 2013.

[54] X. Hu and P. K. T. Mok, "Analysis and design of three-state controlled transition mode for a buck-boost converter with efficiency and stability enhancement," *2013 IEEE International Symposium on Circuits and Systems (ISCAS2013)*, Beijing, 2013, pp. 697-700.

[55] E. Abramov, T. Vekslender, O. Kirshenboim and M. M. Peretz, "Fully Integrated Digital Average Current-Mode Control Voltage Regulator Module IC," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 485-499, June 2018.

[56] T. Vekslender, E. Abramov, O. Kirshenboim and M. M. Peretz, "Hardware efficient digital auto-tuning average current-mode controller," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-8.

[57] C. Fang and R. Redl, "Subharmonic Instability Limits for the Peak-Current-Controlled Boost, Buck–Boost, Flyback, and SEPIC Converters With Closed Voltage Feedback Loop," in *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 4048-4055, May 2017.

[58] O. Kirshenboim and M. M. Peretz, "Stability Analysis of Boundary and Hybrid Controllers for Indirect Energy Transfer Converters," in *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3360-3371, April 2016.

[59] T. Ritoniemi, T. Karema, and H. Tenhunen, “Design of stable high order 1-bit Sigma-Delta modulators,” in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1990, vol. 4, pp. 3267–3270.

[60] A. P. Dancy and A. P. Chandrakasan, “Ultra low power control circuits for PWM converters,” *in Proc. IEEE PESC Conf.*, 1997, pp. 21–28.

[61] P. M. Aziz, H. V. Sorensen, J. V. D. Spiegel, “An Overview of Sigma-Delta Converters,” *IEEE Signal Processing Magazine*, vol. 13, pp. 61-84, 1996

[62] T. Ritoniemi, E. Pajarre, S. Ingalsuo, T. Husu, V. Eerola, T. Saramiki, “A Stereo Audio Sigma-Delta A/D Converter”, *IEEE Journal of Solid State Circuits", vol. 20, pp. 1514-1523, 1994.*

[63] Y.Qiu, J. Sun, M. Xu,K. Lee, and F.C. Lee, “Bandwidth improvements for peak-current controlled voltage regulators,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1253–1260, Jul. 2007.

[64] Y. Panvo and M. M. Jovanović, “Design consideration for 12-V/1.5-V, 50-A voltage regulator modules,” *IEEE Trans. Power Electron*., vol. 16, no. 6, pp. 776–783, Nov. 2001.

[65] E. Abramov, T. Vekslender, O. kirshenboim and M. M. Peretz, “Fully-integrated digital average current-mode control 12V-to-1.xV voltage regulator module IC,” *IEEE Journal of Emerging and Selected Topics in Power Electron.* - Early Access, 2017.

[66] J. Chen, A. Prodić, R. W. Erickson, and D. Maksimović, “Predictive digital current programmed control,” *IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 411–419, Jan. 2003.

[67] H. Peng and D. Maksimović, “Digital current-mode controller for DC-DC converters,” in *Proc. IEEE Appl. Power Electron. Conf. Expo*. (*APEC*), pp. 899–905, 2005.

[68] M. Ilic, D. Maksimović, “Digital average current-mode controller for dc–dc converters in physical vapor deposition applications”, *IEEE Trans. Power Electron*., vol. 23, no. 3 pp. 1426-1436, Mar. 2008.

[69] B. J. Patella, A. Prodić, A. Zirger, and D. Maksimović, “High-frequency digital PWM controller IC for DC-DC converters,” *IEEE Trans. On Power Electronics,* Vol. 18, No. 1, Pm 11, Jan. 2003.

[70] T. B. Cho, P. R. Gray, “A 10b, 20 Msample/s, 35mW pipeline A/D converter,” *IEEE Journal of Solid-State Circuits,* vol. 30, pp. 166-172, 1995.

[71] Y. Zhu, C. Chan, U. Chio, S. Sin, S. U, R. Paulo, F. Maloberti, “A 10-bit 100MS/s reference free SAR ADC in 90 nm CMOS,” *IEEE Journal of Sold State Circuits,* vol. 45, pp. 1111-1121, 2010.

[72] J. M. de la Rosa, “Sigma-Delta modulators: tutorial overview, design guide, and state-of-the-art survey,” *IEEE Transcriptions on Circuits and Systems,* vol. 58, pp. 1-21, 2011.

[73] R. T. Baird, T. S. Fiez, “14-bit 500 kHz delta-sigma ADC with 16 times oversampling,” *IEEE Custom Integrated Circuits Conference,* May, 1995.

[74] A. Iwata, “The architecture of delta sigma analog-to-digital converters using a VCO as a multibit quantizer,” *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 8, pp. 941–945, Aug. 1999.

[75] M. Z. Straayer et al., “A 12-Bit, 10-MHz bandwidth, continuous-time ADC with a 5-bit, 950-MS/s VCO-based quantizer,” *IEEE J. Solid-State Circuits,* vol. 43, pp. 805-814, Apr. 2008.

[76] Z. Zhao, A. Prodić, and P. Mattavelli, “Self-Programmable PID compensator for digitally controlled SMPS,” *IEEE Workshop on Computers in Power Electronics*, pp. 112-116, 2006.

[77] R. Paul, L. Corradini, D. Maksimovic, “Adaptive non-inverting buck-boost IC with on-chip sigma-delta ADC for portable applications*,” IEEE Workshop on Control and Modeling for Power Electronics (COMPEL),* June 2010.

[78] R. B. Ridley, “A new continuous –time model for current-mode control [power converters],” *IEEE Transcripts on Power Electronics,* vol. 25, pp. 2903-2912, 2010.

[79] G. Li, Y. M. Tousi, A. Hassibi, and E. Afshari, “Delay-line-based analogto-digital converters,” *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 56, no. 6, pp. 464–468, Jun. 2009.

[80] A. Radic, S. Ahsanuzzaman, A. Parayandeh, A. Prodic, “Analog-to-digital converter for input voltage measurements in low-power digitally controlled switch-mode power supply converters,” *Power Electronics and Applications*, pp. 1-8, 2011.

[81] Z. Lukic, N. Rahman, and A. Prodic, “Multibit Σ–Δ PWM digital controller IC for DC–DC converters operating at switching frequencies beyond 10 MHz*,” IEEE Trans. Power Electron*., vol. 22, no. 5, pp. 1693– 1707, Sep. 2007.

[82] M. Maymandi-Nejad and M. Sachdev, “A monotonic digitally controlled delay element,” *IEEE J. Solid-State Circuits*, vol. 40, pp. 2212–2219, Nov. 2005.

[83] M. D. Seeman and S. R. Sanders, "Analysis and Optimization of Switched-Capacitor DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841-851, March 2008.

[84] M. N. Gitau and C. L. Kala-Konga, "Multilevel switched-capacitor DC-DC converter with reduced capacitor bank," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Glendale, AZ, 2010, pp. 576-581.

[85] H. Le, S. R. Sanders and E. Alon, "Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters," in *IEEE Journal of Solid-State Circuits*, vol. 46, no. 9, pp. 2120-2131, Sept. 2011.

[86] F. Zhang, L. Du, F. Z. Peng and Z. Qian, "A New Design Method for High-Power High-Efficiency Switched-Capacitor DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 832-840, March 2008.

[87] S. R. Sanders, E. Alon, H. Le, M. D. Seeman, M. John and V. W. Ng, "The Road to Fully Integrated DC–DC Conversion via the Switched-Capacitor Approach," in *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4146-4155, Sept. 2013.

[88] C. Cheung, S. Tan, C. K. Tse and A. Ioinovici, "On Energy Efficiency of Switched-Capacitor Converters," in *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 862-876, Feb. 2013.

[89] Y. Lee, H. Huang and T. Chou, "Bidirectional DC-DC converter with multiple switched-capacitor cells," *2014 International Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE ASIA)*, Hiroshima, 2014, pp. 421-428.

[90] D. Cao and F. Z. Peng, "Zero-Current-Switching Multilevel Modular Switched-Capacitor DC–DC Converter," in *IEEE Transactions on Industry Applications*, vol. 46, no. 6, pp. 2536-2544, Nov.-Dec. 2010.

[91] D. Cao and F. Z. Peng, "A family of zero current switching switched-capacitor dc-dc converters," *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Palm Springs, CA, 2010, pp. 1365-1372.

[92] R. C. N. Pilawa-Podgurski, D. M. Giuliano and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 4008-4015.

[93] E. Frachtenberg, "Holistic Datacenter Design in the Open Compute Project," in *Computer*, vol. 45, no. 7, pp. 83-85, July 2012.

[94] O. Jong, Q. Li and F. C. Lee, "Resonant Switched-Capacitor Converter with Multi-Resonant Frequencies," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 2177-2184.

[95] H. Setiadi and H. Fujita, "Control and Performance of New Asymmetrical Operation for Switched-Capacitor-based Resonant Converters," *2018 International Power Electronics Conference (IPEC-Niigata 2018 -ECCE Asia)*, Niigata, 2018, pp. 626-631.

[96] S. Jiang, C. Nan, X. Li, C. Chung and M. Yazdani, "Switched tank converters," *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 81-90.

[97] Y. Li, X. Lyu, D. Cao, S. Jiang and C. Nan, "A 98.55% Efficiency Switched-Tank Converter for Data Center Application," in *IEEE Transactions on Industry Applications*, vol. 54, no. 6, pp. 6205-6222, Nov.-Dec. 2018.

[98] Infineon (2019, April) “Powering next generation datacenters: Infineon’s 48V high-efficiency, two-stage architecture power distribution” [Online].

[99] S. Li, W. Xie and K. M. Smedley, "A Family of an Automatic Interleaved Dickson Switched-Capacitor Converter and Its ZVS Resonant Configuration," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 255-264, Jan. 2019.

[100] A. Penczek, A. Mondzik, Z. Waradzyn, R. Stala, A. Skała and S. Piróg, "Switching strategies of a resonant switched-capacitor voltage multiplier," *2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe)*, Warsaw, 2017, pp. P.1-P.10.

[101] Zhe Zhang and S. Cuk, "A high efficiency 500 W step-up Cuk converter," *Proceedings IPEMC 2000. Third International Power Electronics and Motion Control Conference (IEEE Cat. No.00EX435)*, Beijing, China, 2000, pp. 909-914 vol.2.

[102] K. W. E. Cheng, "New generation of switched capacitor converters," *PESC 98 Record. 29th Annual IEEE Power Electronics Specialists Conference (Cat. No.98CH36196)*, Fukuoka, 1998, pp. 1529-1535 vol.2.

[103] A. Cervera and M. M. Peretz, "A Family of Switched-Resonant Converters With Wide Conversion Ratio and Controlled Sourcing Features for Volume-Sensitive Applications," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 910-921, June 2019.

[104] E. Hamo, A. Cervera and M. M. Peretz, "Multiple Conversion Ratio Resonant Switched-Capacitor Converter With Active Zero Current Detection," in IEEE Transactions on Power Electronics, vol. 30, no. 4, pp. 2073-2083, April 2015.

[105] H. Wu, C. Wei, Y. Hsu and R. B. Darling, "Adaptive Peak-Inductor-Current-Controlled PFM Boost Converter With a Near-Threshold Startup Voltage and High Efficiency," in *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1956-1965, April 2015.

[106] B. Sahu and G. A. Rincon-Mora, "An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive On-Time Pulse-Frequency Modulation (PFM) Control," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 2, pp. 312-321, Feb. 2007.

[107] A. Cervera and M. M. Peretz, "Digital self-tuning controller for ZCS resonant converters operating in the 10MHz-range," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-7.

[108] A. V. Peterchev, Jinwen Xiao and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," in *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 356-364, Jan. 2003.

[109] Hao Peng, D. Maksimovic, A. Prodic and E. Alarcon, "Modeling of quantization effects in digitally controlled DC-DC converters," *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, Aachen, Germany, 2004, pp. 4312-4318 Vol.6.

[110] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," *PESC97. Record 28th Annual IEEE Power Electronics Specialists Conference. Formerly Power Conditioning Specialists Conference 1970-71. Power Processing and Electronic Specialists Conference 1972*, Saint Louis, MO, USA, 1997, pp. 21-27 vol.1.

[111] L. Balogh, “Fundamentals of MOSFET and IGBT Gate Driver Circuits”, *Texas Instruments Application report*, Oct. 2018.

[112] J. Knobloch, J. Martis, R. Cipin and Z. Nouman, "Test stand for obtaining power transistors switching characteristics during aging," *2017 IEEE International Conference on Environment and Electrical Engineering and 2017 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, Milan, 2017, pp. 1-5.

[113] Pit-Leong Wong and F. C. Lee, "Switching action delays in voltage regulator modules," *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335)*, Dallas, TX, USA, 2002, pp. 675-678 vol.2.