BEN-GURION UNIVERSITY OF THE NEGEV

FACULTY OF ENGINEERING SCIENCES

DEPARTMENT OF ELECTRICAL ENGINEERING

STATE-SPACE ORIENTED ADVANCED ANALYSIS AND CONTROL METHODS OF SWITCHING CONVERTERS

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE MSc. DEGREE

By: Yara Halihal

Supervised by:

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January 2015

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January 2015

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תקציר

העבודה המוצגת נכנסת תחת התחום של ממירים אלקטרוניים לעיבוד אנרגיה חשמלית, כאשר המרכיב העיקרי הוא הממיר הממותג אשר לתוכו נכנס חשמל ברמה אחת ויוצא ממנו חשמל ברמה אחרת או/ו בצורה אחרת, והכל כפונקציה של מרכיבי הממיר והבקרה. את הקטגוריה של ממירים ממותגים ניתן בין היתר לחלק לשני סוגים, כאלו בהם מעבר האנרגיה מהכניסה למוצא הוא ישיר וכאלו שלא. האנליזה והפיתוחים בעבודה מתייחסים לשלושת הטופולוגיות המרכזיות של ממירי DC-DC. הראשונה היא ממיר באק, אשר מוריד מתח, ממיר בוסט אשר מעלה מתח, ובאק בוסט שביכולתו גם להעלות וגם להוריד מתח.

עד כה, נהוג היה לבקר ממירים בשיטות של יצירת מערכת משוב אשר מבוססת על פונקציית תמסורת לאות קטן של הממיר. מאחר ותהליך זה מבוסס על אנליזה במישור התדר, התוצר הסופי היה מערכת עם רוחב סרט מוגדר. המגבלה של מערכת בעלת רוחב סרט סופי היא בכך שהמערכת מיועדת לתקן שינויים שקורים בתחום הפעולה של רוחב הסרט של המערכת, כתוצאה מכך, חלק מהתכונות אליהן ניתן להגיע באמצעות ממירים ממותגים אינן מנוצלות.

באופן עקרוני, במצב עבודה יציב, בחירת הרכיבים נקבעת לפי עוצמת האדווה ביציאה. טענה זו איננה מתאימה למערכות מודרניות מכיוון שבחירת גודל הרכיבים נקבעת לפי מצב המעבר הגרוע ביותר. עקב כך, גודל האלמנטים הריאקטיביים, הסליל והקבל, המהווה את עקב האכילס מבחינת נפח הממיר, הוא גדול בהרבה, זאת מאחר ועליהם לספק את האנרגיה ברגע הראשון במצב המעבר עד שהמערכת מספיקה להגיב במגבלות רוחב הסרט שלה. מאחר שמערכת הבקרה לא מתוכננת לעמוד בשינויים גדולים, המשמעות היא שהשטח הכללי במערכות אלקטרוניות, במיוחד במערכות ניידות, מאוכלס רובו בספקי כוח בגלל גודלם הפיזי הגדול של הקבלים והסלילים.
על מנת להתנתק מהקשר לרוחב הסרט, ניתן לפנות לשיטות בקרה המיועדות לטפל במצבי המעבר. שיטת בקרה מוכרת שהוצגה נקראת time-optimal, מטרתה היא להחזיר את המערכת למצב יציב במינימום זמן, מתוך ההנחה שמינימום זמן יביא גם למינימום נפילת מתח, ומתוך כך, גודל הרכיבים יהיה הקטן ביותר. הטענה הזו התבררה כנכונה רק למקרים בהם מדובר בממירים מסוג העברת אנרגיה ישירה כדוגמת ממיר הבאק. כאשר מדברים על ממירים בהם העברת האנרגיה איננה ישירה, כדוגמת בוסט ובאק-בוסט, מינימום זמן התאוששות לא מביא עמו מינימום נפילת מתח ומסתבר שהמתח אף נופל יתר על המידה. העבודה המוצגת מיוחסת לשיטה שמטרתה להביא למינימום נפילות מתח ושינויי זרם מתוך ההצדקה שהיא תביא למימדים הקטנים ביותר של הרכיבים. השיטה נקראת minimum-deviation control.

ניתוח במרחב המצב מתייחס לאפיון המערכת, הדינמיקה של מהמערכת בעזרת מסלולים המתוארים על המרחב כאשר הקואורדינטות הן משתני המצב. על ידי כך מקבלים התנתקות ממישור הזמן וכך ניתן לבחון את משתני המצב על המערכת. זוהי דרך נוספת פשוטה וישימה יותר לבחינת התנהגות המערכת תחת תנאי עבודה שונים גם למצב יציב וגם לטראנזיאנט, ובנוסף מאפשרת לחקור כיצד המערכת תתנהג תחת אסטרטגיות בקרה שונות. מרחב המצב הינו אופציה טובה לוויזואליזציה של מאפייני המערכת, נוכל לבחון את זרם הסליל בכל נקודה ונקודה ביחס למתח הקבל על כל נקודה ונקודה.

מתוך המרחב הגאומטרי חולצה האינפורמציה אשר בעזרתה ניתן היה לבטא את נקודת השינוי המינימאלי באופן אנליטי. תכנון הבקר ממורכז מסביב לסטיית המתח המקסימלית האפשרית המתוכנתת מראש, שנקבעת בהתבסס על מגבלת תדר המיתוג. הניתוח נעשה גם למקרה של עומס זרם קבוע, וגם למקרה של עומס התנגדותי.

מעבר לניתוח האיכותי, הגרפי של שיטת ה- Minimum-deviation הוכחו הקיום והיציבות של השיטה. מאחר ומדובר בבקרה לא לינארית, שיטות ניתוח לינאריות המבוססות על ניתוח מודל ממוצע לאות קטן לא מספיקות ולכן האנליזה מבוססת על מודל דיסקרטי לאות גדול.

לבסוף, על סמך הניתוח והפיתוחים התאורטיים, נבנה מערך ניסוי של ממיר בוסט המבוסס על בקרה דיגיטאלית מבוססת FPGA. הבקר שנבנה משלב בתוכו בקרה לינארית (PI) לפרקי הזמן בהם המערכת נמצאת במצב יציב, ובקרת טרנזיאנט (minimum-deviation) המטפלת במצבי המעבר.

בעבודה מוצגות תוצאות אשר משוות בין העבודה של בקר ה- PI –ו- time-optimal לעומת ה- minimum-deviation. ניתן לראות כי נפילת המתח ב- time-optimal היא כ- 13% ממתח היציאה לעומת minimum-deviation בה הנפילה היא של רק כ- 4% בלבד, מה שמעיד על חיסכון משמעותי במימדי המערכת והאנרגיה אשר תסתובב במערכת.

נסכם את מטרות המחקר בקצרה:

(1) ייצור הבסיס התאורטי לתכנון של שיטות בקרה יעילות לממירים ממותגים מבוסס על מרחב מצב.

(2) תיאור של שיטת בקרה חדשה בשם minimum-deviation בעזרת כלים של מרחב המצב.

(3) הוכחת קיום ויציבות של השיטה באמצעות תאוריות בקרה מתקדמות וכלים של מרחב המצב.

פורסם מאמר הנוגע בתכנון ויישום בקרת PI מבוססת FPGA ב- "IEEE Control and Modeling for Power Electronics (COMPEL) 2014" [15]. בנוסף, מאמר מלא העוסק במציאת נקודת המינימום לטופולוגיות הממיר המרכזיות, הוכחת יציבות לבקרה הלא לינארית המדוברת ויישום של שיטת הבקרה על ממיר בוסט המבוסס על הבקר ההיברידי (PI + Minimum-deviation), ישלח לעיתון.

Abstract

The field of power electronics deals with energy processing by electronic circuits. The fundamental building block is the switch-mode converter, which receives electrical power in one form at its input terminals and produces electrical power in another form at its output terminals, all governed by the control. The main function of the switch-mode power supply (SPMS) is to deliver regulated energy from a power source, to a load with high efficiency, while maintaining the load requirements, such as voltage level, output voltage deviation, and response time.

Following the recent proliferation of portable electronics and the rise in popularity of alternative energy sources, there has been a sharp increase in the demand for more compact, lighter, more energy efficient, and more economical power sources [1]-[3]. As this trend continues, the requirements are becoming more and more challenging. Tighter output voltage regulation, a faster response time to load and/or input voltage changes and a lower volume – these are the major concerns in the design of present-day SMPSs – and they are creating a 'bottle-neck' in the advancement of the technology. The limitations stem primarily from the present lack of both advanced design methods for SMPSs, and current control methods that are specifically oriented toward *load and line transient* requirements.

The physical size and volume of the switch-mode converter are directly proportional to the allowed stress and voltage deviations of the components [4]-[8]. Current design methods for SMPSs are based on a closed-loop operation in the steady state. Sizing of the components is based on worst-case transient response conditions, taking into account that the system bandwidth is not wide enough to accommodate the initial (fast) change of output voltage [5]-[14]. Consequently, the output filter is rated to absorb the 'instantaneous' change of energy and is therefore overly sized. A generic design method orientated toward the transient response is still lacking.

Currently, where a fast response and a cost-effective implementation are of key importance, analog linear controllers are mainly used [9]-[12]. However, following the rapid advancement of digital technology, the integration of digital controllers in switch-mode power applications has become a viable alternative. The main limitation of all of the designs that are based on linear small-signal compensators, regardless of the extraction method, is that the system response is still bounded by the bandwidth of the design, which is constrained

by other static and dynamic requirements, such as the steady-state error and stability. Moreover, the primary design objective of the compensators is to minimize the error between the value of the current output voltage and the desired reference value. This implies that any change in the loading conditions, or in the input voltage, will only be corrected after it has already affected the output voltage. These limitations have motivated the use of nonlinear compensation schemes that can be designed to respond more rapidly to load or line variations and are not bounded by the bandwidth of the system, which is regulated by the linear small-signal compensator. An example for such advanced nonlinear control methods is the time optimal control [46]-[55], which has demonstrated an ultimate improvement in the dynamic response for direct energy transfer converters. In this case, the time-optimal response always results in the minimum possible output voltage deviation and output capacitance value. However, for indirect energy transfer systems, this is not the case. Here, the time-optimal response often produces a larger-than-minimum output voltage deviation and causes extra current stress of the components. Furthermore, in this case, implementation is usually more hardware demanding than that for direct energy transfer converters. Therefore, for the case of an indirect energy transfer converter, an optimization of the switching sequence, based on the voltage drop and current stress, result in a more efficient transient response than that obtained with a time-optimal control, and a further reduction of the converter size can be obtained. Different converter configurations have been examined, using the state-space approach, in order to extract the relations between the state variables and the line and load conditions of each converter topology.

The proposed research program will cover a number of issues: an investigation of the limiting factors, with an aim at improving the transient response and the sizing of the resultant components; an understanding of the relationships between the signals in the time domain and the state-space; mapping the possible convergence contours of state variables in switching systems; and characterization of the practical limitations for the convergence of switching power systems. System stability will be explored and verified and then applied in the development of control strategies that will be implemented on digital platforms. All of the issues to be investigated will be examined theoretically and validated experimentally.

A paper on a FPGA-based design and implementation of a PWM/CPM controller has been published in the proceedings of the IEEE Control and Modeling for Power Electronics (COMPEL) Workshop 2014 [15]. Also, a full paper on a unified state trajectory approach, for minimum deviation transient recovery of PWM converters, including a stability analysis, is to be submitted.

Thesis Overview

This work addresses the present-day challenges in the advancement of switch-mode converters. The research investigates a new hybrid digital control method for DC-DC switching converters that consists of two (or more) smaller modules of linear and nonlinear control methods. The conceptual approach will be to set one module "in charge of" regulating the output voltage during steady-state operation, while the other is active during line and load transients and is "in charge of" recovering the output voltage to the steady-state value. By doing so, each module can be designed specifically for its own operation, the requirements of the output filter can be eased, and the overall size of the SMPS can potentially be reduced.

Additionally, a stability analysis is provided to approve the presented nonlinear control validity. A brief summary of the research and the main results is given next:

The work proposes an efficient non-linear control method named minimum-deviation control. It will be shown using a state-space plane approach and a large signal stability analysis, and that this generic control method and its derivations will be causing the system to converge with a minimum charge loss, and the minimum time possible, while satisfying the performance goals; i.e., to provide the optimal switching sequence that will result in the desired response of the system. Special attention will be paid to the state variables of the converter (inductor current and output voltage) in order to achieve an enhanced transient performance. A prototype that integrates the modular converter structures, with the required control schemes, was constructed for the purposed experimental validation and performance evaluation, in terms of transient response, component stress, and stability of the closed-loop system.

The results of the research lay the foundations to future research areas, along with design guidelines and experimental proof. The current proposal will establish a new operational methodology for SMPSs, which is based on large-signal controller design, rather than on the conventional linear small-signal operation.

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Firstly, I would like to thank my current supervisor, Dr. Mor Mordechai Peretz, who joined my thesis in the second year. Dr. Peretz exposed me to new and very interesting research ideas. In the time together, we had a very large amount of challenging work. His trust, engorgement, creative thinking, availability, and optimism, were refreshing and greatly inspired and enriched my growth as a student and researcher. His excellent guidance and support led me to absorb a great satisfaction from our work and accomplishments. For all these reasons, and more, I am grateful and glad to have him as my supervisor.

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I am lucky to have worked with each of my two supervisors, and I am indebted to them, more than they know.

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Acronyms and Abbreviations

PWM – Pulse-width modulation
SMPS – Switch-mode power supply
MOSFET– Metal oxide semiconductor field effect transistor
SCC – Switch-capacitor converter
CCM – Continuous conduction mode
DCM – Discontinuous conduction mode
FPGA– Field programmable gate array
SIC – Switched inductor converter
VLSI – very-large-scale integration
DSP – Digital signal processors
IC – Integrated circuit
VMC – Voltage mode control
CMC – Current mode control
PCMC – Peak current-mode control
ACM – Average mode control
SM – Sliding-mode
EMI – Electromagnetic- interference
ADC – Analog-to-digital control
CPM – Average mode control
VSS – Variable structure system
DL – Delay-line
HR – High-resolution
LUT – Lock-up tables

Inline References Legend

X.XX – Section / Chapter number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure
Equation Chapter (Next) Section 1

1. Introduction

1.1. Overview of power converters

1.1.1. Introduction to power converters

The amount of prevalent applications, such as dc-dc converters, energy harvesting systems, battery chargers, different power supply systems, and more, which are designed based on power electronics technology, is increasing. The power electronics field is concentrated on processing electrical power, which is the rate at which electrical energy is transferred by an electrical circuit using electronic devices [4], [16]-[17]. The power rating is between milliwatts, which is relevant to a mobile phone for example, to megawatts, in electrical power transmission systems. Electronic circuits that are associated with electrical power conversion and control are called power converters. With the exception of the most simple battery powered devices, all electronic equipment requires some sort of power conversion [19]. One of the most important practical properties is the reliability of the power converter. Hence, there is a high demand for robust electronic devices and control circuits.

As illustrated in Fig. 1.1, a power converter can be described as a network of electrical components that behaves as a linker, an adapter, a converter, or a transformer, between two or more sources, generally between a generator and a load. The basic elements are of two types; one is of nonlinear elements, mainly electronic switches, and the second is of linear reactive elements such as capacitors, inductors, or transformers. The linear reactive elements are used for intermediate energy storage, and also, for voltage and current filtering. They represent the Achilles heel of the power converter's size, weight, and cost point of view. The efficiency of a power converter is generally defined as the ratio between the output and input power (1.1). An ideal converter has 100% efficiency, meaning that no parasitic effects affect the converter operation [20].

$$\eta = \frac{P_{out}}{P_{in}} , \tag{1.1}$$

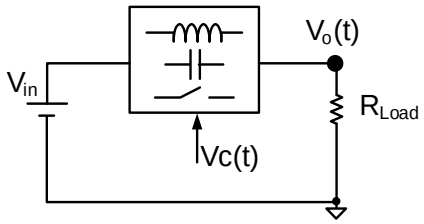


Fig.1.1. General description of a power converter.

1.1.2. Converter classification

Converters may be classified in several ways. Here, some common classification examples will be mentioned. The most common classification of power conversion is by the change of electrical energy type as a part of processing and controlling the flow of power, between the input and the output of the power converter. The change could be for example:

- From one voltage level to another voltage level (DC to DC), namely converter.
- From direct current (DC) to alternating current (AC), namely inverter.
- From alternating current (AC) to direct current (DC), namely rectifier.
- Transformer conversion (AC to AC).

In the presented research, the focus is on DC-DC conversion, which is needed in most systems.

Another sort of classification is stated by the ratio between the rates of the input signal and the output signal. If the converter accomplishes a ratio that is smaller than one, then the converter is referred to as a voltage step-down, or a current step-up. If it is bigger than one, it is well known as a voltage step-up, and if it is either bigger or smaller, it is known as a current-or-voltage step-up [4], [18].

One more classification that is relevant to this research is that of direct energy transfer converters and indirect energy transfer converters, which will be discussed later in this chapter.

1.1.3. DC-DC converters

There are two basic methodologies for accomplishing power conversion – linear and switch-mode regulation. Historically, the first one is the linear regulation (Fig. 1.2) which achieves its active voltage regulation characteristics by using one or more semiconductor devices (bipolar transistors or MOSFETs) operating in their linear region [19]. In a nutshell, linear regulators have a simple structure and operation, a low output noise, and very good regulation, especially with the integrated circuits that are available today. On the other hand, their efficiency is inversely proportional to the difference between the input and desired output voltage. The second methodology is the switch-mode power converters (SMPC),

which among all electronic converters, they considered to be the most common technology [21]. In this case, the voltage conversion is accomplished by switching one or more semiconductor devices between 'on' and 'off' states. Switch-mode converters are mostly known for their high efficiency. A good design can have an efficiency of 95% for example.

The fundamental switched dc-dc converter receives electrical power in one form or level at its input terminals, and converts it to electrical power in another form or level at its output terminals, by temporarily storing the input energy, and then releasing it to the output. Basically, its operation is based on switching a reactive element, which can be an inductor or capacitor or both, between the input and the output of the converter, charging and discharging, respectively. Using an inductor as the main reactive energy storage element is considered to be the most popular choice, since switched inductor converters (SICs) present a higher efficiency, a simpler design, lower costs, and a higher reliability, then those of the switched capacitor converters (SCC). Switched capacitor converters use the capacitor as their main energy storage element and have the advantage of a flexible circuit size reduction.

A power stage can operate in one of the two following states: a continuous current mode (CCM), where the inductor current never falls to zero, or a discontinuous current mode (DCM), where the inductor current falls to zero until the end of each cycle [22]. This work mostly focused on the continuous current mode of the converter operation.

SMPs are also sub-divided into resonant variable frequency topologies and Pulse Width Modulated (PWM) converter topologies. Here, the focus is on switched PWM converters.

It should be noted that although there are many known converter topologies, only the three most common switch-mode power converters, which are the buck, the boost, and the buck boost, are presented and explored in this work. Fig. 1.3 shows an example of a buck converter power stage schematic, where Q is an n-channel MOSFET switch, D represents the output diode, C is the output capacitor, L is the inductor, and Load represents the load seen by the power stage output.

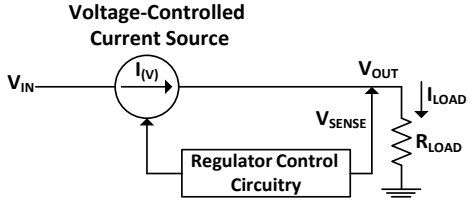


Fig.1.2. Linear regulator general scheme.

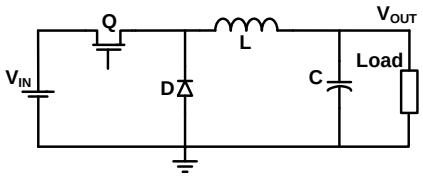


Fig.1.3. Buck converter power stage schematic.

1.1.4. Direct energy transfer topologies

As was mentioned earlier in this chapter, switch-mode converters are classified into direct energy transfer converters and indirect energy transfer converters. The direct conversion is achieved when the conversion is accomplished without an energy storage stage, meaning, the converter transfers energy directly from the input to the output (assuming power losses are negligibly small) during the on-time of the converter switch(s) [20]. Accordingly, ideally, the input power will be equal to the output power at any time. In this work, the examined direct energy transfer topology was the buck converter.

The buck configuration is a voltage step-down converter, meaning, it is used to reduce the input voltage to a lower voltage. The basic schematic and waveforms of the buck converter behavior are shown in Fig. 1.4. Its operation can be described by separating it into two stages, controlled by a switch that alternately connects and disconnects the input voltage to the inductor. In the first stage, the switch is turned on, and in the second stage, the switch is turned off. In the steady-state operation, during the on-time, the input source provides energy for the output as well as for the inductor. As a result, the inductor current rises from zero to the peak current with a slope of $\frac{Vin}{L}$; this current flows into both the load and the output capacitor. During this stage, the inductor stores energy that equals to $\frac{1}{2}LI_L^2$. The second stage starts when the switch is turned off; the input voltage applied to the inductor is now removed. During this stage, the inductor voltage reverses, hence, the inductor current flows through the load and back through the diode. Also, during this time, the output capacitor is discharging into the load. Therefore, the total load current during the off-time is the sum of the inductor and capacitor currents. After the inductor is completely discharged, the current stops flowing in all elements until a new cycle starts. The advantages of the buck converter are its simplicity and low cost. The disadvantages include a limited power range, and a DC path from the circuit's input to its output, when the switch is shorted [4], [18].

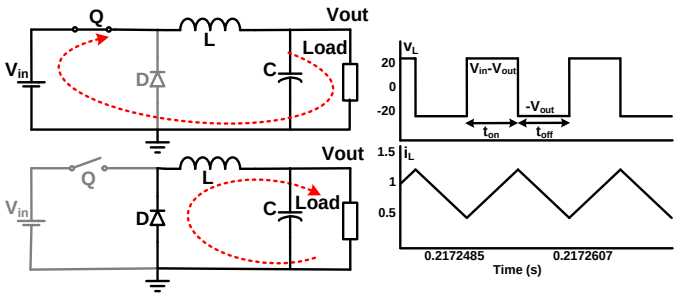


Fig.1.4. Buck converter scheme and waveforms.

1.1.5. Indirect energy transfer topologies

In contrast to the case of direct energy conversion, an indirect energy conversion in PWM converters uses one or more stages to store energy temporarily, causing the converter to accomplish the energy transfer, only during the off-state of the switching element(s) [19]. In this work, the focus is on two indirect converter topologies, which are the boost and the buck-boost converters.

The boost configuration, shown in Fig. 1.5, is a voltage step-up converter. During the switch on-time, the inductor is charged through the input source, and the load current is drawn from the output capacitor. As the switch element turns off, the inductor voltage reverses, and therefore, the energy stored in the inductor is released to the output load, thus causing the current to flow through the diode, which in turn isolates the load from the input. The advantages of the boost converter include its simplicity, the ability of increasing the voltage without the use of a transformer, and a low component count. On the other hand, due to the load current coming from the output capacitor, during the off-time, the boost converter suffers from a relatively high output ripple current.

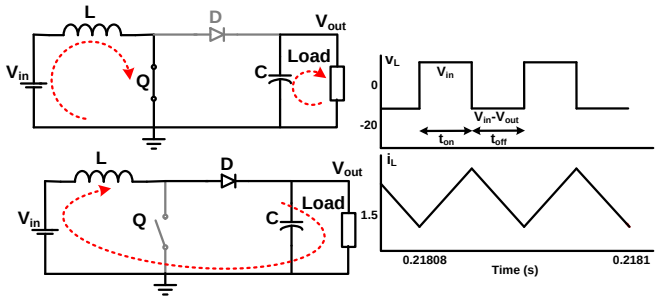


Fig.1.5. Boost converter scheme and waveforms.

The buck-boost configuration, as shown in Fig. 1.6, can either step-up or step-down the voltage. The traditional buck-boost topology output voltage is generated opposite in polarity to the input. In the on state, the diode prevents current from flowing to the load side, therefore, the inductor is charged through the directly connected input voltage source, and thus, the inductor current is increasing linearly. At this stage, the output load energy is supplied by the output capacitor. When the switch is off, the inductor will be disconnected from the input voltage supply, causing the inductor to discharge itself to the output capacitor and load via the diode. The higher the inductor current is at the end of the on-time period, the more voltage the inductor will need to provide in order to produce it. This means that the output voltage is adjustable, based on the duty-cycle of the switch.

The advantages include the ability for combining the functions of a step-up converter and a step-down converter. Another advantage is its simplicity, and low component count, which

results in lower costs and a higher efficiency of the system. Drawbacks include the need of a floating driver, because of the disconnection of any of the switch terminals to the ground. Another drawback is the need for a bigger input filter which is resulted by the pulsed input current.

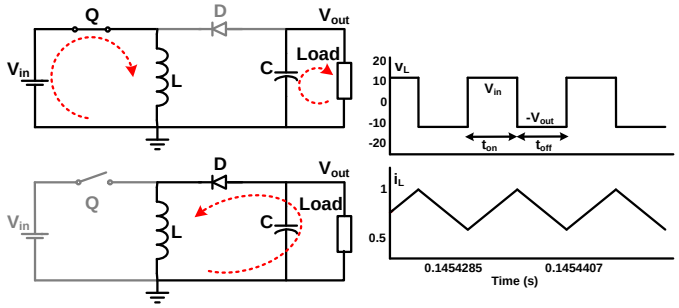


Fig.1.6. Buck-boost converter scheme and waveforms.

Each of the three presented topologies was explored for both the constant current load case and the resistive load case.

1.1.6. Constant current load representation

A constant current load, or a current step load, is a case where the load current is externally defined, regardless of the voltage upon it. Consequently, the delivered power will vary. The constant current load can be modeled with a current source as shown in Fig. 1.7 for an example of a boost converter.

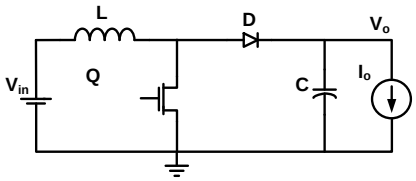


Fig.1.7. Constant current load boost converter circuit.

The analytical representation of a constant current load boost converter's behavior (state-equations) for each of the two switching states is presented below.

For the on-state:

$$(\mathrm{I})\ \frac{di_L}{dt}=\frac{V_{in}}{L}\ ;\ (\mathrm{II})\ \frac{dv_C}{dt}=-\frac{I_o}{C}, \tag{1.2}$$

For the off-state:

$$(\mathrm{I})\ \frac{di_L}{dt}=\frac{V_{in}-V_o}{L}\ ;\ (\mathrm{II})\ \frac{dv_C}{dt}=\frac{1}{C}(i_L-I_o), \tag{1.3}$$

The same process is also presented for the two other converters in Tables I and II.

1.1.7. Resistive load representation

A resistive load in an electrical circuit converts current into other forms of energy, such as heat. The load current varies linearly with the load resistance ($I_R = \frac{V_R}{R}$). Also, this linear relationship explains why the load current is proportional to the voltage across this load. The voltage drop, changing through time, in a corresponding manner as it appears across the output capacitor.

The analytical representation of a resistive load boost converter's behavior (state-equations) for each of the switching states is presented below.

For the on-state:

$$(\mathrm{I})\ \frac{di_L}{dt} = \frac{V_{in}}{L}\ ;\ (\mathrm{II})\ \frac{dv_C}{dt} = -\frac{v_C}{CR}, \tag{1.4}$$

For the off-state:

$$(\mathrm{I})\ \frac{di_L}{dt} = \frac{V_{in} - v_C}{L}\ ;\ (\mathrm{II})\ \frac{dv_C}{dt} = \frac{1}{C}\left(i_L - \frac{v_C}{R}\right), \tag{1.5}$$

The same is also presented for the two other converters in Tables I and II.

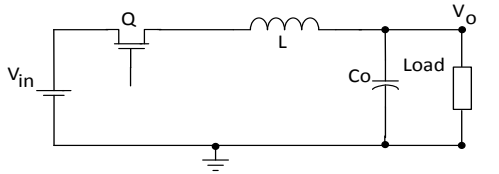
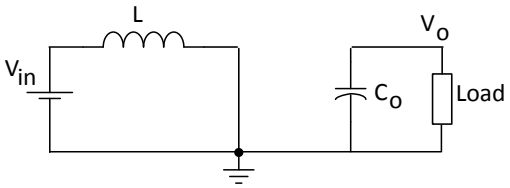
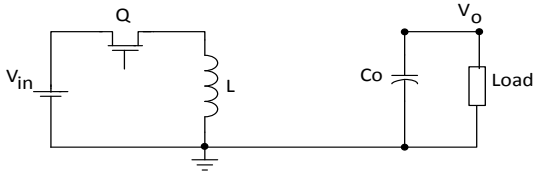
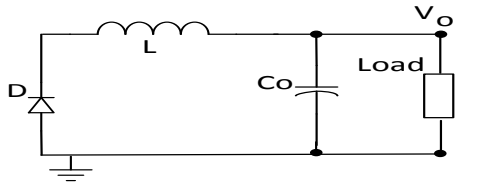
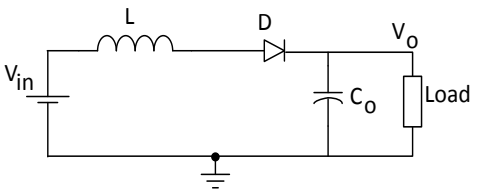
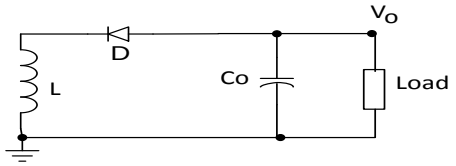
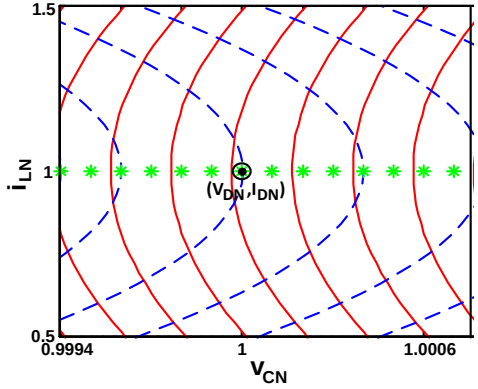
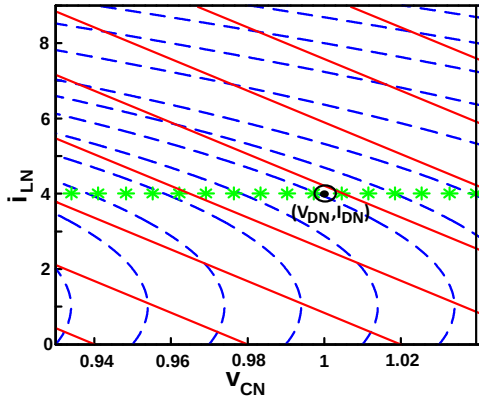
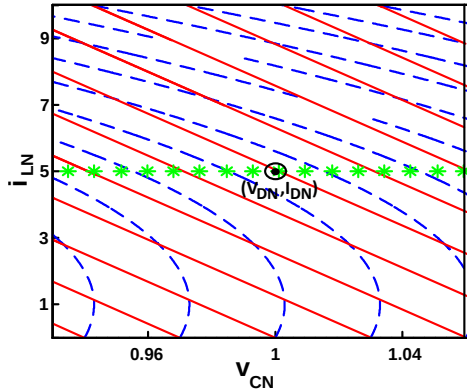
state			direct energy transfer		
Topology			Buck	Boost	Buck-boost
T_{on}	a	Equation	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}-V_{oN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{V_{oN}}{C_N R_N}\right)$ 	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=-\frac{V_{oN}}{C_N R_N}$ 	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=-\frac{V_{oN}}{C_N R_N}$ 
	b	Solution	$v_{CN}=-\frac{Z_{rN}^2}{2(V_{oN}-V_{inN})}(i_{LN}^2-i_{L0N}^2)+\frac{Z_{rN}^2 V_{oN}}{R_N(V_{oN}-V_{inN})}(i_{LN}-i_{L0N})+v_{C0N}$	$v_{CN}=-\frac{Z_{rN}^2 V_{oN}}{R_N V_{inN}}(i_{LN}-i_{L0N})+v_{C0N}$	$v_{CN}=-\frac{Z_{rN}^2 V_{oN}}{R_N V_{inN}}(i_{LN}-i_{L0N})+v_{C0N}$
T_{off}	c	Equation	$\frac{di_{LN}}{dt_N}=\frac{-V_{oN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{V_{oN}}{C_N R_N}\right)$ 	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}-V_{oN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{V_{oN}}{R_N}\right)$ 	$\frac{di_{LN}}{dt_N}=\frac{-V_{oN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{V_{oN}}{R_N}\right)$ 
	d	Solution	$v_{CN}=-\frac{Z_{rN}^2}{2V_{oN}}(i_{LN}^2-i_{L1N}^2)+\frac{Z_{rN}^2}{R_N}(i_{LN}-i_{L1N})+v_{C1}$	$v_{CN}=-\frac{Z_{rN}^2}{2(V_{oN}-V_{inN})}(i_{LN}^2-i_{L1N}^2)+\frac{V_{oN}Z_{rN}^2}{R_N(V_{oN}-V_{inN})}(i_{LN}-i_{L1N})+v_{C1N}$	$v_{CN}=-\frac{Z_{rN}^2}{2V_{oN}}(i_L^2-i_{L1}^2)+\frac{Z_{rN}^2}{R_N}(i_{LN}-i_{L1N})+v_{C1}$
	e	Graphical state-trajectory			

Table.I. State equations and solutions of trajectories in the i_{LN} vs. v_{CN} plane for the presented topologies in the case of constant current load.

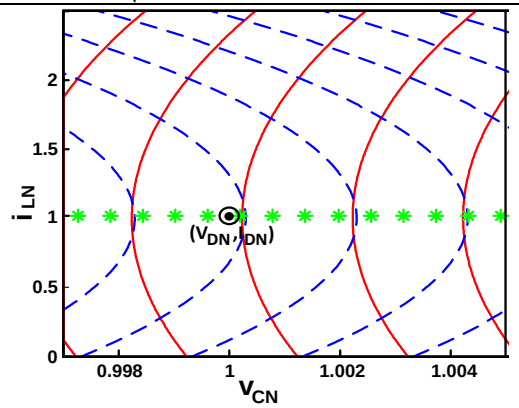
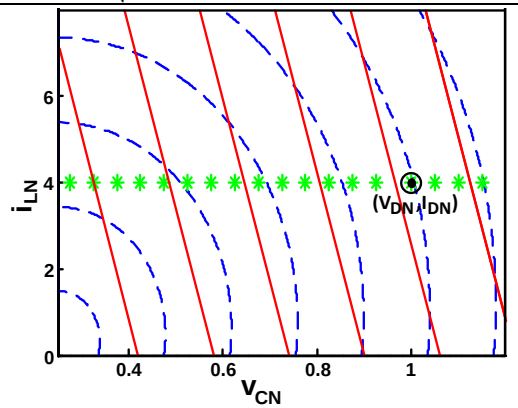
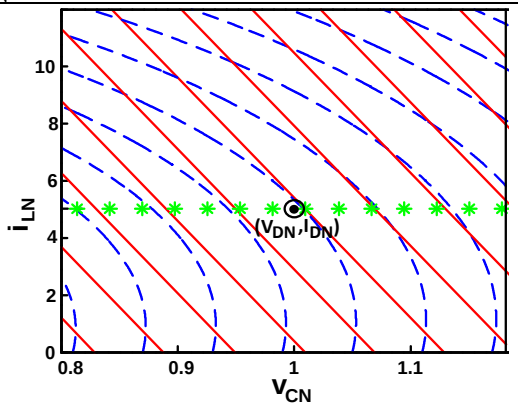
state			direct energy transfer	indirect energy transfer	
Topology			Buck	Boost	Buck-boost
T_{on}	a	Equation	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}-v_{CN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{v_{C0N}}{R_N}\right)$	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=-\frac{v_{C0N}}{C_N R_N}$	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=-\frac{v_{C0N}}{C_N R_N}$
	b	Solution	$v_{CN}=V_{inN}\pm\sqrt{(v_{C0N}-V_{inN})^2+Z_{rN}^2\left(i_{L0N}-\frac{v_{C0N}}{R_N}\right)^2-Z_{rN}^2\left(i_{LN}-\frac{v_{C0N}}{R_N}\right)^2}$	$v_{CN}=-\frac{Z_{rN}^2 v_{C0N}}{R_N V_{inN}}(i_{LN}-i_{L0N})+v_{C0N}$	$v_{CN}=-\frac{Z_{rN}^2 v_{C0N}}{R_N V_{inN}}(i_{LN}-i_{L0N})+v_{C0N}$
T_{off}	c	Equation	$\frac{di_{LN}}{dt_N}=\frac{-v_{CN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{v_{C1N}}{R_N}\right)$	$\frac{di_{LN}}{dt_N}=\frac{V_{inN}-v_{CN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{v_{C1N}}{R_N}\right)$	$\frac{di_{LN}}{dt_N}=\frac{-v_{CN}}{L_N}$ $\frac{dv_{CN}}{dt_N}=\frac{1}{C_N}\left(i_{LN}-\frac{v_{C1N}}{R_N}\right)$
	d	Solution	$v_{CN}=\pm\sqrt{(v_{C1N})^2+Z_{rN}^2\left(i_{L1N}-\frac{v_{C1N}}{R_N}\right)^2-Z_{rN}^2\left(i_{LN}-\frac{v_{C1N}}{R_N}\right)^2}$	$v_{CN}=V_{inN}\pm\sqrt{(v_{C1N}-V_{inN})^2+Z_r^2\left(i_{L1N}-\frac{v_{C1N}}{R_N}\right)^2-Z_r^2\left(i_{LN}-\frac{v_{C1N}}{R_N}\right)^2}$	$v_{CN}=\pm\sqrt{(v_{C1N})^2+Z_{rN}^2\left(i_{L1N}-\frac{v_{C1N}}{R_N}\right)^2-Z_{rN}^2\left(i_{LN}-\frac{v_{C1N}}{R_N}\right)^2}$
	e	Graphical state-trajectory			

Table.II. State equations and solutions of trajectories in the i_{LN} vs. v_{CN} plane for the presented topologies in the case of resistive load.

It is important to mention, that in this work, the following approximated state equations were used, in order to simplify the analysis. For these approximations, legitimacy is based on the assumption of a negligibly small output voltage change during each switching period. Later, in SubSection 1.2.7, a more detailed explanation will be given about the 'on' state approximation.

The approximated on-state equations are:

$$(\mathrm{I})\ \frac{di_L}{dt}=\frac{V_{in}}{L}\ ;\ (\mathrm{II})\ \frac{dv_C}{dt}=-\frac{v_{C0}}{CR}, \tag{1.6}$$

The approximated off-state equations are:

$$(\mathrm{I})\ \frac{di_L}{dt}=\frac{V_{in}-v_C}{L}\ ;\ (\mathrm{II})\ \frac{dv_C}{dt}=\frac{1}{C}\left(i_L-\frac{v_{C1}}{R}\right), \tag{1.7}$$

where v_{C0} and v_{C1} are the initial capacitor voltage of the on-state and off-state in each switching cycle, respectively.

1.2.State-space representation of PWM converter

1.2.1. Introduction

Analyzing the power stage of a circuit is a prime step for designing the control circuit. Neglecting nonlinearities introduced by transformers, or solid-state devices, in the case of a steady-state operation, a power converter could be referred to as a linear-time-variable circuit. Therefore, it is easy to examine the converter's steady state switching stages, by using any method related to the theory of linear circuits (such as the transfer function method) [23]. However, in transient cycles, a power electronic circuit becomes nonlinear, and hence, it is more difficult to be analyzed by known linear methods. Transient cycles are better analyzed using state-space representation, which refers to system's characterization, and system's dynamic examination, via trajectories, described upon an appropriate state-space plane, which coordinates are the system state variables. Nowadays, more and more applications mostly operate in the transient state. Consequently, the state-space representation is used extensively in "modern" control theory. It is used to study large-signal properties and the control strategies for dc-dc converters.

Moreover, the state-space representation is an excellent alternative way to describe the system model, instead of the conventional, and convenient, old method of representation in terms of transfer functions. There are several advantages to using the state-space representation when compared with a transfer function analysis, and other methods [4], [24]. Here are some of them:

- In contrast to transfer function analysis, state-space representation can be applied to nonlinear systems.
- It can be applied to time invariant systems.
- A more compact representation of equations.
- It is an effective option for the visualization of the system's characteristics.
- It enables an examination of the system's behavior under different control strategies.
- It can be easily applied to systems with multiple inputs and multiple outputs.
- In contrast to a transfer function, which is defined only under zero state initial conditions, it is possible and easy to incorporate the effect of initial conditions in the solution.

1.2.2. State-space map construction

The state-space is considered as a working region that describes the system and its operation, by states defined appropriately on the state-space. The state-space axes are defined as state variables, and the state of the system can be represented as a vector within that space. The state variables are the smallest set of system variables that are needed to represent the system dynamics at any given time [25]. In an electrical system, it is usually the inductor current and the capacitor voltage. The general procedure for creating a state-space map is according to the following steps:

- Deriving the system equations (in electrical systems it is usually done by Kirchoff's circuit laws).
- Defining the system's inputs, outputs, and state variables.
- Reformulating the system's state equations using the new variable notation and eliminating the time parameter.
- State-space and its trajectories can be drawn based on the new system equations.

The information gained through an examination of the state-space plane trajectories has led to the development of a new method of a minimum-deviation control law for DC-to-DC converters [26]-[27]. This could provide a significant improvement in the system's performance and characteristics.

1.2.3. Moving along the trajectories

In the following, traveling along the trajectories will be described using the example of a boost converter operation. During the on-time, the capacitor voltage is decreasing, and the inductor current is increasing, and the opposite is for the off-time. Accordingly, as shown by the arrows in Fig. 1.8, for instance, moving along a given path on the trajectory map corresponds to the above described voltage and current behavior. As long as the transistor switch is on one of these states, the system state must follow this particular state trajectory, until the switch is turned to the other state, and so on. Besides, in order to be able to move from one state to another, first, there needs to be an intersection, between the two states, at the point of switching, and second, this path should finally lead to the steady state trajectory, or else, this path is not possible, as there are some forbidden directions [28]. The control law must be able to follow permissible paths and bring the system's trajectories to the target of the steady-state point. Mapping the possible trajectories, and understanding their implication, seems therefore a necessary first stage in the development of a digital control method.

1.2.4. Target point representation

Whenever there are parameter uncertainties, or external disturbances in the system causing it to be thrown out of a steady-state mode, the system's objective is to achieve the target point, which is defined here as the new steady-state operating point indicated by (V_D, I_D). The target point is defined by the information available in the converter power stage and its operation. Therefore, each converter model has a different definition or expression for its own target point.

Steady-state is referred to as the state where the output voltage recovers back to its nominal value, and the inductor current reaches the new steady-state inductor current, as defined by the new nominal output current and the duty-cycle. For the boost and buck boost converters, because of their indirect-energy transfer feature, the new steady-state point current I_D is defined by $\frac{I_o}{D_{off}}$ where D_{off} indicates the steady-state off-time nominal duty-cycle which has a different definition for each one of the converters (1.8),

$$D_{off}\big|_{boost} = \frac{V_{in}}{V_{out}} \;\; ; \;\; D_{off}\big|_{buck-boost} = \frac{V_{in}}{V_{in}+V_{out}} \;\; ; \;\; D_{off}\big|_{buck} = \frac{V_{in}-V_o}{V_{in}}, \qquad (1.8)$$

Since the buck converter is defined as a direct-energy transfer topology, the desired new steady-state inductor current I_D is the new output current itself, I_O.

1.2.5. General definitions of state-space representation

In the following, the process of construction, and the examination of the state-space plane trajectories, of each of three converter topologies, will be presented. Both constant current and resistive loads cases will be considered. In order to find the analytical representation of the state-space plane $\left(v_C, i_L\right)$, there is a need to relate v_C to i_L. This relationship, however, must be time independent, namely, $v_C = f\left(i_L\right)$ when $f\left(\cdot\right)$ is time independent. All of the converter models and data were normalized so that the target output voltage V_{ref}, the rated output current, I_{ref}, and the new load, R, are all unity. Accordingly, the normalized parameters and variables are denoted as follows:

$$\begin{aligned} &V_{oN} = \frac{V_o}{V_{ref}}, I_{oN} = \frac{I_o}{I_{ref}}, v_{CN} = \frac{v_C}{V_{ref}}, i_{LN} = \frac{i_L}{I_{ref}}, T_{ref} = \sqrt{LC}, t_N = \frac{t}{T_{ref}} \\ &R_N = R\frac{I_{ref}}{V_{ref}}, C_N = C\frac{V_{ref}}{I_{ref}T_{ref}}, L_N = L\frac{I_{ref}}{V_{ref}T_{ref}} \end{aligned} \tag{1.9}$$

where i_L and v_C represent the inductor current and capacitor voltage, respectively, V_o and I_o are the nominal output DC voltage and current respectively, C is the output capacitor, and L is the inductor.

For all models, it was assumed that all of the components were ideal, namely, no additional parasitic effects were taken into account. Stated differently, it was assumed that there was no power dissipation. Therefore, the output and input capacitors' equivalent series resistance (ESR), the inductor series parasitic resistance, the switch on resistance, and the diode forward resistance, were not taken into account.

The graphical and mathematical representations of the converter model and the state-space trajectories, for each of the three direct and indirect energy transfer configurations, are summarized in Tables I and II. Note that the derivations of the circuit state equations involve the use of Kirchhoff's current and voltage laws. The difference between the various trajectories is in the initial state of the system, for which each trajectory corresponds. Throughout this work, in the figures, on-state and off-state trajectories are indicated by red solid lines and blue dashed lines, respectively.

1.2.6. Constant current load state-space representation

Here the detailed procedure for creating a state-space map for the case of a constant current load dc-dc converter is demonstrated.

As an illustration, the procedure is implemented on a constant current load boost converter. For the on-time, the time parameter was eliminated, by using simple mathematical operations on both state equation results and combining them. Equation (1.10) presents the two state equation solutions for the on-state, two differential equations (Table.I.a) where the time is still explicit, and the obtained combined solution, which eliminates the time parameter, is presented in (1.11).

$$\left(\mathrm{I}\right)\ v_{CN} = -\frac{V_{oN}}{C_N R_N} t_N + v_{C0N} \quad ; \quad \left(\mathrm{II}\right)\ i_{LN} = \frac{V_{inN}}{L_N} t_N + i_{L0N}, \tag{1.10}$$

$$v_{CN} = -\frac{Z_{rN}^2 V_{oN}}{R_N V_{inN}} \left(i_{LN} - i_{L0N}\right) + v_{C0N}, \tag{1.11}$$

where v_{C0N} and i_{L0N} represent the normalized capacitor voltage, and the inductor current initial system state for the on-time trajectories, respectively; the V_{inN} symbol represents the input source voltage, and the Z_{rN} symbol is a short form that indicates the impedance $\sqrt{\frac{L_N}{C_N}}$.

For the off-time, the time parameter was eliminated by using mathematical manipulations on the differential state equations (Table.I.c). For example, equation (1.12) presents the combined differential equation for the off-state, where the constant current load boost converter is considered and (1.13) represents its appropriate solution.

$$C_N \left(V_{inN} - V_{oN}\right) dv_{CN} = L_N \left(i_{LN} - \frac{V_{oN}}{R_N}\right) di_{LN}, \tag{1.12}$$

$$v_{CN} = -\frac{Z_{rN}^2}{2\left(V_{oN} - V_{inN}\right)} \left(i_{LN}^2 - i_{L1N}^2\right) + \frac{V_{oN} Z_{rN}^2}{R_N \left(V_{oN} - V_{inN}\right)} \left(i_{LN} - i_{L1N}\right) + v_{C1N}, \tag{1.13}$$

where v_{C1N} and i_{L1N} represent the capacitor voltage and the inductor current initial system state for the off-time trajectories, respectively. Fig.1.8 shows the resulted state-space trajectories map. The line of asterisks represents the new steady-state inductor current, and

the circled point is the target new steady-state point. Results for the other cases are presented in Table. III.

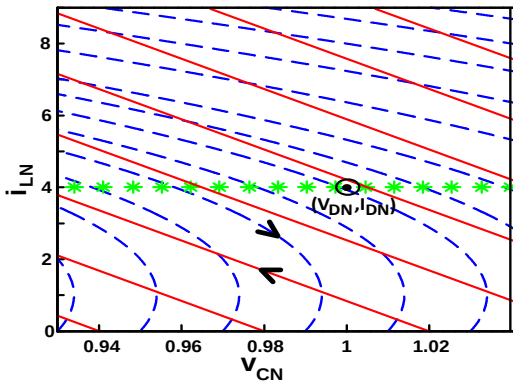


Fig.1.8. State-space trajectories map of a constant current load boost converter.

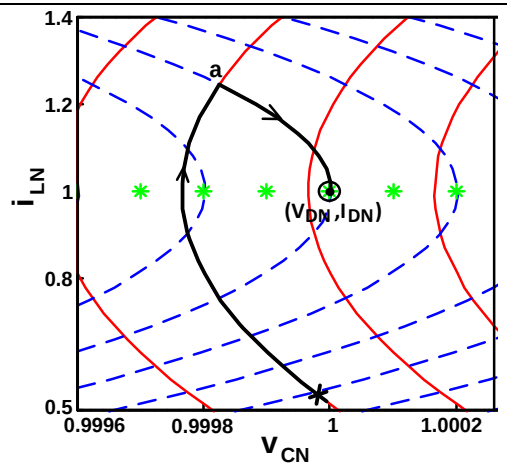
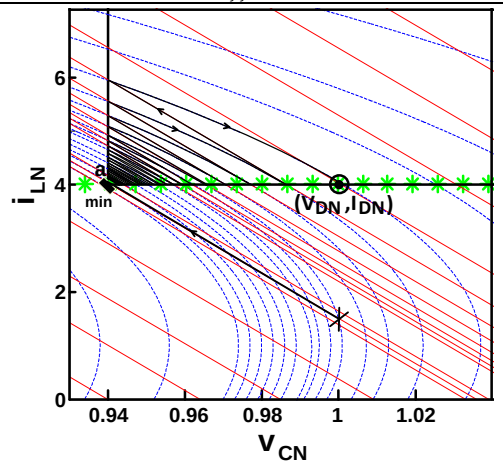
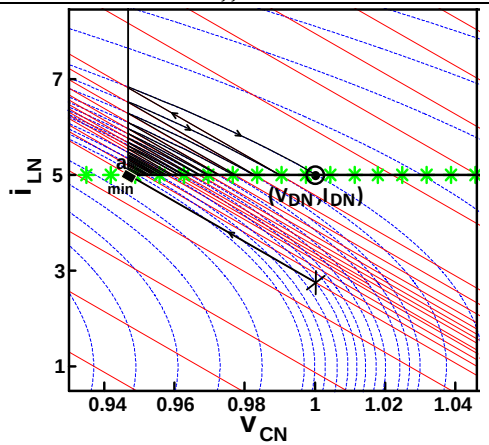
type		min	direct energy transfer	indirect energy transfer	
topology			Buck	Boost	Buck-Boost
Constant current load	a	V_{minN}	$v_{CON} - \frac{Z_{rN}^2}{2V_{inN}D_{offN}}(I_{TN} - i_{LON})^2$	$v_{CON} - \frac{Z_{rN}^2 I_{TN}}{V_{inN}}\left[\frac{I_{TN}}{D_{offN}} - i_{LON}\right]$	$v_{CON} - \frac{Z_{rN}^2 I_{TN}}{V_{inN}}\left[\frac{I_{TN}}{D_{offN}} - i_{LON}\right]$
	b	I_{minN}	I_{TN}	$\frac{I_{TN}}{D_{offN}}$	$\frac{I_{TN}}{D_{offN}}$
	c				
Resistive load	d	V_{minN}	$v_{CON} - \frac{R_N v_{CON}}{R_N^2 - Z_{rN}^2}\left[-\frac{Z_{rN}^2}{v_{CON}}(I_{TN} - i_{LON}) - \frac{R_N D_{offN}}{1 - D_{offN}} + \sqrt{\left(\frac{D_{offN}}{1 - D_{offN}}\right)^2 (R_N^2 - Z_{rN}^2) + \frac{Z_{rN}^2}{I_{TN}^2}\left(i_{LON} - \frac{V_{inN}}{R_N}\right)^2}\right]$	$v_{CON} - \frac{R_N D_{offN}}{1 + D_{offN} + \frac{R_N^2}{Z_{rN}^2}\cdot D_{offN}^2}\left[\frac{I_{TN}}{D_{offN}} - i_{LON}\right]$	$v_{CON} - \frac{R_N D_{offN}}{1 + \frac{R_N^2}{Z_{rN}^2}\cdot\frac{D_{offN}^2}{1 - D_{offN}}}\left[\frac{I_{TN}}{D_{offN}} - i_{LON}\right]$
	e	I_{minN}	$I_{TN} - \frac{v_{CON}}{R_N^2 - Z_{rN}^2}\left[-\frac{Z_{rN}^2}{v_{CON}}(I_{TN} - i_{LON}) - \frac{R_N D_{offN}}{1 - D_{offN}} + \sqrt{\left(\frac{D_{offN}}{1 - D_{offN}}\right)^2 (R_N^2 - Z_{rN}^2) + \frac{Z_{rN}^2}{I_{TN}^2}\left(i_{LON} - \frac{V_{inN}}{R_N}\right)^2}\right]$	$\frac{I_{TN}}{D_{offN}} - \frac{1 + D_{offN}}{1 + D_{offN} + \frac{R_N^2}{Z_{rN}^2}\cdot D_{offN}^2}\left[\frac{I_{TN}}{D_{offN}} - i_{LON}\right]$	$\frac{I_{TN}}{D_{offN}} - \frac{1}{1 + \frac{R_N^2}{Z_{rN}^2}\cdot\frac{D_{offN}^2}{1 - D_{offN}}}\left[\frac{I_{TN}}{D_{offN}} - i_{LON}\right]$

Table.III. Equations of minimum point in the i_{LN} vs. v_{CN} plane.

1.2.7. Resistive load state-space representation

The same analysis was also conducted for the case of resistive load DC-DC converter.

Same as for the above case of constant current load, an example of a boost converter is presented. Equations (1.14)-(1.17) represent the process and results done and obtained for this case (Table.II.a and Table.II.c).

$$\left(\mathrm{I}\right)\ v_{CN} = -\frac{v_{C0N}}{C_N R_N} t_N + v_{C0N} \quad ; \quad \left(\mathrm{II}\right)\ i_{LN} = \frac{V_{inN}}{L_N} t_N + i_{L0N}, \tag{1.14}$$

$$v_{CN} = -\frac{Z_{rN}^2 v_{C0N}}{R_N V_{inN}} \left(i_{LN} - i_{L0N}\right) + v_{C0N}, \tag{1.15}$$

$$C_N \left(V_{inN} - v_{CN}\right) dv_{CN} = L_N \left(i_{LN} - \frac{v_{C1N}}{R_N}\right) di_{LN}, \tag{1.16}$$

$$v_{CN} = V_{inN} \pm \sqrt{\left(v_{C1N} - V_{inN}\right)^2 + Z_{rN}^2 \left(i_{L1N} - \frac{v_{C1N}}{R}\right)^2 - Z_{rN}^2 \left(i_{LN} - \frac{v_{C1N}}{R_N}\right)^2}, \tag{1.17}$$

Fig. 1.9 shows the resulted state-space trajectories map. Results for the other cases are presented in Table. III.

As already mentioned, a first order approximation on the on-state solution of the resistive load converter was used to simplify the state-space plane examination. The on-state trajectory equation was approximated to be linear (1.15) instead of exponential (1.18). As can be seen from Fig. 1.10.a this approximation is legitimate since the difference between the solutions is very small for the region of interest (point 'min') when a practical system operating conditions are considered. It should be also noted that although a second order approximation is more accurate (Fig. 1.10.b), still the first order approximation was chosen to be used. This is due to the much simpler analysis and minimum-deviation point expressions obtained when the first order approximation is used. In addition, as will be explained and demonstrated later, since practically the thresholds are taken to be larger than the calculated minimum, this small difference between results won't anyway give any advantage, therefore it can be ignored. Equations (1.4) and (1.18) represent the accurate case state equations and their result, respectively.

$$v_{CN} = v_{C0N} e^{-\frac{L_N}{R_N C_N V_{inN}} \left(i_{LN} - i_{L0N}\right)}, \tag{1.18}$$

Activating tailor approximation on equation (1.18) results with the reported solution (1.15) for the resistive load case.

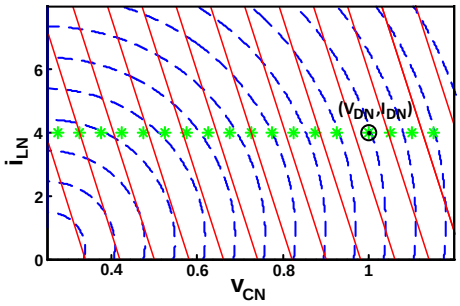


Fig.1.9. State-space trajectories map of a resistive load boost converter.

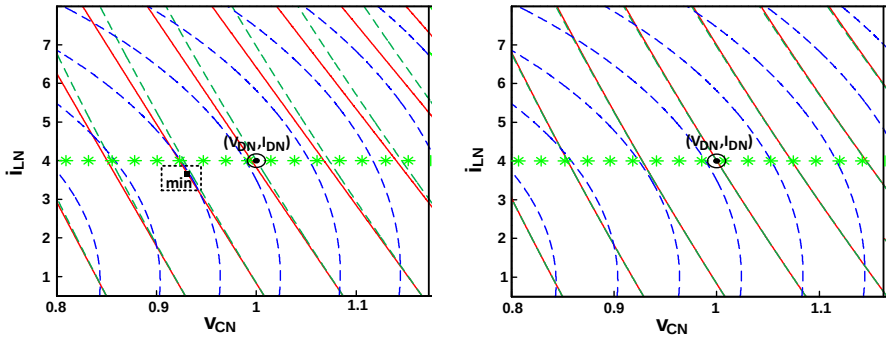


Fig.1.10. Resistive load boost accurate on-state trajectories (dashed green lines) versus their approximation (solid red lines). (a) First order approximation (b) Second order approximation.

An accurate analytical solution and an appropriate state space representation for the case of a resistive load converter for indirect energy transfer topologies already exist and reported in literature such as [29]-[32]. These papers use the obtained state-space trajectories to analyze their relevant control methods and stability. Only these papers don't deal with the minimum-deviation control and they also meet with a difficulty to analyze the obtained trajectory map directly. In addition, drawbacks of requiring sophisticated analog circuitry or heavy and complex expression obtained complicate the control design and implementation. Here, using the accurate solution will result with very complicated analysis and numerical solution which is problematic in the sense of software implementation, and more important unnecessary for this research goal. For these reasons, the above presented legitimate approximations and assumptions were used both for on and off states.

1.2.8. Resistive load and constant current load differences

Table.I.e and Table.II.e diagrams show that there are differences between the resistive load case and the constant current load case trajectories shape. First, the state trajectories are parallel to each other in contrast to those of the resistive load case. Also, for the constant current load,

the on-state trajectories are represented by linear lines and the off-state trajectories by parabolas, while the resistive load case include exponential on-state trajectories and ellipsoidal off-state trajectories. The reason for these differences is the different behavior of the system's output current for each case.

1.3. Linear control methods

1.3.1. Voltage mode control (VMC)

Voltage-mode control (VMC) is a control technique used in many power systems where the duty cycle is adjusted to regulate the output voltage based on the value of the error between the sensed output voltage and the reference voltage [33]-[34]. Steady-state is achieved when the actual output voltage equals the voltage reference.

As can be seen from Fig. 1.11 the voltage-mode control loop contains three main stages. These three stages are the output stage, the modulator gain, and the voltage loop compensation [35] to ideally allow for a predictable bandwidth with unconditional stability. The voltage loop compensation includes calculating the voltage error by comparing the voltage at the feedback to the reference voltage and then using an error amplifier to create an error current with the required frequency compensation for maintaining stability of the control loop. This output is then fed to a modulator. A PWM signal is generated using the PWM modulator. Two topologies for generating a PWM signal are the fixed ramp voltage [37] and feed forward voltage topology [38]-[39].

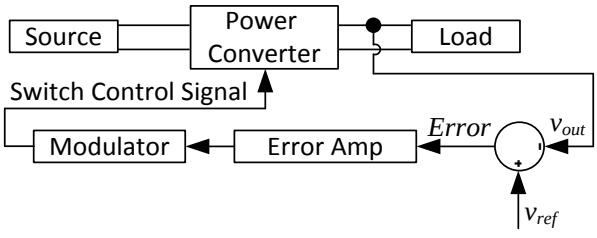


Fig.1.11. Concept of voltage mode control.

In a voltage mode regulator, the PWM signal is generated by a comparator triggered by a sawtooth ramp generated from a clock signal as shown in Fig. 1.12. This ramp can be a fixed-slope sawtooth ramp, or a ramp whose slope is proportional to the input voltage as in the feed forward configuration.

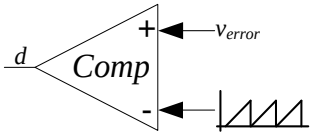


Fig. 1.12. PWM Generator.

The resulted signal of this PWM generator is determined by the error voltage value. When the error voltage value is 0 V, the duty cycle is 0%, and when it is equal to the peak of the ramp voltage, duty cycle is equal to 100%. When the output voltage changes, the error voltage also changes, this in turn alters the comparator threshold. Usually, voltage mode control contains only one loop.

1.3.2. Current mode control (CMC)

Current-mode control (CMC) has been a popular and effective control technique for power converter systems [40]. An ideal current-mode converter is only dependent on the dc or average inductor current. It is controlled with a two loop system [41]. The inner loop or current loop turns the inductor into a voltage controlled current source, effectively removing the inductor from the outer voltage control loop at dc and low frequency. The inner loop uses a PWM modulator which receives the sensed inductor current ramp, and a reference current obtained by the outer voltage loop to determine the switch control signal.

The fundamental difference between voltage-mode control and current-mode control is the PWM modulation. A fixed external ramp is used in voltage mode control, while the inductor current ramp is used in current-mode control. Current-mode control schemes have several advantages to offer over voltage-mode control. Since a CMC behaves like a current source, voltage variation at the input doesn't go through to the output, what makes the CMC power converter more immune to an input disturbance compared to a VMC converter [33]-[34]. Also, since the CMC control-to-output transfer function can be simplified to a first order system, CMC converters have simpler dynamics and the system stabilization is simpler to implement. Another advantage of the CMC over VMC is that CMC provides inherent over-current protection due to the immediate switch current limit. Current mode control is implemented mostly with two approaches:

1) Peak-current mode: Among the different ways to implement CMC, peak current-mode control (PCMC) is probably the earliest and simplest approach. A block diagram of a PCMC power converter is presented in Fig. 1.13. As it can be seen from Fig. 1.13 PCMC places a fast current loop inside the voltage control loop. The inner current loop senses the actual inductor current and directly compare it to the current reference I_{ref} using a PWM comparator to monitor and maintain the peak inductor current equal to the reference current I_{ref}. This reference current is set by the outer loop, or voltage loop, in which the output voltage is compared to a voltage reference. PCMC has the advantage of fast response, especially when there is no or a little slope compensation which will be discussed later in this paragraph.

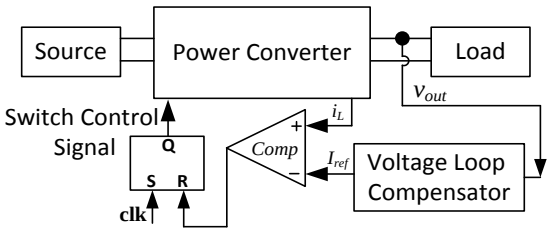


Fig.1.13. Block diagram of peak-current mode control power converter system.

Conventional PCM control suffers from a number of drawbacks:

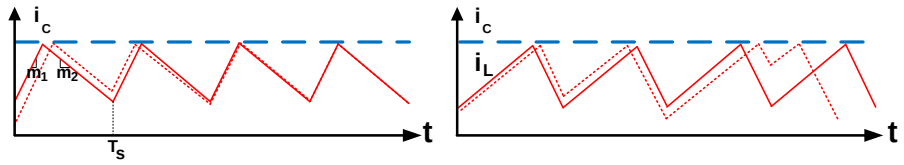
- Instability caused by sub-harmonic oscillation when duty-cycle exceeds 0.5.
- Average currents of the converter can be controlled only in the inductor.
- Due to ripple and slope compensation issues, operation is less accurate compared to ACM.
- Lower loop gain compared to ACM cause PCM to be more susceptible to noise (including switching noise).

Average current-mode control (ACMC) overcomes those disadvantages at the expense of a more complicated design and analysis.

Slope compensation: One of the drawbacks of the PCM control compared to other control strategies such as the ACM control is instability known as subharmonic oscillation for certain operating conditions. This instability occurs for duty-cycle that is greater than 50%, when the inductor ripple current is higher from its initial value by the start of next switching cycle. Meaning that, instability issue exists when the current feedback loop is closed, because the disturbance grows larger with each cycle. As shown in Fig. 1.14, duty cycle that is greater than 50% in peak current-mode control leads to large deviations from the nominal operating point and subharmonic oscillations occur [4]. The slope compensation is obtained by simply adding to the current reference or to the sensed current signal an external compensating ramp signal that must be greater than one-half of the down-slope of the inductor current waveform (1.19) [4], [42]. Practically, by applying the slope compensation (Fig .1.15), any tendency toward sub-harmonic oscillation is reduced within one switching cycle which lowers the sensitivity of the duty ratio to noise in the control signal.

$$m > -\frac{1}{2} m_2 , \tag{1.19}$$

where m is the slope of the slope compensation ramp, and m_2 is the down slope of the current waveform, which is equal to $\frac{V_o R_L}{L}$ both for buck and buck-boost converters, and to $\frac{(V_o - V_{in})R_L}{L}$ for the case of the boost converter.



(a) (b)

Fig.1.14. Subharmonic oscillations in peak current-mode control: (a) D<0.5, and (b) D>0.5.

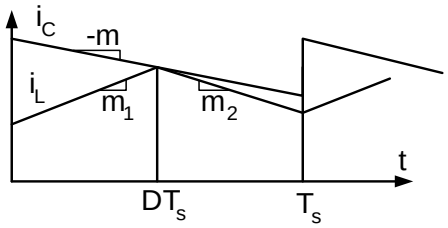


Fig.1.15. Addition of slope compensation to the control signal.

While answering the condition given in (30) is desirable for sub harmonic stability, any slope which answers (30) will cause the converter to behave less like an ideal current mode converter and more like voltage mode converter. Therefore, there is a trade-off between the inductor ripple current and slope compensation [42]. It is also important to mention that a power converter suffers from subharmonic oscillation only when it operates in continuous conduction mode (CCM), so a discontinuous conduction mode (DCM) power converter doesn't need a slope compensation to stabilize the system. That is because during DCM the inductor current goes down to zero before the end of each switching cycle, so disturbances from previous switching cycle have no influence on the next switching cycle.

2) Average-current mode: In contrast to the PCM control, the ACM control system, as illustrated in Fig. 1.16, average and compensate its measured inductor current using an additional compensator in its current loop. The reference current is determined by the voltage error obtained by the voltage loop. The error between the averaged current and the reference current is compared to a sawtooth signal, and finally, the result determines the PWM signal of the power switch control.

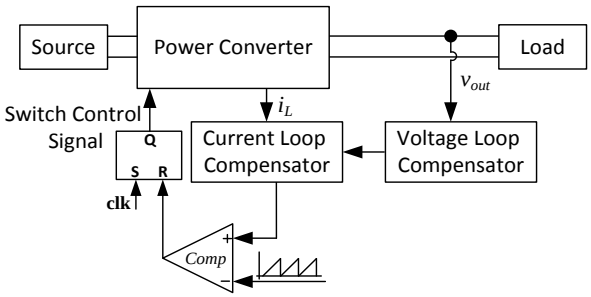


Fig. 1.16. Block diagram of average-current mode control power converter system.

At the expense of more complex design and analysis, several important advantages of the ACM control over PCM control are achieved [34], [43]:

- The additional compensator in ACMC eliminates the need for slope compensation.
- ACMC tracks the average inductor current with a high degree of accuracy.
- Excellent noise immunity is achieved due to eliminating any current errors in previous switching cycles via the additional ramp signal.

1.4.Steady-state response and Transient response of a system

Due to stability issues and system performance in control system analysis and design, it is better to design controllers that take care of the complete system response, which is the sum of the steady-state and transient responses.

In electronics, steady-state is an equilibrium condition of a circuit or network. This equilibrium behavior will continue as long as the system is in steady-state. Steady-state stability is the ability of a system to regain its equilibrium state. It is limited to small and gradual changes in the system operating conditions, and mostly focused on keeping the bus voltages close to their nominal values. Investigating whether a power system could maintain stability under continuous small disturbances is done under the name of dynamic stability also known as small-signal stability [23].

Ideally, external disturbances can't affect the output voltage. However, in reality, a control circuit has to ensure that a disturbance caused by a change in the input voltage or load won't be propagated to the load [23].

The transient response is the response of a system to a change in equilibrium. Since energy of the electric and magnetic fields cannot be changed instantaneously in capacitive and inductive elements in a circuit, the inductor current and capacitor voltage cannot be altered abruptly. Therefore, transient occurs during a transition from one operating condition to

another that has a different amplitude, phase, shape, or frequency of the circuit steady-state nominal voltage. Electronic device may operate erratically when transient arise, that can cause operation at decreased efficiencies and failure.

This work research and discussion are focused on the transient stability aspects of a power system.

1.5.Nonlinear control methods

The hybrid nature of DC–DC converters represents a big challenge for control design. Classical linear control methods are designed at one nominal operating point, therefore, they often fail to perform satisfactorily under large parameter or load variations.

Moreover, from the control point of view, indirect energy transfer converters are more difficult to control than direct energy transfer converters. The difficulties are due to the non-minimum phase structure seen by the appearance of the control input both in voltage and current equations. Different control algorithms are applied to regulate the DC-DC converters for achieving a robust output voltage. In order to deal with variations of the system parameters and large signal transient, the linear control techniques will have to be replaced or integrated with non-linear control methods such as the time-optimal control, hysteretic control, boundary control, minimum-deviation control, and sliding-mode control. A brief description for each of these methods will be given next.

1.5.1. Time optimal control

Time-optimal control methods have been widely applied to improve transient performance of dc-dc converters. Basically, time-optimal main objective is to regulate the average output voltage to its nominal steady-state value as fast as possible [44]. It is widely accepted and justified in many works that the time-optimal control switching sequence attempt to compensate the lost capacitor charge through a single on/off control action [46]-[51], [56]. Systems operating with time optimal control law present short response times to external disturbances.

Time-optimal controllers [45]-[54] have demonstrated ultimate improvement in the dynamic response for direct energy transfer converters, such as buck and forward topologies. Ideally, In this case, the time-optimal response always results in the minimum possible output voltage deviation and output capacitance value. However, for indirect energy transfer systems, such as a boost or flyback converters, this is not the case. Here, the time-optimal

response often produces a larger-than-minimum output voltage deviation, and causes extra current stress of the components. Furthermore, the implementation of the optimal methods for these systems is usually more hardware demanding than that for direct energy transfer converters. This is because the controller is required to solve a set of fairly complex operating-point-dependent equations [45]-[46], [51]-[52]. As a consequence, the time-optimal controllers still have not been widely adopted for these converters.

1.5.2. Sliding mode control

The SM control technique is a non-linear control method that can be used to control switching converters [57]. The main advantages of the sliding mode control over PWM control are its robustness, stability, simpler implementation and good dynamic response [58].

A switching boundary, σ, is defined to dictate the switching actions. Switching surface control mostly depends on the surface shape and how states interact at the surface crossing. The SM control approach is based on choosing an appropriate first-order sliding surface in the state space. When the sliding regime exists, the system's present state point eventually moves onto the intersection, of all the individual switching boundaries $\sigma_i(x) = 0$ ($i = 1,2,\ldots,m$). The hypersurface defined by the intersection of all m switching boundaries, $\sigma_i(x) = 0$, is called the sliding surface, $S(x)=0$. Here for example, Fig. 1.17 shows a sliding surface drawn as a black solid line (This converter is a second order system with one control input. Therefore, the dynamic response obtained under sliding mode control is of order one. Meaning that, the steady-state, and the dynamic response, can be expressed as a one dimensional sliding surface (sliding line) in the phase plane), and two 'on' and 'off' state lines that cross each other in the sliding surface. This surface defines the rule for proper switching, it must be designed properly to comply with the converter dynamics. Meaning, it has to ensure that for any initial state, the system state trajectory first reach the sliding surface in finite time, and then follow this surface to evolve toward the stable operating point [59].

In sliding mode control, three conditions must be fulfilled in order to guarantee the stability of motion in the sliding regime [60]. The first is the reachability condition which requires the system to eventually reach the sliding surface, $S(x)=0$ from any generic starting point. The second condition is the existence of sliding regime on the manifold. The existence condition is often termed as the reachability condition since meeting the reachability condition will also answer the existence condition [61]. In mathematical terms this condition is expressed by

(1.20). The third condition needed to be satisfied is the stability of the reduced-order system evolution on the manifold, meaning that the stability of response must be guaranteed along the sliding surface to ensure that the system moving along the surface will move towards the desired steady-state point. In the case where any of the conditions or all doesn't exist, the system motion won't be confined to stay on the sliding surface and obviously, the system won't converge to the desired unique steady state operating point.

$$\begin{cases} \dfrac{dS}{dt} > 0 \quad ; \quad 'on'\,(S < 0) \\ \dfrac{dS}{dt} < 0 \quad ; \quad 'off'\,(S > 0) \end{cases}, \tag{1.20}$$

Ideally, the controller operates at an infinite switching frequency, where the switching is within an infinitesimal distance around the sliding surface, to allow the state variables follow a certain reference path to achieve the desired dynamic response and steady-state operation [62]. However, implementing the SMC at infinite switching frequency in power converters arise the issue of practical design considerations. This is due to too high switching losses, inductor saturation and core loss, frequency exceeding beyond switch ratings, and electromagnetic-interference (EMI) noise issues resulted by the extreme high switching speed [63]. Hence, finite practical range of switching frequency must be implemented in order to have an effective controller operation. A more generalized method of the sliding mode control is the boundary control which will be discussed later in this section.

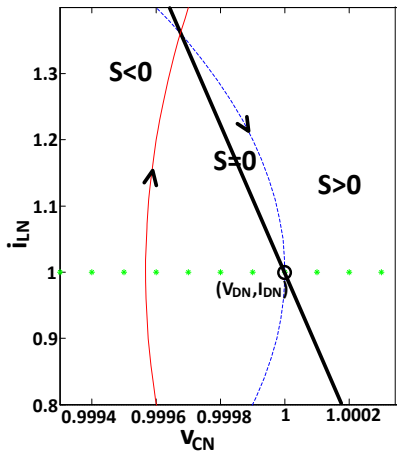


Fig.1.17. Buck converter sliding mode definition.

1.5.3. Hysteretic control

In the ideal case of SM control, the system trajectories are always directed along the sliding surface, this requires an infinite switching frequency. However, an infinite switching

frequency may not be acceptable in a real system. This is because it could lead to undesirable practical problems, such as, variable switching frequency resulted by input and output voltage variations, chattering phenomena [64], and more. These issues make the SMC implementation to be challenging. Hence, the SMC should be used when its switching frequency is limited by a practical range. To this end, several methods have been already proposed and presented in literature [65]-[69], [84]. Among them there are methods of sliding mode control with hysteresis to ensure a finite switching frequency [58], [62], [65].

The hysteresis control methods force control updates to only occur alternately at the hysteresis band boundaries while restricting the system trajectory to move within the hysteresis bands [70]. The main advantages of hysteretic controllers over other control methods like the ideal SM control include fast response to load transient, robustness, and they are also characterized with simple design and implementation. However, to this end, still several issues needed to be considered such as variable switching frequency operation and stability analysis [64], [70].

1.5.4. Boundary control

Boundary control is a large-signal tool used for the design of switching power converters. Generally speaking, boundary control is a geometric based control method that splits the state space of a given converter with a switching surface, σ, such that on one side of the boundary, the control switches are turned on (on-state trajectories), and on the other side they are turned off (off-state trajectories) [30]. The boundary must be defined to pass through the desired operating point. Switching boundary control is a generalized method of sliding mode control concepts [31], [35]. A useful boundary not necessarily shows sliding behavior.
For a two mode switching converter, the switching boundary is a line given by

$$k_I \left(I - I_{ref} \right) + k_V \left(V - V_{ref} \right) = 0, \tag{1.21}$$

where k_I and k_V are the current and voltage gains, respectively, I and V are the states of the state-space, and I_{ref} and V_{ref} are the inductor current and capacitor voltage references, respectively. By varying the gains and selecting different operating points on the load line (i.e., changing the reference values), the converter can be made to operate in the vicinity of any point on the load line.

Large-signal stability conditions also need to be established [30], [31]. There are several considerations needed to be included in boundary controller design, here some of them are addressed:

- In order to avoid chattering, stable boundary controllers require frequency limiting or timing constrains.
- During discontinuous mode under certain conditions limit cycles [71]-[72] might occur.
- Steady-state errors occur due to parameter uncertainties or external disturbances.
- Line and load regulation might be very poor due to the correspondence of the current reference to a specific set of parameters [30].

1.5.5. Minimum-deviation control

Recently emerged hardware-efficient digital controllers [73]-[76] enable implementation of advanced nonlinear control methods for low to medium power systems, improving dynamic performance and, consequently, drastically reducing the size of the output capacitor. Among them, time-optimal [45]-[54] controllers have demonstrated transient response with virtually the smallest possible voltage deviation, for direct energy transfer converters. However, for the indirect energy transfer topologies, the fastest transient response usually does not coincide with the minimum possible output voltage deviation**.** The problem of the overly large inductor peak current has been addressed in [47] and in [52], and several modifications of the optimum-time controller proposed. Those include systems that put a hard limit on the maximum inductor current [47], based on the components rating, and alter the converter configuration with extra switches, to create additional energy paths [52]. By looking at Fig.2.1 it can be seen that, the extra inductor current rise time (beyond its new steady state value), during which the energy for replacing the lost capacitor charge is collected, increases the current beyond its new nominal value and causes a larger than the minimum possible voltage deviation. This is because the capacitor discharging process continues during the extra time. To solve this problem, the minimum-deviation controller has been developed [26]-[27], [77]-[78]. The main goal of the minimum-deviation controller is to provide a significantly smaller output voltage deviation and lower current stress, allowing for output capacitor and inductor reduction, respectively. Also, a simpler controller implementation compared to time-optimal solutions is achieved due to the elimination of

complex calculations of the switch 'on' and 'off' times and from the sole reliance on the amplitudes of the state space variables, which are relatively easy to acquire [45]-[53].

In summary, as will be shown throughout this work and in [26]-[27], this design approach brings three main advantages compared to the time-optimal solutions for indirect energy-transfer converters [46]-[53]:

1. The computational complexity is drastically reduced creating a possibility for much simpler, i.e. hardware-efficient, controller implementation.
2. The method results in a significantly smaller output voltage deviation allowing reduction of the output capacitor.
3. The maximum inductor current is lower, approximately equal to nominal steady-state value, reducing the current stress and allowing for the output inductor reduction.

It should be noted that this work concentrates on both constant current load and resistive load cases. The following chapters will be focused on the minimum-deviation control analysis, and more information and examples will be given.

1.6.Large signal stability analysis

1.6.1. Introduction

The commonly used controller stability analysis is based on the converter linear small signal time averaging model [4], [79]-[80]. However, the time-average method related to the linear controllers such as P, PI, and PID essentially ignores the switching cycle and dynamics details, it is only an approximation of the low frequency converter dynamics and it requires sufficiently high switching frequency to be accurate [81]-[82]. This standard stability analysis can be applied in the vicinity of steady-state, but when transient operation is examined, the linearized small signal model won't be appropriate. Moreover, even if the averaged model is accurate, for many switching converter topologies it will be highly nonlinear and difficult to analyze, so their large-signal characteristics will have a different behavior from that of the expected from the small-signal design approaches. Thus, designing them with the basic control methods to achieve a fast dynamic response over large range of supply and load disturbances variations is impossible. Therefore, in large-signal transient operations, non-linear controllers are investigated, and so, stability conditions can be stated by using the Lyapunov second theorem for the large-signal discrete-time model. These types of controllers

have the advantage of their option for an immediate reaction to a transient condition.

1.6.2. Lyapunov second theorem

Lyapunov's second method is wildly used nowadays [83]-[85]. It is a theoretical tool used for stability analysis of nonlinear differential equations of an examined system without solving the equations. This stability method requires the generation of the Lyapunov function which can be tricky and hard to be done. For linear, time invariant systems, however, this search is not too hard. In order to easy understand and visualize the idea behind this method, a physical system can be considered. A physical system can only store finite energy, thus, if that energy is always being dissipated over time and never restored except at the equilibrium point, then eventually, when the energy is gone, the system must reach this final resting state which is the equilibrium [84]. Lyapunov function is the mathematical representation of the system "energy". However, finding a function that gives the precise energy of a physical system can be difficult and sometimes it may not even be applicable. Since this work mostly focus on large signal analysis, only the discrete-time definition of the Lyapunov function will be presented. Let $V(\mathbf{x})$ the Lyapunov function of a given system (1.22).

$$\mathbf{x}(k+1) = \mathbf{f}(\mathbf{x}(k)) \quad \mathbf{f}(0) = 0, \tag{1.22}$$

The main argument in Lyapunov's theorem is that existence of Lyapunov function in $\mathbf{x}$ assures that the equilibrium solution $\mathbf{x}(k) = 0$ for the given system (1.22) is asymptotically stable.

If the following three conditions hold ($V(\mathbf{x})$ is a scalar function), Lyapunov stability of the examined system is achieved:

1. $V(\mathbf{x}=\mathbf{0}) = 0$, and $V(\mathbf{x})$ is continuous in $\mathbf{x}$.
2. $V(\mathbf{x})$ is positive definite, *i.e.* $V(\mathbf{x}) \geq 0$. With $V(\mathbf{x}) = 0$ only if $\mathbf{x} = \mathbf{0}$.
3. $\Delta V(\mathbf{x}) \triangleq V(\mathbf{f}(\mathbf{x}))-V(\mathbf{x})$ is negative definite, i.e., $V(\mathbf{f}(\mathbf{x}))- V(\mathbf{x})\leq 0$ with $\Delta V(\mathbf{x})=0$ only if $\mathbf{x}=\mathbf{0}$.

1.7. Digital control vs. Analog control

In low-to-medium power supplies, processing power from a fraction of watt to several hundreds of watts, where cost-effective implementation is of key importance, analog controllers have been predominantly used [9]-[12]. There, a fast response is usually achieved by designing a wide bandwidth control loop.

In the recent years, technology advances in very-large-scale integration (VLSI) have made digital control of DC-DC converters with microcontrollers and digital signal processors (DSP) possible [86]. Therefore, following the rapid advancement of digital technology, digital control has established a dominant role as efficient regulator for switch-mode power supplies (SMPS). Nevertheless, despite its obvious advantages which will be described below, digital control has not become a common practice yet. The major reason for this is that to obtain a level of performance similar to that of the analog design, there is a need for fast processors with powerful computational resources, and the cost thus is considerably higher than that for the analog solution [76], [87]-[100]. The common practice today of digital control analysis and design is based on translation of analog control methods to the digital domain and therefore, misses the true virtues that can be offered by digital control technology.

Analog controllers main advantages compared to digital controllers include: wider bandwidth, higher resolution, more efficient and accurate, easier design, and lower costs. On the other hand there are also some drawbacks such as: degradation due to component aging, component temperature drift, more parts (lower reliability), limited upgrades, limited in performing smart control algorithms, and also more difficult to perform fine tuning and adaptations.

The major advantages of digital control over analog control are increased flexibility by software changes, better way to implement computational functions, well-defined behavior, no drift in digital parts, less parts (higher reliability), they are not subjected to component tolerances and aging effects, tenability and suitability for “smart” control strategies, therefore, more advanced control methods (non-linear) such as fuzzy logic control [101]-[103], adaptive control [104]-[105], optimal control [50], [106], and more are available, better for communication applications, and shorter design cycles [86]. Disadvantages may result in degradation in the controller performance include: higher costs, limited bandwidth due to sampling delays, might involve complex programing, and also, since this is a new technology it is still not widely accepted.

Areas such as power electronics, system and control, and computer systems, show an increasing interest in the digital control of switch mode DC-DC converters. Digital control design methods for dc-dc converters include direct and indirect design approaches [86]-[103], [107]. In the direct design approach, the converter's small-signal model is first converted into a discrete-time model. This way, digital controllers can be directly designed using a

generated discrete-time model. In the indirect design approach, first, the analog controller is designed based on a converter's small-signal model, and then it is converted into a digital controller.

Present-day digital controllers, excluding an IC design, are implemented on either DSP cores or FPGAs. For operating frequencies in the range of several hundred kHz, DSPs with specialized integrated peripherals (DPWM, ADC, etc.) are available. For higher operating frequencies, and for more advanced control schemes (e.g. CPM or time-optimal control), an FPGA design is the preferred option. There, however, additional auxiliary components are required for peripherals which, to some extent, limit the capabilities of the controller. It would be highly advantageous if the main peripheral units that are required could be integrated into the FPGA, and are made configurable. In this way, the optimization and evaluation process of the controller operation would be eased, as well as for providing a straightforward platform for IC integration via synthesis tools.

1.8.Motivation, objectives, and the significance of the research program

Digital power management is expanding fast, and is, in fact, one of the buzzwords in power electronics. Due to the increasing interest, a lot of research has recently been focused on this subject, especially when nonlinear control methods are examined. There already exists several nonlinear control methods, which deal with transients better than conventional linear control methods, but as mentioned in the introduction, non-direct energy transfer configurations still suffer from a large voltage drop and current stress, and are usually more hardware demanding than those for direct energy transfer converters. The main objective of this research is to provide the analytical tools, and some practical counterparts, for the attractive and economical realization of flexible power supplies and digital control, and will thus provide the tools for the further miniaturization of power management systems and improved energy processing efficiency.

In this thesis, the research is focused on:

- Full behavioral theorems based on state-space analysis
- The development and analysis of minimum-deviation control algorithms
- Exploring and verifying system stability for the proposed nonlinear control method
- Full combined controller design and guidelines for the efficient realization of digital hardware

- Experimental validations of the proposed controller

The results of this study can directly contribute to the research and the development of a new generation of flexible power supplies, and non-linear control methods. This study provides tools and the theory to further research and develops of this subject.

2. Unified state trajectory approach for the minimum deviation of light-to-heavy load transient recovery of PWM converters

This chapter presents the theoretical considerations and lays down the basics for the design of a minimum-deviation controller. A simplified light-to-heavy load transient overview for a minimum-deviation control law is first presented, followed by a more specific examination of the different converter topologies that have been examined in this research.

2.1. Constant current load boost converter control method approaches

2.1.1. Light-to-heavy load transient

Here, a more specified operation of the minimum-deviation control method is demonstrated via a constant current load boost converter example. Fig. 2.1 shows the load current, the inductor current, and the output capacitor voltage, during transients, both in the time and the state-plane domains. In Fig. 2.1.a, a typical light-to-heavy response of a time-optimal controlled boost converter is depicted. Fig. 2.1.b shows the operation of a near minimum-deviation controlled boost converter.

The diagrams of Fig. 2.1.a can be used to review the operation of the time-optimal controllers and address some of their drawbacks. As soon as a load transient from I_{out_old} to I_{out_new} is detected, at point *'x'*, the boost converter switch turns on, causing the inductor current to ramp up with a V_{in}/L slew rate, and the capacitor voltage to slope down, at an I_{out_new}/C rate. The peak inductor current, I_{peak}, at the time instant *a*, is usually significantly larger than its new steady-state value $I_{out\_new}/Doff$. Over the following interval, *a* to *b*, when the transistor is turned off, this excess current is used to replace the lost capacitor charge that occurred during the transistor on time. In that way, the fastest possible recovery time to the new steady state is achieved. On the other hand, as already explained in the introduction, unlike in direct energy transfer converters, for indirect energy transfer topologies, the time optimal response does not necessarily result in the minimum output voltage deviation.

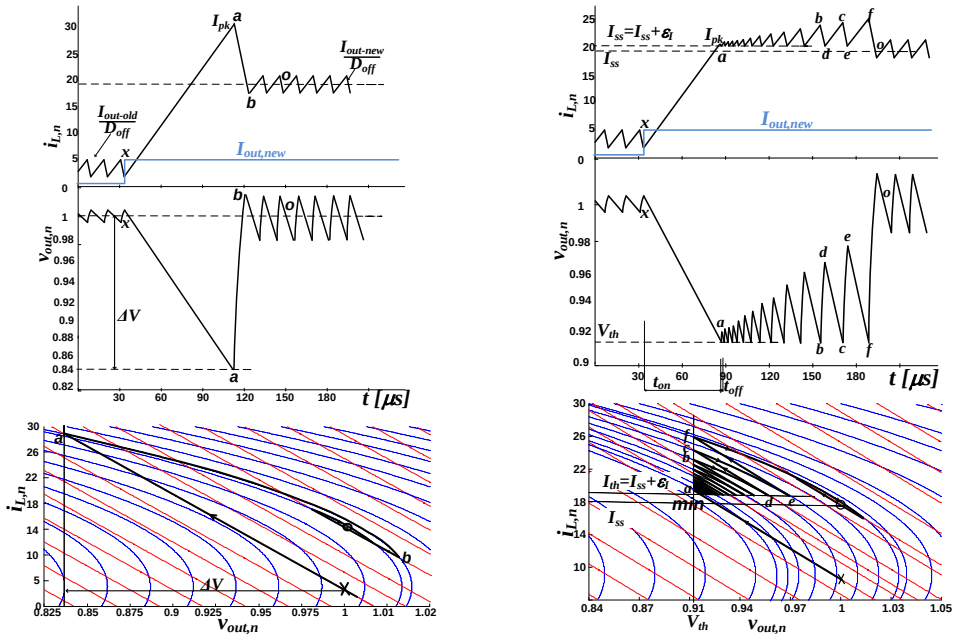
A solution to this problem is provided by the programmable deviation controller. The recovery from a transient is performed in a two-step process. Upon detection of a transient, during the first step, the transistor of the boost is turned on. Over this period, the controller estimates the new load current, and accordingly, sets two lower limits; i.e. thresholds, for the

output voltage V_{th}, and for the inductor current I_{th}, such that the threshold inductor current is slightly larger than its defined minimum-deviation point current value of I_{min}, (by ε_I) i.e.

$$I_{th} = I_{min} + \varepsilon_I \,, \tag{2.1}$$

These two values are than used to determine the switching sequence upon the initial 'turn on' of the transistor; i.e. the switching sequence for the second phase of the recovery from the transient. The voltage threshold value is calculated such that, for a given frequency operation range, the output voltage deviation is minimum.

During the recovery phase, the transistor on-time is controlled by the voltage threshold reference, and its off-time, by the current threshold value. By comparing Figs. 2.1.a and 2.1.b, as discussed in the introduction chapter, at the expense of a slightly slower recovery time, several advantages of this implementation are achieved over a time-optimal solution. Namely, due to a shorter period in which the capacitor is discharged, a lower output voltage deviation ΔV and current stress are obtained. Also, the computational demands are significantly reduced. This is because the calculation of the switch transition point values (labeled as *a* to *e* in Fig. 2.1.b), is much simpler than the calculation of the point *a* for the time-optimal case (Fig. 2.1.a), which usually involves solving a set of nonlinear operating condition dependent equations [48], [51], [52]. The advantage can also be understood through the recognition that the programmable deviation controller eliminates the need to accurately calculate the transistor's on and off times, which are explicit parameters, and deal with the amplitudes of the signals that can be measured relatively easy. It can also be observed from Fig. 2.1.b, that the minimum voltage deviation ('min', Fig. 2.1.b) occurs when the converter operates such that a slope of the first 'on state' matches the local slope, i.e., a derivative of an 'off state' on the state-plane. As pointed out in [27] and demonstrated in [29]-[32], [60], this location is also the intersection point of the first ‘on’ state trajectory and the load line (the value of the new steady-state current – a minimal current threshold). However, convergence to the steady state (point *'0'*) from this point would require an operation at a very high switching frequency (theoretically infinite, for the case when V_{th} is equal to the minimum deviation) and, as such, is not practical. Therefore, as presented in the next paragraph (2.2.2), V_{th} is set to be slightly lower than the minimum voltage deviation, and the switching frequency range is limited.



(a) (b)

Fig. 2.1. Constant current load boost converter for light to heavy load transient control methods operation: inductor and load current (top), output voltage (middle), and state-plane representation of the voltage and current (bottom). Systems parameters are: V_{in}=12V, V_{out}=48V, I_{load} – from 1A to 4.5A. (a) ideal time-optimal controller (b) near-minimum-deviation controller.

2.1.2. Programmable-deviation control

It can be observed from Fig. 2.1.b and also from previous works [15] that choosing the first switching 'off' intersection point, exactly at the theoretically defined minimum-deviation point ('min', Fig. 2.1.b), requires high switching frequency (infinite in the ideal case), and requires more cycles to reach steady-state, which might not be practical in some applications. Therefore, a compromise has to be made between the allowed deviation, the recovery time, the switching frequency, and the current stress. As an example, Fig. 2.2 shows simulation results for the case when V_{th} is set to be 4% lower than the minimum possible deviation, and the switching frequency is limited to a practical value**.**

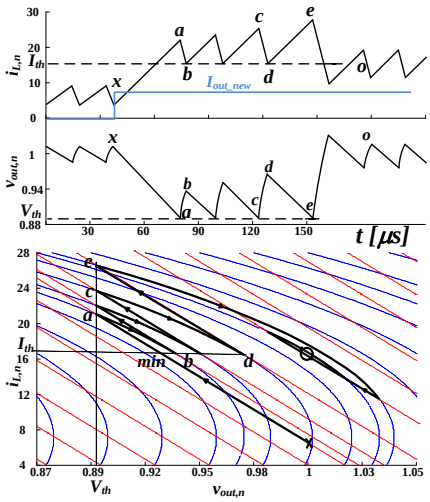


Fig. 2.2. Operation of the programmable -deviation controller in a constant current load boost converter for light to heavy load transient (maximum switching frequency is limited). Inductor and load current (top), output voltage (middle), and state-plane representation of the voltage and current (bottom). Systems parameters are: V_{in}=12V, V_{out}=48V, I_{load} – from 1A to 4.5A.

Another aspect of comparison and superiority of the programmable-deviation controller, over the time-optimal approach, is the issue of switching losses during a transient event. Considering the somewhat longer transient recovery period of the programmable-deviation control, as a time frame for comparison, it can be observed that the introduced method has fewer switching actions (Fig. 2.2) than the time-optimal one (Fig. 2.1.a). This is because the switching sequence governed by the suppression logic (comparator action) operates at a lower switching rate than the steady-state switching rate, which in the case of the time-optimal solution is resumed earlier. In addition, the programmable-deviation controller operates with a lower peak current that allows the selection of smaller power switches with lower parasitic capacitances. As a consequence, the following benefits, in the context of switching losses, are obtained: (a) a lower peak current, (b) power switches with smaller parasitic capacitance, and (c) fewer switching actions over the voltage recovery period.

2.2.Resistive load boost converter control method approach

In this section, the implementation of the minimum-deviation control method assuming a resistive load converter is considered. Here, for example, Fig. 2.3 presents the inductor current, the output current, and the capacitor voltage, during transients both in time and state-plane domains. Fig. 2.3.a. and Fig. 2.3.b. show typical light-to-heavy responses of the near minimum-deviation, and the time-optimal control methods, respectively, on a resistive load boost converter. The presented example in Fig. 2.3 illustrates the system response to a load

change from three and a half smaller output resistor loads and no change in the input voltage. Although the constant current and resistive loads have the same principle of operation, there are several differences that will be discussed in Section 2.4.

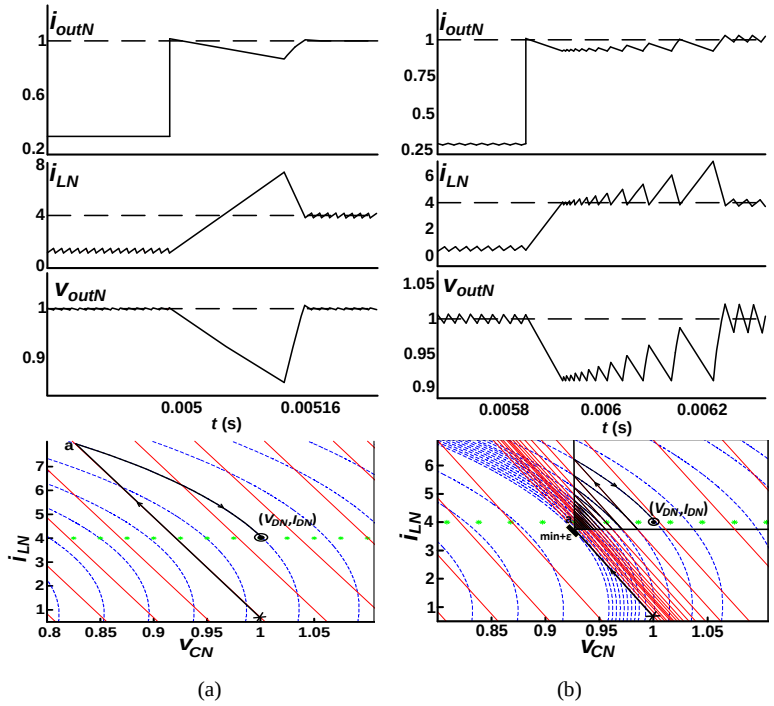


Fig. 2.3. Resistive load boost converter for light to heavy load transient control methods. Demonstrating a case which the operation is not limited by any practical constraints. Output voltage, inductor current and output current in time domain and state space plane. (a) Ideal operation of a minimum-deviation controller (b) Principal of operation of time-optimal controller.

2.3. Control approach for buck and buck-boost topologies

The graphical description and the analytical expressions of the minimum-deviation point of the buck-boost converter, as presented in Table.III, reveal that the idea, the results, and the conclusion obtained, are similar to those of the boost converter. This conclusion is foreseeable when observing the similarity between the state-equation of each of these two types of converters (Tables I and II).

For the case of direct-energy transfer converters, such as the buck converter, in contrast to indirect-energy transfer topologies, as it has already been mentioned, the time-optimal control results are not only with a minimum recovery time, but also with a minimum over-shoot.

Using the procedure presented in the next Chapter (“Locus of the minimum-deviation point”), the minimum-deviation point capacitor voltage, and the inductor current expressions,

were found for both cases of constant current, and resistive loads, for each of the discussed topologies. The results are presented in Table.III.

2.4.Resistive load vs. Constant current load

As was mentioned earlier, there are several differences between the minimum-deviation implementation results of constant current and resistive loads. First, for a constant current load step, the output current stays fixed on its new value, while in the resistive load case, it behaves as the output voltage. For the later, this means that in response to a load change, the output current will first increase itself to its new nominal value, and then, due to the drop of the output capacitor voltage, it will decrease slightly during the inductor current recovery. Secondly, as shown in Figs 2.1.b and 2.3.a, the minimum-deviation point of the resistive load is achieved for a lower capacitor voltage drop, and a lower inductor current stress, when compared to those of the constant current load case. This difference is due to the fact that for the constant current load, the inductor current must first reach the new steady-state value.

2.5.Options for minimum-deviation control implementation

It is important to mention, that the presented work's special interest is in the minimum-deviation point location on the state-space plane. Therefore, the control technique used for the second phase of the recovery from transient can be chosen. In this work, the two fixed thresholds (V_{th} *and* I_{th}) determine the switching sequence upon the initial turn on of the transistor. This way is considered to result in a significantly simpler hardware implementation. Another example, which is demonstrated in Fig. 2.4, uses one constant threshold, V_{th}, and the other threshold is the load line, which, for SMPC, represents a converter operating at infinite switching frequency, and depends only on system and state values. A power converter has a range of steady-state operating points. These points together form a load line as in traditional circuit analysis [52]. This line also gathers all the points of equal ‘on’ and ‘off’ state trajectories slopes, which are referred to, in the presented method, as the minimum-deviation points. This technique will result in a faster recovery to steady-state, and lower capacitor voltage, and inductor current deviations, during the second phase. Hence, it is more efficient in terms of energy dissipation. On the other hand, designing the load line and matching the control algorithm to it, is more complicated, and more hardware demanding, when compared to the first one presented.

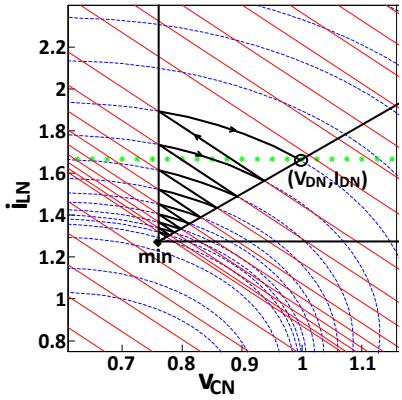


Fig. 2.4. Principle of operation of a proposed modified controller implemented on a resistive load boost converter for L-to-H load transient.

3. Locus of the minimum-deviation point

3.1. Introduction

One of the objectives of this research is to describe the system in its most general form. Therefore, the state-space plane is examined as a geometrical space. By knowing the trajectory's behavior and shape, the state-space can be used to extract information about the minimum-deviation point.

The thresholds of the output voltage and the inductor current, during a light-to-heavy load transient, are selected such that the voltage deviation is minimized, and at the same time, the converter has sufficient energy to converge to the new operating point. That is, the inductor current that is reflected to the output has to be larger than the new steady-state output current value, in order to restore the charge balance of the output capacitor. An explanation of this conjecture can be found from the state trajectories of Fig. 2.2. They show that, to facilitate a trend of voltage increments, toward the steady-state point '*0*', from a starting of point '*x*', the initial 'on' time must be long enough to ensure that the following 'off' time starts at a point where the inductor current is higher than the current of the next 'on' time. In Fig. 2.2, those two points are labeled as *a* and *b*, respectively. From the state-space point of view, this means that the inductor current must climb up the on-trajectory to a point where the slope of the trajectory is equal to, or greater than, the slope of an intersecting off-trajectory (point 'min', Fig. 2.2). Therefore, the precise location of the minimum-deviation point on the state space plane can be derived by solving several equations, defined mostly by using simple geometrical arguments. More details will be given in the following section.

Next, the general idea used, in order to find the analytical expression for the discussed theoretical minimum-deviation point, is represented only by the known system parameters, and is explained through examples. For the following derivations, it was assumed that all of the components are ideal, and that the new value of the load current step is known.

3.2.Process of finding the minimum-deviation point

3.2.1. Boost converter

3.2.1.1. Constant current load

Here, for example, this process of expressing the minimum-deviation point is performed on a constant current load boost converter. In this particular case, the minimum-deviation point can easily be found by comparing the ‘on’ state equation slope (3.1), with the appropriate ‘off’ state equation slope (3.2), and then extracting the minimum-deviation point current (3.3) and voltage (3.4) using algebraic manipulations of the ‘on’ state equation (1.6).

$$m_{onN} = \left.\frac{di_{LN}}{dv_{CN}}\right|_{'on'} = -\frac{V_{inN} R_N}{V_{oN} Z_{rN}^2}, \tag{3.1}$$

$$m_{offN} = \left.\frac{di_{LN}}{dv_{CN}}\right|_{'off'} = \frac{\left(V_{inN} - V_{oN}\right) R_N}{\left(i_{LN} - \frac{V_{oN}}{R_N}\right) Z_{rN}^2}, \tag{3.2}$$

$$I_{\min N} = \frac{V_{oN}^2}{V_{inN} R_N} = \frac{I_{oN}}{D_{offN}}, \tag{3.3}$$

$$V_{\min N} = v_{C0N} - \frac{Z_{rN}^2 I_{oN}}{V_{inN}} \left(\frac{I_{oN}}{D_{offN}} - i_{L0N} \right), \tag{3.4}$$

3.2.1.2. Resistive load

For the example of a resistive load boost converter, the process for obtaining the discussed tangent point was simplified by using some basic concepts of the circle theory. For this purpose, the ‘off’ state trajectory equations were normalized (3.5), in a way that instead of an ellipse form a circulate form, (3.8) was obtained.

$$i_{LN}^* = i_{LN} \cdot Z_{rN}\,, \tag{3.5}$$

Using the above defined new normalization (3.5), the appropriate normalized ‘on’ state solution was also obtained (3.6).

$$\left(i_{LN}^* - i_{L0N}^*\right) = -\frac{V_{inN} \cdot R_N}{v_{C0N} \cdot Z_{rN}} \left(v_{CN} - v_{C0N}\right), \tag{3.6}$$

According to (3.6), the solution is a linear function written in a slope-intercept form. Hence,

the slope is immediately given by,

$$m_{onN} = -\frac{V_{inN} \cdot R_N}{v_{C0N} \cdot Z_{rN}}, \tag{3.7}$$

The resulted off-state trajectory equation (3.8) describes a circle in the new normalized state-space plane ($v_{CN}(t)$ vs. $i_{LN}^*(t)$), which is centered on $\left(V_{inN}, i_{L2N}^*\right)$, and its radius r is given by $\sqrt{\left(v_{C1N} - V_{inN}\right)^2 + \left(i_{L1N}^* - i_{L2N}^*\right)^2}$.

$$\left(v_{CN} - V_{inN}\right)^2 + \left(i_{LN}^* - i_{L2N}^*\right)^2 = \left(v_{C1N} - V_{inN}\right)^2 + \left(i_{L1N}^* - i_{L2N}^*\right)^2, \tag{3.8}$$

where: $i_{L2N}^* = \frac{v_{C1N}}{R_N} \cdot Z_{rN}$

Since v_{C1N} is the initial capacitor voltage off-time condition, which is the minimum-deviation voltage, i_{L2N}^* can be expressed by (3.9).

$$i_{L2N}^* = \frac{V_{\min N}}{R_N} \cdot Z_{rN}, \tag{3.9}$$

According to the geometry of a circle, a tangent line to a circle at a point on the circle's circumference is perpendicular to the radius to that point. Fig. 3.1 illustrates the geometrical relationship needed in order to complete the approach. The start point indicated as $\left(v_{C0}, i_{L0}^*\right)$ represents the last previous steady-state operating point before a transient occurred.

As it can be observed in Fig. 3.1, based on the geometrical relationship between the on-time trajectory, and the tangent off-time trajectory, the slope of the straight line between the tangent point and this off-time circle center is determined by the on-time trajectory, as given in (3.10),

$$m_{2N} = -\frac{1}{m_{onN}} = \frac{v_{C0N} \cdot Z_{rN}}{V_{inN} \cdot R_N}, \tag{3.10}$$

Substituting the minimum-deviation point in equation (3.6), will result with equation (3.11), and its appropriate normal equation is presented in (3.12).

$$\left(I^*_{\min N} - i^*_{L0N}\right) = -\frac{V_{inN} \cdot R_N}{v_{C0N} \cdot Z_{rN}}\left(V_{\min N} - v_{C0N}\right), \tag{3.11}$$

$$\left(I^*_{minN} - i^*_{L2N}\right) = \frac{v_{C0N} \cdot Z_{rN}}{V_{inN} \cdot R_N}\left(V_{minN} - V_{inN}\right), \tag{3.12}$$

Now, simple algebraic manipulations on the above equations ((3.11) and (3.12)), and then a transformation back to the original state-space coordinate system ($v_{CN}(t)$ vs. $i_{LN}(t)$), result in the minimum-deviation point capacitor voltage (3.13) and the inductor current (3.14) expressions.

$$V_{minN} = v_{C0N} - \frac{R_N D_{offN}\left[\frac{I_{TN}}{D_{offN}} - i_{L0N}\right]}{1 + D_{offN} + \frac{R_N^2 \cdot D_{offN}^2}{Z_{rN}^2}}, \tag{3.13}$$

$$I_{minN} = \frac{I_{TN}}{D_{offN}} - \frac{1 + D_{offN}}{1 + D_{offN} + \frac{R_N^2}{Z_{rN}^2} \cdot D_{offN}^2}\left[\frac{I_{TN}}{D_{offN}} - i_{L0N}\right], \tag{3.14}$$

As it can be observed from the obtained analytical results of the constant current load case, given in equations (3.3) and (3.4), and when compared to those of the resistive load case given in (3.13) and (3.14), as long as the initial on-state current, i_{L0N}, is lower than the target current, $\frac{I_{TN}}{D_{offN}}$, the minimum current stress and voltage drop will be lower for the resistive load case.

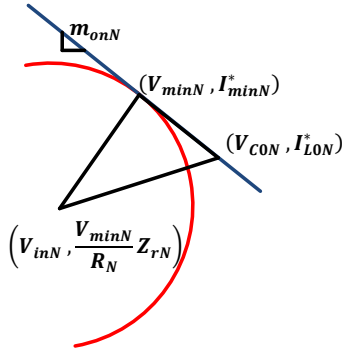


Fig.3.1. Geometrical way for expressing the minimum-deviation point for indirect energy transfer

3.2.2. Buck and buck-boost converters

Since a buck-boost description can be obtained by only shifting the boost 'off' trajectory circles centered by V_{inN}, the process of finding the minimum-deviation point and the resulted conclusions, presented for the boost converter, are also valid for the case of the buck-boost converter. The results are presented in Table. III.

For the presented direct energy transfer converter, buck, finding the minimum-deviation point locus is different from the one presented for the indirect energy transfer topologies. According to Tables. I and II, solving the state-equations for the buck converter results, with both 'on' and 'off' state-space trajectories having an elliptical shape, at the 'on' trajectories will be centered on the input voltage, and the 'off' trajectories will be centered on zero voltage.
In this case, the defined minimum-deviation point current is the same current of the appropriate 'on' ellipse center. Also, since this is a direct energy transfer case, the minimum-deviation point current is the point where the inductor current and the output current are equal. Therefore, the relationship between the minimum-deviation point current and the voltage can be written as:

$$I_{\min N} = \frac{V_{\min N}}{R_N}, \tag{3.15}$$

Now, all that is left is to substitute (3.15) in the 'on' state equation of the resistive (Table. II), or the constant current (Table. I) load buck converter. As a result, an equation with one variable, V_{minN}, will be left, and finally expressions for V_{minN} and I_{minN} will be derived.

The point that represents the center of the circle is also the valley inductor current point, hence, for the constant current load case, this point is also the target current, I_{DN}.

4. Minimum-deviation control (heavy-to-light) geometrical approach

4.1.Introduction

As it was previously mentioned, when there is an abrupt transition from a light load to a heavy load, the output voltage drop is proportional to the resistance ratio. In the case where there is a transition from a heavy to a light load, the circuit operates in the opposite manner; the capacitor voltage will increase, and the inductor current will drop along the path to a new steady-state point.

For heavy-to-light transitions (Fig. 4.1 and Fig. 4.2), the control operation principle is similar to this of the buck converter in a light-to-heavy load transition. In both cases, the time-optimal control [51]-[52], [54]-[56] which is characterized by a minimum recovery time for step-load transients, also results in a minimum possible capacitor voltage and inductor current deviations. In the heavy-to-light transition case, where a minimum-deviation control strategy is adopted, the transistor is turned off until the output voltage recovers from the initial overshoot, and then goes back to its steady state value. Thereafter, the steady-state, i.e. PI, mode of controller operation is resumed, with the initial inductor current reference set to be equal to the estimated steady-state value.

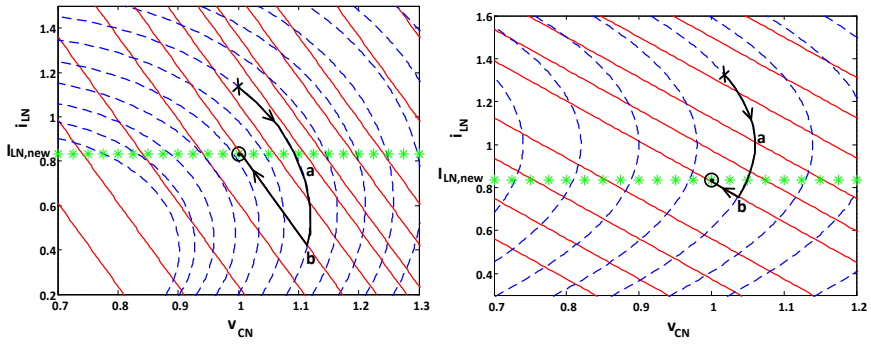
4.2.Control geometrical approach and examples

It can be observed from Fig. 4.1 and Fig. 4.2 that the recovery from heavy-to-light transient starts with turning the transistor 'off', until the inductor current is smaller than the new load current nominal value, or its equivalent in state-space, until the state is at the point where the trajectory slope changes from negative to positive (point ‘a’, Fig. 4.1). This point is the absolute minimum-deviation of the trajectory [27], [60]. Turning the transistor on before this point will result in a larger overshoot, a longer transient, and may cause a runaway situation [28] (i.e. the output voltage continues to increase). The intuitive physical explanation for this is that the inductor current is still higher than the load current, and that any additional charge will increase the deviation. Once this point is reached, one may select the switching sequence towards a steady state. This can be done either in small increments,

similar to the presented minimum-deviation control for a light-to-heavy case, or by keeping the transistor ‘off’, until the output voltage reaches the time-optimal switching point; then it will switch on until the trajectory reaches the new steady state point (point ‘O’, Fig. 4.1), the same as for the time-optimal case. Since either of these methods will result in the same overshoot, the latter has been adopted in this work, because it involves fewer transitions, and therefore, is faster, and requires less computing resources.

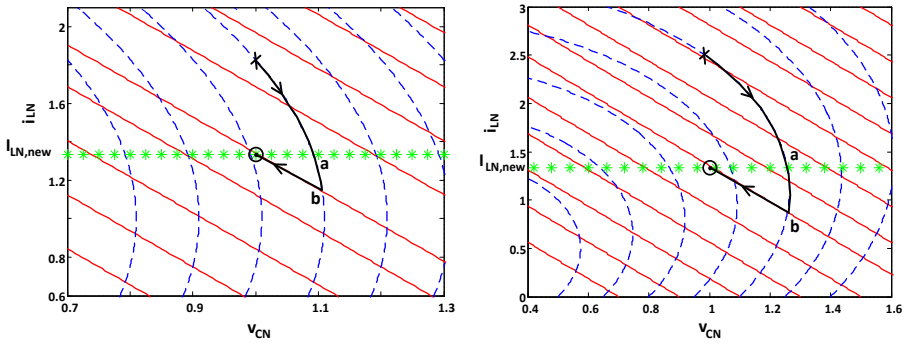
This converter control law can, in theory, achieve a steady-state operation, within one ‘on’ and ‘off’ switching cycle, regardless of the system's initial state or operating conditions.

Fig. 4.1 presents the state space-plane principle of the operation of the proposed minimum-deviation controller, for the dc-dc boost converter, in the case of heavy-to-light load transition. Fig.4.1.a shows the control operation of the constant current load case, and Fig.4.1.b shows the control operation of the resistive load case. It can be seen that the main difference between the constant and resistive loads, is in the fact that for the former, the 'off' ellipse center current remains constant, while for the latter, it changes as a function of the initial state.



(a) (b)

Fig. 4.1. State-plane representation of the voltage and current presenting the operation of the programmable-deviation controller in a boost converter for heavy-to-light load transient: (a) for the constant current load case (b) for the resistive load case.



(a) (b)

Fig. 4.2. State-plane representation of the voltage and current presenting the operation of the programmable-deviation controller in a buck-boost converter for heavy-to-light load transient: (a) for the constant current load case (b) for the resistive load case.

As it can be seen from Fig. 4.2, in the case where the buck-boost converter is considered, the direction and the path from the starting point (indicated with ‘X’), to the target point (indicated as ‘O’), is the same as for the boost converter (Fig. 4.1); the only difference is in the current and voltage references.

And finally, in the case of the buck topology, the procedure is similar to the one used for the light-to-heavy load transient; the only difference is the opposite direction order of moving along the trajectories.

5. Stability analysis

5.1.Introduction and motivation

The presented minimum-deviation control method establishes a new operational methodology for SMPSs, which is based on a large-signal controller design, rather than on the conventional linear small-signal operation. In this case, derivation of the system stability by the conventional small-signal tools, such as the loop-gain analysis, is no longer valid. There are a few reported cases in the literature, e.g., [29]-[32], [47]-[48], that investigated the large-signal system stability of SMPSs for particular cases of boundary control and buck converter. Analytical analysis and tools from control theory were applied on the models developed to investigate system control, and were applied in an attempt to gain a better understanding and potentially develop a generic stability criteria for such systems.

Here, in order to theoretically ensure the existence and the stability of the system under the presented results (Table. III) of a minimum-deviation control qualitative approach, a stability analysis was performed based on Lyapunov's second theorem [83]-[85].

Variable structure systems (VSS) [108]-[109] are systems by which their structure varies over different parts of their state-space, during time, and with respect to the structure control law. Switched-mode power supplies are generally variable structured systems because of the presence of a switching action. A known favored derivation of the variable structure control system theory is the sliding mode (SM) control [57]-[61].

The motivation of the research is to prove that the suggested qualitative definition for the minimum-deviation point is applicable to be the first point where it is allowed for the first switching action to occur. Hence, for the purpose of stability analysis, there is no need to define the switching system in the same way as the suggested minimum-deviation control technique does, because such a process is complicated, and more importantly, unnecessary for the purpose of only approving the suggested definition. Hence, in order to ease the process of stability investigation, the sliding surface denoted as S was chosen as a linear function (5.1) of the state variables.

5.2.Stability analysis for a minimum-deviation control method

5.2.1. Minimum-deviation stability proof

The presented stability analysis method can be used for all three dc-dc converters and it is illustrated here in detail only for the boost converter. The results are then given also for the two other converters.

The stability problem was investigated using mathematical tools. For this purpose, it was first considered that the sliding surface is expressed by the convenient popular way of a linear combination of the two defined state variables (5.1) being equal to zero. This way, studying and examining the stability of trajectories, on the sliding surface, can be done by applying the theory of linear differential equations, which simplifies the analytical problem.

$$S = \hat{i_L} - \lambda \hat{v_C}, \tag{5.1}$$

$$\hat{i_L} = i_L - I_D \quad ; \quad \hat{v_C} = v_C - V_D, \tag{5.2}$$

where $\hat{i_L}$ and $\hat{v_C}$ represent the inductor current and the capacitor voltage errors (5.2) with respect to the new steady-state point, respectively, and λ represents the slope of this switching function. This slope is attributed as a control parameter, since it expresses the dependence of the sliding surface of the system's characteristics. Since only the ideal case of an SM control is necessary for the presented stability analysis, no practical considerations were included in the sliding surface definition (5.1).

The description of all reviewed converters may be expressed in the following compact form (5.3) which also represents the control problem definition.

$$\dot{x} = Ax + Bu + D, \tag{5.3}$$

where u is the control input defined by the switch position, and x indicates the system state error variables vector defined by (5.4).

$$x = \begin{bmatrix} x_1 & x_2 \end{bmatrix}^T = \begin{bmatrix} \hat{v_C} & \hat{i_L} \end{bmatrix}^T = \begin{bmatrix} v_C - V_D & i_L - I_D \end{bmatrix}^T, \tag{5.4}$$

For the case of the resistive load boost converter, equation (3.1) coefficient matrices are defined by (5.5).

$$A=\begin{bmatrix} 0 & \frac{1}{C} \\ -\frac{1}{L} & 0 \end{bmatrix} \;;\; B=\begin{bmatrix} -\frac{\hat{i_L}+I_D+\frac{v_{C0}-v_{C1}}{R}}{C} \\ \frac{\hat{v_C}+V_D}{L} \end{bmatrix} \;;\; D=\begin{bmatrix} \frac{I_D}{C}-\frac{v_{C1}}{RC} \\ \frac{V_{in}-V_D}{L} \end{bmatrix}, \tag{5.5}$$

In the following, the condition for the existence and the reachability of the sliding mode which is guaranteed, if both the sliding surface function, S, and its derivative $\dot{S}$, approach zero, when $t \to \infty$ is first presented. This will ensure that the system dynamics will reach and be maintained on the sliding surface. Then, the conditions for the stability of motion in the sliding regime will be determined.

$$\begin{cases} \frac{dS}{dt}=\frac{dx}{dt}\cdot\nabla S>0 \;\;;\;\; 'on'\,(S<0) \\ \frac{dS}{dt}=\frac{dx}{dt}\cdot\nabla S<0 \;\;;\;\; 'off'\,(S>0) \end{cases}, \tag{5.6}$$

when,

$$\nabla S=\begin{pmatrix} \frac{dS}{dx_1} \\ \frac{dS}{dx_2} \end{pmatrix}=\begin{pmatrix} \frac{dS}{d\hat{v_C}} \\ \frac{dS}{d\hat{i_L}} \end{pmatrix} \;\;;\;\; \frac{dx}{dt}=\begin{pmatrix} \frac{dx_1}{dt} \\ \frac{dx_2}{dt} \end{pmatrix}^T=\begin{pmatrix} \frac{d\hat{v_C}}{dt} \\ \frac{d\hat{i_L}}{dt} \end{pmatrix}^T, \tag{5.7}$$

Equations (5.6) and (5.7) present the general form of the existence and the reachability of the sliding mode condition. As can be seen from (5.8), substituting (5.7) in (5.6) results in a simplified form of the existence condition.

$$\begin{pmatrix} \frac{d\hat{v_C}}{dt} & \frac{d\hat{i_L}}{dt} \end{pmatrix}\cdot\begin{pmatrix} \frac{dS}{d\hat{v_C}} \\ \frac{dS}{d\hat{i_L}} \end{pmatrix}\begin{matrix} >_{'on'} \\ <_{'off'} \end{matrix} 0, \tag{5.8}$$

Expanding (5.8) for the case of the resistive load boost converter ((5.2)-(5.4)) in terms of the slope λ results with,

$$\begin{cases} \lambda > -\dfrac{RC}{v_{C0}}\dfrac{V_{in}}{L} & ;\ 'on'\,(S<0) \\ \lambda < -\dfrac{C}{L}\left(\dfrac{v_C - V_{in}}{i_L - \dfrac{v_{C1}}{R}}\right) & ;\ 'off'\,(S>0) \end{cases}, \tag{5.9}$$

The slope of the sliding surface needs to be chosen to satisfy (5.9) in order to ensure the sliding mode existence. The 'on' state condition in (5.9) is usually more stringent [61], and hence, this is the one that will be used to define the appropriate range of slopes.

Now, after wording the condition for the existence and the reachability of the sliding mode, the next step will be to define the condition for the stability of motion in the sliding regime.

Satisfying the condition for the stability of the sliding regime response will guarantee that the system trajectories travelling along the surface will move towards the desired steady-state operating point. In order to define this condition, first, there is a need to find the relationship between the inductor current and the capacitor voltage, without solving the differential state equations. To this end, the equivalent control method will be used.

The equivalent control is an analytical tool that mostly serves to study the behavior, and to obtain an overall description, of a system under SM control [58], [61].

For the sake of generality, u is attributed to be the general control input, and it is composed of a sum of the two control input components (5.9). One is a nonlinear component, the switching component u_n (5.10), which is used in order to eliminate the parameter uncertainties and external disturbances [58], [61]. The second is the equivalent control component u_{eq}, which is the average input control signal [58]-[61], and it is a function of the nominal parameters of the system. The equivalent control component will guarantee that the sliding mode trajectories of the system are driven to the surface $S(x)=0$.

$$u = u_{eq} + u_n, \tag{5.10}$$

$$u_n = k_1 sgn(S), \tag{5.11}$$

where k_1 is a negative constant [120]-[123], and $sgn(S(x))$ is defined as follows,

$$sgn\left(S\left(x\right)\right)=\begin{cases}+1\,;S\left(x\right)>0\\-1\,;S\left(x\right)<0\end{cases}, \tag{5.12}$$

Under the ideal SM, it is assumed that the point that represents the present state of the system stays on the sliding surface $S=0$, hence, the time derivatives of the sliding surface equal zero. In the presented case, the relevant derivative is $\frac{dS}{dt}=0$. This is used in order to find the equivalent control input. In this case, applying the equivalent control method to the chosen dynamic system equation (5.1), results in the equivalent control input's appropriate definition of u_{eq} (5.13).

$$u_{eq}=-\left[\frac{\partial S}{\partial x}B\left(x\right)\right]^{-1}\left(\frac{\partial S}{\partial x}Ax+\frac{\partial S}{\partial x}D\right), \tag{5.13}$$

For the case of the resistive load boost converter (5.5), the equivalent control can be written as presented in (5.14).

$$\bar{u}_{eq}=\frac{V_{in}-L\frac{di_L}{dt}}{v_C}, \tag{5.14}$$

where $\bar{u}$ is defined as the complementary of u, meaning that: $\bar{u}=1-u$.
Substituting the obtained complementary equivalent control signal (5.14) in (5.3)-(5.5) results in,

$$Ri_L\left(V_{in}-L\frac{di_L}{dt}\right)=v_{C0}v_C+RCv_C\frac{dv_C}{dt}-\left(v_{C0}-v_{C1}\right)\left(V_{in}-L\frac{di_L}{dt}\right), \tag{5.15}$$

In order to obtain a good small signal, as well as a power band-width for the practical converters, it is necessary to assume (5.16) [61].

$$V_{in}>>L\frac{di_L}{dt}, \tag{5.16}$$

This assumption ensures that the inductor current ripple is less than twice the input current in the boost converter case, which is a necessary condition for the convergence under the CCM mode operation, that is characterized with lower ripple currents and a more steady operation when compared to the DCM mode. Practically, this assumption is legitimate, since typically, designers are careful to choose the current ripple to be up to 20% of the average current.

Therefore equation (5.15) reduces to,

$$i_L = \frac{v_{C0} v_C}{R V_{in}} + \frac{C v_C}{V_{in}} \frac{dv_C}{dt} - \frac{1}{R}\left(v_{C0} - v_{C1}\right) \ , \tag{5.17}$$

The relationship between the inductor current and the capacitor voltage, which was obtained in (5.17), can also be expressed in terms of the error voltage and the current (5.2), as shown in equation (5.18),

$$\hat{i_L} + I_D = \frac{v_{C0}\left(\hat{v_C} + V_D\right)}{R V_{in}} + \frac{C\left(\hat{v_C} + V_D\right)}{V_{in}} \frac{d\left(\hat{v_C} + V_D\right)}{dt} - \frac{1}{R}\left(v_{C0} - v_{C1}\right), \tag{5.18}$$

For the next steps, the expression obtained in (5.18) should be separated into two parts; one part represents the dc part, I_{DC} (5.19), and the other represents the ac part, i_{AC} (5.20),

$$I_{DC} = I_D = \frac{v_{C0} V_D}{R V_{in}} - \frac{1}{R}\left(v_{C0} - v_{C1}\right), \tag{5.19}$$

$$i_{AC} = \hat{i_L} = \frac{v_{C0}}{R V_{in}} \hat{v_C} + \frac{C \hat{v_C}}{V_{in}} \frac{d\hat{v_C}}{dt} + \frac{C V_D}{V_{in}} \frac{d\hat{v_C}}{dt}, \tag{5.20}$$

In this case, in order to simplify the calculations, a substitution (5.21) will be used.

$$R_s = -\frac{1}{\lambda}, \tag{5.21}$$

Substituting the expression for the inductor current obtained in (5.20) in the sliding surface equation (5.1) results in,

$$S = a(t)\hat{v_C} + b(t)\frac{d\hat{v_C}}{dt}, \tag{5.22}$$

The equivalent control is used when a sliding regime exists, meaning $S(x)=0$. As a consequence, a first order differential equation is obtained from (5.22), and its solution is presented by (5.23)-(5.24).

$$\hat{v_C}(t) = \exp\left(-\frac{a(t)}{G + G\frac{\hat{v_C}(t)}{V_D}} t \right), \tag{5.23}$$

where,

$$G = \frac{CR_s V_D}{V_{in}}, \tag{5.24}$$

Algebraic manipulations of equation (5.23) result with equation (5.25).

$$G \cdot ln\left(\hat{v_C}(t)\right) + \frac{G}{V_D}\hat{v_C}(t)ln\left(\hat{v_C}(t)\right) = -a(t)\cdot t, \tag{5.25}$$

The condition for guaranteeing the stability of response along the sliding surface (5.26) was derived from equation (5.25), for the asymptotic reaction (i.e. $t \to \infty$, $\hat{v_C}(t)$ is decreasing). Also, since the current and voltage of the minimum-deviation point are necessarily lower than those of the steady state point, only the region where the slope λ is positive is relevant. Based on the definitions given in (5.21) and (5.24), it can be determined that $G < 0$. These two claims provide the desired stability condition which is $a(t) < 0$, or in slope terms:

$$\lambda < \frac{v_{C0}}{RV_{in}}, \tag{5.26}$$

As can be seen from (5.26), this result fits the physical definition of the minimum-deviation point. This slope represents the surface, where the current of each point on this surface equals v_o/RD_{off}, when v_o represents the output current of this point. Therefore, first time switching 'off' at this point means, that the first switch is done at the point, where the inductor current equals the current reflected to the output. This is the minimal inductor current needed for the inductor to start feeding the load, instead of the output capacitor, so the output voltage could start evolving back to the desired steady-state voltage.

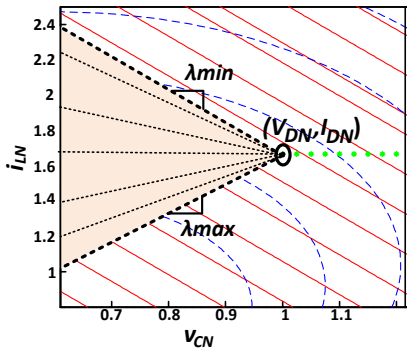
The slope (5.27) is defined with respect to the desired new steady-state point, (V_D, I_D).

$$\lambda = \frac{I_L - I_D}{V_C - V_D}, \tag{5.27}$$

where (V_{CN}, I_{LN}) is a chosen point on the sliding surface.

5.2.2. Stability analysis results and conclusions

The presented results in (5.28) and Fig. 5.1 summarize the slope (λ) of the sliding manifold's s conditions for the stability and the existence of the chosen surface in the case of a resistive load boost converter.



(5.28

Fig. 5.1. Slopes available region presented in the resistive load boost converter state-space plane diagram.

It is important to emphasize that these conditions (5.27) are tight, since they are necessary conditions for the system's response stability.

In order to find the slope of the surface that connects the minimum-deviation point with the steady-state point, it is necessary to substitute the appropriate analytical expression for (V_{min}, I_{min}) listed in Table. III in (5.26) instead of (V_C, I_L). The result is indicated as $\lambda_{\min\_dev}$ and presented by (5.29).

$$\lambda_{\min\_dev} = \frac{v_{C0}}{RV_{in}} + \frac{1}{R}, \tag{5.29}$$

It is claimed that only the points of lower a capacitor voltage and a higher inductor current, from those of the minimum-deviation point, could have a stable response in the sense of Lyapunov. Otherwise, the inductor won't be charged enough to be able to start feeding the load instead of the output capacitor. As a result, the output capacitor voltage won't return back to its steady-state value, meaning that the system won't be stabilized. Accordingly, the condition presented in (5.30) must exist.

$$\lambda \le \lambda_{\min\_dev}, \tag{5.30}$$

By comparing the resulted upper limit of the slope range obtained by the stability analysis (5.28), with the slope range determined by the minimum-deviation process (5.29)-(5.30), it is

clear that the difference between the two is a factor of $\frac{1}{R}$. This difference has a very little relative practical affect on the result. It is important to note that there is an inherent difference between the geometrical and the stability-analysis approaches. Indeed, the minimum-deviation point obtained by the geometrical approach, guarantees, that the system will not diverge, given that some practical operating conditions are met, and that the first-order Taylor approximation is valid. On the other hand, the minimum-deviation point obtained by the stability analysis, guarantees that the system will converge to the new steady-state.

Equalizing the slope range's upper limit, obtained by the stability analysis (5.28), with the slope definition (5.27), will result in the analytical expression of the deviated minimum-deviation point indicated by (V_{min} , I_{min}). Eq. (5.31) presents the normalized (1.9) result for the case of the resistive load boost converter.

$$\left\{\begin{array}{l} V_{mind\,N} = v_{C0N} - \dfrac{R_N D_{offN}\left[\dfrac{I_{TN}}{D_{offN}} - i_{L0N}\right]}{1+\dfrac{R_N^2 \cdot D_{offN}^2}{Z_{rN}^2}} \\ I_{mind\,N} = \dfrac{I_{TN}}{D_{offN}} - \dfrac{\left[\dfrac{I_{TN}}{D_{offN}} - i_{L0N}\right]}{1+\dfrac{R_N^2 \cdot D_{offN}^2}{Z_{rN}^2}} \end{array}\right\}, \tag{5.31}$$

Accordingly, it can be concluded, that the suggested method to find the minimum-deviation point, derived in Subsection 3.2, is the outcome of the presented stability analysis. Moreover, since the obtained slope formula in (5.26), or in (5.29), is independent of the initial current, i_{L0}, it can be concluded, that this slope appropriate surface, connects all the minimum-deviation points for the different load steps.

Another definition approved by the presented stability analysis was of the lower limit of the sliding manifold slope, which defines the appropriate time-optimal paths with a stable behavior for any load step defined by i_{L0}. This slope is the lower limit of the slope range (5.28), which defines the manifold that ensures that a system trajectory on the manifold will converge to the steady-state point. Any intersection point under this surface, where this point 'off' trajectory meets the steady state point, defines an appropriate stable time-optimal path according to its initial state ('X', Fig. 5.2). Meaning that, moving along this path will result, with one switching in order to return the system back to steady state. This point of switching

in the case of time optimal, represent the point, where there is enough current to compensate for the total charge needed for, the current step, and for the loss of charge in the capacitor during the inductor charging. Fig. 5.2 shows an example of different stable time-optimal control paths, which differ by their initial state ('X', Fig. 5.2). Each path includes only one switching action, which is represented by the intersection point between the appropriate 'on' trajectory, and the 'off' trajectory that meets the steady-state point. All these time-optimal paths exist under the manifold upper limit, represented by a black dashed line in Fig. 5.2. This is a reasonable conclusion, under the fact that this slope is also equal, to the slope of the 'on' state trajectory that its initial state is the steady-state point, meaning that, this line defines the limit of optional 'on' trajectories, which are part of a stable time-optimal path, leading to the steady-state point.

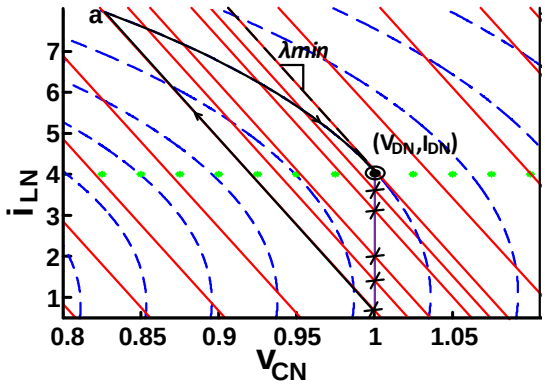


Fig. 5.2. Resistive load boost converter for light to heavy load transient. Time-optimal response to different step-load transients is illustrated.

The same procedure of stability analysis was also done for the constant current load boost converter. The resulted range of slopes for this case is given in (5.32). The minimum-deviation point derived from the upper limit of the resulted stability condition (5.32) is identical to the one obtained by the minimum-deviation procedure (Table. III.a and Table. III.b).

$$\begin{cases} -\dfrac{RC}{v_{C0}}\dfrac{V_{in}}{L} \le \lambda \le 0 \\ \lambda = \dfrac{I_L - I_D}{V_C - V_D} \end{cases}, \qquad (5.32)$$

For the buck-boost converter, exactly the same slope range as for the boost converter was obtained for both of the resistive load case (5.28) and the constant current load case (5.32).

The deviated minimum-deviation point expression can easily be obtained in the same way as was presented for the case of the boost converter.

The same control stability analysis was also performed for the buck converter. The resulted upper slope limit (5.33) is exactly the same as the one obtained by the minimum-deviation approach (Table. III). As it has already been explained, in the case of the buck converter, the time-optimal control law also results with minimum deviation, therefore, the slope range (5.33) is limited only from one side. Also, as it has already been explained for the case of the indirect energy transfer converters, this slope is legit by the physical definition of the minimum-deviation point. First switching 'off' at any point on the surface defined by this slope, means, that the first turn 'off' is at the point, where the inductor current is equal to the output current, v_o/R, which is the current reflected to the output in the case of the direct energy transfer converter.

$$\begin{cases} \lambda \le \dfrac{1}{R} \\ \lambda = \dfrac{I_L - I_{ref}}{V_C - V_{ref}} \end{cases}, \tag{5.33}$$

The good correlation between the results of the minimum-deviation control law, and the appropriate stability analysis condition, approve the stability of the system under the minimum-deviation control. Meaning that, stability in the sense of Lyapunov is guaranteed, when using the minimum-deviation control method.

6. Practical Implementation and Experimental Results

In this chapter, an evaluation of the performance of the proposed robust minimum-deviation control design, via the resistive load boost converter topology example, is presented.

To demonstrate the effectiveness of the introduced programmable deviation control method, and to verify the theoretical analysis, an experimental prototype was constructed, based upon the diagram shown in Figs. 6.22, and 6.12. The 12 V to 48 V, 100 W resistive load boost converter operates at a switching frequency of 100 kHz. The digital controller was implementing the PI steady-state control law, and the new transient recovery algorithm was implemented, with an FPGA based prototype [32] and readily available analog to digital converters. In the following, first, the chosen converter design parameters will be presented, then the chosen linear control design and implementation will be discussed, and finally, the total control system design and implementation will be examined and verified.

6.1. Boost converter application - peripherals

6.1.1. Design parameters and specifications of the examined converter

Table. IV and Table. V summarize the design parameters and the main component selection of the experimental prototype, accordingly.

Parameter	Value	Notes
C_{out}	30 µF	
L	150 µH	
R_{old}	100 Ω	
R_{new}	40 Ω	
R_{tot}	~29 Ω	
R_{sense}	0.1 Ω	For current sense
f_s	100 kHz	Nominal switching frequency
D	0.75	Nominal duty-cycle
V_{in} (max.)	12 V	
V_{out} (max.)	48 V	
I_{out}	0.5 A → 1.7 A	Output current step
P_{out} (max.)	100 W	

Table. IV. Parameters of the experimental prototype.

Component	Name	Notes
MOSFET	BUZ11	NMOS
Inductor	ETD29, 3F3	
Output diode	D10L20U	Shottky
Driver	IR2113	
FPGA	EP4CE115F29C7	
Comperator	MAX912	
Current amplifier	EL2250C	Bandwidth: 125 MHz

Table. V. Components selection of the experimental prototype.

6.1.2. Current sense

The inductor current was sensed with a low value sense resistor R_{sense} of 0.1Ω. Fig. 6.1 shows in detail the current sense and the amplification unit. The measured voltage across R_{sense} represents the inductor current by the relationship of $K_I i_L$, where K_I is the current amplification factor. This voltage is then amplified in order to suit the voltage rate of the current comparator input ports. Then, it enters the positive port of the current comparator ($Comp_I$) and compared with the reference current obtained from the FPGA.

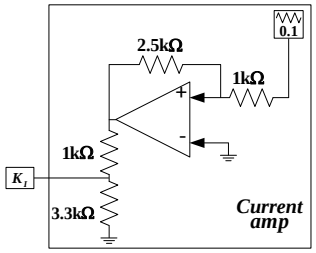


Fig. 6.1. Current sense model.

6.2. Linear control design and implementation

6.2.1. Abstract

In this section, the design and implementation of a full FPGA oriented PWM/CPM controller that was used in this study is introduced. The controller realization has been enabled by a newly developed ADC and by high-resolution DPWM peripheral units, as developed by a team in our lab, based on delay line technology that has been specially modified to a FPGA design and constraints. The new ADC is capable of converting a sample with resolution of a 10 bits within 300ns. The DPWM has demonstrated a capability of producing an 11bit signal at 1.6MHz. The CPM operation is verified on a 12-48V, 100W boost converter.

The FPGA design and implementation of the PWM/CPM digital controller includes integrated DPWM and ADC peripherals (using an all-digital realization) and reduces the

number of auxiliary components. The introduced controller architecture is depicted in Fig. 6.2. It follows the classical two-loop CPM design, with a fully digital outer voltage loop, while for the inner current loop, an analog comparator *i_cmp* is utilized [4], [40]-[42]. The voltage loop creates a digital reference for the peak current value $i_{ref}[n]$ that is then converted into an analog equivalent, with a digital-to-analog converter (DAC), that is realized by a simple RC filter, that is fed by a high-frequency high-resolution (11bit @ 1.6 MHz) DPWM unit. The current reference is calculated by a PI compensator based on the error signal of the voltage loop $e[n]$, and the resulting output of the DAC is compared to the sensed value of the inductor current $i_L K_I(t)$ with the comparator *i_cmp*. The output of the comparator is then sent to the S-R latch and a pulse width modulated signal $c(t)$ is created. The output voltage is sensed using a modified delay-line (DL) based ADC. To allow a CPM operation at duty ratios above 0.5, and to avoid sub-harmonic oscillations [4], [111], an additional DPWM signal (at lower frequency) is generated, and is summed with the generated current reference, in order to create the artificial slope for compensation.

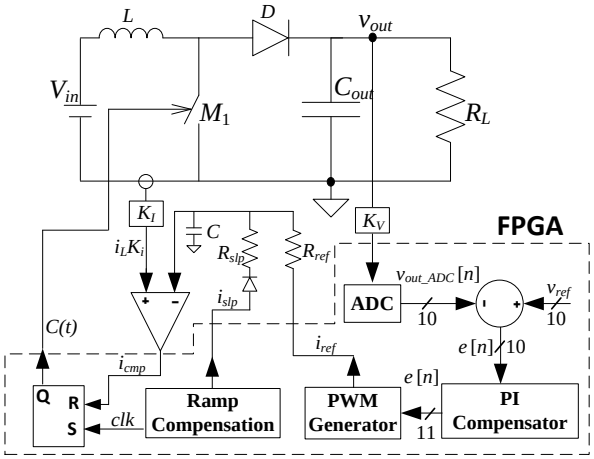


Fig. 6.2 Architecture of the FPGA-based CPM controller.

6.2.2. Implementation of the linear controller

The adopted approach to realize the DL-ADC, in the presented implementation, follows a two-step conversion, that is, a voltage-to-time converter that is followed by a delay line based counter. It is facilitated by using a string of digital buffers with a fixed propagation time. The digital representation of the voltage is obtained by the count of active cells within the pulse length. Since this method does not require a variable supply voltage, it is more suitable for FPGA implementation.

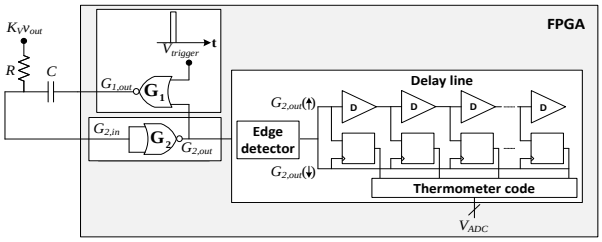


Fig.6.3. FPGA implementation of a delay-line ADC.

Fig. 6.3 shows the ADC configuration that has been used. The time counter delay string is implemented by using asynchronous buffers, which in the current design features a relatively fixed propagation delay of 300ps per cell. To achieve a 10bit resolution, 1024 buffers are used. To facilitate a simple voltage-to-time conversion using digital architecture and by using FPGA, a simple monostable multivibrator (i.e. one-shot timer) has been employed by adding two additional gates. To complete the circuit functionality, the initial time constant is created by using an auxiliary *RC* network that is connected to the FPGA ports. The sensed voltage is connected to the resistor *R*, creating the analog link.

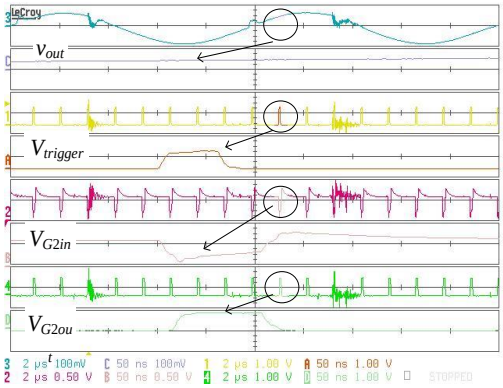


Fig. 6.4. Operation of the experimental DL-ADC.

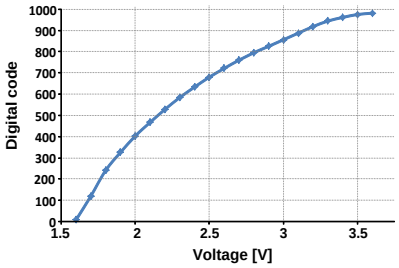


Fig. 6.5. The static conversion characteristics of the experimental DL-ADC.

The description of the DL-ADC operation is assisted by the timing diagram of Fig. 6.4, which shows experimental waveforms of the converter. A start-of-conversion, i.e. a trigger signal, activates the one-shot. The resultant pulse length, T_{pulse}, as a function of the sensed voltage is expressed as:

$$T_{pulse} = RC \ln\left(\frac{V_{DD}}{V_{sample} - V_{threshold}}\right), \qquad (6.1)$$

where V_{DD} is the supply voltage to the FPGA, $V_{threshold}$ is the transition voltage of the or gate (typically ½ of V_{DD}) and $V_{sample}=K_v v_{out}$ is the value of the sensed signal. As can be observed, the voltage range is limited from ½ V_{DD} to V_{DD}. For cases that a range of 0 to ½ V_{DD} is of interest, the sensed signal can be offset by -½ V_{DD} using a simple resistive divider.

The output signal of the one-shot timer (G_{2out}) contains the required data for the voltage level and also provides the start and stop signals for the counter. The edge detector generates a start-of-conversion signal with the rising edge of G_{2out} and a stop-of-conversion and capture signal with its falling edge. The resulting thermometer code is then converted into a digital value by summation of 2s-complement based algorithms. It can also be observed from Fig. 6.5 that the power transistors switching action introduces noise on the sensed signal which may result in an erroneous measurement. This however, does not affect the closed-loop operation of the system, which relies on a single sample per switching cycle.

The static conversion characteristics of the experimental DL-ADC are shown in Fig. 6.5. As can be observed, and also be foreseen from (6.1), since the voltage-to-time conversion is based on a simple RC one-shot timer, the static conversion curve has exponential characteristics, as opposed to the desired linear one. However, in the context of voltage regulation, this has a negligibly small effect on the performance of the system in closed-loop, since the operation is around a steady-state point, and the deviations from that point are minor, when compared to the entire range of the ADC. Therefore, within the vicinity of the steady-state, the exponential curve can be fairly approximated to be a linear one. For cases that a general-purpose ADC, with a linear conversion curve is required, a post-conversion look-up-table linearization unit can be added, based on the known deviation of an exponential curve of (6.1) from a linear one.

In the following, a realization of the high-resolution DPWM and the generation of the slope compensated current reference are described. A high-resolution (HR) correction signal is essential in order to avoid undesirable limit cycle oscillations [71]-[72].

The construction and the operation of the FPGA-based HR DPWM are illustrated in Figs. 6.6 and 6.7, respectively. To facilitate a variable digital pulse width, with a resolution that equals the propagation delay of a single gate, three major components are constructed: a ring oscillator realized using DL, an *N* cell multiplexer, and a xor gate.

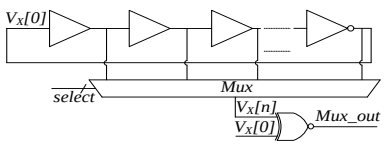


Fig. 6.6. Construction of the FPGA-based HR DPWM.

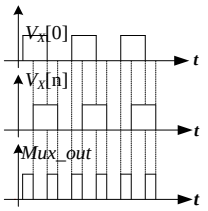


Fig .6.7. Operation of the FPGA-based HR DPWM.

The ring oscillator is constructed using a chain of buffers, creating a fixed frequency signal with 50% duty ratio. The frequency out of the ring oscillator is programmable by selecting the number of delay cells, and is expressed as:

$$f_{ring\_osc} = \frac{1}{2Nt_{pd}}, \tag{6.2}$$

where N is the number of buffers in series, and t_{pd} is the propagation delay of a single cell (approximately 300ps in the current design).

A controlled duty ratio signal is achieved by an xor operation between the first input buffer of the ring oscillator (X[0]) and the n^{th} cell of the ring oscillator (X[n]). Access to n^{th} cell is obtained by a shift register vector that controls the selection bits of the mux. For example, to generate a signal with a 30% duty ratio out of a 1000-cell string, an xor operation of between X[0] to X[300] is carried out. It should be noted that due to the xor action, the effective output frequency is twice f_{ring_osc}.

To facilitate the CPM operation, the current reference to the comparator i_{ref} is generated by filtering out the high frequency component of the DPWM signal, by using a simple RC network, as depicted in Fig. 6.2. To avoid sub-harmonic oscillations under the steady-state operation for cases where d>0.5, a lower frequency (at the switching frequency) DPWM signal is generated, and summed onto the current reference signal using an attritional resistor as depicted in Fig. 6.2. The experimental timing diagram, of the current reference DPWM, and the resultant slope-compensated reference, is shown in Fig. 6.8.

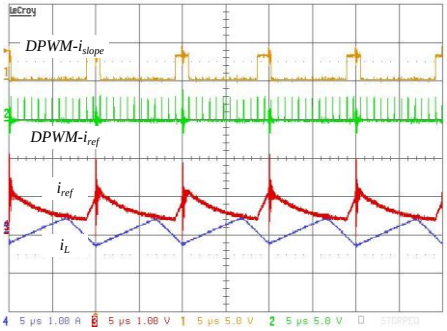


Fig. 6.8. Operation of the experimental slope-compensated current reference signal generation.

6.2.3. PI controller realization

The compensator design and a detailed description of the system's gains are provided in by the following. To complete the controller implementation, a voltage-loop compensator is required. In this study, the compensation scheme has been realized under the assumption that the inner current loop has a wider bandwidth than the desired loop dynamics, and that sampling of the output voltage is obtained once per cycle. Under the CPM operation, the power stage control-to-output transfer function, taking into accounts all of the system gains, can be expressed as:

$$A_{OL} = \frac{K_V K_I K_{ADC} K_{PWM} R_L}{sC_{out} R_L + 1}, \tag{6.3}$$

where K_V and K_I are the voltage and current sensing gains (Fig. 6.2), respectively, K_{ADC} and K_{PWM} are the gains of the ADC and the DPWM, R_L is the load resistance, and C_{out} is the output capacitance.

In this study, a PI compensation scheme has been realized based on the functional diagram of Fig. 6.9. The discrete-time representation of the PI compensation can be expressed as:

$$v_C = v_{C-1} + K_1 v_e - K_2 v_{e-1}, \tag{6.4}$$

where K_1 and K_2 are the PI gains.

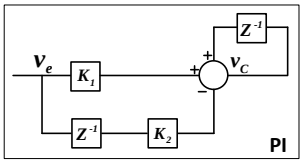


Fig. 6.9. PI compensation scheme.

6.2.4. Experimental results of the PI controller

An experimental prototype has been built and examined according to Fig. 6.2 and Tables IV, and V, only that for this purpose of building only the PI controller a larger output capacitor of 75 μF has been used. For the target converter, an 8 bits ADC resolution has been found to be sufficient, resulting in an approximate 10mV resolution. The CPM operation, using a 12bit current reference signal, and slope compensation has been verified. The controller has been implemented on a Cyclone IV FPGA – Altera (EP4CE115F29C7), and requires only 6500 logic elements, allowing for its implementation with only 7% of the resources of a low cost FPGA system.

Fig. 6.10 shows the response of the experimental CPM controlled boost converter to a 25W to 80W to 25W load transient. As can be observed, a well regulated response is obtained with a dynamic performance that is comparable to other reported CPM controllers, with the advantage of a fully digital design, with a very low gate count realization. In conclusion, the entire controller realization (compensator and peripherals), as used in this study, requires a relatively modest amount of logic elements, allowing for a cost-effective CPM solution.

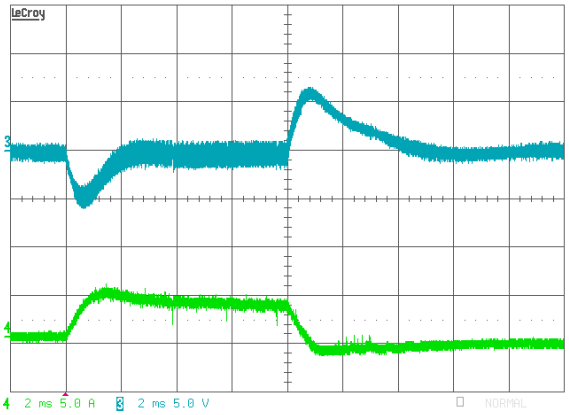


Fig.6.10. Experimental load transient response (25 W to 90 W to 25 W) of the CPM controlled boost converter using the new controller. Ch.3(upper trace): the ac component of the output voltage, 5V/div; Ch.4 (bottom trace): inductor current, 5A/div. The time scale is 2 ms/div.

6.3. The hybrid control system implementation

In this modification, two novel blocks are added. Namely, a *transient suppression block* and a *self-tuning estimator* of the output current are introduced. Upon a load transient detection, these blocks take over the task of creating the pulse width modulated signal, from the conventional controller, and provide a transient response with a near minimum possible voltage deviation. The transient suppression block implements a new transient control algorithm, that dynamically changes the on and off transistor times, based on pre-set values of the peak/valley inductor current and the pre-programmed maximum allowable voltage deviation. The estimator's role is to provide the suppression logic, with an estimate of the new inductor current that is needed for the algorithm. Once the transient recovery is completed, the controller returns to a steady-state operation.

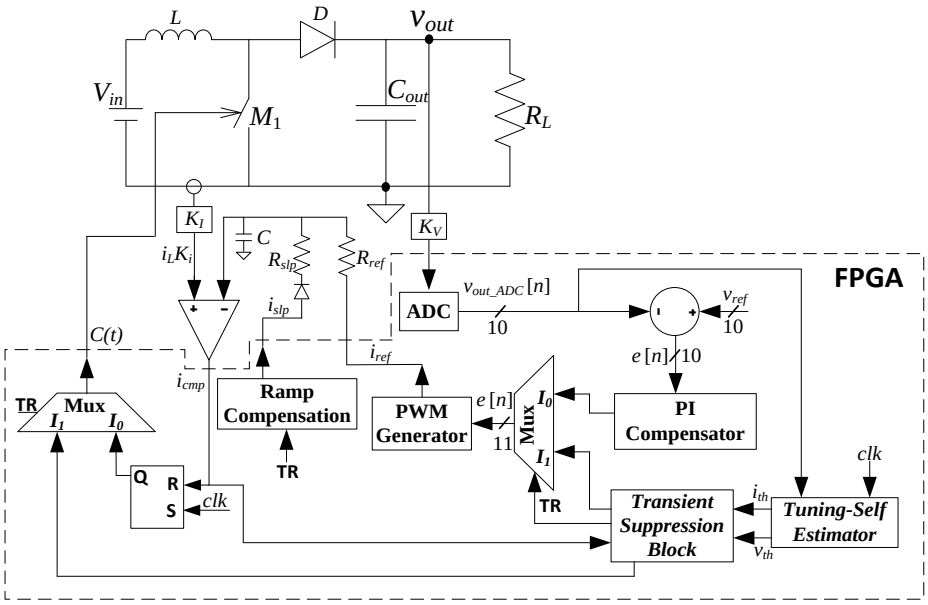


Fig.6.11. Programmable-deviation controller regulation operation of the boost converter.

The time-optimal control solutions, for the boost converter [51]-[52], [55]-[56], usually require continuous and fast sampling, i.e. oversampling of both state variables. They also require fairly demanding calculations, to determine the converter operating point (its location on the state-space), and thus creating the switching sequence. The programmable-deviation controller operates with much simpler algorithm, and can be implemented by sampling the output voltage at the switching frequency rate, i.e. without oversampling. As shown in Fig. 6.11, the controller is a modification of a simple mixed-signal peak current programmed mode controller, where the *self calibration block* and *transient suppression logic* are added.

As described below, the self-calibration logic is used to determine the voltage and the current threshold values, V_{th} and I_{th}, as described in Chapters 2 and 3. These two values are then passed on to the transient suppression logic that creates the switching sequence.

The implementation of the self-tuning estimator of is based on a look-up-tables (LUT) and on an estimation of the load current (and from it, the steady state inductor current), through a comparison with a measurement of the known current value, named the unity current. The look-up-table of the estimator is populated during the converter start up. Over that period, the LUT's entries are stored, i.e. the current and voltage threshold values are created, from a measurement of the output capacitor voltage derivative, during the on-time of the switch M_1. After the writing of the values in the tables is completed, the voltage deviation of the capacitor is used as an address to determining the LUT outputs, i.e. V_{th} and I_{th} values.

Finally, the corresponding values of the threshold current and the voltage are produced by the LUT. These values are then passed to the transient suppression logic that suppresses the output voltage deviation, by applying the switching sequence as described in Chapter 2 and as depicted with the flowchart diagram of Fig. 6.12. The flowchart diagram of Fig. 6.12 depicts the general stages in order to determine the switching sequence.

To reduce the sensitivity of the threshold voltage estimation on the system parameters, an estimation of the system's components can be applied. An output capacitance estimation method has been developed and is described [26]. A reliable estimation of the inductance value can be obtained by using the method developed in [110].

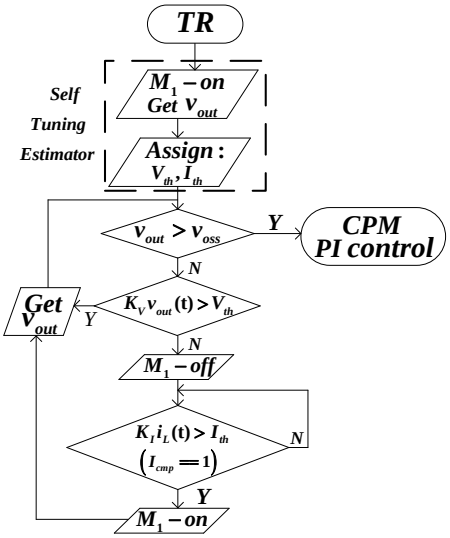


Fig. 6.12. Flowchart of the transient suppression algorithm
(voss is the steady-state value of the output voltage).

Furthermore, an alternative, more robust, programmable-deviation control scheme, that realizes the initial charging phase, based on the inductor current, rather than on the output voltage, and is therefore, less dependent of the converter parameters that can be used. The algorithm and the results are briefly delineated next.

6.3.1. Current thresholds based upon aprogrammable-deviation control scheme

The programmable voltage deviation control method that has been introduced in this work provides both theoretical and practical insights into the load transient behavior of indirect energy transfer converters. On the other hand, the preliminary concept as described in Chapter 3 may result in an inconsistent performance due to parameter uncertainties. The values of *L* and *C* may vary, and the input voltage is not constant in a number of applications. These factors can affect the accuracy of the threshold calculations and the performance of the

programmable-deviation controller. Therefore, it would be highly advantageous, if the threshold settings could be extracted, based on the new load current only, and thus by eliminating uncertainties that may appear in the system. A possible solution for this problem is an alternative realization of the self-tuning estimator unit, for thresholds calculations, which its operation is described with the help of the flowchart shown in Fig. 6.13 and experimentally demonstrated in Fig. 6.14 (a zoomed in version of Fig. 6.20). The operation principle of the controller is similar to its precursor (described in Chapters 2 and 3), with the exception that upon the detection of the transient, and an estimation of the new load current (point '*a*', Figs. 6.13 and 6.14), the first 'on' interval of the transistor, is controlled by the current threshold, such that (2.1) is satisfied; i.e. the inductor current is slightly larger than its new minimum-deviation point value $I_{th}=I_{min}+\varepsilon_I$.

Once the first current threshold has been reached (point '*b*', Figs. 6.13 and 6.14), the controller measures the output voltage and assigns $V_{th}=v_{out}$ (point *'b'*). From this point on, the voltage is recovered using the transient suppression logic as described earlier. At the instance that the output voltage has reached its new steady-state value (point '*c*', Figs. 6.13 and 6.14), the controller resumes a regular current programmed mode (CPM) operation.

Using this alternative approach, the thresholds' settings become depended on the new load current only, hence eliminating system uncertainties.

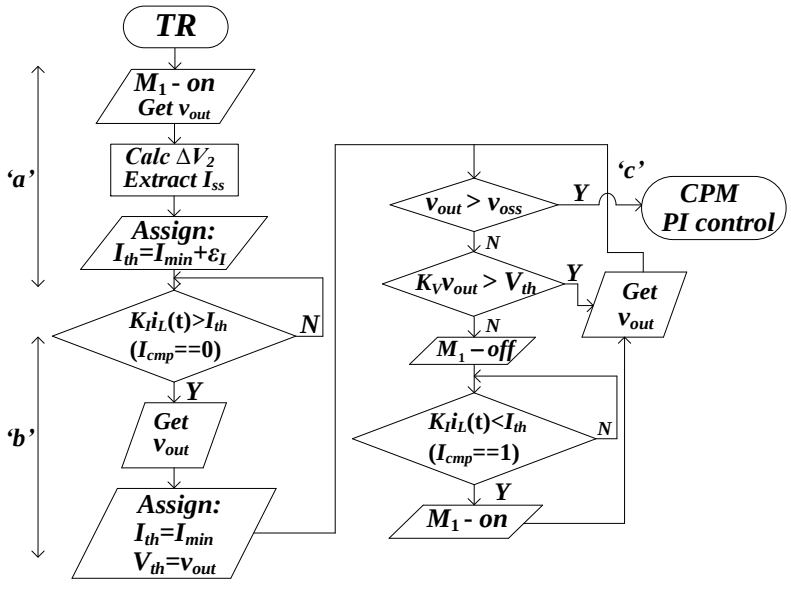


Fig. 6.13. Flowchart of the current threshold based transient suppression algorithm.

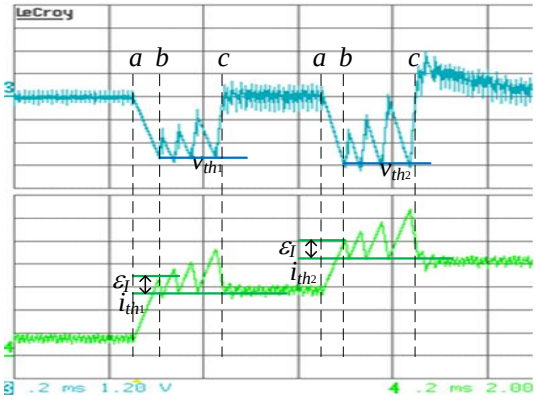


Fig.6.14. Experimental demonstration of the current threshold based programmable deviation control for two consecutive light-to-heavy load transients (25W to 90W to 140W). The additional charging current εI (for both steps) has been set to 15% of the first load step.

6.4. Experimental verifications

6.4.1. Practical controller implementaion details

The entire controller realization (CPM and the programmable-deviation) only requires 9000 logic elements, allowing for its implementation, with only 20% of the resources of a low cost FPGA system, such as [112], whose price is comparable, or even lower, than that of simple microcontrollers, as is widely used in the industry, e.g. [113]-[114].

The performance of the controller was tested for a voltage sampling rate being equal to the switching frequency and for the case when the output voltage was over sampled, at a 32 x sampling rate. The performances of the introduced controller were also compared with that of a-state-of-the-art time-optimal solution, which was built following the implementation demonstrated in [48], [51]-[52]. Also, comparisons with a conventional mixed-signal peak current programmed mode controller [110]-[118] (PCPM), requiring a much simpler implementation than that of the time-optimal solutions, were performed.

6.4.2. Light-to-heavy experimental results

Figs. 6.15 and 6.16 show a comparison of the transient responses, of the time-optimal solution, and the introduced programmable-deviation controller, for a light to heavy load transient. In both cases, the output voltage was sampled 32 times. It can be seen that the output voltage deviation, for the programmable deviation controller, is about 1.8 times smaller, than that of the time-optimal system, and that the current stress is reduced by 1.4 times. These results show that the programmable deviation controller, allows for the use of a significantly smaller output capacitance value (about 1.8 smaller), switching components

with a 1.4 times lower peak current ratings, and with an inductor with about a 1.85 times smaller maximum energy storage capacity, which is proportional to the squared value of the peak inductor current.

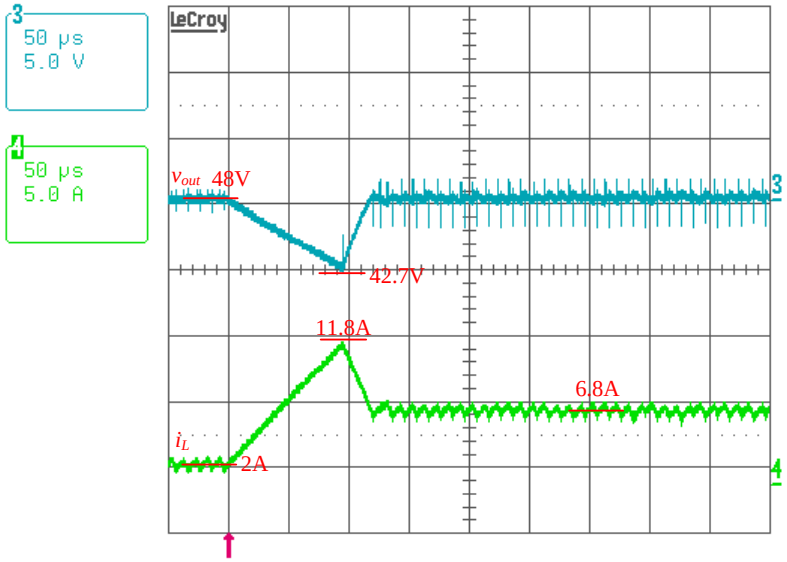


Fig.6.15. Light-to-heavy load transient response (25 W to 90W) of the time-optimal controller with 32x sampling rate. Ch.1 (upper trace): the ac component of the output voltage, 5V/div; Ch.2 (bottom trace): inductor current, 5A/div. The time scale is 50µs/div. Operating conditions: V_{in} = 12 V, V_{out} = 48 V, L= 150 µH and C_{out} = 30 µF.

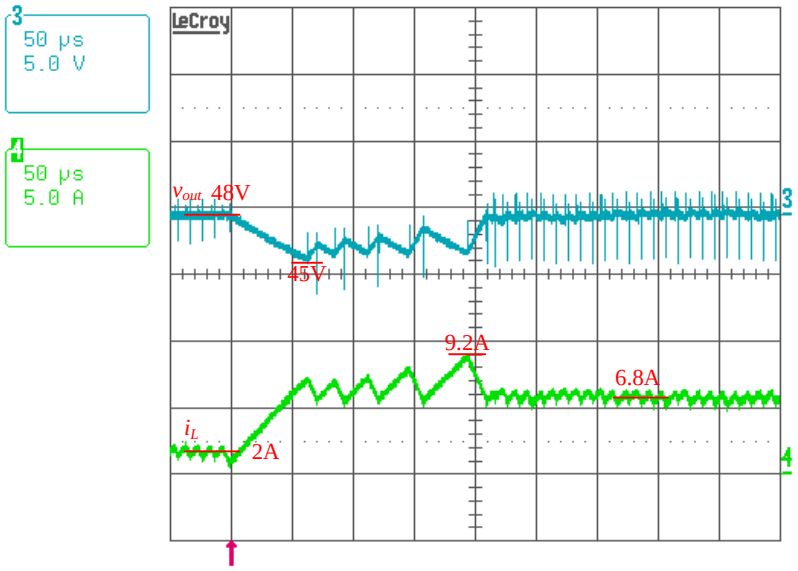


Fig.6.16. Light-to-heavy load transient response (25 W to 90 W) of the programmable-deviation controller with 32 x sampling rate. Ch.1 (upper trace): the ac component of the output voltage, 5V/div; Ch.2 (bottom trace): inductor current, 5A/div. The time scale is 50 µs/div. Operating conditions: V_{in} = 12 V, V_{out} = 48 V, L= 150 µH and C_{out} = 30 µF.

Figs. 6.10 and 6.17 can be used to compare between the transient responses of a conventional PCPM controller [11],[110],[116]-[119] requiring one voltage sample per switching period, with that of a programmable-deviation solution, for the case when a 32x sampling rate is applied. The PCPM controller is regulated with a fast loop, having the bandwidth of

approximately 1/10 of the switching frequency. It can be seen that for the case of a programmable-deviation solution, the transient response is drastically improved. By comparing the responses of a programmable deviation controller, for once per cycle and 32x sampling rates, it can be seen that an empathic reduction in the sampling rate, has a minor effect on the transient performance, thus allowing for a simple ADC to be used. Results demonstrate that, even with a much lower sampling rate, the performance of a programmable deviation controller, is significantly better than that of a time-optimal solution (shown in Fig. 6.15).

The right side load step in Figs. 6.10 and 6.17 can be used to compare between the transient responses of the programmable deviation and PCMP controllers, for heavy to light load transients, for the case when both controllers sample the output voltage once per switching cycle. It can be seen that, even after a 2.5 times larger output capacitor has been used for the PCPM experimental controller, for the new controller, the deviation is about 2 times smaller, allowing for the additional reduction of the output capacitor value. The results confirm that this, relatively small modification of the conventional current programmed mode architecture, drastically improves the transient performance, and hence, allowing for a significant reduction of the reactive components.

6.4.3. Heavy-to-light and two consecutive load steps experimental results

Another set of experiments was carried out in order to validate the concept with respect to the state-plane theory as described in Chapter 3, and to verify the robustness of the method for consecutive load transients.

Fig. 6.17 shows a light-to-heavy and a heavy-to-light load transient, in a single frame, as well as with their state trajectory plot. Fig. 6.18 shows the operation of the programmable deviation controller for two consecutive load steps, demonstrating a tight voltage regulation. It should be noted that the load step results, presented in Fig. 6.18, have been implemented with the modified algorithm for the threshold selection, as described in Subsection 6.1.4.

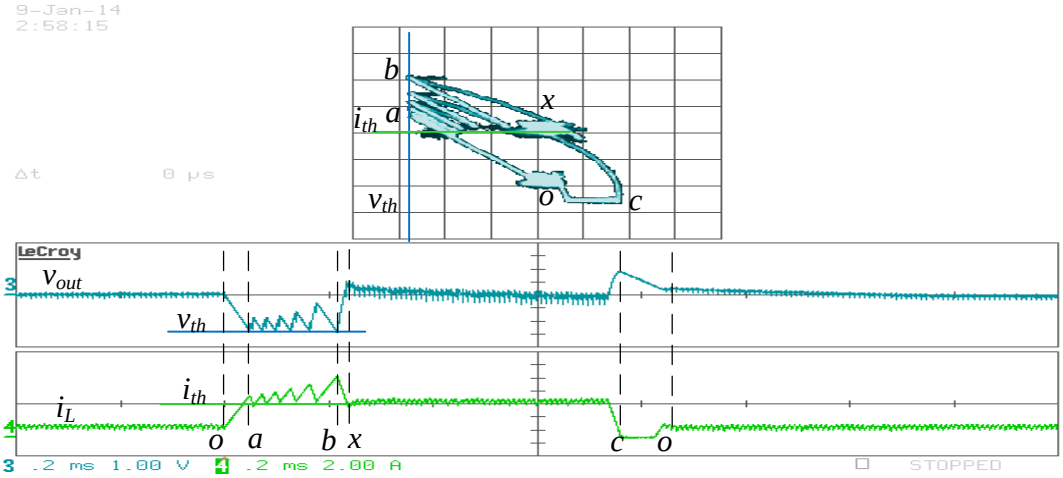


Fig.6.17. Light-to-heavy – heavy-to-light load transient response (25 W to 90 W to 25 W) of the programmable-deviation controller with its corresponding state trajectories. Upper plot: XY plot (X-output voltage, Y-inductor current). Lower plot: Ch.3 (upper trace): the ac component of the output voltage, 1V/div; Ch.4 (bottom trace): inductor current, 2A/div. The time scale is 200 µs/div. Operating conditions: V_{in} = 12 V, V_{out} = 48 V, L= 100 µH and C_{out} = 25 µF.

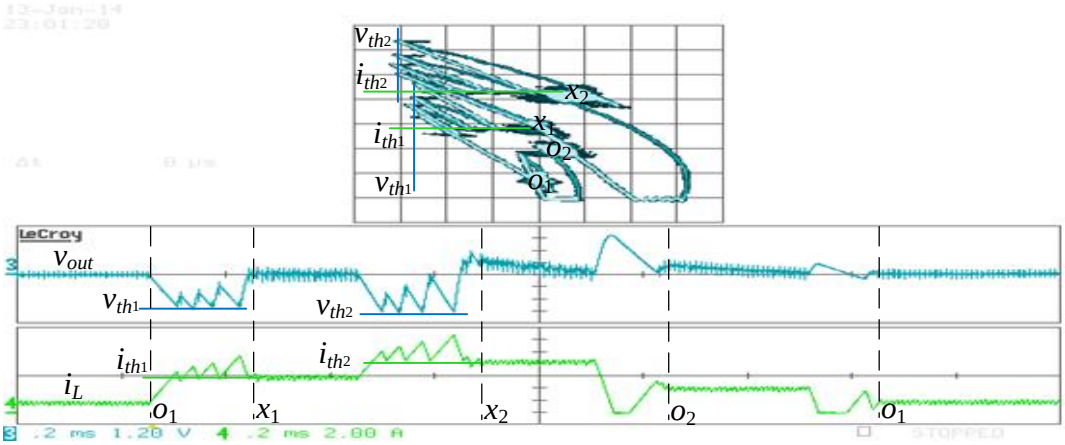


Fig. 6.18. Tight voltage regulation of the programmable-deviation controller for two consecutive load transients (25 W to 90 W to 140 W to 75 W to 25 W) with the corresponding state trajectories. Upper plot: XY plot (X-output voltage, Y-inductor current). Lower plot: Ch.3 (upper trace): the ac component of the output voltage, 1.2V/div; Ch.4 (bottom trace): inductor current, 2A/div. The time scale is 200 µs/div. Operating conditions: V_{in} = 12 V, V_{out} = 48 V, L= 100 µH and C_{out} = 25 µF.

6.4.4. Experimental summary and conclusions

The hardware-efficient programmable deviation controller for indirect energy transfer converters, introduced in this work, is a modification of the conventional mixed-signal peak current mode programmed (PCPM) architecture. The controller is designed around the fact that, for indirect energy transfer converters, the time-optimal response does not coincide with the minimum possible voltage deviation. Therefore, it is designed with the goal of providing a near minimum possible voltage deviation, for a controlled switching frequency operating range. Compared to the time-optimal solutions, the programmable deviation controller has

several advantages. They include a smaller output voltage deviation during transients, lower current stress, and an implementation of a much simpler hardware, not requiring complex computations, and with a high sampling rate analog-to-digital converter. These advantages allow for a significant reduction of reactive components of the converter and result in a lower current stress on the semiconductor switches.

In steady state, the controller operates as a simple PCPM output voltage regulator. During transients, the controller sets the boundaries for the inductor current and the output voltage, such that the near minimum voltage deviation for a pre-determined frequency range is obtained, and that the convergence towards the new steady state condition is ensured. The boundaries are set based on the founding that, in the case of a boost converter, the theoretical/ideal minimum-deviation requires the boundary current to be equal to its new steady state value for the case of a constant current load, or lower (a minimum-deviation point current) for the resistive load case, the boundary voltage is equal to its minimum-deviation. For that particular case, the converter recovers to the new steady state, operating at the infinite switching frequency. To limit the switching frequency, an analysis of the relationship of the minimum voltage boundary value, for the frequency constrained case, is performed, and accordingly, is used in the control algorithm.

The effectiveness of the introduced controller is experimentally verified, through comparisons with the time-optimal and conventional PCMP solutions. The results confirm, that this modification of the PCMP architecture, results in significantly better transient performance, than the other solutions, while eliminating the need for a high sampling rate ADC and complex computations.

7. Discussion

7.1. Contributions of the research

These research developments provide both theoretical and practical insights into the load transient behavior of direct and indirect energy transfer converters, for both cases of constant current and resistive loads. The theoretical analysis has established the relationship between converter state variables and a criterion to guarantee a convergence toward the steady-state. As a consequence, the control task of recovery from a load transient has been significantly simplified and reduced to the realization of two comparators, one for each state variable (transient suppression logic block). Furthermore, within the defined boundaries, the concept allows independence in the selection of the current and voltage thresholds. This may assist in further research and lead to an improvement of the controller.

The interest in digital transient control follows a major interest of many research and industrial groups, who focus on aspects of circuit theory, electronics, micro-electronics, control theory, signal-processing, and computer science. These groups may also benefit from the outcome of this study.

This work has helped to establish a new operational methodology for SMPSs, which is based on a large-signal controller design, rather than on the conventional linear small-signal operation. In this case, derivation of the system stability, by conventional small-signal tools, such as a loop gain analysis, is no longer valid. The results presented in this research provide analytical tools, and practical counterparts, to aid researchers and designers in exploring and designing digital power management systems. The results can lead to a more attractive and economical realization of flexible power supplies, and digital control, and will thus provide the foundation for further miniaturization of power management systems, with improved energy processing efficiency. It is hoped and expected that this study will provide the basics and the tools for the development of a new generation of flexible power supplies.

A detailed stability analysis of the various methods has been provided, using analytical tools from control theory, to demonstrate the practicality of the proposed approach.

7.2. Future work

The theoretical results and ideas gained in this work, could serve as the basics for the development of more effective and simpler transient control methods, for indirect energy transfer topologies, and an example is presented in Subsection 2.5.

Ideal power converters were assumed in this work's developments and analysis, meaning that no power dissipation factors, such as parasitic resistance, parasitic capacitance, and parasitic inductance of components, have been taken into account. A future, more general work, will include these, and more power consumption factors, and will make comparisons between different transient control methods, from power losses and from efficiency point of view.

Here, the focus has been on the three dominant and basic topologies of buck, boost, and buck-boost converters. In the future, efficiency, effectiveness, and simplicity of the presented method, and its modifications, could be validated on more complicated topologies. Additionally, this control approach could be integrated with different topologies to obtain a more beneficial control operation.

8. References

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