BEN-GURION UNIVERSITY OF THE NEGEV
FACULTY OF ENGINEERING SCIENCES
DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

DEVELOPMENT AND IC IMPLEMENTATION OF DIGITAL POWER MANAGEMENT PLATFORM

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE MSc. DEGREE

By: Yevgeny Lazarev

Supervised by:
Dr. Mor Mordechai Peretz

February 2016

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Chairman of graduate studies committee:

Name…… Date: ……

February 2016

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המחבר:	יבגני לזרב	.....	תאריך: .....
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יו"ר ועדת הוראה לתואר שני:

שם: .... תאריך: .....

February 2016

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This thesis work is dedicated to my wife, Svetlana, who has been a constant source of support and encouragement during the challenges of graduate school and life. I am truly thankful for having you in my life. This work is also dedicated to my parents, Larisa and Nicholas, who have always loved me unconditionally and whose good examples have taught me to work hard for the things that I aspire to achieve.

∞

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תקציר

ממירי DC-DC מהווים פתרון יעיל להמרה של מתח כניסה לא מבוקר למתח יציאה מבוקר ויציב. בהשוואה לספקי כח לינאריים, ממירים ממותגים מספקים יעילות וצפיפות ההספק הרבה יותר גבוהה. באופן מסורתי, מתודולוגית הבקרה הייתה אנלוגית. בעשור אחרון הטכנולוגיה של מעגלים משולבים התקדמה בצורה משמעותית ואיפשרה שימוש ברכיבי DSP ומיקרו-בקרים לצרכים של בקרה דיגיטלית. פתרונות הבקרה הדיגיטאלית נפוצים בסביבה שבה שנדרש משטר בקרה חכם ומיוחד ע"מ להצדיק את מחיר המימוש הגבוה. היתרונות העיקריים של מערכות מבוססות בקרה דיגיטאלית על בקרה אנלוגית מתבטאים ביכולות תכן גבוהות, משאבים חישוביים מתקדמים, אפשרות הקטנה של רכיבים פסיביים ,טולרנטיות גבוהה למקורות עם השתנות פרמטרית, אפשרות ליישום של אסטרטגיות שליטה מורכבות ויכולת תפקוד במצבי עבודה שונים. יכולת פונקציונלית של ניטור המערכת היא בעלת חשיבות רבה עבור יישומים עם רמת אמינות גבוהה אשר מסוגלים לאסוף ולעבד נתונים סביבתיים. כיול עצמי מאפשר למפצה דיגיטלי להתאים את הפרמטרים שלו בהתאם למערכת וע"י כך מבטל את הצורך בכיול והתאמה ידנית כפי שנעשה במערכות אנלוגיות. בשל יתרונות הבקרה הדיגיטלית, שימוש ב-SMPS הפך לנפוץ במערכות מסוגים שונים כגון תקשורת, בקרה ועיבוד שמספרם גדל בצורה משמעותית. עם יישומם DC-DC SMPS במערכות של הדור האחרון ואפליקציות משובצות, הביאו לאתגרים חדשים במונחים של ביצועים דינאמיים גבוהים, אדווה סטטית, גודל ומשקל של המערכת. פרמטר של גודל הפך לאחד המוקדים העיקריים בתכן הכולל, ולכן מעבר לעבודה בתדרים גבוהים תאפשר להקטין את גודלם של הרכיבים הפסיביים (כמו סלילים וקבלים).

בשנים האחרונות הוצעו פתרונות דיגיטליים רבים בשוק היישומים. קיים שימוש רחב בספקי כח במחשבים נייחים או ניידים משולבים עם שבבי בקרה דיגיטלית רב-פאזיים לאיזון מתחי המוצא (VRMs). בהקשר זה, תחרות עם פתרונות בקרה אנלוגיים הובילה לשיקולים חדשים בהיבט של עלות וביצועים. היום יישום של בקרה דגיטלית נוטה לכיוון של ASIC שכולל בתוכו את כל המרכיבים העיקריים של הבקרה הדיגיטלית, למשל, ממיר אנלוגי לדיגיטלי (ADC), DPWM, חומרת שליטה ,מעגלי הגנה קונבציונלית וניטור מאשר יישום על בסיס פלטפורה של DSP או מיקרו בקר.

תכן של מערכות משובצות מבוססות ASIC, במונחים של יכולות דינאמיות, שטח סיליקון וצריכת חשמל הוא נושא מאתגר וזוכה לתשומת לב מוגברת מצד קהילת המדענים בשנים אחרונות. מערכות דיגיטליות טהורות דורשות מודולים מהירים בעלי ביצועים ורזולוציה גבוה. לדוגמא, את דיוק התיקון, בהשוואה למערכות אנלוגיות, ניתן להשיג רק באמצעות כמות ביטים מספיקה (בתלות במערכת) כאשר את פרמטר זה ניתן להשגה רק בעזרת הגדלה של שטח הסיליקון הכללי. מגבלות אחרות שמיוחסות לבקרה דיגיטלית כוללות את זמני התגובה של הבקר אשר מוגבלים ע"י קצב דגימה, רמת קוונטיזציה וכו'.

במהלך העבודה יוצגו פתרונות למרכיבים העיקריים בבקרה דיגיטלית כמו ממיר אנלוגי לדיגיטלי (ADC) ו-DPWM מבוססי מערך של תאי השהייה, תוצאות סימולטיביות ומעשיות מפורסמות ב-[4]-[1]. Ring ADC ו-Window ADC משמשים לביצוע המרה מהירה מאות אנלוגי לדיגיטלי ברזולוציות שונות עם שטח סיליקון מינימלי. Ring DPWM משלב בתוכו יכולת תיקון של מתח מוצא ברזולוציה של תא השהייה בודד, שטח סיליקון קטן יחסית וצריכת הספק נמוכה. כל המודולים יוצגו ברמות אפליקציה שונות – מרמה של מודול בודד עד לרמת מערכת.

היום קיים מגוון רחב של בקרים דיגטליים משולבים. חלק משמעותי מתוכם מבוסס על תכן אנלוגי או משולב כאשר זה מונע מהמפתח להשתמש בתכנים קודמים בעת מעבר מטכנולוגיה אחת לטכנולוגיה אחרת. מימוש דיגיטלי מלא נותן יתרון עצום בנושא של יישום והוא מאפשר להשתמש בזמן הפיתוח בתאים הסטנדרטיים אשר באים בשילוב עם טכנולוגיית היצור. לפיכך, גישה דיגיטלית מלאה חוסכת בזמן הפיתוח כתוצאה מיכולת המחזור של התכנים הקודמים.

תוצאות מעשיות של מודולי בקרה SMPS מסוגים שונים עשויות להיות רחוקות מהתוצאות הסימולטיביות. מימוש ישיר על סיליקון של תצורת הבקרה החדשה עלולה להיות מסוכנת בשל השפעתן של טעיות בתפיסה של הבקרה עצמה או טעויות במהלך היישום בעזרת כלי CAD. נדרש שלב ביניים בין סימולציה ומימוש ע"ג הסיליקון על מנת להפחית את סיכויי הכישלון. במימוש דיגיטלי מלא, ניתן להשיג את השלב הביניים בעזרת רכיב FPGA שמאפשר שימוש רב פעמי בתהליך המימוש, בדיקה וניפוי. בנוסף, ערכת פיתוח של FPGA מצויידת בכילים פריפריאליים מגוונים ע"מ לבצע שלבי אינטגרציה ברמות שונות. בעזרת רכיב FPGA ניתן בקלות יחסית לבצע את שלב הוכחת הרעיון והוא מהווה ייחוס נוסף להתנהגות תצורת הבקרה לאחר מימוש ע"ג הסיליקון.

Abstract

Switch based DC-DC converters efficiently convert an unregulated DC input voltage into a regulated DC output voltage. Compared to linear power supplies, switching power supplies is provided much more efficiency and power density. Traditionally, the control methodology for DC-DC converters has been analog control. In last decade, technology advanced in very-large-scale integration (VLSI) has been made digital control of DC-DC converters with microcontrollers and digital signal processors (DSP) are possible. Digital solutions are fairly common in environments, where intelligent control strategies for power management are required and fully justified the increased cost of a digital control system. Main advantages of a digital control system over an analog solution are represented by the high degree of programmability, and computational power, the reduced need for external passive components and the consequent decreased sensitivity, tolerance to sources of parametric variations, the possibility to be implemented complex control strategies, as well as to be easily switched through different modes of operation, targeting for highest efficiency or optimized dynamic performances. System monitoring functions are of extreme importance for high-reliability applications, and their implementation is strongly pointed to digital solutions, which are able to collect and process environmental data. Self-tuning, is also known, as auto-tuning functions, allows a digital compensator to be adapted its parameters to the specific power plant under control, having eliminated the need for manual design or calibration, and enhanced controller modularity, and versatility. Due to digital control advantages, SMPS have been, widely, used in portable communication systems, and media products, which have been grown, explosively, in recent years. With the DC-DC SMPS application in the last generation portable systems and embedded applications, new challenges have been observed, in terms of high dynamic performance, static output ripple, size, and weight. A size parameter of DC-DC converters is becoming one of the primary focuses in the overall design. Therefore, the technology for high switching frequency operation to reduce the passive components size, like inductors and capacitors, to obtain miniaturization is urgently needed.

In recent years, however, digital solutions have been proposed in the consumer applications market. Point-of-load power supplies employed in desktop/laptop computers are examples, along with digital control ICs for multiphase converters employed in the Voltage Regulation Modules (VRMs). In this context, the competition with analog solutions is led to reconsider the previous statements, concerning cost, and performances trade-offs. Rather than pointing to expensive microcontroller or DSP platforms, the digital solutions for consumer applications are more prone to the ASIC implementations, with integrated the A/D conversion and pulse-width

modulation resources, control hardware, conventional protection circuitry and – depending on the application – communication, system monitoring and auto-tuning functions.

Design of a digital control IC, in terms of dynamic capabilities, area and power consumption is a challenging issue, and has been gained the increased attention from the scientific community over the last years. Leaving apart mixed-signal solutions, the pure digital systems for SMPS control are, invariantly, required the fast A/D converter, and are optimized the digital pulse-width modulators (DPWMs). Accuracy, comparable to the analog controllers, is achieved only by means of sufficient bit resolution. These factors are led to be increased the overall area consumption. The other limitations are, specifically, encountered in the digital system, including reaction times of the digital controller, which are limited by the sampling rate, as well as quantization phenomena, such as the limit cycle oscillations.

The completely integrated digital controllers feasibility was demonstrated the innovative solutions for the main constituents of the digital controller, namely the A/D converter, and the digital pulse-width modulator are presented and published [1]-[4]. The Ring ADC, and the Window ADCs are used for fast conversion times and small area requirements. A ring oscillator-multiplexer DPWM is implemented, while a hybrid counter/delay line architecture is considered, as a suitable tradeoff between the resolution, area and power consumption.

Today a wide range of IC controllers is available. Significant portion of these controllers is based on analog or mixed signal design, which is prevented using of reverse engineering during switching one type of technology to another. All-digital orientation of IC controllers is given the indefinite advantage in implementation, and it is facilitated the development process by using of standard cells, which are combined with the production technology. Thus, the all-digital approach has been saved development time, as a result of the scalability properties.

An experimental examination of different types of control laws for the SMPS circuits may be far from the simulation results. The ASIC implementation of novel type of the control law may be risky, and not expanded upon the desired results bringing, due to the effect of errors in the concept of the control law or during the ASIC integration. Additional intermediate, "proof of concept", step is required to decrease the chances of failure. In the all-digital approach, it can be implemented on the FPGA unit, which is allowed the reusability for several tests and equipped with the tools for multilevel debugging and integration process. The concept proof of digital control on the FPGA design realization may be, easily, achieved, and it is also provided a reference value, comparatively, to the ASIC results.

Objectives

The primary objectives of thesis have been described as follows:

- Research existing implementation of digital control methods and their advantages of against analog ones in low-power high switching frequency SMPS circuits;

- Exploring, development and implementation of ADC and DPWM modules for all-digital SMPS control method suitable for variable control laws;

- Enhancing of static and dynamic response performance by new all-digital high resolution ADC and DPWM modules;

- Preparing well-defined all-digital design flow for SMPS control, which includes FPGA and ASIC implementation by pre-prepared ADC and DPWM macros.

The thesis will be organized as follows:

Chapter 1 presents the state-of-art in digital and analog control with the advantages and disadvantages of each one. It introduces the basic structure of SMPS controllers and its primary functional blocks. The practical implementation of digital control issues, and challenges, as processing time, limit cycle oscillations, and resolution properties are detailed here. A bibliography observing of ADC and DPWM in lower-power SMPS in recent years is also given. Comparison between different architectures of ADC and DPWM, in terms of power consumption, silicon area and difficulties in realization has been done.

Chapter 2 provides a background on time-to-digital converters (TDC) and motivate delay line approach implementation. The historical TDC trends have been discussed, a number of TDC modern architectures has been described, and the benefits of oversampling method have been considered.

Chapter 4 proposes comparison between the ASIC and FPGA architectures. The primary TDC methods, suitable for the FPGA design, have been described. The FPGA implementation issues, like design flow, placing and routing and signal propagation time non-linearity are detailed here.

Chapter 3 outlines two kinds of the all-digital ADC approach, based delay line string. It is included all intermediate design steps, like concept description, RTL, gate-level simulations, and final experimental results in different work spaces. The results have been published in Electrical & Electronics Engineers Conference in Israel (IEEEI) [1].

Chapter 4 introduces the DPWM module, suitable for wide range of reference frequencies. It is included all the intermediated design steps, like concept description, RTL, gate-level simulation. The results have been published in IEEE Workshop on Control and Modeling for Power Electronics (COMPEL) [3] and IEEE Applied Power Electronics Conference (APEC) [4]

Chapter 5,6 show practical silicon implementation and experimental results at macro and system level of delay line ADCs. Front end and back end design procedure have been described. Four working modes, like Ring ADC, Window ADC, Gyrator controller, and all the modules disabled are implemented on chip. High level architecture, external, and internal pins, all-system logic, and RC parasitic simulation have also been described. The results have been published in Electrical & Electronics Engineers Conference in Israel (IEEEI) [2].

Chapter 7 presents the conclusions of the thesis and discusses a future work.

Acknowledgments

Several people deserve recognition for their help for the accomplishment of this work.

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A very special thanks to my wife, Svetlana, for making me laugh, supporting me and comforting me in ups and downs throughout all this.

Finally, I wish to thank my parents for their support and trust through my personal and academic life.

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Acronyms and Abbreviations

ADC – Analog-to-digital converter
ASIC – Application-specific integrated circuit
ATC – Analog-to-time converter
CMOS – Complementary metal-oxide-semiconductor
CAD – Computer-aided design
DFT – Design for test
DL – Delay line
DLL – Delay-locked loop
DPWM – Digital pulse width modulation
DSP – Digital signal processor
FPGA – Field programmable gate array
GRSCC – Gyrator resonant switched-capacitor converter
HDL – Hardware description language
IC – Integrated circuit
LAB – Logic array block
LE – Logic element
LSB – Least significant bit
LUT – Look-up table
LVDS – Low-voltage differential signaling
MSB – Most significant bit
NRE – Non-recruiting expenses
PET – Positive electron tomography
PI – Proportional-integral
PID – Proportional-integral-derivative
PLL – Phase-locked loop
PVT – Process voltage temperature
PWM – Pulse width modulation
RAM – Random access memory
ROM – Read only memory
SH – Sample and hold
SMPS – Switched-mode power supply
SOC – System-on-chip
UPS – Uninterruptible power supply
TDC – Time-to-digital converter
TIM – Time interval meter
VCO – Voltage controlled oscillator
VRM – Voltage regulator module

Inline References Legend

X.XX – Chapter / Section number
(X.XX) – Equation
[XX] – Reference
Fig. X.XX – Figure

1. Introduction

1.1.Digital control application in low-power and high-frequency SMPS

1.1.1. Analog control in DC-DC circuits

Most SMPS are operated with analog controllers, especially in the low-power applications, because of its simplicity and low cost [5]-[8]. The close-loop operation offers the large performance in keeping the output voltage quite constant and restraining the overshoot during reference voltage or external load changes. Presently, most of the SMPS products are still predominantly controlled by the analog circuit control. The analog controlled SMPS, shown in Fig. 1.1, operates as follows:

The output voltage V_{out}, and the desired voltage V_{ref} are compared and then, the value of signal error $\varepsilon = V_{ref} - V_{out}$ is obtained. The error value is provided to the input of the controller. The controller can be implemented by using an operational amplifier, and a network of the passive components, such as resistors and capacitors. The output of the controller is the control signal, which is provided to the PWM module, which is transforming the control signal into duty cycle with the switching frequency f_s.

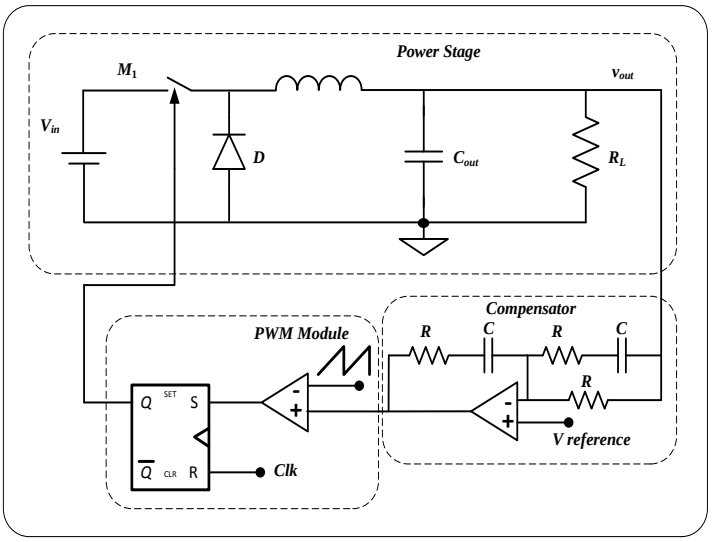

Fig. 1.1 A basic example of analog controlled buck converter

In fact, for practical application, a number of passive elements are needed to construct the compensator or to adjust the switching frequency, filter the switching noise, etc. [9]-[12]. It can be seemed, that the analog controller SMPS is required a lot of the external passive components, and this architecture is increased the overall size of the portable system. Also, the analog components are sensitive to the environmental influence, such as temperature,

aging, noise, and fabrication process, which it is resulted in lack of flexibility, low reliability, not to be mentioned the parameter auto-tuning, and the system diagnosis. Besides, it is difficult to be applied the sophisticated control algorithms, with the analog approach implementation. In addition, to meet the size miniaturization demand, the high switching frequency f_s is indispensable. However, in higher switching frequency operation, the analog controller signal transmission though the process will be suffered from the limitations of band-width and large gain variation. The variability of the integration technology is more critical, with higher switching frequency. Although the analog control is still dominant in the SMPS applications, it is becoming less adequate to meet the complex requirements of higher switching frequency for the passive components reduction, and the dynamic response improving in today's portable devices [14][21].

1.1.2. Digital control in DC-DC converters

The digital control has gained more and more popularity in the field of Power Electronics (see Fig. 1.2). Having based on micro-processor or Digital Signal Processor (DSP), it has been applied for several years in motion control, an in medium to high power line-frequency based application, such as rectifiers, inverters, and uninterruptible power supplies (UPS). Generally, these digital control systems present the sufficient resources to accommodate the modest switching frequency of the converter in range of kHz, where the PWM signals of interest are generated by DPWM core at low and medium power applications. In these medium to high power applications system, the size is not the primary focus, either the power consumption. However, for the battery-powered portable applications, like cell phones and the PDA products, higher switching frequencies in the MHz and tens of MHz range are needed, in order to reduce the size of the passive components. Such high switching frequency cannot be achieved by the traditional digital control mentioned before. Furthermore, the power consumption traditional DSP digital controllers are not critical in medium to high-power levels, while in battery-powered system, where it is definitely resulted in low efficiency, when this power consumption is compared to the output power. Moreover, low-power portable applications are driven by cost, which means the digital controller cost, and complexity are very important. Because of the requirements of high speed, high frequency, small size, low power, and low cost are difficult to achieve simultaneously, most DSP and other controllers are either too expensive and complex, or too high power consumer, or too slow to be able to perform the required high-performance, and real time control task.

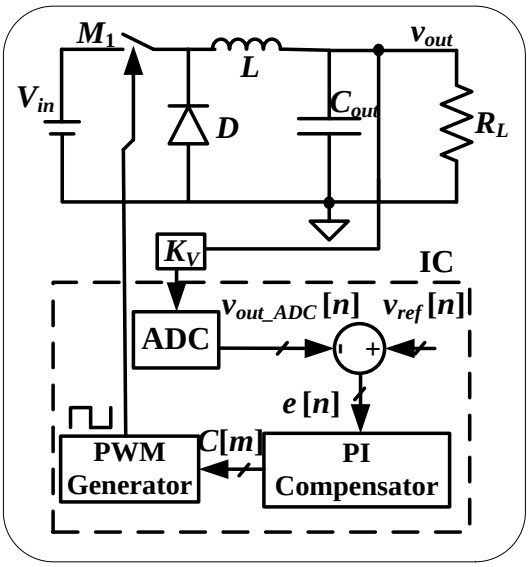

Fig. 1.2 A basic example of digital controlled buck converter

In order to reduce size and improve the system performance, recently the digital controllers in dedicated ASIC or monolithic IC rather, than the traditional DSP has become an attractive research topic in SMPS for high performance applications in portable electronics. Figure illustrates the block diagram of a digitally controlled buck converter. In general, the digital controller consists of three primary blocks: analog-to-digital converter (ADC), digital control law and digital PWM (DPWM), and all these blocks should be integrated in single chip. The digital controller SMPS operates simultaneously, as the analog controller, as follows:

The output voltage V_{out} subtracted from reference voltage V_{ref} is resulted in the voltage error ε. The ADC transfers the analog error to discrete in digital terms $\varepsilon[n]$. During each switching period, the error value is sent to the control law block, where the controller makes algorithm calculation to regulate the output by new digital control duty $c[m]$ of PWM ratio. Through the DPWM block, the digital duty value is converted into the time analog signal to driver MOSFET switches.

As shown in Figure, the complete digital controller that contains three blocks (ADC, Control-law and DPWM) can be realized, totally, on IC chip, which significantly reduces the size of the overall SMPS. The ADC can be designed, using analog-to-digital CMOS technologies at low cost. The algorithm calculation of the control law can be implemented with internal structure of the logic circuit, without any external analog component. Thus, the digital controller should be less sensitive to the environment, than analog counterpart. Also digital control law offers possibility to implement more sophisticated control strategies and other intelligent interface functions that are impractical in analog. Another noticeable merit

is, that digital controller signal transmission through the process can be used to address the limitation of bandwidth, and large gain variation that is associated, with the traditional analog approaches. In addition, by using the available automated design soft tools, and Hardware Description Language (HDL), digital controller system design cycle can be accelerated, and it offers a degree of programming flexibility to modify the update the product, that is impossible in the analog design[22]-[26],[72].

From the comparison between analog and digital control mentioned above, it can be seen, that digital control in the SMPS application has the advantages as follows:

- Advanced control algorithms implementation;
- Flexibility and programmability;
- Size miniaturization and high frequency;
- Less susceptible to the components and variations;
- Alleviation for the limitation of bandwidth and large gain variation in the control law;

1.1.3. Background review of Analog-to-Digital Converters (ADC)

This chapter presents the various figures of merits, having associated with ADCs. It includes review of ADCs and trends. Most famous architectures, suitable for the digital controlled SMPS, have also been included.

1.1.3.1. ADC performance – static considerations

Several static parameters limit both the achievable resolution, and conversion speed of A/D converters. One of these parameters, the component mismatch, is dependent on the process, used fabricate the ADC, as well as the components design. Consider, for example, a simple 2-bit flash ADC. In order to setup the reference voltages, to which the input compared, a ladder of 2^2 R valued resistors could be used. The input voltage is compared to each of these 4 reference voltages, with a comparator. If the resistor values were not well matched, the reference voltages would not be exact, and the resulting digitization would be non-linear. Likewise, if the comparator offsets were not matched, the digitization would behave just, as if the reference voltages were not exact.

Power dissipation is another parameter that limits the ADC performance. It is shown in following chapter, that the conversion speed of flash converter is limited by settling time of a single comparator. Therefore, implementing a converter would require a comparator that is capable of settling in less. Also a comparator consists of several gain stages followed by

a decision making latch. Thus, the settling time of the comparator is determined by the time required for the gain stages to amplify the input signal enough to trigger the latch, in addition to the settling time of the latch. If the gain portion of the comparator can be approximated, as a single pole system, the rise time of the input to the latch is the exponential decay, toward the final value, and the time constant of the decay is determined by the comparator bandwidth. The settling time decreasing of the comparator would be required the comparator bandwidth increasing. Thus, increase in bandwidth can be achieved by several means, including the clever system design. However, given a circuit topology, the bandwidth is proportional to the trans-conductance of the devices [27]. Since, the trans-conductance is proportional to current, having dissipated more power will be resulted in faster comparators. Therefore, the speed of a flash converter in a given process technology is limited by the power, that can be spent in the comparators.

Other static parameters also limit the performance of A/D converters, such as die area. However, these problems can all be solved by laser trimming for accuracy, increasing power consumption, having spent more money on silicon area, and so on.

1.1.3.2. ADC performance – dynamic considerations

The dynamic performance limitations are more complex and harder to be solved, than the static ones. First, consider the dynamic problems in a simple flash converter. Unless the comparators present a varying load, the resistor ladder should be maintained a stable set of the reference voltages. However, the comparator performance is much less, dynamically, stable. First, comparators are taken some finite time to make a decision. Until the digital output of the comparator has settled to either a '0' or a '1', the comparator is in a metastable state. In order to avoid metastable states, the comparator is needed to settle more quickly. As argued in the last section, this can be achieved by consuming more power. However, there is a fundamental limit to how fast the comparator can be made, which is related to the speed of the device technology, having used to implement the converter[28]. It is given, that current IC processes can produce transistor with f_T in excess of tens gigahertz, the comparator metastability only limits the ADC performance at very high speeds.

Another dynamic performance limiting factor is noise in the ADC. There are many noise sources in a comparator circuit, including the thermal noise in resistors and thermal, shot, and flicker noise in transistors. All of these noise sources can be referred to the input of the circuit, and, if this input referred noise is of the same order of magnitude, as an LSB, the ADC accuracy will be suffered. As it is in the case with the comparator settling time, the

power consumption increasing can be solved the problems, due to noise sources in the ADC. If the thermal noise in the resistor ladder is a problem, the resistor values can be decreased, lowering the noise, but increasing the current through the ladder. If transistor noise were the dominant source, increasing the current through the transistors would be helped, because the noise power in a transistor is, inversely, proportional to the trans-conductance.

1.1.3.3. Sample-and-Hold unit

The sample-and-hold (S/H) is an important analog building block, which is used to sample analog input signal, and hold the sampled value over the entire conversion time for subsequent processing. To limit the errors, due to charge injection and clock feedthrough, a single-ended bottom plane is switched capacitor sample, and hold circuit, having used in the ADC designs.

1.1.3.4. Resolution requirements of the Analog-to-Digital Converter (ADC)

Normally, analog control provides a very fine resolution in the output voltage. The output voltage can be adjusted to any arbitrary value, which is only limited by loop gain and noise levels. However, because of the quantizing elements exist in the ADC and DPWM, the digital controller has a fine set of discrete levels in nature. Thus, the quantization of A/D converter and DPWM is critical to both static and dynamic performance of power converters.

The need for certain amount of accuracy in representing analog signals by their digital equivalents governs the ADC resolution of the ADC number of bits. Resolution of the ADC should be such that the output voltage error of power converter tightly falls within the allowed voltage range. That is the least significant bit (LSB) of the ADC (V_{LSB}) has to be less, than the allowed maximum scaled output voltage variation ΔV (1.1).

$$V_{LSB} = \frac{V_{max}}{2^{N_{ADC}}} \leq \Delta V \times G = \Delta V \times \frac{V_{ref}}{V_{out}} \tag{1.1}$$

where G is the scaled factor of voltage sensor and, V_{ref}, V_{out} and V_{max} are the reference, output, and maximum output voltage, respectively. Then, the required resolution $N_{ADC}$of ADC, with respect to a chosen reference voltage level can be acquired by:

$$\mathrm{N_{ADC}} \geq \text{integer}\left[\log_2\left(\frac{\mathrm{V_{max}}}{\mathrm{V_{ref}}} \times \frac{\mathrm{V_{out}}}{\Delta \mathrm{V}}\right)\right] \tag{1.2}$$

where the integer function takes the upper rounded integer value of the product. Equation indicates the minimum number of bits of the ADC to meet output voltage regulation requirement of power converters. For example, a voltage regulator with $1.5V$ reference

voltage, allowed voltage variation, if $G = 1$, and the voltage scale range of ADC is $1.8V$, then a minimum 9-bit resolution will be required for the ADC.

Hence, any sensed voltage higher than V_{ref} should be scaled down to V_{ref}, and, appropriately, reflected in feedback gain, while designing the control loop. In a particular, the SMPS application, the need for sensing output voltage or inductor current decides the minimum required resolution, since the resolution should be higher, than the tolerable output voltage or inductor current ripple. The ADC resolution is the key to the fast system response as errors in the loop can have higher resolution, and can be quickly corrected.

Another important criterion for the ADC choice is its conversion time, and power consumption from time of measurement at the input to the availability of the digital word at its output register. Modern high speed ADCs still have around hundreds of nanoseconds of conversion time [20],[21]. The conversion time can also be interpreted, as the maximum allowable sampling frequency f_{samp} of the ADC. There are three important effects of conversion time delay. Firstly, such a delay prevents immediate controller action, due to this time delay, and secondly, its presence is a limit to the sampling frequency and, hence, limits the bandwidth of all the system. Finally, for the low-power high-frequency SMPS applications, the power consumption of the ADC is becoming critical, with the increase in sampling frequency.

1.1.3.5. Flip-flop's metastability

The counter structure and the quantizing register in advanced ADC types (e.g. ADC based delay line) is usually build-up by Sense-Amplifier based flip-flops (SAFF) and/or D flip-flops.

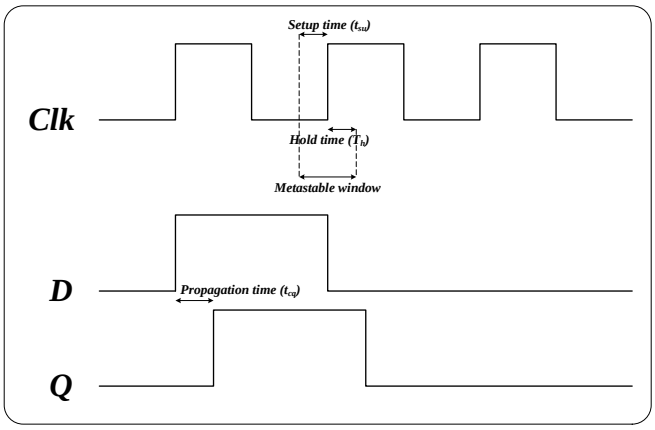

Fig. 1.3 Setup and hold time definitions

The counter structure and the quantizing register in advanced ADC types (e.g. ADC based delay line) is usually build-up by Sense-Amplifier based flip-flops (SAFF) and/or D flip-flops. A well-known problem with these building blocks is their susceptibility to metastability. Metastability occurs when flip-flop setup and hold times are violated. The result is that the flip-flop's output is not well defined and can be anything between the two stable states, '1' logic or '0' logic, and, therefore, seriously degrade the performance of the ADC structure [29],[30]. The definitions used for metastability characterizing are, setup time t_{su}, hold time t_h, propagation delay t_{cq} and metastability window according to the Fig. 1.3.

1.1.3.6. Analog-to-Digital Convertor (ADC) architectures

1.1.3.6.1. Flash A/D converter

A block diagram of a flash A/D converter presented in Fig. 1.4. The Digital-to-Analog Converter (DAC) converts the digital reference word D_{ref} to an analog voltage ΔV_{ref}, which is the input reference range of the ADC[29],[30]. Note that this DAC can be slow compared to the response time of the regulator, since D_{ref} is constant, then a number of comparators (2^N) are connected to ΔV_{ref} through an offset network with steps $\Delta V_{ref}/2^N$, creating 2^N quantization bins around ΔV_{ref}. The controlled quantity of error voltage is fed in the other input of the comparators. Note that, since ΔV is compared against ΔV_{ref}, the resulting digital signal D_e the difference between the two, which is like a window of digital representation for the error signal ΔV. Hence, the window architecture implements both an ADC and an error amplifier.

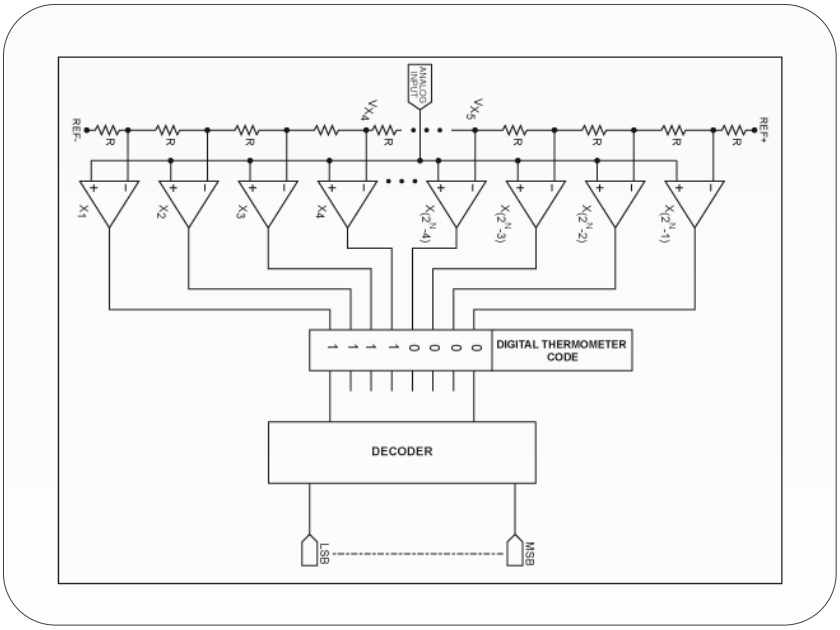

Fig. 1.4 Flash ADC simlifed architecture

The flash ADC has the advantage of fast conversion within only one cycle. However if ΔV exceeds the range of the ΔV_{ref} window during a large transient, these comparators turn all the converter on or off (depending on the direction of the transient), in an attempt to clamp ΔV. To solve this issue, a larger window and faster comparators are needed, which results in the cost increase of silicon area and power consumption.

Flash converters are suffered from bubble errors (also they are called the sparkle codes). A valid thermometer code consists of a series of all '0' and all '1', like 00001111. An out of place '0' or '1' is called a bubble, and it is the result of comparator ambiguity, imperfect input settling time, or comparator timing mismatch. Most modern flash converters are used the encoding techniques, that minimizes the effect of bubble error.

1.1.3.6.2. Delay line A/D Converter

The delay line ADC was proposed, in order to avoid the increase of silicon area, and power consumption [31]-[35]. The delay line A/D converter is based on the principle, that the propagation delay of a logic gate in standard CMOS process is increased, if the gate supply voltage is reduced. To the first order, the propagation delay t_{pd}, as a function of the supply voltage V_{DD} is given by:

$$t_{pd} = K \times \frac{V_{DD}}{(V_{DD}-V_{th})^2} \tag{1.3}$$

where V_{th} is the CMOS device threshold voltage, K is a constant, that depends on the device or process parameters, and the capacitive loading of the gate. It can be observed, that increasing V_{DD} is resulted in a shorter delay. For supply voltages higher, than the threshold V_{th}, the delay is approximately inversely proportional to V_{DD}. There are a number of possible implementations of the delay cell.

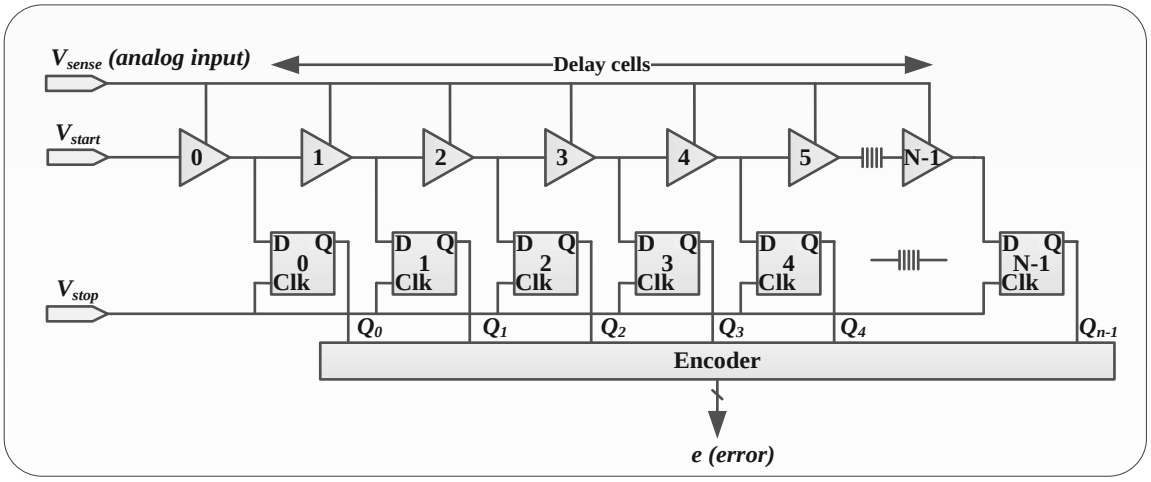

Fig. 1.5 Delay line ADC classic architecture

A basic delay line A/D converter consists of a series of such delay units, as shown in Fig. 1.5. A string of delay cells (consisting of logic gates) forms a delay line supplied from the sensed analog voltage V_{sense}. Each delay cell has an input and output pins.

Initially, at the beginning of each switching cycle, a "start" signal is sent to delay line ADC. After a fixed time, T_{sample}, a sampling pulse is generated and passes through a string of D flip-flop register, the output of each unit delay cell will be stored in the register. The working principle is the same, like the TDC module except the propagation time, which is the function of V_{sense}. Since the logic signal transmitting speed has an inverse proportion to power supply V_{DD}, the number of '1' logic of sampling results will be augmented, with the increase of power voltage V_{DD}. It should be noted, that a high resolution can only be achieved in a small window range of the ADC.

The basic delay line ADC converter is resulted in a reference voltage V_{ref}, that is, indirectly, determined by the length of the delay line, and by delay-versus-voltage characteristic of the delay cell. In practice, because of process, and temperature variations, the reference value, having obtained by the basic delay line ADC configuration cannot be, precisely, controlled. Variations in the effective V_{ref} result in variations of the regulated output voltage, and the power supply may be failed to meet the specified static, and dynamic voltage regulation. Therefore, the delay line ADC, with the precise self-calibration ability against process and temperature is needed.

The two conversions are performed in each switching period. In one half of the switching period, the reference voltage V_{ref} is applied to the A/D converter. The result of the reference conversion e_{ref} is ideally 0, but the actual value can be different, because of the process, and temperature variations as it mentioned before. The reference conversion result e_{ref} is stored in the register. In the second part of the period, the input analog voltage V_{sense} is applied to the ADC, and the result is subtracted from e_{ref} to be obtained the (precisely calibrated) value of the error signal. If desired, the reference conversion for the purpose of calibration of the delay line ADC does not have to be performed every switching period.

1.1.3.6.3. ADCs based on Voltage-to-Frequency conversion

In a voltage-to-frequency conversion is based the ADC architecture, the input signal is converted to frequency (or phase), and, then quantized by a frequency (phase) quantizer. The main challenge is the precision and linearity of the voltage-to-frequency conversion. Typically, this time-based ADC uses a voltage-controlled oscillator (VCO), as a voltage-to-frequency converter, where the frequency is controlled by the analog input voltage, V_{in}[36].

During a limited amount of time, t_{sample}, the output of the VCO is fed to a counter, which detects the edge changes ("high-to-low" or "low-to-high") of the VCO output and, accordingly, quantizes the frequency. The counter output is processed by a mapping table, which stores the characteristics of the VCO. The resolution of the ADC is determined by the maximum and minimum VCO frequency and t_{sample} as:

$$Resolution = \log_2\left(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}}\right) \tag{1.4}$$

where, f_{sample} is the inverse of t_{sample} and f_{max} and f_{min} are the maximum, and minimum VCO frequency, respectively.

In order to increase ADC speed and resolution, a multiphase VCO, such as ring VCO can be employed, as described in Fig. 1.6. During the sampling period, the VCO converts the analog input voltage to proportional phase value. The output is, coarsely, quantized by a counter, which is counting rising and falling edges. The residual phase or coarse quantized error is quantized by the phase detectors tapped to different stages of the ring oscillator. Assuming N_{cell} stages in the ring VCO, the resolution is modified to:

$$Resolution = \log_2\left[\left(\frac{f_{max}}{f_{sample}} - \frac{f_{min}}{f_{sample}}\right) \times 2 \times N_{cell}\right] \tag{1.5}$$

There are many challenges involved in implementing these architectures, such as jitter, linearity of the VCO, process type, voltage supply, and the temperature (PVT) variations. The main advantage of this architecture is that the VCO acts, as the voltage to frequency converter and quantizer at the same time. The VCO along with a pulse counter can work, as a high-speed quantizer. A VCO also produces first order noise shaping, because of the phase of the output pulse is an integrated quantity of the input voltage. Most VCOs suffer from a non-linear relationship between the input voltage and output frequency. To improve linearity, the VCO can be configured with feedback, as a 2^{nd} order $\Sigma\Delta$-ADC.

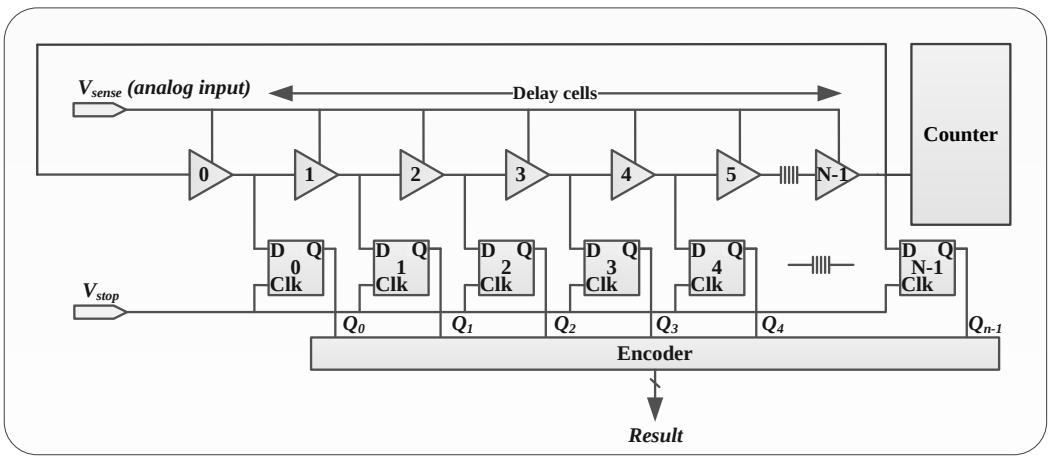

Fig. 1.6 VCO-based ADC architecture

1.1.4. Background review of digital pulse width modulation (DPWM)

This section discusses the various methods of implementing digital pulse width modulation, such as counter based, delay line based, and hybrid. This section also discusses some common modulator techniques. The three common modulators are leading edge, trailing edge, and double edge modulation. The next section discusses the operation, and delay caused by digital pulse width modulators.

1.1.4.1. Resolution requirements of DPWM

By nature, the signal generated by the DPWM can only provide discrete duty cycle values. Therefore, the output voltage is also only a set of discrete output voltages. In order to ensure steady state behavior in controlled variable, it is necessary, that the resolution of the DPWM output is higher the resolution of the ADC. This is to make sure, that any quantized control value from output of DPWM can drive the control variable to a zero error in binary. This a necessary condition to avoid a low frequency oscillations, which are called the limit cycle oscillation [37]-[39]. Fig. 1.7 shows the output voltage V_{out} behavior, with DPWM resolution lower, and higher, than the ADC resolution, respectively. It is essential, that the resolution of the DPWM should be high enough to avoid the limit cycle oscillation phenomena.

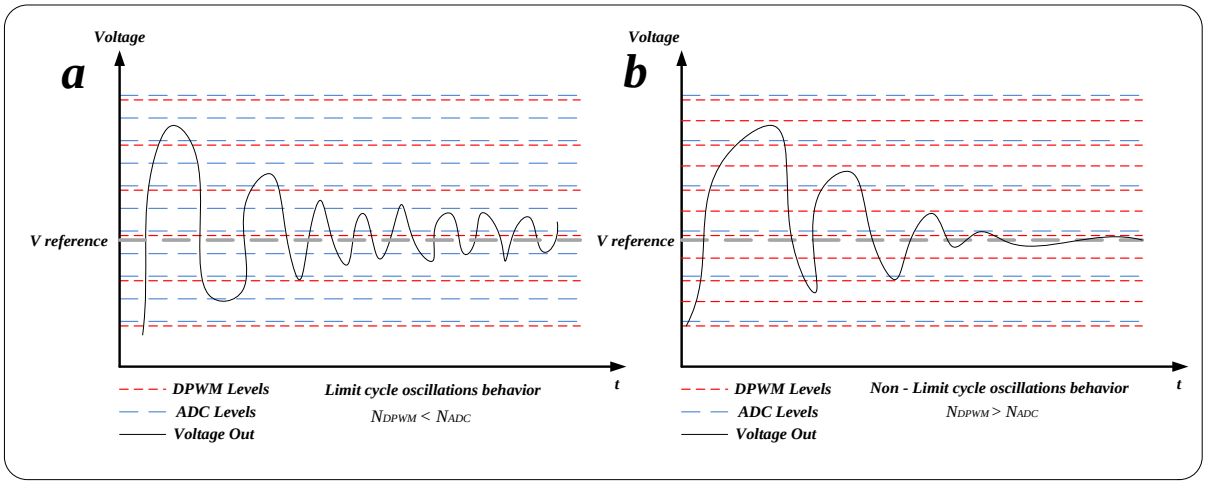

Fig. 1.7 Behavior of output voltage with (a) DPWM resolution lower, than ADC resolution; (b) DPWM resolution higher, than ADC resolution

A necessary condition to avoid the limit cycle oscillation is, that the change ΔV in the output voltage cause by one LSB change in the duty cycle ratio ΔD has to be smaller, than the analog equivalent of the LSB of the ADC. For the SMPS synchronous buck converter widely used for voltage regulators:

$$\Delta V = V_{in} \times \Delta D = \frac{V_{in}}{2^{N_{DPWM}}} \leq \frac{V_{max}}{2^{N_{ADC}}} \times \frac{V_{out}}{V_{ref}} \quad (1.6)$$

where V_{in} is the input voltage, N_{DPWM} is the bit number of DPWM resolution. Thus, the minimum number of the DPWM is given, as:

$$N_{DPWM} \geq integer\left[N_{ADC} + \log_2\left(\frac{V_{ref}}{V_{max} \times D}\right)\right] \quad (1.7)$$

where $D = V_{out}/V_{in}$ is the duty ration in steady-state. In order to avoid limit cycle oscillation, it can be seen from equation, that the number of bits is required for DPWM generator, N_{DPWM}, is at least larger by one bit, than the ADC resolution in steady-state, thus N_{DPWM} is described by:

$$N_{DPWM} \geq N_{ADC} + 1 \quad (1.8)$$

Indeed, if the DPWM resolution is lower, than the ADC resolution, there is no the DPWM level, that maps into the ADC binary code, corresponding, to the reference voltage. In steady-state, the controller will be attempting to track the zero-error binary code. However, due to the lack of corresponding DPWM level, it will alternate between the DPWM levels around the zero-error binary code, as shown in Fig. 1.7. This will be result in a non-equilibrium behavior, such as the steady-state limit cycling. Therefore, it is very important to achieve a high resolution in the DPWM generation, in digital control of the DC-DC converters. Theoretically, as long as the clock frequency of the digital circuit is high enough, compared to the switching frequency, the limit cycle oscillation can be avoided. Unfortunately, the required clock frequency will be too high to be implemented efficiently.

A high resolution DPWM is required to eliminate limit cycle oscillations on output voltage. However, the increase in DPWM resolution implies the increase in system clock frequency. The system clock reflects the power consumption of the digital control system in future silicon implementations. Moreover, Electro-Magnetic Compatibility is distributed over the harmonics of the system clock signal. Higher frequency would mean a possible correlation, with communication signals in radio frequency range embedded systems.

1.1.4.2. DPWM architectures

1.1.4.2.1. Counter based DPWM

The basic operation of DPWM implemented in the digital domain, using counter will discussed. In analog PWM, the error signal is compared, with ramp signal and PWM pulses are generated. In digital PWM, the duty cycle is compared, with the counter value, and the DPWM signal generated [42]-[44]. As an example 10 bit duty cycle will be in range of 0 to

1023. The transformation of analog to digital is performed by converting the error signal to duty cycle, using the ADC. The ramp signal is produced, using a counter. The resolutions of DPWM are finite, when compared to the analog one. In other words, DPWM has better output regulation and less or no limit cycle oscillations. Counter based DPWM has modulation delays. These delays occur, when there is a change in duty cycle. Counter based DPWM is implemented, using counters, as shown in Fig. 1.8.

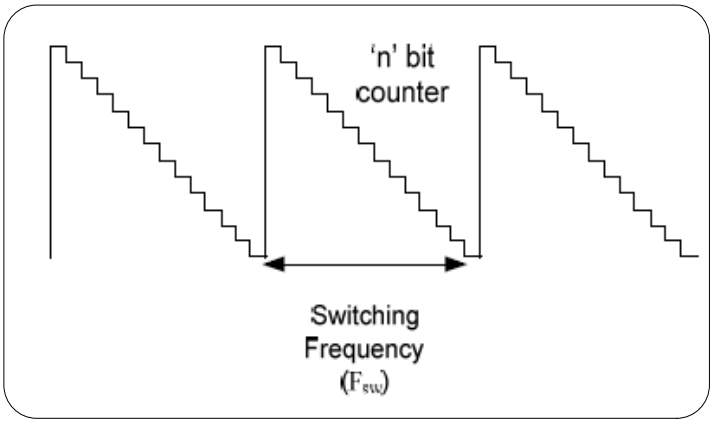

Fig. 1.8 Behavior of DPWM based counter

The counter can be either up counter, down counter, or an up-down counter, depending on modulation scheme. When the counter counts down, then it depicts the leading edge modulator. When the counter counts up, then it depicts the trailing edge modulator. When the counter counts up and down, then it depicts the dual edge modulator. The input clock frequency F_{clk} of the counter is directly proportional to switching frequency F_{sw}, and number of bits n. The relationship can be expressed, as follows:

$$F_{clk} = F_{sw} \times 2^n \tag{1.9}$$

The main advantages of the counter based DPWM are simplicity and linearity. In order to achieve high resolution, the number of bits in the counter should be high. Unlike that, the main disadvantage of counter based DPWM is need for high clock frequency, and high power consumption. For example, a 10 bit DPWM, with switching frequency of 1MHz. the required clock frequency will be, approximately, 1GHz, and also power consumption will be high. Therefore, implementation of high frequency and high resolution counter based DPWM would be difficult, in terms of timing properties. The three common modulators have already been implemented, using counter based technique is discussed below.

Leading-Edge Digital Pulse Width Modulation – the leading-edge DPWM block diagram, and its operation waveform are shown in Fig. 1.9. The duty cycle and counter are inputs to a comparator. The counter type is a down counter. The output of the comparator turns the DPWM pulse on, whenever the duty cycle is higher, than the counter value. The DPWM

will be turned off only at the end of switching cycle. The S-R flip flop sets the DPWM high, when the duty cycle is greater, than counter value, and resets, when the main counter finishes counting to the zero value.

Under the transient load condition at point t_3, as shown in Fig. 1.9 (b), the duty cycle drops below the counter, but the modulator cannot respond to the change, it waits, until he and of the switching cycle, to turn off the DPWM. The turn off delays results in overcharging the inductor. Therefore, inductor delivers more power to output and cause extra overshoot or ring back in output voltage. So, this conventional leading-edge modulation has delay in turning off the DPWM [51]-[53].

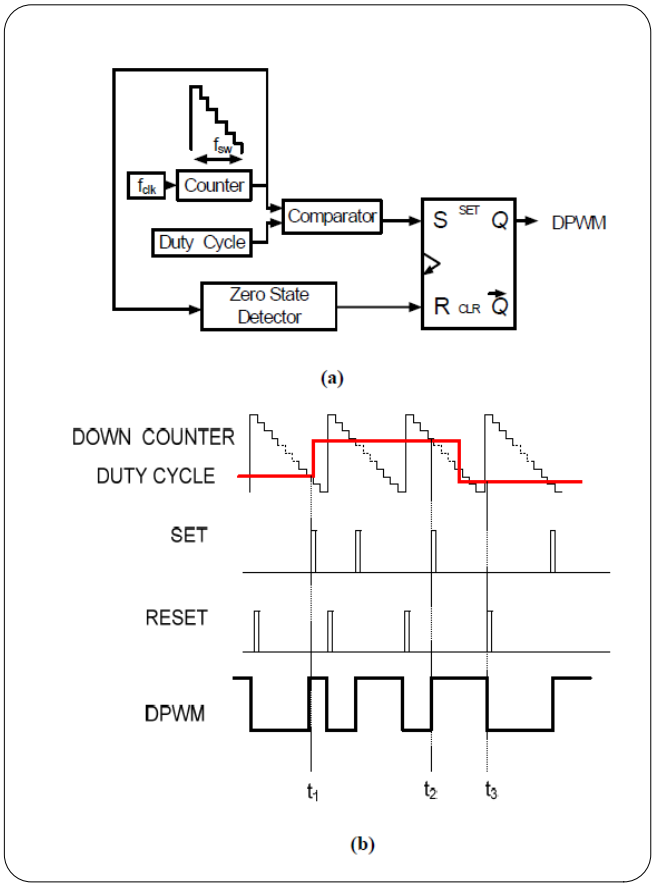

Fig. 1.9 Leading edge DPWM; (a) block diagram; (b) behavior

Trailing-Edge Digital Pulse Width Modulation – trailing-edge DPWM block diagram and its operation waveforms are shown in Fig. 1.10. In trailing edge modulation, the DPWM is turned on by the clock signal, and it is turned off by output of the comparator. The inputs to the comparator are similar to leading edge modulation. But here, the counter is an up counter type. In this scheme, turning on the DPWM pulse is fixed, and turning off the pulse is done by output of the comparator. Therefore, initially at the starting of switching cycle, the DPWM is turned on, and if the duty cycle values go below the counter, the comparator the DPWM is turned off. In this case, after the DPWM is switched off by comparator, and, if the

duty cycle goes high in the same switching cycle, then the modulator will not respond to the change it waits, until the next switching cycle. At point t_1, as shown in Fig. 1.10 (b), the duty cycle goes above the counter, but the modulator cannot respond to the change, it waits, until the end of the switching cycle, to turn on the DPWM. Therefore, this causes a turn on delay [51]-[53].

Dual-Edge Digital Pulse Width Modulation – the block diagram of dual-edge DPWM and its operation waveform are shown in Fig. 1.11. The counter in this conventional scheme is an up/down counter. In the first half of the switching cycle, the counter acts, as either up or down, and in the second half of the cycle, it acts, either down or up, or vice versa. When the counter value is greater, than duty cycle, then the DPWM pulse is set to high. Half of the switching cycle acts, as the leading edge, and other half of the switching cycle acts, as the trailing edge. Therefore, in this case, turn on and turn off delay times exist, and are shorter, when compared to the leading edge and trailing edge modulator [51]-[53].

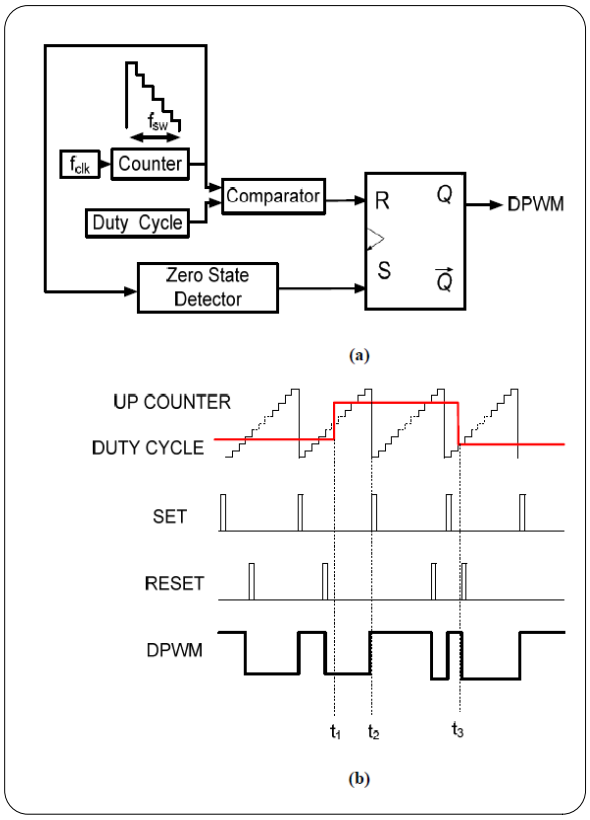

Fig. 1.10 Trailing edge DPWM; (a) block diagram; (b) behavior

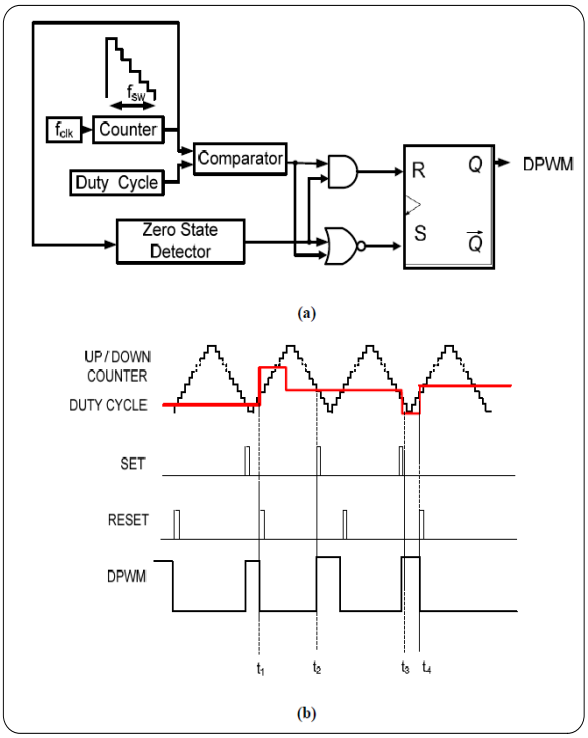

Fig. 1.11 Dual-edge DPWM; (a) block diagram; (b) behavior

1.1.4.2.2. DPWM based delay-line approach

The block diagram of alternative method to generate DPWM signal with high resolution at low power is to employ a delay line structure [17][41],[42], as shown in Fig. 1.12. It takes the advantage of the latency of the common circuit elements (e.g. logic elements, flip-flops, etc.). This type of modulation employs delay cells, having connected in cascade. The pulse width is quantized, as a function of delay cells. For an n bit duty cycle, 2^n delay elements are used. The selection of the delay cells is made by multiplexer unit. The multiplexer is selected in such a way that for 'n' bit duty cycle, $2^n : 1$ multiplexer is used. Therefore, the control signal for the multiplexer is also 'n' bit. The value of these 'n' bits control signal is the duty cycle value. Selection of the delay cells are performed by the multiplexer's control signal. The total delay of the delay line is adjusted to be matched the reference clock period.

The power loss is significantly reduced, compared with the fast counter-comparator scheme, as the fast clock is replaced by a delay line, which operates at the switching frequency of the converter. However, the disadvantage of this method is, that the size of multiplexer is increased, exponentially. Moreover, the linearity of digital-to-time domain conversion depends on the delay cell. Like the delay line ADC, the accuracy of delay propagation is sensitive to the various effects, such as temperature, manufacture process, voltage supply, etc.

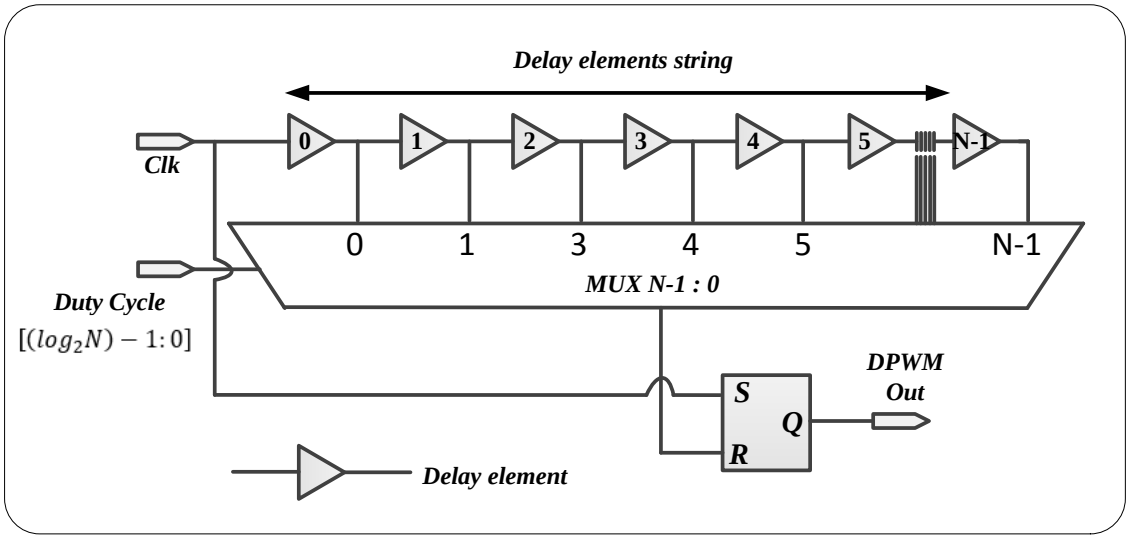

Fig. 1.12 Delay-line DPWM

1.1.4.2.3. Segmented delay-line DPWM

Based on the delay-line DPWM, another similar structure of the delay-line, with multiplexer scheme in the segmented DPWM, where the delay blocks are not of equal length, but are assembled in a way, that it is allowed them to be driven directly by a digital code [45],[46]. For example, a 6 bit DPWM, with 3 segments of delay line is shown in Fig. 1.13.

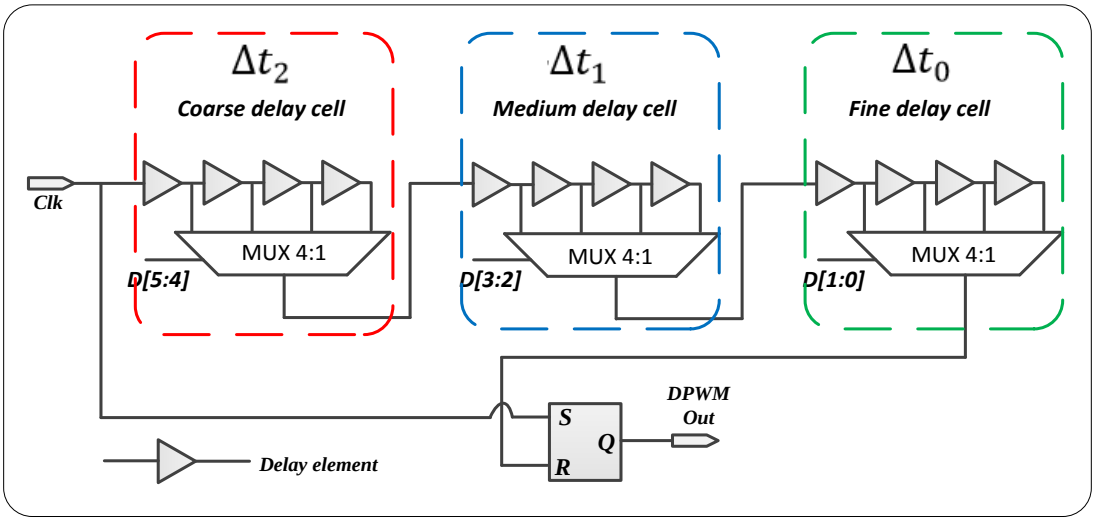

Fig. 1.13 Segmented delay-line DPWM

Each segment has a 4 to 1 multiplexer controlled by two bits of $d[n]$. The delay in each of the four elements of the segment is given by the following formula:

$$\Delta t_2 = 4\Delta t_1 = 16\Delta t_0 \tag{1.10}$$

For 6-bit DPWM implementation with delay line DPWM, it will be required $2^6 = 64$ delay cells, with fine delay characteristic of Δt_0. By contrast, with the implementation in segment delay line DPWM, only $(2^2 + 2^2 + 2^2) = 12$ delay cells of fine-delay and coarse-

delay are required, of which 4 "coarse" cells with Δt_2 delay, 4 "moderate" cells with Δt_1 delay, and 4 "fine cells with Δt_0 delay. That is greatly reduced the number of fine-delay cells, and, consequently, save the silicon rea and power consumption. The segment delay line DPWM has the benefit of reducing the total are required in system, but also suffers from the degraded linearity, as well as the delay line DPWM.

1.1.4.2.4. DPWM based ring oscillator

A ring oscillator DPWM scheme has area and power considerations, similar to those of the delay line approach. In this scheme [47]-[50], the ring oscillator in the DPWM runs in current starved mode, and by adjusting the supply current frequency can be controlled in the entire ring. The ring frequency is obeyed the relationship:

$$f = \frac{\alpha \times I_{avg}}{C_{load}} \times V_{swing} \tag{1.11}$$

where I_{avg} the current is supplied to the ring oscillator, C_{load} is the equivalent capacitor in the ring, V_{swing} is the voltage swing in the ring, and α is a technology coefficient. Thus, the switching frequency of the converter can be controlled by adjusting the ring oscillator current. The DPWM scheme, having used ring oscillator for n-phase application, is shown in Fig. 1.14. Each delay element output is connected to the phase detector block, based on MUX properties, that can be selected the appropriate signals from the ring. During the operation, a square wave is propagated along the ring. When the rising edge is reached the end of the ring, the falling edge of signal is started its propagation through the ring. An inverse was achieved, when falling edge is reached the last buffer. The XOR gate, having approached to the phase detector, provides multiplication of the output frequency in factor of two, as it has been described in the following formula:

$$f = \frac{2}{\sum_0^{N-1} T_{single\ delay\ element}} \tag{1.12}$$

This approach is required the similar propagation time of '0' logic, and '1' logic through the delay element. Although this scheme has also the limitation of linearity, and sensitivity to variation, the advantage of differential symmetric approaching is able to be increased the converter performance. Since the different phases can be tapped out from symmetric positions on the ring, this technique is especially suitable for the multiphase DPWM generation, such as the digitally controlled multiphase SMPS.

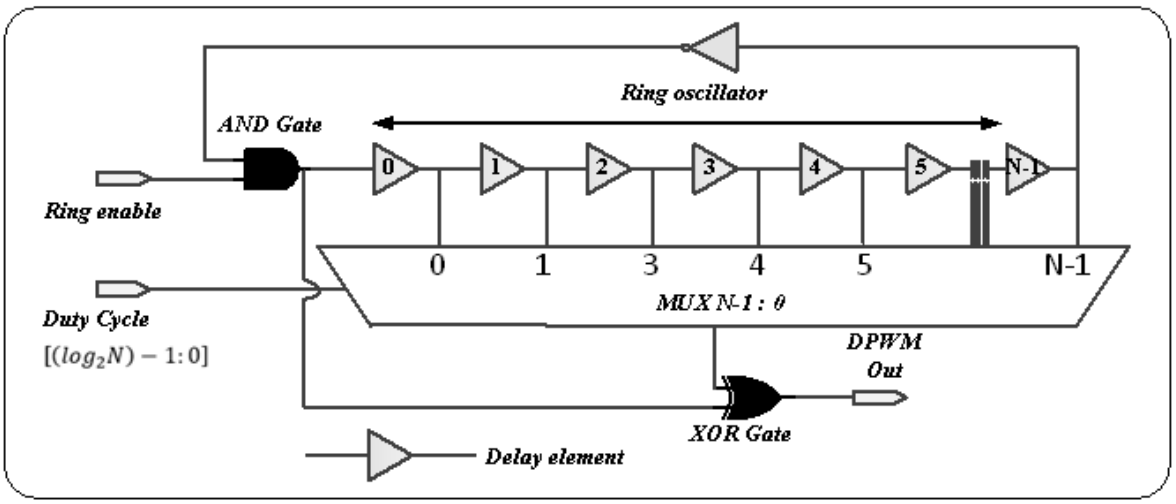

Fig. 1.14 DPWM based ring oscillator

1.1.5. Background review of Time-to-Digital Converters (TDC)

Accurate measurement of time has been played a critical role in the development of science through the history, having started, with the earliest examples of analog clocks, based on solar motion, and water flow, and including the most accurate cesium resonators available today. As a subset of time-keeping technology, the time-to-digital converters (TDC), or the Time Interval Meters (TIM), are, practically, allowed for precise measurement of the time between two independent events. Historically, the TDC have had their significant application in the experimental physics [54]. Today, the TDC are continued to serve an important role not only in the experimental applications, but also in commercial time-of-flight applications, such as laser range finding and positive electron tomography (PET) medical imaging technology [55].

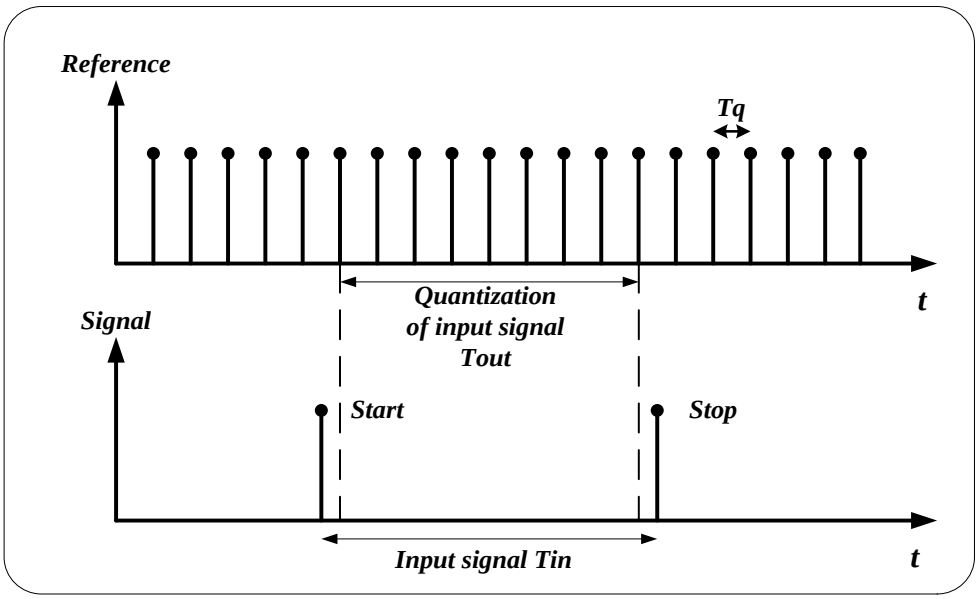

Fig. 1.15 Time quantization general concept

The relatively new applications for TDC, that have emerged is closed-loop timing systems, which are fully integrated in the silicon technology. Since the advanced CMOS processes have already begun to offer extremely compact, robust, and flexible processing power, many applications have begun to be replaced the traditional analog signal processing blocks, with digital signal processing. Such a shift in architectural design places, a relatively increased burden on the mixed-signal interface, especially, in terms of the converter performance.

The Fig. 1.15 is responsible for describing the general operation of the TDC that can be served, as an entry point into the discussion of many different TDC architectures, and ideas [56]. The input time interval, $T_{signal} = t_{stop} - t_{start}$, can be divided up to a number of smaller reference time intervals. An estimate of signal length can be, trivially, calculated by counting the number of intermediate reference pulses or events, although there is an error to this method at both the beginning and the end of measurement:

$$T_{error}[n] = T_{stop}[n] - T_{start}[n] \tag{1.13}$$

Having given these definitions, can be expressed the input and output relationship for the TDC, as:

$$T_{out}[n] = T_{in}[n] - T_{error}[n] \tag{1.14}$$

Or equivalently, in terms of the TDC integer output, as:

$$Out[n] = \frac{T_{in}[n] - T_{error}[n]}{T_q} \tag{1.15}$$

Since the raw TDC resolution is limited by T_q, so the great deal of effort over the years has been made in this value reducing, either, directly, thorough technology advancement, or effectively, by using design techniques, a few examples of which will be covered later in following section. While these efforts have made significant progress in improving the TDC resolution, the applications are continued to be demanded the best resolution and effective measurement range.

Certainly, the best way to achieve an optimal TDC resolution performance is to wait, i.e. to follow the Moor's law, until scaling enables better performance, with the known TDC techniques. While this may be a valid approach for some applications, it does not aid the TDC design in optimizing resolution performance for specific technology. Given the difficulty in improving the raw resolution in s standard CMOS process, then it has become much important for me to fully explore techniques such, as oversampling to improve effective resolution performance.

Moreover, when considering future CMOS TDC and process scaling, it is well known, that transistor and parasitic mismatch has been become a very real and significant problem for the most advanced technologies. Therefore, while intrinsic delay may be continued to decreasing in the future, it is also required the accuracy of the delay to be improved, as well, for the traditional TDC architectures, for benefit from this. Mismatching can be a bottleneck for many TDC architectures. Therefore, having achieved high performance in the presence of large delay, the mismatch is a critical requirement for the TDC future implementations.

As it has been mentioned before, the TDC modules have a wide range of applications. This work is being focused on the TDC implementation, as a significant block of delay line ADC. The next section will be reviewed some state-of-the-art TDC architectures, along with their tradeoffs.

1.1.6. Process variations in Time-to-Digital Converters (TDC)

The variations are important issue of the performance and behavior of the TDCs, because the process, and environmental variations influence, the behavior, and the performance of time-to-digital converters (TDCs). Environmental parameters such, as the PVT (Process, Supply and Temperature) have global impacts on the performance for the circuit block of the TDC. The main reason for the local variations is random dopant fluctuation, and line edge roughness. Both phenomena are critical especially in heavily scaled process, where the quantization effects have been become visible.

In the TDC, the variations have been changed the gate delays in the delay line, and the buffer tree of the stop signal. The impact of local variations in the TDC, especially a buffer tree, is uncertainly of the arrival time of the stop signal. One reason of the uncertainly is the deterministic skew in a buffer tree. Another reason is the local process variations that are caused the skew even in a perfectly balanced tree.

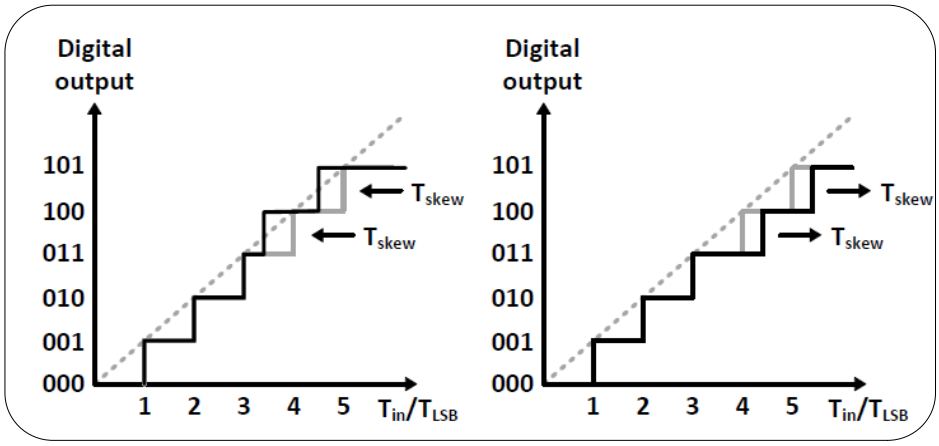

Fig. 1.16 Impact of clock skew on TDC

The Fig. 1.16 shows two groups of delay elements together, with their sampling flip-flop. Each buffer level is caused the skew in the associated branches of a buffer tree. The TDC characteristics, having caused by the skew (uncertain value), are illustrated in Fig. 1.16 (a). $T_{skew} > 0$ means, that the second group of delay elements is sampled later, than the first group, and $T_{skew} < 0$ all step positions, having related to the second group, are shifted to the right (see Fig. 1.16 (b)). If a T_{skew} is larger, than T_{LSB}, this results not only in a DNL error, but also in the missing code. These facts are caused an increased step width at the handover point of the two groups. This means, that the uncertainty of the arrival time of the respective branches is partially correlated, and the prediction of variation effects is became complicated [57]-[59].

Also, the uncertainty of the arrival time grows, with the length of the delay line. Therefore, the delay line should be considered to avoid increasing the uncertainty of the arrival time. In addition, the one more variation should be considered. That is the variations for the comparators inside the TDC. The variations for the comparators, which are the components of the TDC, are also the important issues, with the TDCs. For example, the blackout time of the comparators, functionally, affects the TDC offset, the gain and the resolution. The offset error is not critical in the most applications. The TDC gain, however, delineates the change of the output word per change of the input time interval. This paper has been based on the all-digital TDC implementation, so all the analog issues may be negligible.

1.1.7. Various architectures of Time-to-Digital Converters (TDC)

1.1.7.1. Time-to-Digital Converter (TDC) based on basic delay-line

To increase the measurement resolution, beyond the maximum, feasible clock frequency of each counter clock cycle has to be sub-divided asynchronously by a time-to-digital converter. The Fig. 1.17 illustrates, that the counter values, then, it provides a coarse quantization of the measurement interval, and the TDC a fine sub-quantization [60],[61]. The subdivision of the reference clock interval, is also known, as reference clock interpolation, is done by multiply phases using of the reference clock. A ring oscillator, having consisted of k delay stages, for instance, generates k, equally, spaced versions of the clock signal.

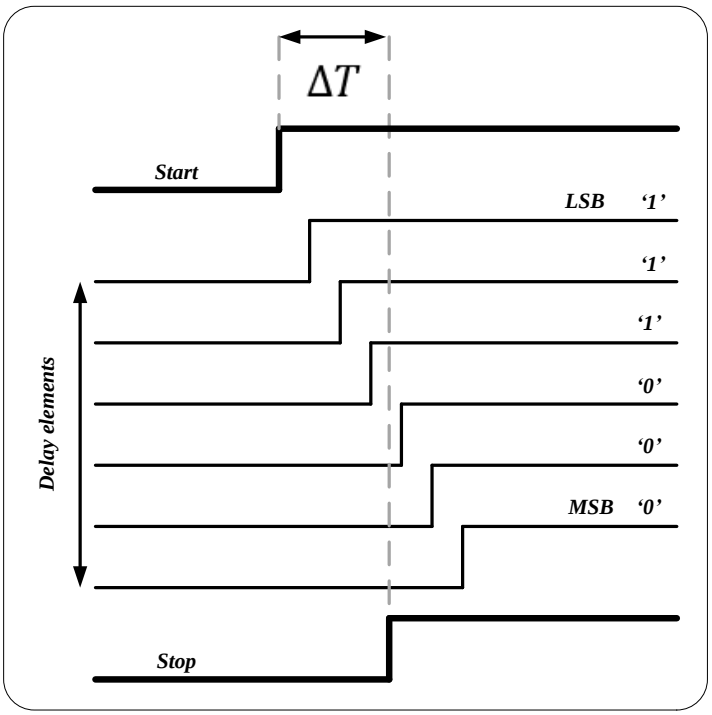

Fig. 1.17 Operatinng principle of TDC based delay-line

An even higher resolution is achieved by delaying the original reference clock in a chain of the digital delay elements. The resolution, then, is depended on the delay of delay elements in the chain. The Fig. 1.17 illustrates the operating principle of the TDC, based on the digital delay line. The reference clock, which is in a more general sense an arbitrary start signal, is delayed along the delay line. At the arrival of the stop signal, the delayed version of start is sampled in parallel. The flip-flop unit can be used, as a sampling element. The sampling process freezes the state of the delay line at the instance, where the stop signal is occurred. This results in a thermometer code, because all the delay stages, which have already been passed by the start signal give a '1' logic value at the outputs of sampling elements, all the delay stages, which have not been passed by the start signal yet give a '0' logic value. The position of the ones transition in this thermometer code is indicated, how far the start signal could be propagated during the time interval, having spanned by the start and the stop signals. Hence, this transition is a measure for the time interval. The number N of all sampling elements, with a '1' logic output is related to the measurement interval ΔT, accordingly, to in the following equation:

$$N = \frac{\Delta T}{T_{LSB}} \tag{1.16}$$

where T_{LSB} is the delay of a single delay element in the delay line. The time interval ΔT can be calculated from the number of '1' logic outputs by the following equation:

$$\Delta T = NT_{LSB} + \varepsilon \tag{1.17}$$

where ε describes the quantization error, that is arisen, as a delay element has been, either passed by the start signal yet, or not. Any intermediate state is not possible.

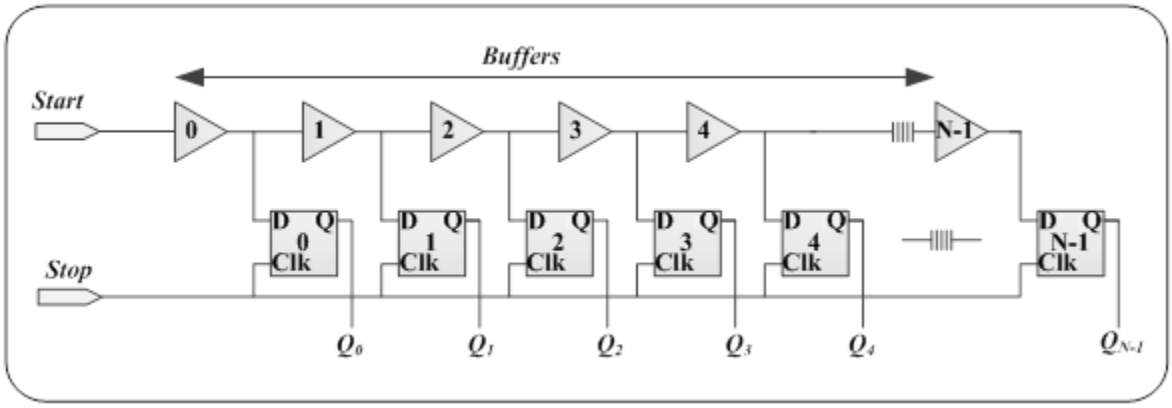

Fig. 1.18 Implementation of basic TDC based delay-line

An implementation of the basic delay line TDC is shown in Fig. 1.18. The start signal ripples along a buffer chain, that is produced the delayed signals. The flip-flops are connected to the outputs of the delay elements, and the state of the delay line sample on the rising edge of the stop signal. Any skew in this buffer tree, directly, is contributed to the non-linearity of the TDC characteristics. For a correct thermometer code, the skew between adjacent branches in this tree has to be smaller, than T_{LSB}, which is made the design challenging.

1.1.7.2. Time-to-Digital Converter (TDC) based on inverted delay-line

The resolution can be doubled by the buffer replacing by the CMOS inverters. The inverters' use means, that both the rising and the falling signal transitions are used for the measurement. Hence, the thermometer code, at the outputs of the sampling elements, is became a pseudo thermometer code, with alternating ones and zeros. The length of the measurement interval is indicated not by a '1' → '0' transition, but by a phase change of the alternation '1' → '0' sequence.

1.1.7.3. Time-to-Digital Converter (TDC) based on Vernier delay-line

The Vernier delay sampling technique is one of the older techniques for time digitization that has been adopted for the resolution improving is shown in Fig. 1.19. The principle of the measurement has been originated from the Vernier ruler [62]-[64]. Two delay lines are required. The delay time of the delay cell in two delay lines is different. By using the Vernier method, the small time difference can be measured. The key point is the delay difference of the delay cell in two delay lines, which should be exactly equivalent to the clock period,

having divided by number of delay cells. In reality, the sampling process can be equivalent to the flash sampling. The bin size of the Vernier sampling is given by the following way:

$$T_{bin} = T_1 - T_2 = \frac{T_{clk}}{2^m} \tag{1.18}$$

where T_1 and T_2 are the delay time of the delay cell in two delay line, respectively. Parameter m is the number of bits for digital outputs. Setting the suitable values of T_1 and T_2, the delay difference of T_1, can be interpolated by T_{bin}. However, the Vernier method uses the multiply sampled clocks, which has been generated from the delay line, with the delay time of T_2.

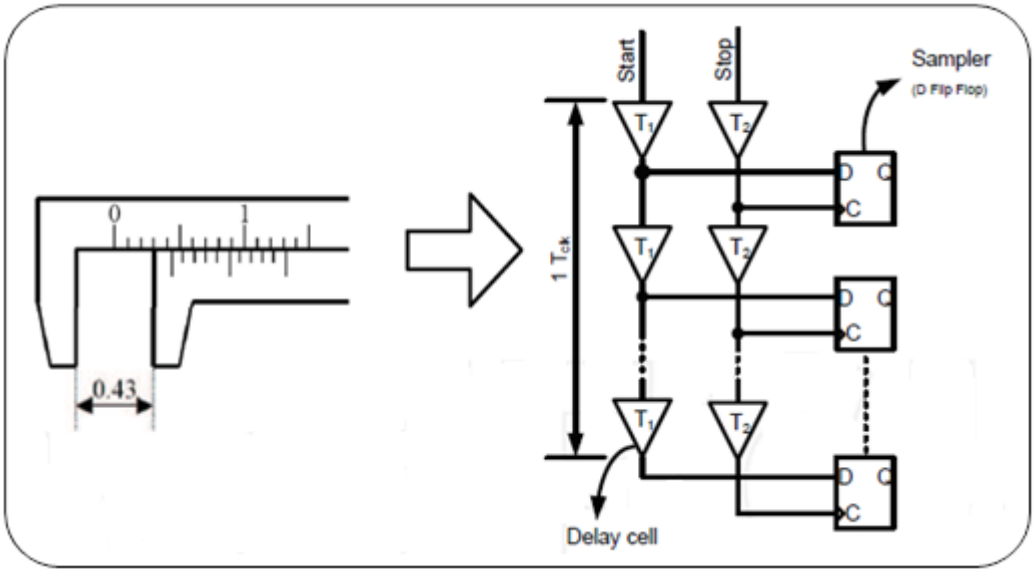

Fig. 1.19 Multiphase samping using the Vernier delay-line

To realize the TDC using Vernier delay line, two DLLs should be employed. Thus, the synchronization of the multiphase clock is very important for this method.

2. FPGA-based approach for Time-to-Digital Converters

The FPGA – Field-Programmable Gate Array (FPGA) is a semiconductor device, having contained the programmable logic components, which are called "logic blocks", and programmable interconnects. The logic blocks can be programmed to perform the function of basic logic gates such, as AND, and XOR, or more complex combinational functions such, as the decoders or the mathematical functions.

The ASIC – Application-specific integrated circuit (ASIC) is an integrated circuit, having designed for a particular use, rather than intended for general-purpose use. The processors, RAM, ROM, etc. are examples of the ASICs.

The FPGA versus the ASIC (see Fig. 2.1) – difference between the ASICs and the FPGAs, mainly, depends on costs, tool availability, performance and design flexibility. They have their own pros, and cons, but it is designers' responsibility to find the advantages of the each of them, and use, either the FPGA, or the ASIC for the final product. However, recent developments in the FPGA domain are narrowing down the benefits of the ASICs ones.

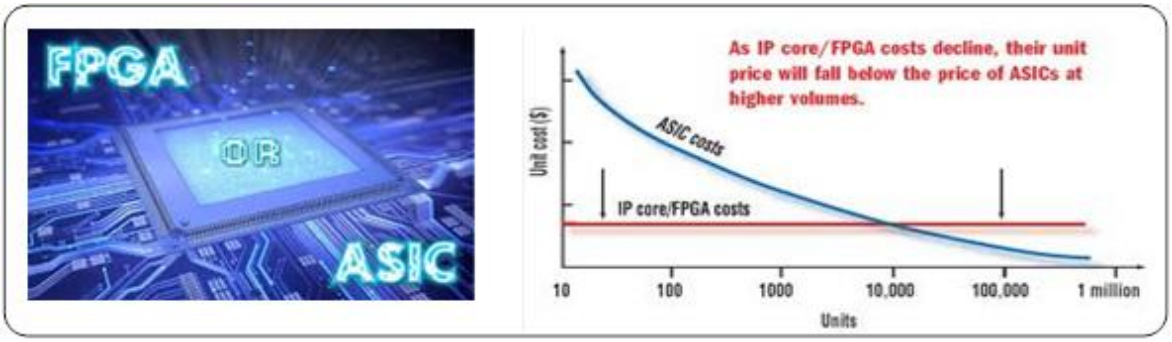

Fig. 2.1 The ASIC versus the FPGA tradeoff[65]

2.2. Review of FPGA design advantages

- Faster time-to-market: no layout, masks or other manufacturing steps are needed for the FPGA design. The readymade FPGA is available and burn your HDL code to the FPGA.
- No NRE (Non-Recurring Expenses): This cost is typically associated with an ASIC design. For the FPGA, this is not there. The FPGA tools are cheap. The ASIC you pay the huge NRE, and tools are very expensive.
- Simpler design cycle: This is due to software that handles much of the routing, placement, and timing. Manual intervention is less. The FPGA design flow eliminates the complex, and time-consuming floor planning, place and route, timing analysis.
- More predictable project cycle: The FPGA design flow eliminates potential re-spins, and wafer capacities of the project, since the design logic has already been synthesized, and verified in the FPGA device.

- Reusability: The reusability of the FPGA is the main advantage. The prototype of the design can be implemented on the FPGA, which could be verified for almost accurate results, so that it can be implemented on the ASIC. If design has faulted change the HDL code, generate bit stream, program to FPGA and test again. The modern FPGAs are reconfigurable both partially and dynamically.

2.3. Review of FPGA design disadvantages

- Power consumption: power consumption in the FPGA is more. You don't have any control over the power optimization.
- Design size limit: You have to use the resources, available in the FPGA. Thus, the FPGA limits the design size.
- Quantity price: Good for low quantity production. As quantity increases, cost per product increases, compared to the ASIC implementation.

2.4. Review of ASIC design advantages

- Lower unit costs: For very high volume designs costs comes out to be very less. Larger volumes of the ASIC design prove to be cheaper, than implementing design, using the FPGA.
- Speed: The ASICs are faster, than the FPGA: the ASIC gives design flexibility. This gives enormous opportunity for speed optimizations.
- Low power: The ASIC can be optimized for required low power. There are several low power techniques such, as power gating, clock gating, pipelining, etc. are available to achieve the power target.
- Analog: In the ASIC, you can implement analog circuit, mixed signal designs. This is generally not possible in the FPGA.
- DFT: In the ASIC DFT (Design for Test) is inserted. In the FPGA DFT is not carried out (rather for the FPGA no need of the DFT).

2.5. Review of ASIC design disadvantages

- Time-to-market: Some large ASICs can be taken a year, or more to design. A good way to be shortened the development time is to make prototypes, using the FPGAs and, then switch to the ASIC.
- Expensive Tools: The ASIC design tools are very much expensive. It is taken a huge amount of the NRE.

2.6. *Brief introduction to FPGA*

This chapter describes a short introduction to the FPGA world and shows the principles of the FPGA-based time measurements.

2.6.1. General description of FPGA

The Field-Programmable Gate Array devices, known, as the FPGA [66], are the programmable devices, capable of implementing any digital logic circuit. The offer a designer the flexibility of creating a wide array of logic circuits at a low cost, because it is not necessary to be manufactured a new custom, having made the integrated circuit each time. The FPGA's have been found to be a practical platform solution for, as the medium, well as the low volume applications. The FPGA unit is an IC, which is provided a large number of programmable logic gates, with, also RAM and DSP blocks are included as shown in Fig. 2.2.

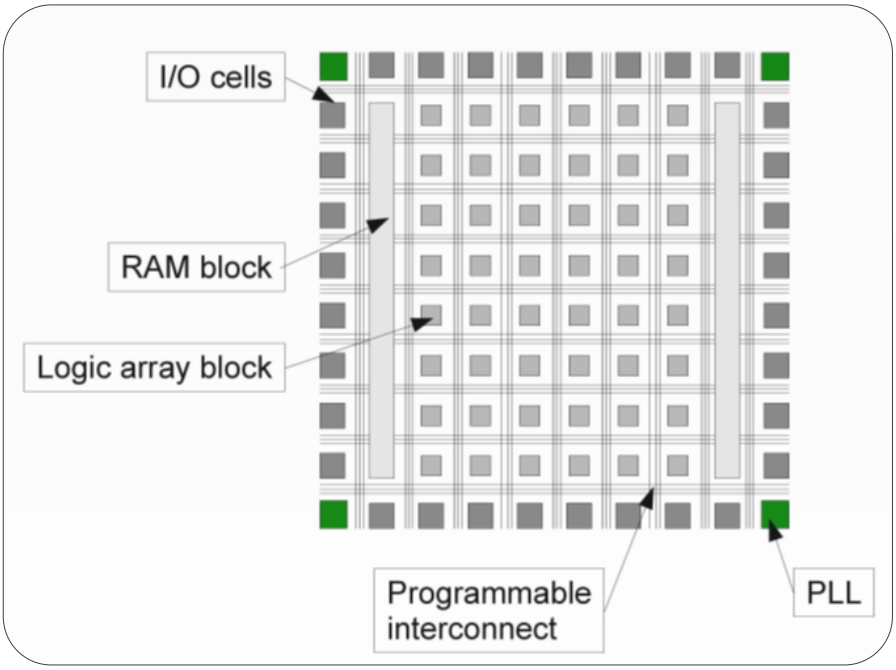

Fig. 2.2 FPGA chip general description

The functions of the logic gates can be programmed, and makes it possible to implement more complex digital functions. Each design is based on the specific interconnection of LE (logic elements), which consists, in general, of input and output ports, lookup tables (LUT) and flip-flop as described by Fig. 2.3. The logical behavior is dependent on the LUT configuration. The architectural structure of LE is varies from vendor to vendor, for example, the ALTERA or the XILINX are today's leaders, and even form the FPGA family to the FPGA family of same vendor. In case of Cyclone IV, by ALTERA, each 16 LE are arranged

in a logic array block. The logic blocks inside the logic array block are interconnected by local, global and carry chain properties. The LABs are arranged in grid. The signal routing between LEs and LABs is controlled by the FPGA configuration, which is referred to, as a firmware.

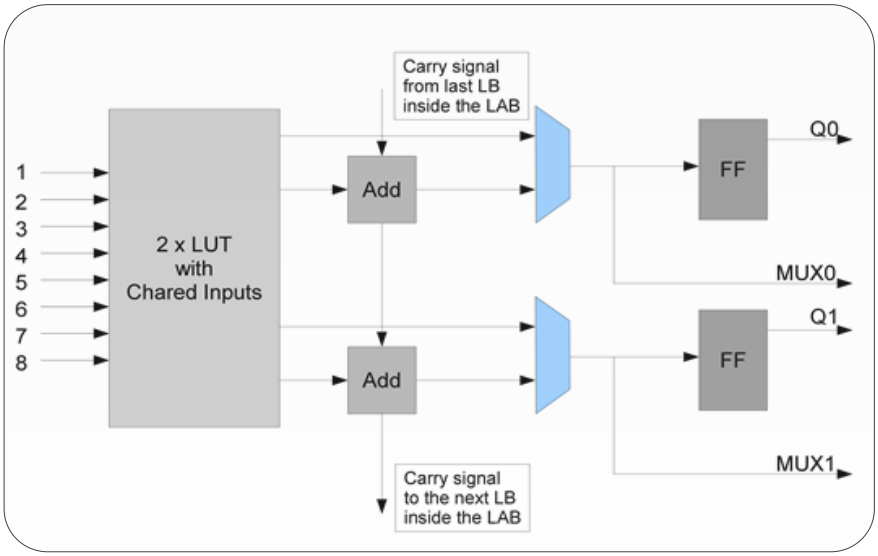

Fig. 2.3 Internal description of Logic Element (LE)

The FPGA functions are determined by the firmware supplies the flexible configuration. The number of logic elements varies from 500 to 800,000, which make it possible to be chosen the appropriate size for the application.

2.6.2. FPGA design flow

The creation of programmable, "ready to burn", file for the FPGA includes 4 major flow steps [66].

- RTL description is the first step. The most common way is to describe the design logic with hardware description language – HDL. There are two main languages for this purpose: VHDL and Verilog. In addition, design software supports predefined logic IP modules. The design is programmed by linking the signals of the modules in the block diagrams. The design software converts HDL descripted file to logic modules and cares to connect them, depending on constraints supplied by the developer. The description in this step can be completely functional, so no information of how the design implemented on chip has to be included.
- The second step includes functionality test of the design. No timing information is included, that is why this simulation is called the functional simulation.

- The third step is the synthesis of the design, which outputs the netlist, that describes the whole design on the logic primitive's level (e.g. gates, flip-flops and etc.), in accordance to the FPGA unit, that has already been chosen.
- The last step is making "Place and Route" process. Here, the design is placed on the FPGA, and the used logic elements are connected by the place and route fitter. This step needs constraints from the designer, who has to define the input or the output ports, timing constraints or placements assignments. This possibility allows making physical optimizations. At the end, the FPGA programming file is generated.

The traditional CAD flow is a straightforward approach to the implementation of the logic circuits. As it was described before, the CAD flow proceeds linearity, and decisions, having made in one stage, are not modified in the following stages. For example, the synthesis optimization during logic synthesis does not account for accrual delays in the circuit. The delays are undefined, until the circuit is placed and routed. Thus, an optimization, that was originally promising, may be turned out to sub-optimal.

2.6.3. FPGA test platform

To demonstrate the proposed peripherals functionality, as the DL-ADC and the DPWM, suitable for digitally-controlled systems, a test platform, having based on a low-cost board DE0-Nano, and includes the Cyclone IV family FPGA unit EP4CE22F17C6N. The FPGA board with the USB controller is used to connect to a host PC, which runs the ALTERA's software, that can be programmed online the digital peripheral implementation, which has been described in the VHDL RTL language. The ALTERA's design tool, the Quartus®II, are allowed to be designed description, function and gate-level simulation, are checked timing violations, mapping, placement and routing properties. The USB connector is used to download the final synthesized product to the FPGA board. Since the automatic synthesis simulation, timing analysis, and verification tools are available for the FPGA implementation, it is delightful, that all these well-established, and automated tools can be, dramatically, speeded-up the design procedure. Moreover, the design can be, easily, moved to another FPGA board or be modified to meet the new requirements.

2.6.4. Commercial FPGA device

This section presents the commercial FPGA device, the Cyclone IV EP4CE22F17C6N, which has been used during the work.

The Altera Cyclone IV is the FPGA device, that consists of five major components: Logic Array Blocks (LABs) to implement arbitrary logic functions, memory blocks to store data, Digital Signal processing (DSP) blocks to speeded-up the arithmetical operations, as multiplying and accumulating, the Phase Locked Loop modules to be altered the phase and the frequency of the input clock, and I/O pads to access the outside world. All of these components are interconnected by the programmable routing network.

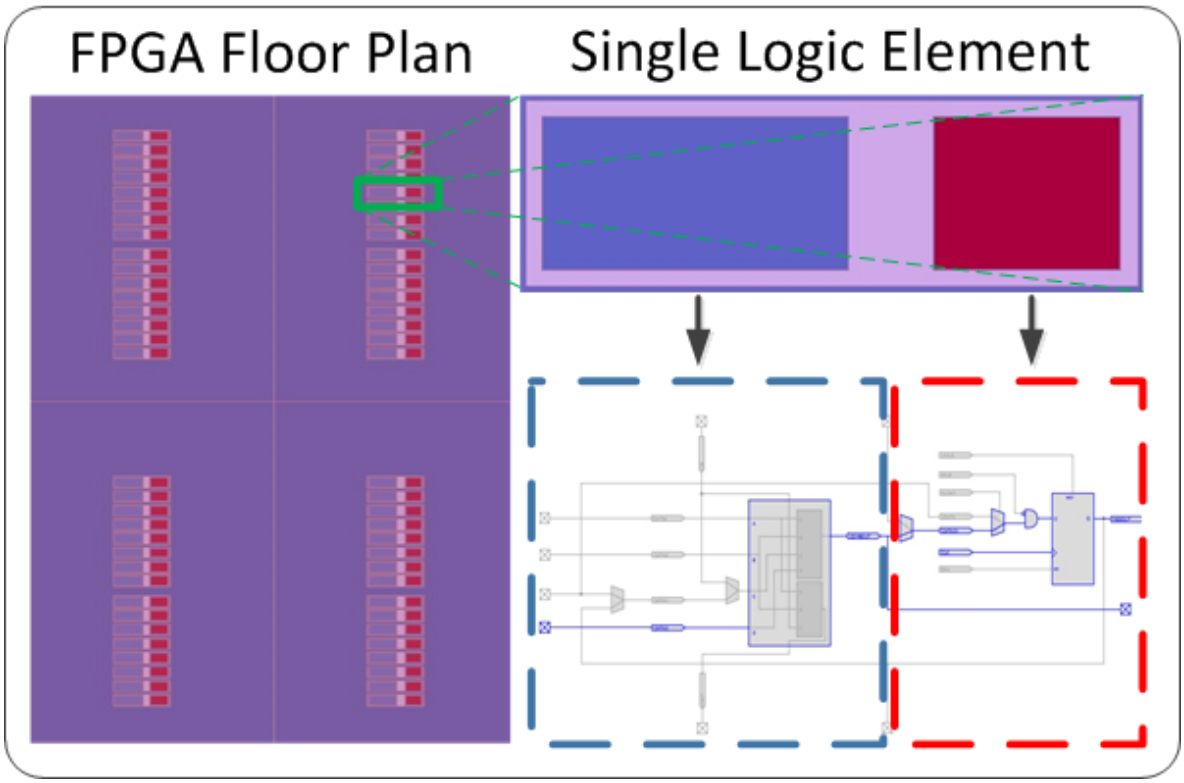

Fig. 2.4 The FPGA floor plan – LABs and LE level

Each LAB is consisted of 16 Logic Elements (LEs), see Fig. 2.4, which are operated in the normal or the arithmetic mode. In normal mode, the LE is configured, as a single four-input lookup table (LUT), and register. The output of an LE is, either the output of the LUT, or the output of the register, whose data input comes from the LUT. This mode is useful for the arbitrary logic functions implementation. To be, efficiently, implemented the arithmetic operations, the LE can be configured into the arithmetic mode. In this mode, the LE is produced two additional ports: the carry-in and carry-out signals, which are allowed to be connected to adjacent LE via the dedicated routing.

2.6.5. Low-level primitives design

The hardware description language (HDL) coding style can have the significant effect on the results quality, than can be achieved for the programmable logic designs. Although

synthesis tools optimize HDL code for both logic utilization, and performance, sometimes the best optimizations are required the engineering knowledge of the design. Therefore, it is important to consider the HDL coding style, that is adopted, when the programmable logic design creating.

Low-level HDL design is the practice of low-level primitives and assignments using in the HDL code to be dictated a particular implementation for a piece of logic [67]. Low-level primitives are small architectural building blocks, that are assisted you in the design creation. The Quartus®II software is allowed the low-level HDL design techniques using, that can help to achieve better resource utilization of the faster timing results.

In terms of the TDC design, the small cones of logic or time delay buffers can be implemented with the LCELLs primitives. The same result can be achieved, either, manually, or by the "keep" command using in the synthesis assignments. Another option for delay buffer implementation can be achieved with the WYSIWYG primitives, which have been described in the Quartus®II HDL libraries. It is parametrized, family-dependent primitives that are corresponded to device features, such logic cells, I/O elements, etc. The Quartus®II compiler creates atom representation from the text file, and synthesizes the design, so that the atoms preserve the WYSIWYG structure of the netlist file. The atoms, having generated by the Quartus®II software, are similar to the WYSIWYG primitives in the netlist files, having generated by the other EDA tools.

The WYSIWYG primitives, and their Quartus®II, - having generated atom representation, allow the other EDA synthesis tools to be achieved better implementation of a design, and allow more control over, how the design should be implemented in the FPGA device. The Altera provides the atoms models simulation for the functional and timing simulation.

2.7. Time measurement approaches for FPGA implementation

There are different approaches for the TDC implementation on the FPGA. Most of them are used the small signal delay from single logic element, like the primitive cell, but it also possible to be used the fast inputs LVDS or PLL. Time resolution of a hundreds of picoseconds can be achieved by tapped delay line method. This implementation method has time bin size varies, because the delay elements, and the signal routing have different propagation time. The propagation time between two LEs and two LABs is different; the delay between two neighboring logic array blocks is much bigger. This produces, so called "ultra wide" TDC bins, which are, typically, bigger, with respect to the LE interconnection. The fast carry signals usage between logic blocks neglects the routing delay. An optimal

uniform propagation delay can be achieved by routing, and cell calibration, but is also depends on the environment temperature.

2.7.1. TDC based on tapped delay-line

One of the first FPGA-based TDC has been developed in last decade, with time resolution of hundreds of picoseconds [70]. This TDC has been used a tapped delay line. The tapped-delay line exploits the signal propagation time, through the logic elements for time measurement performance.

Although, there are different possible implementations, the tapped delay line based on carry signals improves the TDC bin size, because the carry signals have the smallest propagation delay, which improves the TDC bin. The very fast FPGA-based TDCs use the carry signals for local interconnection between LE.

The start signal for the time measurement propagates, through a line of delay elements connected in series. After each delay element, the signal is tapped and fed to the input of a flip-flop, which triggers the flip-flops to save the status of the delay line. Fig. 1.5 shows a schematic of a tapped delay line. The time is decoded by the position of the start signal in the tapped delay line. It is important to be sure, that the decoder finds a real transition, which is realized by also checking the following flip-flops, if these stays at the new signal value of the real transition are found.

The TDC realization with this method doesn't prevent time bin size variability, because the delay elements, and the signal routing have different propagation time. A cell-by-cell calibration is necessary, which also depends on the temperature. Furthermore, it is not always possible to construct all delay elements, with the same size, because of the FPGA architecture. The fast carry signals usage between the logic blocks is not possible in several FPGA families. When all logic blocks, inside a logic array block, are used, the next logic element in the neighboring logic array block has to be taken. The delay between two neighboring logic array blocks, like the LAB, is much bigger, than between for two neighboring logic blocks, like LE. This produces, so called "ultra-wide" TDC bins, which are, typically, bigger by a factor of three to five, with respect to the small bins. One possibility to avoid the "ultra-wide" bins is to be propagated a multi-transition start signal, instead of a signal transition start signal, through the delay line. This method is called the wave union. If one transition is in an "ultra-wide" time bin, then, then the other is in a normal time bin. This arrangement, effectively, subdivides the "ultra-wide" bins, having used the information of both transitions in the time encoding. A time resolution of below tens

picoseconds is reachable, with this method. The drawback of this design is the requirement of a relatively large amount of logic elements for a single TDC channel, in addition to the bin size calibration and temperature dependence.

2.7.2. TDC based on ring oscillator

The ring oscillator is a self-oscillating system. It is being constructed by a buffer connecting, with an inverter, having looped back to the buffer input. The system frequency is determined through the delay between the two logic elements, which are given their result back to the input of other element. In the example, shown in Fig. 2.5, the AND gate is the buffer, and the NOR gate is responsible for the incoming signal inverting.

The ring oscillator method uses the two ring oscillators, with a small frequency difference [68],[69]. The two ring oscillators are started, with two different signals. The TDC starts signal triggers, the flip-flop of the slower ring oscillator, and the TDC stop signal triggers the start of the faster ring oscillator. The two resulting clocks are used for two separate counters, which are started to count at beginning of the oscillations. A phase detector triggers the latching of the two counter values at the moment, when the fast clock, and the slow clock are in phase. The Fig. 2.6 shows the waveform for the ring oscillator TDC.

The slow/fast counter value n1/n2, and the time period of the corresponding oscillators T1/T2 determine the measured time $T_{Start-Stop}$.

$$T_{Start-Stop} = n_1 \cdot T_1 - n_2 \cdot T_2 \tag{2.1}$$

The fast ring oscillator is built, with a flip-flop, an AND gate, and a NOR gate. The slow oscillator uses an additional AND gate, as a delay between the two logic gates. By adding an AND gate to the NOR gate, the frequency of the oscillator decreases. The periods of such a ring oscillator are of the order of some nanoseconds. The clock period difference of the two ring oscillators represents the time resolution of the TDC.

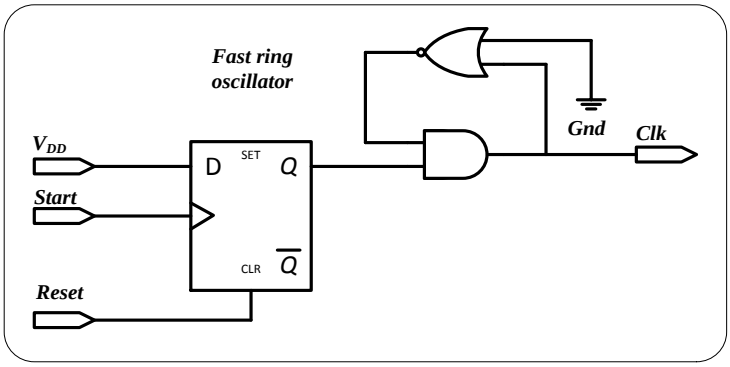

Fig. 2.5 Classic approach for ring oscillator

The ring oscillator TDC represents an event-driven asynchronous TDC, this does not fit to a clock driven synchronous TDC. An additional drawback of this method is that the maximum number of counts for the fast counter, until the synchronization is reached is rather high, which results in a low maximum hit rate for the TDC channel. This rate is, typically, in the low MHz region.

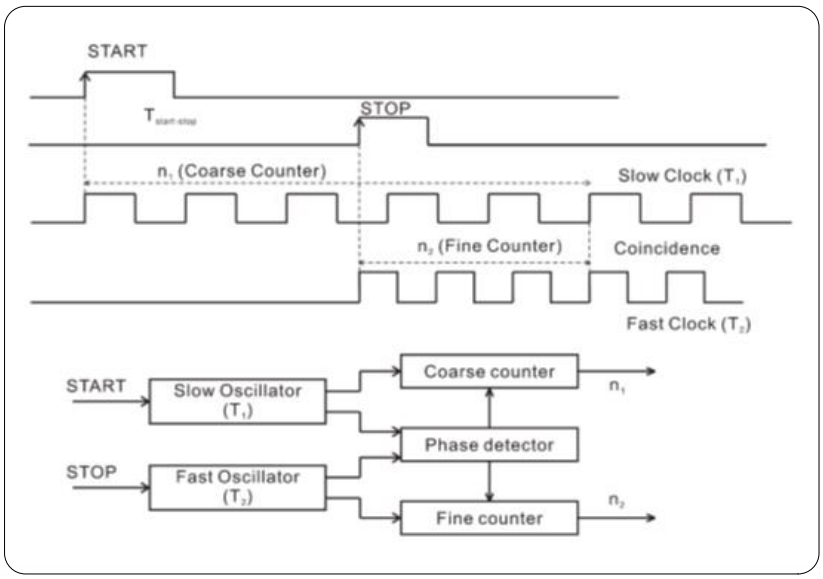

Fig. 2.6 Waveform of ring oscillator method

This makes this method not suitable for the usage in a high occupancy detector. Furthermore, the ring oscillator frequency depends strongly on the temperature.

2.7.3. Fast sampling with Low-Voltage Differential Signaling (LVDS) receivers

The modern FPGAs have been equipped with LVDS (Low-voltage differential signaling) inputs, which are used for the high speed data transfer from chip to chip. These receivers sample the input, with a frequency of about 800MHz, it is possible to sample a signal of a single detector channel, directly, with these fast inputs [71]. The deserialized data of the detector channel are analyzed to determine the measured time by searching for signal level transitions in the data. The position of the transitions, inside the data stream, represents the time of the hit. The time resolution of the TDC depends on the sampling frequency. It is possible to be increased the time resolution by using two or four LVDS receivers sampling one detector channel signal. In this case, these LVDS receivers use clocks, which are the phase shifted to each other. The phase shift between the LVDS receivers represents the time bin size, and it is possible to reach time resolutions below the LVDS receiver clock period.

2.7.4. Fast counter method

This time measurement is realized by latching the value of the counter, having run with the high frequency V, when a start or a stop signal is occurred. The difference of the counter value n_1 for the start signal, and the counter value n_2 for the stop signal represents the measurement time. The time Δt is equal to the counter difference Δn times the counter period T.

$$\Delta t = \Delta n \cdot T, \Delta n = n_2 - n_1, T = \frac{1}{V} \tag{2.2}$$

The maximum frequency for the logic blocks, inside the FPGA, is limited to 250MHz, today, which makes it necessary to combine two or four phase-shifted counters to reach time resolution below 1 ns. The phase-shift between the counter clocks represents the size of the time bin of the TDC. The first counter measures the coarse time, and the other three counters sub-divide the clock period by a factor of four as described by Fig. 2.7.

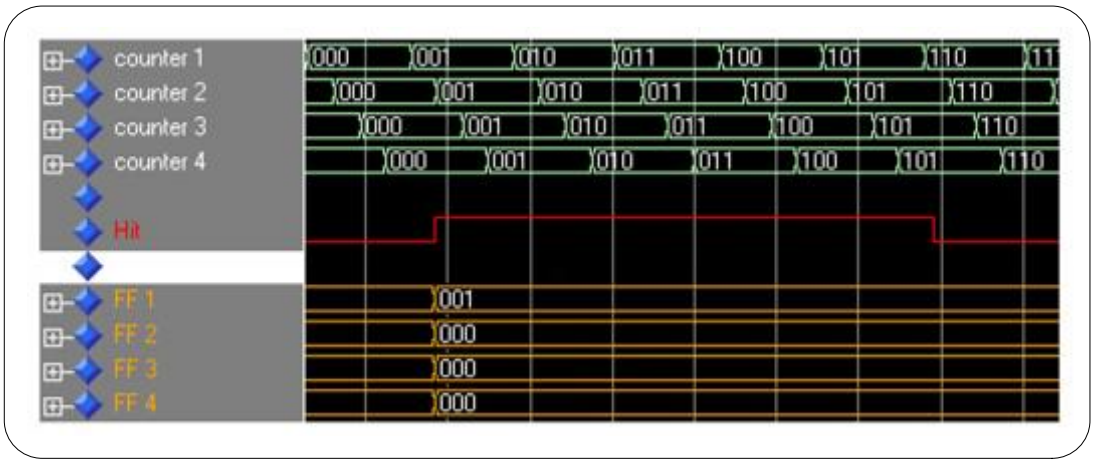

Fig. 2.7 Waveform of fast counter method

The division of the counter period is referred, as fine timing, which can be achieved also by the other techniques.

2.8. FPGA routing techniques

As it has already been discussed earlier, in the FPGA, the computing functionality is provided by its programmable logic blocks, and these blocks are connected to each other through the programmable routing network. This programmable routing network provides the routing connections among logic blocks and I/O blocks to be implemented any user-defined circuit. The routing interconnect of the FPGA consists of wires and programmable switches, that form the required connection. These programmable switches are configured, having used the programmable technology.

Since the FPGA architectures claim to be potential candidate for the implementation of any digital circuit, their routing interconnect must be very flexible, so that they can accommodate a wide variety of circuits, with, widely, varying routing demands. Although the routing requirements vary from circuit to circuit, certain common characteristics of these circuits can be used to, optionally, the routing interconnect design of the FPGA architecture. For example, most of the design is exhibited, locally, hence, requiring abundant short wires. But, at the same time, there are some distant connections, which are led to the need for sparse long wires. So, care needs to be taken into account, while the routing interconnect designing for the FPGA architectures, where we have to address both flexibility and efficiency. The routing resources arrangement, relative to the arrangement of logic block of the architecture, plays a very important role in the overall efficiency of the architecture.

2.9. FPGA placement techniques

Placement algorithms determine, which logic block, with in the FPGA, should be implemented the corresponding logic block (instance), are required by the circuit. The optimization goals consist in placing connected logic blocks close together to minimize the required routing (e.g. wire length-driven placement), and sometimes to place blocks to balance the wiring density across the FPGA (routability-driven placement). To investigate the placement architectures, fairly, we must make sure, that the CAD tools are being attempted to use every FPGA's feature. This means, that the optimization approach, and goals of the placer may be changed from architecture to architecture.

2.10.On-FPGA routing, and placement properties for TDC applications

There are four known methods for routing and, placement of delay elements on the FPGA (see Fig. 2.8). These cases do not include pin planner property.

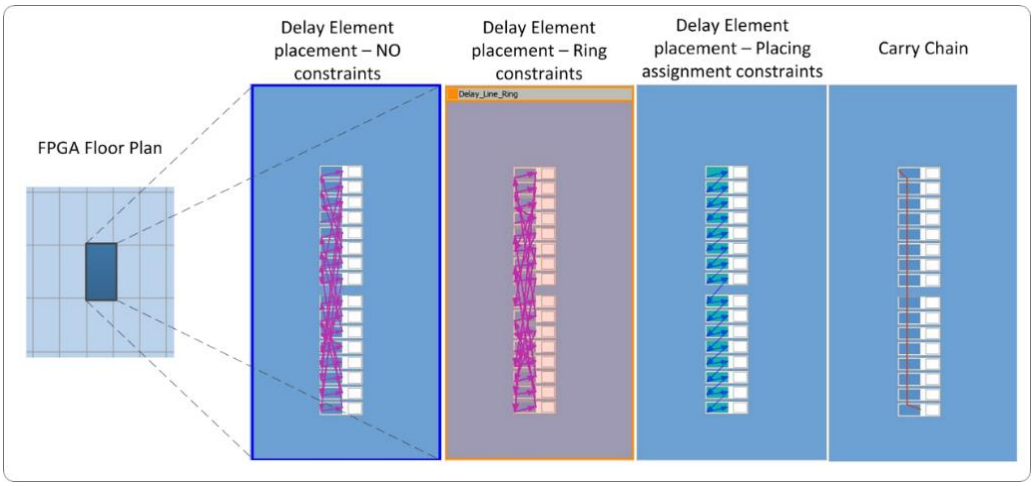

Fig. 2.8 The routing methods of delay elements on the FPGA chip

- Arbitrary - this method is based on unconstraint free placement, synthesis tool allowed, having made the placement, arbitrarily. The location and interconnection of logic blocks, or elements, have been determined by synthesis tool, and may be changed, randomly, after each place and route process.
- Logic lock – this method is based on the LAB optimization properties. The logic lock regions are flexible, reusable floorplan location constraints that help to place logic on the target device. Assign entity instances or nodes to logic lock region directing the fitter to place those entity instances, or nodes inside the region during fitting. The entity instances and nodes, having been assigned to a logic lock region, are referred to, as members. The Chip Planner tool supports merging for the asymmetric logic lock forms producing.
- Location assignment – this method is based on the LE optimization properties. The fitter is constrained to be placed the logic element on the FPGA specific location. It is required the low level design knowledge, and careful use, in order to avoid timing violations. This is very useful for the TDC design, because of the interconnection timing delays decrease.
- Carry chain – this method is based on carry pin routing method, which includes the automatic location assignment. Having originally developed for quick adders and comparators, it allows interconnecting between the logic elements without "slow" general purpose routing structures. The FPGA manufactures is also made sure, that the logic elements for speed along the carry chain path.

2.10.2. Comparison results

The propagation time comparison is being described, as follows. The example has already been implemented on single LAB, or 16 LE units. As expected, the worst result has been achieved in the arbitrary method, where the best performance is achieved in the carry chain method, according to the TABLE I.

TABLE I. PROPAGATION DELAY AS FUNCTION OF ROUTING METHOD

Placement Method	Signal Delay - 16 Delay Elements (ns)
Arbitrary	6.442
Logic Lock	6.439
Location Assignment	6.257
Carry Chain	4.5

2.11.The Logic Element, as a primitive part of the delay-line

According to what has been noted earlier, the LE, is the smallest logic element in the FPGA unit, which has two work modes: normal (see **Error! Reference source not found.** (a)) and arithmetic (see **Error! Reference source not found.** (b)). In the normal mode, there are 4 inputs (A, B, C and D), with the specific properties for static and dynamic delays. In the TDC applications, the main objective is to be reached the minimum propagation delay through the delay component, in order to get the maximum measuring resolution. In other words, 4 types of delay elements are available for implementation, when the maximum propagation delay is achieved for 'A' input, and the minimum propagation delay is for 'D' input. In case of arithmetic mode, the two more pins are added, carry in and carry out, which allows to build the carry chain dedicated for the arithmetical operations, but suitable for the TDC implementations, and provides the minimum propagation time, or the maximum timing results. According to ALTERA's requirements, the carry chain can't be connected, directly, to the I\O blocks, so the first, and the last logic element are implemented, in normal mode.

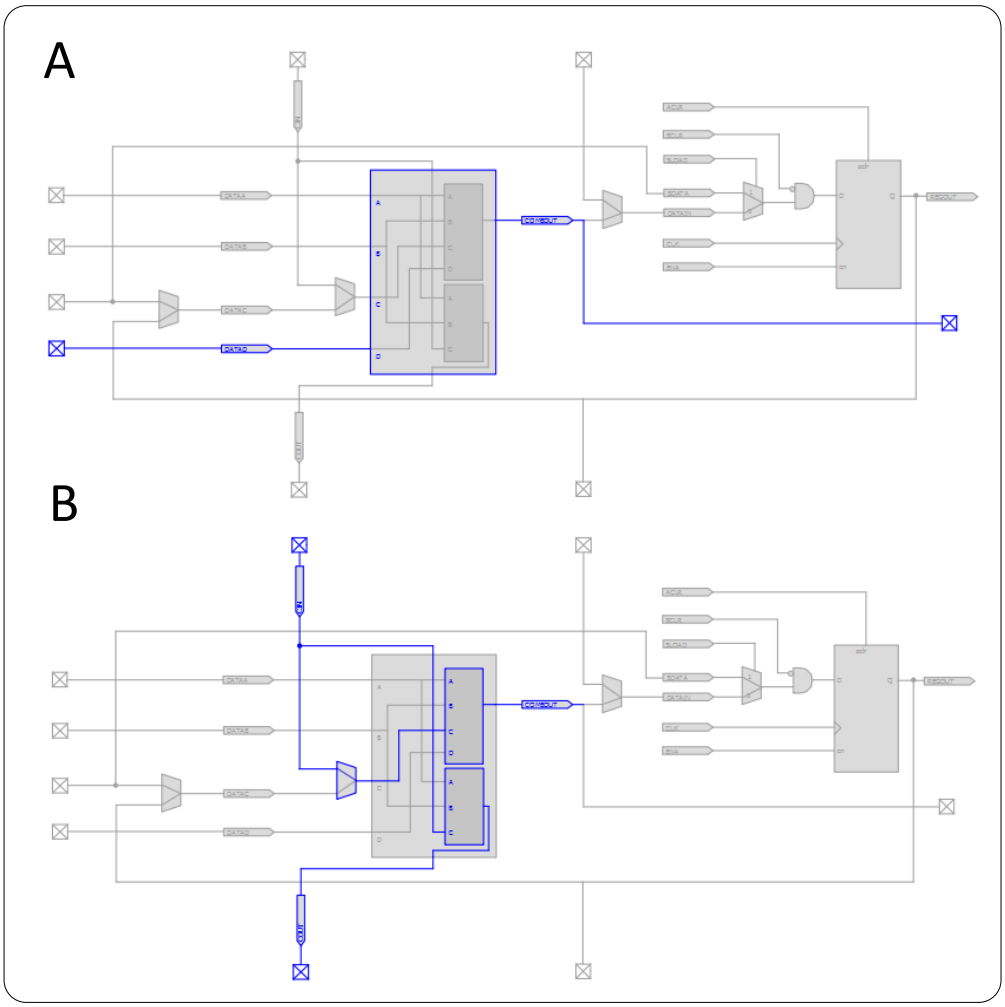

Fig. 2.9 The Logic Element (LE) placement (a) normal mode with 'D' interconnection; (b) arithmetic mode with carry chain interconnection

The propagation time, through single element comprised is described, as follows. An example is implemented on the single LE, depending on its I/O pin. As it has been mentioned before, each LE has 4 inputs, with the variable propagation delay, and the single output, with constant delay. Also carry I/O can be used. The worst result has been achieved, through 'A' type input, where the best performance is achieved, through the carry pins, according to the TABLE II.

TABLE II. PROPAGATION TIME COMPARISON

LUT Input Pin	Propagation Delay = Input + Comb. out (ns)
A input	0.8
B input	0.623
C input	0.503
D input	0.351
C_{in}	0.250

2.12.Test bench module

The term test bench, or testing workbench describes a virtual environment, having used to verify the correctness, or soundness of a design, or model, for example, hardware, or software product. In the context of software, or hardware engineering, the attest bench is referred to an environment, in which the product under development is being tested, with the aid of software or hardware tools. The suite of testing tools is often designed, specifically, for the product under test. The software may need to be modified, slightly, in some cases to work, with the test bench, but the careful coding can be ensured, that the changes can be undone, easily, and without introducing.

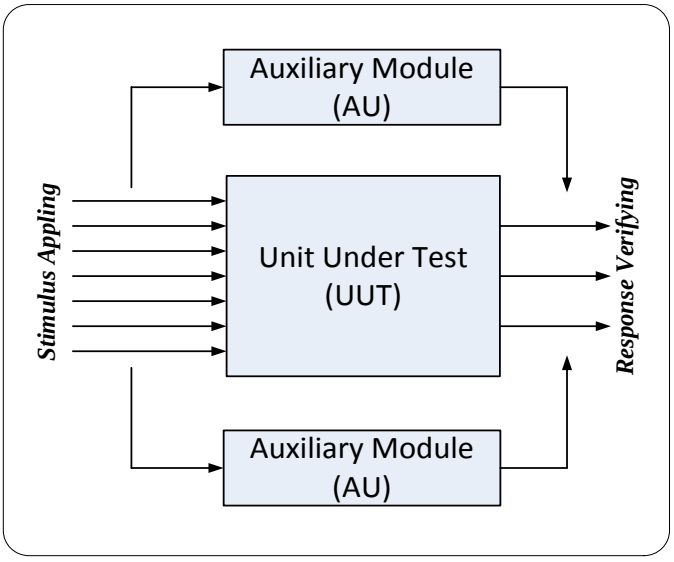

Fig. 2.10 Test bench methodolgy

A test bench in HW (see Fig. 2.10) has three primary purposes:

- Generating stimulus for simulation;
- Applying the stimulus to the entity under the test, and to collect output responses;
- Comparing output responses, with the expected results.

3. All-digital two steps Analog-to-Digital Converter (ADC)

Digital controller realization for modern power management systems has been gained popularity in recent years. A key block in the realization of a digital controller is the analog-to-digital converter (ADC), in which its accuracy, resolution, and speed affect the performance, and stability of the power management system. The use of a conventional high-speed, the high-resolution ADC has been come at the cost of circuit complexity, and silicone (SI) area, having required the custom precision-analog components. Recently, having introduced, the delay-line ADCs (DL-ADCs) have been become an attractive alternative to the conventional ADCs. These ones are offered a cost-effective solution by facilitating the module design process, through the digital implementation, and they can be implemented on a smaller SI area.

The DL-ADC can be categorized by the two approaches, custom-design and standard-cells based. The former has been suited a wide range of applications, but it has been comprised specially-tailored delay units, which are required the significant experience in the custom design process. The latter, though limited by the vendor's standard-cells' constraints, is required knowledge in the digital design flow, having made it an attractive approach.

To realize the DL-ADC using only standard-cells, one can use the sensed analog input, as the delay cells' supply voltage. The propagation along the delay line is affected by the cells' supply, and it serves, as a measure for the analog voltage-level. Although simpler, than custom cells using, this approach is still required the advanced design, since the multiple supplies are required. This work presents an all-digital standard-cell realization of the DL-ADC, with a single supply domain, and can, therefore, be designed, having used a generic digital flow procedure. The architecture is based on a two-step conversion flow as shown in Fig. 3.1. Initial analog-to-time conversion is achieved, by means of a one-shot timer module. It is followed by time-to-digital conversion, accomplished, having used an advanced ring oscillator module realization, which enables high resolution conversion, using a short string of delay cells, regardless of the resolution requirement.

3.1.Principles of the conversion process

In order to avoid of customized delay cells using, the conversion process must be separated in two independent steps, the first cares about the analog signal to pulse conversion, and the second step cares about the produced pulse quantization.

The DL-ADC module comprises two sequential sub-modules for the full analog-to-digital (A/D) conversion. The first sub-module is an analog-to-time (A/T) converter (ATC), which

receives an analog input signal, and outputs a logic-level signal, which varies its pulse length, as a function of the analog input amplitude. The second sub-module is a time-to-digital converter (TDC), which receives the ATC's signal, and quantizes its length to produce the binary representation.

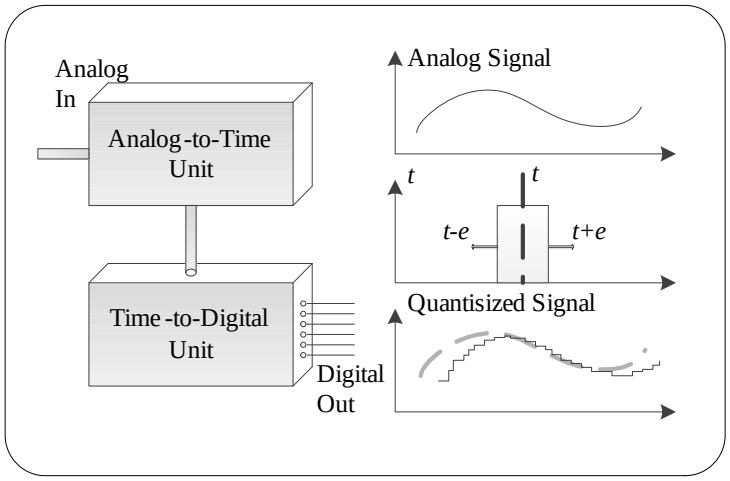

Fig. 3.1 Analog-to-Time Conversion (ATC) and Time-to-Digital Conversion (TDC) flow

3.2.Architecture of Analog-to-Time Converter (ATC)

The ATC illustrated is realized by a two-input variation of a standard one-shot timer (see Fig. 3.2). One input connects to the NOR gate, and it is used to trigger a timed pulse, V_X. The second input receives the analog signal to be used, as the bias-voltage for the R-C timing cell. The pulse length at the output, which depends on the bias, produces a time representation of the analog signal. This R-C based timing mechanism can be expressed, as:

$$T_{pulse} = RC \ln\left(\frac{V_{DD}}{V_{sample} - V_{thershold}}\right) \tag{3.1}$$

where V_{DD} is the supply voltage of the digital cells, $V_{threshold}$ is the logic gate threshold voltage, and $V_{sample} = K_V V_{out}$ is the value of the sampled voltage. As can be observed from formula, the conversion characteristics of the ATC are not linear. However, in the majority of power management applications, such as voltage regulators, the non-linear behavior of the one shot-timer has minor effect on the performance of the system, since the operation centers are around the operating point. For a general purpose of the ADC, which requires the linear behavior, division of the operating domain to linear segments, or post conversion, through look-up table comparison, can be applied to linearize the exponential behavior of the one-shot timing cell.

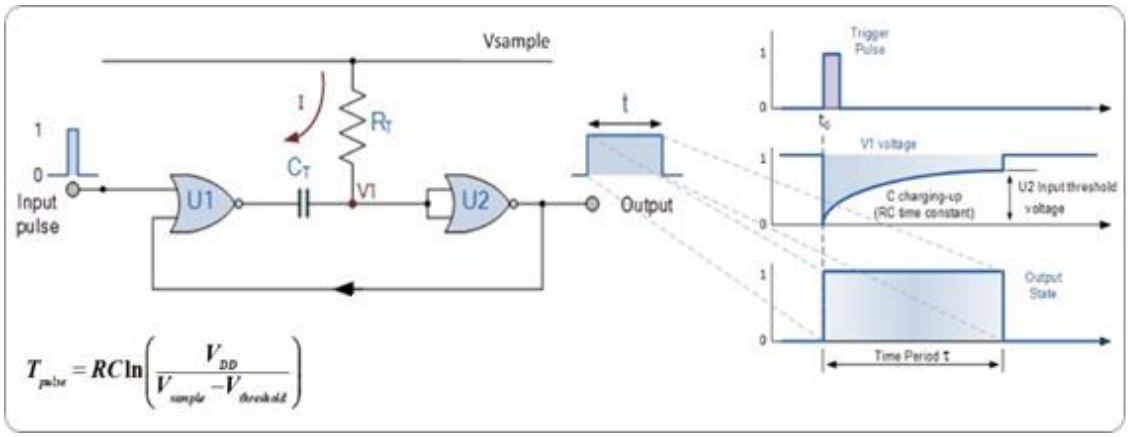

Fig. 3.2 One shot circuit behavior

3.3.Architecture of Time-to-Digital Converter (TDC)

The TDC performs the second step of the analog-to-digital conversion. The basic TDC module has been, schematically, described by Fig. 3.3, consists of a delay line (DL), latch register, translation block, and an output register. The DL is formed by a serially-connected buffer string. When being initiated, the signal pulse V_x from the ATC module is entered, and propagated, through the string, at a rate, which depends on each buffer's propagation delay. Once the pulse ends, i.e. the input returns to low, the DL, momentarily, holds the time information in raw thermometer code, having assumed the complete input pulse duration is shorter, than the string's cumulative propagation delay.

The number of the connected delay-cells in the string, and the buffers propagation time determines the maximum width of the incoming signal V_x, and it can be expressed as:

$$T_{pulse\_max} = t_{pd\_buffer} \times N \tag{3.2}$$

where t_{pd_buffer} is the propagation time of a single buffer, and N is the number of the delay cells in the string.

In order to capture the raw thermometer code information, each cell of the DL branches out to a respective cell in a register of the same length, as the DL. The register consists of the D-FFs, which latch, synchronously, to the falling edge of the input pulse. In this manner, the exacted thermometer value is captured, which, linearly, depends on the input pulse duration.

The thermometer value is further translated to a readable binary value, having used a conversion block. The conversion can be realized in several methods, such as a lookup table, arithmetic calculation, or a Wallace tree translation (see Fig. 3.4). The latter is adopted in this work, due to its high conversion time rate for high resolutions of the ADC converters, and simple realization on IC shows the conversion procedure of the Wallace tree, based on

a count process. The number of ones in the captured thermometer code is quantified, having used, hierarchically, the arranged full adder units, which is given the final result in the binary form.

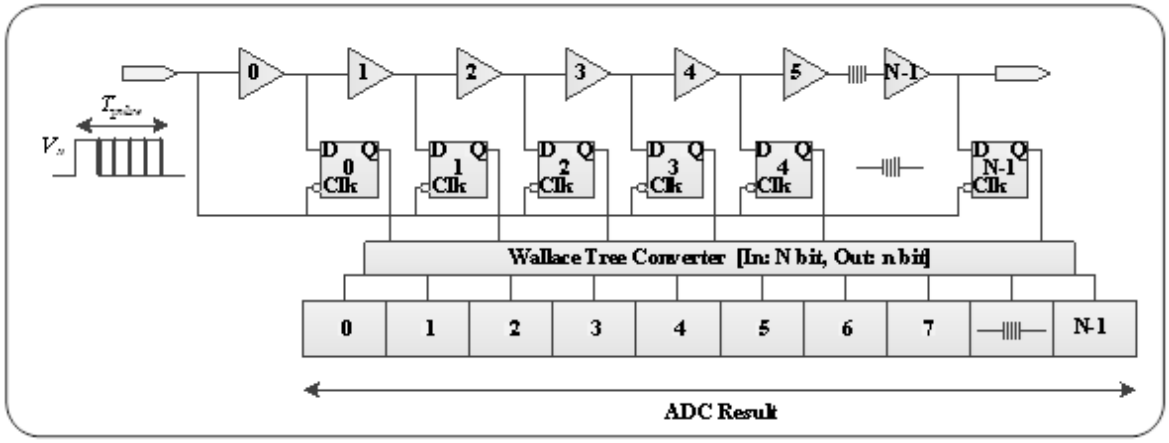

Fig. 3.3 High architecture of the delay line ADC based N-buffers string

The desired output resolution determines the cell-count of each block of the TDC. An n-bit binary output registers back-translates to an expanded 2^n bit thermometer code, hence, the delay cell consists of 2^n buffer, and the D-FF cells. The relationship between the resolution, and the number of the delay cells in the string is given as follows:

$$N = 2^n \tag{3.3}$$

3.3.2. Wallace tree encoder

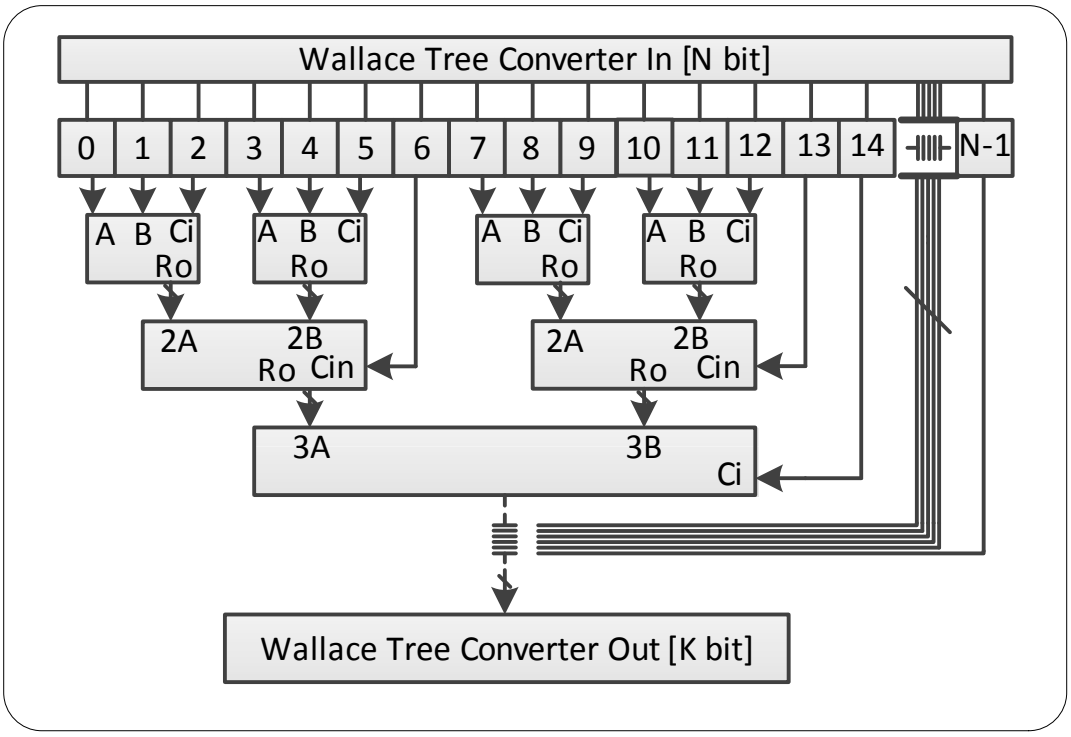

Fig. 3.4 The wallace tree encoder architecture

As it had been noted before, the output of D-FF was described in thermometer code, which includes N elements, and must be converted to the binary representation. The encoder scheme is chosen, as the Wallace tree structure (see Fig. 3.4), which is fast, and can be solved the bubble error in the thermometer code. The thermometer code consists of a string of zeroes, having followed by a string of ones (or vice versa). A bubble error is the situation, where a '1' may be found among the '0', or vice versa, in the thermometer code. This is usually resulted from the timing difference between clock, and signal lines, and from the D-FF metastability errors. As usual, the Wallace tree is consisted of full adder layers, which number is quite dependent of the input word length.

3.4.Architecture of time-to-digital converter having based on ring oscillator approach

It can be deduced from, that the high resolution DL-ADC realization, in this approach, is being increased the number of the delay elements, and the register D-FFs units in the exponential form, having doubled the required silicon area per additional bit, which in higher accuracy ADC may become impractical for its implementation. To overcome this area-demanding constraint, the TDC realization has already been revisited.

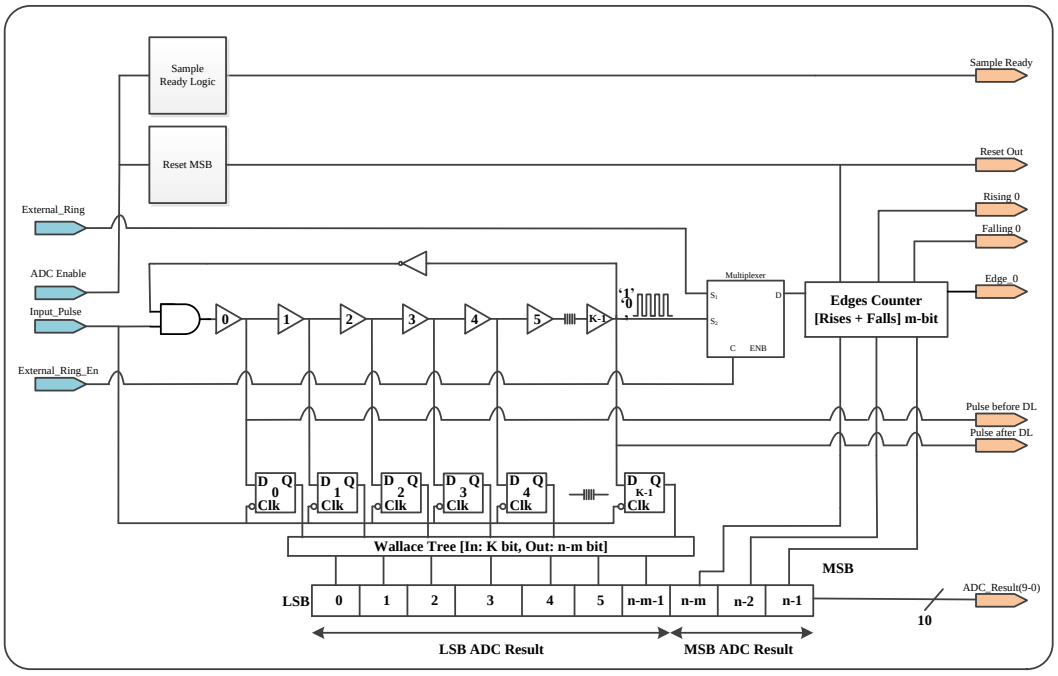

Fig. 3.5 Time-to-digital converter having based on ring oscillator approach

The modified TDC architecture is shown in Fig. 3.5. In this approach, the full delay line counter is replaced by the ring oscillator that feeds a synchronous counter. By doing so, the desired high resolution of the DL-ADC is independent on the string length. The incoming

signal, V_x, from the one-shot timer triggers, the ring oscillator, and the conversion process is started, as shown in the Fig. 3.6.

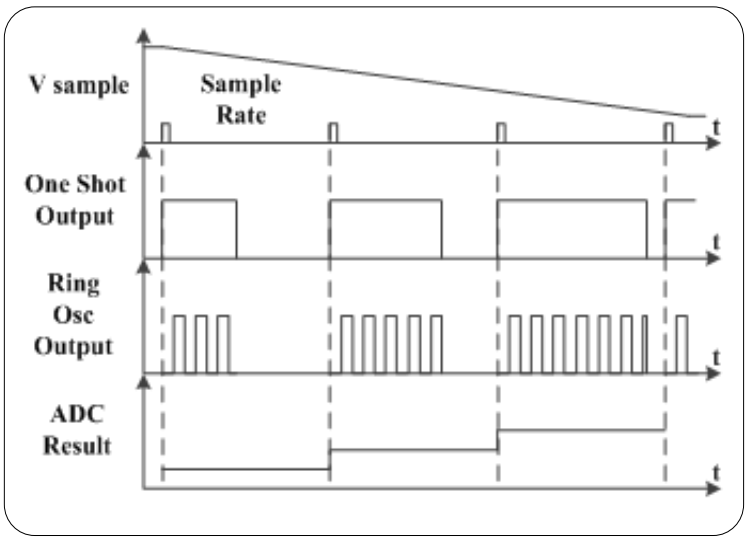

Fig. 3.6 Delay-line ring oscillator ADC expected results

The LSBs of the output register are a direct Wallace tree translation of the short delay line. A counter, having triggered both at rising and falling edges, is connected to the end of the ring-oscillator to count the repetition of full ring propagations, typically a constant time of TDL. The result is conjugated, as the MSBs to the output register. For a counter, with m bits, the maximum number of complete propagations, that can be counted, is 2^{m-1}. Once V_x returns to low, the counter holds the amount of the times TDL fits within T_{pulse}, while the DL holds the residual time difference, with higher time resolution, due to the partial propagation of the last run.

Since the LSBs are obtained out of the ring-oscillator value, in which each buffer output is inverted every full ring cycle, the resulting binary code branches after the Wallace-tree through NOT gates to invert the Wallace tree output, when needed. The inverting action is controlled by the first buffer input value according to the Fig. 3.7.

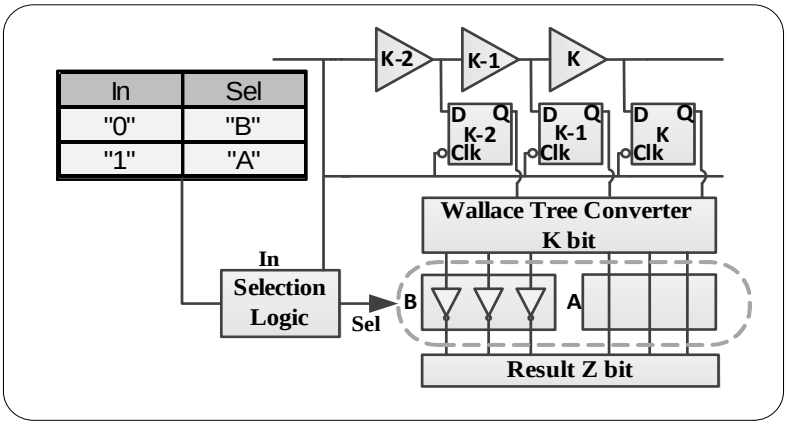

Fig. 3.7 Output result normalization scheme

The relationship between the resolution, and the number of the delay cells in the string of the ring oscillator can be expressed, as:

$$K = 2^{n-m}, n - m \geq 7 \tag{3.4}$$

where K is the number of the delay cells in the string, n is the desired resolution, and m is the bits number of the edges counter.

Due to the timing constraints on the counting process of the edges counter, a minimal number of delay cells, K, in the string is needed. In this study, the string length has been set to 2^7, as shown. It should be noted that, in case of $K < 2^7$, the timing constraints are imposed a more complex design, and increased silicone area.

The expressions indicate, that for the same resolution of the DL-ADC, the string length of the ring oscillator is much smaller, than in the basic approach. As a result, the Wallace tree converter has a smaller number of input ports for evaluation of the thermometer-to-binary conversion, and can be realized, with significantly fewer logical elements, consequently, having reduced the effective silicon area of the design.

3.4.1. Ring oscillator ADC architecture inplementation on FPGA

The architecture, having introduced in the previous sections, has been implemented on the Altera Cyclone IV FPGA for the proof-of-concept. Demonstration of the architecture (see Fig. 3.8) on the FPGA proves, that the design can be implemented, with the standard digital components without any custom cells, or analog circuits. The high-entity design comprises 10 bit resolution depth. The pulse generator, or one shot circuit, having constructed from a pair of the synthesized NOR gates, having connected to an off-chip resistor, and the capacitor (e.g. one shot RC network). In addition to internal digital control blocks for triggering and debug, the ADC output is directed to a binary-to-seven segment converter for display upon the output LCD display.

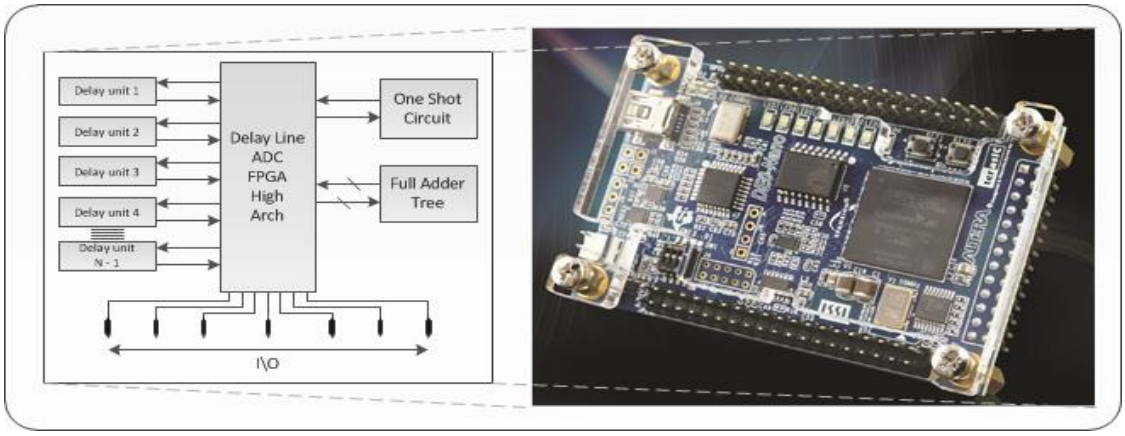

Fig. 3.8 High architecture of the ring oscillator ADC

This design includes some modules, which are critical for their implementation, in terms of placement and routing, like Wallace tree and tapped delay line. The implementation method has been divided on two phases, like the optimal HDL description, and on-chip fine placement. The HDL description must be performed at low-level (see Fig. 3.9,Fig. 3.10), which avoids from the synthesizer to be made changes, as removing the delay cells during compilation, and placement on chip has been described before. The fitter tool is responsible for the placement process, having depended on time or chip area properties. The application techniques are being varied between the designs. Each technique applying does not always improve the final results. The setting and options in the Quartus®II software have their default values that provide the best trade-off between compilation time, resource utilization, and timing performance.

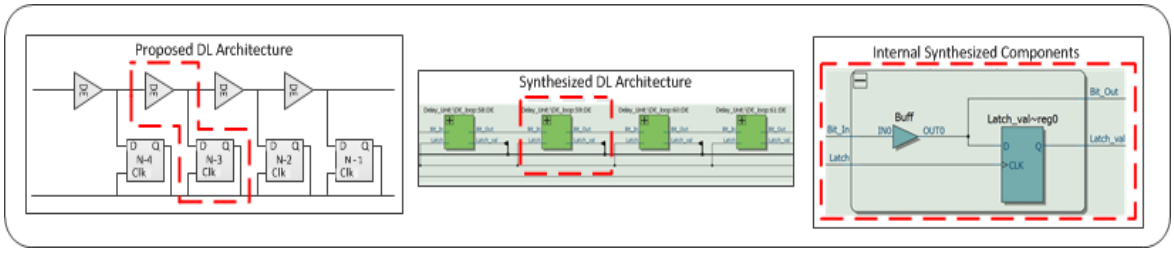

Fig. 3.9 Delay-line: expected versus synthesis result

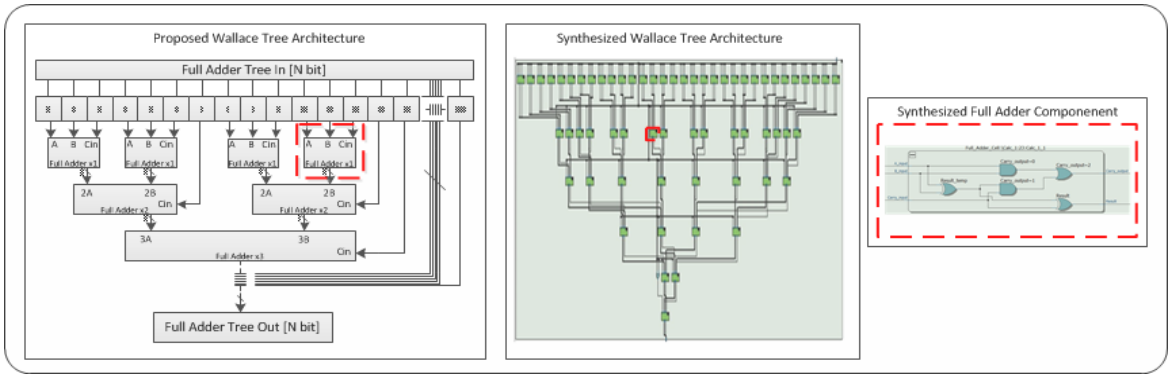

Fig. 3.10 Wallace tree: expected versus synthesis result

3.4.1.2. Simulation results – gate level

In order to verify synthesized design performance, an additional VHDL file should be produced, which is responsible for the module behavior simulating in certain working environmental. The Mentor Graphic tools, ModelSim, and QuestaSim are supported the three primary stimulus languages, like the VHDL, Verilog, and the System Verilog. In this case, the VHDL has already been chosen.

As it has been mentioned earlier, the ADC ring is based on two primary components, as the ATC (Analog-to-Time Converter), well as the TDC (Time-to-Digital Converter), which should be verified, with the test bench environment.

The time-to-Digital module is responsible for the variable length pulse conversion to the binary terms, according to one delay cell resolution. The test bench role is to provide the input pulse, and verify the conversion final results. Each step is increased the input pulse length in 300 picoseconds, the average value of one cell propagation delay. In other words, the incoming pulse length is met the next criteria:

$$0\ ps \leq Pulse\ length \leq 1023 \times 300\ ps \tag{3.5}$$

In accordance with linear vary of the pulse, the outcome result has the saw tooth behavior, as a result of incrementing in one each previous pulse length value. The glitch can be observed on the ADC result, but its influence is negligible, because of the result taking is being followed. The exception of the minimum, and the maximum ranges, have been described, as the minimum value and the maximum values, or 0, and 1023, respectively (see Fig. 3.11).

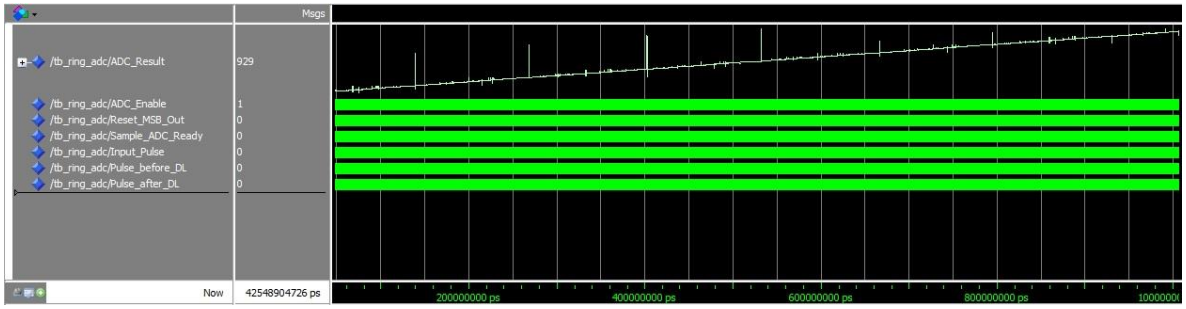

Fig. 3.11 Full sample range delay line ADC based ring oscillator.

In the detailed simulation results, each pin behavior can be observed (see Fig. 3.12):

- ADC Result – sample result;
- ADC Enable – conversion process is started, and allowed one shot circuit working;
- Sample ADC Ready – is indicated the conversion process completion, and is allowed glitches filtering;
- Input Pulse – variable input pulse, each step is increased the length on 300 ps.;
- Pulse Before Delay – output result of the first buffer;
- Pulse After Delay – output result of the last buffer, phase shift of 90º can be observed between the Pulse, Before Delay, and Pulse After delay, due to the ring oscillator behavior.

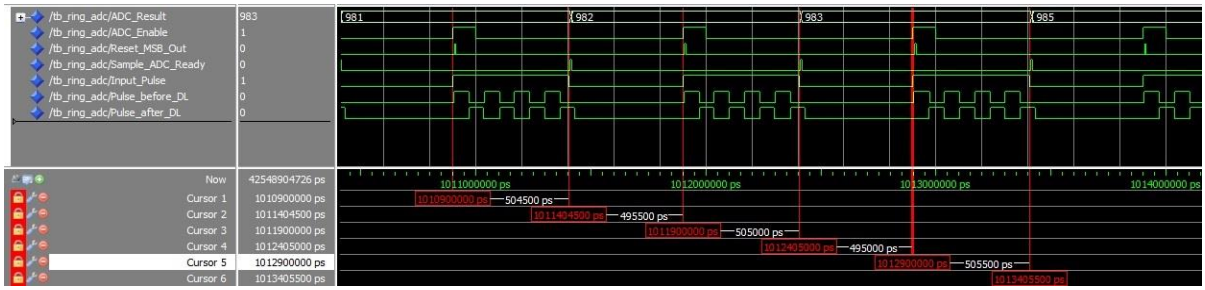

Fig. 3.12 Detailed simulation: delay-line ADC based ring oscillator.

3.4.1.3. Experimental results

The system is operated, with a 3.3V supply, having provided the sample range between 1.7 to 3.3V, conforming to the digital switching threshold around of Vth=1.6V – characteristic of the chosen FPGA where the properties are described in TABLE III.

TABLE III. SETUP SUMMARY PROPERTIES

Altera Cyclone IVE	FPGA Platform
60nm LP CMOS	Process Technology
3.3V	Supply Voltage
10-bit	ADC Bit Depth
1.6–3.3V	Input Voltage Range
400 ns (2.5 MHz)	Conversion Time
450	Number of LE

The maximum, having allowed pulse width, was measured to be, approximately, $T_{pd(max)}$ = 450 ns, which coincides with a T_{pd} = 440 ps delay per delay cell. This pulse width was achieved, with of chip RC values of R = 1kΩ, and C = 500pf. for a time constant of τ = 500 ns for the minimal limit of the sampling voltage range.

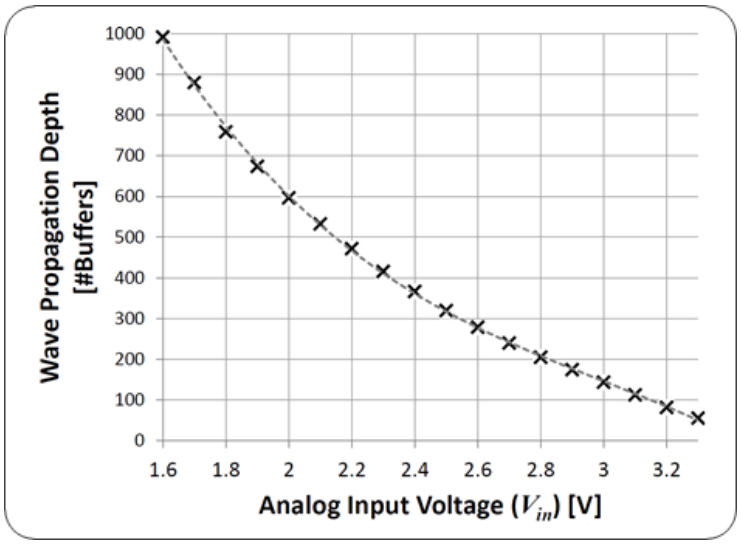

Fig. 3.13 Full sample range: experimental results

The full range functionality of the ADC is further shown in Fig. 3.13, having plotted the sampled propagation depth of the digital wave for the analog input voltages from 1.7V up to 3.3V.

The exponential curve fit is shown the good matching to be provided a linear conversion between the input voltage, and digital output, via a simple look-up table. The primary figures-of-merit of the proposed system have already been summarized in Table.

3.5.Architecture of time-to-digital converter having based on window approach

This part discuses a version of the ADC, having based on general concept of two previous architectures, but in terms of window approaching. Instead of sampling full scale analog signal, this type is responsible for the voltage differences measurement, having compared to the bias point, as it has been shown in the Fig. 3.14.

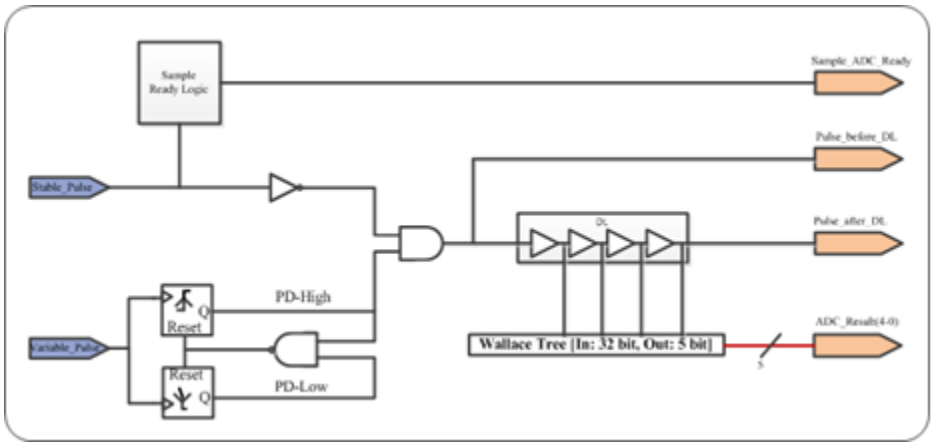

Fig. 3.14 Delay-line ADC based window approach architecture

The time-to-digital converter is received two pulses. The first one is the reference pulse, with constant duration, and the second one is changed, with respect to the sampled voltage around the bias point.

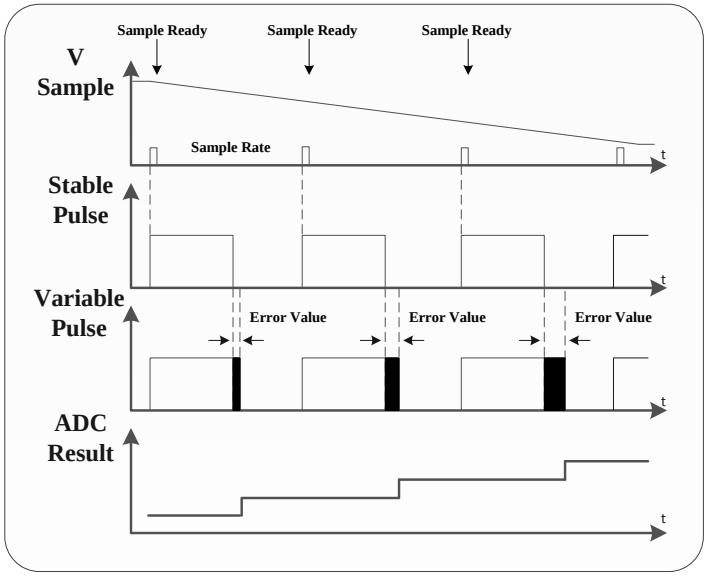

Fig. 3.15 Delay-line ADC based window approach expected results.

The stable reference pulse can be achieved by the internal process, but, in this case, the two pulses are produced by one shot circuit, the first one is being worked, with stable voltage to be supplied and to be produced the bias point, and the second one is varied around it according to experimental results in Fig. 3.15. The logic subtraction result of these pulses

describes the near bias point error value, which is transformed to the binary terms by the delay line in a resolution of one delay cell, as it has been described in the previous ADC versions. The design is supported at the signed and unsigned conversions, respectively, to the number of bits (see Fig. 3.16).

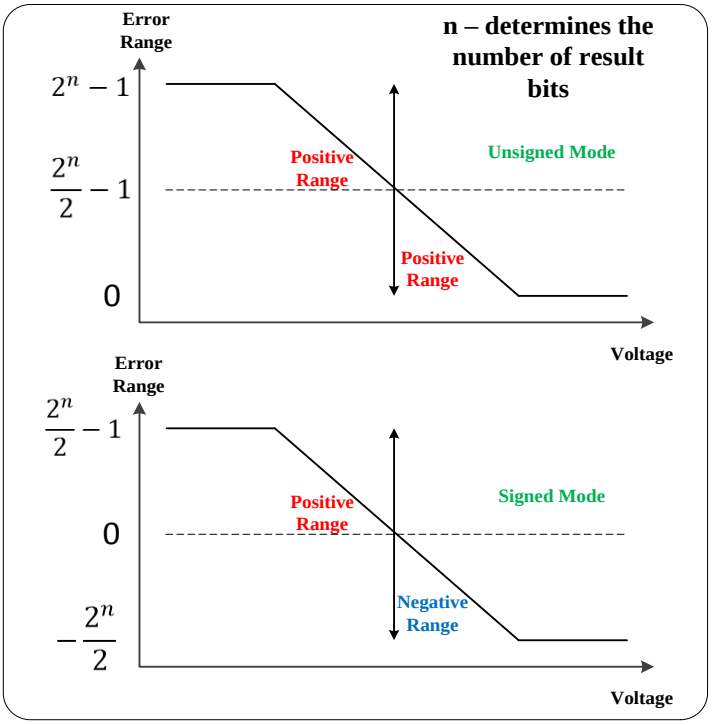

Fig. 3.16 Signed and unsigned result interpritation of window ADC

3.5.1. FPGA window ADC implementation

The Window ADC architecture is quite similar to the Ring ADC, but contrary to the Ring ADC, subtraction of two pulses is performed, instead of ring running. It is based on the four primary components (e.g. delay line, phase detector, sample ready, and two one shot circuits), and the high architecture, which is responsible for the synchronizing between all these submodules.

3.5.2. Window ADC simulation results

The Window ADC is based on the same concept, like the Ring ADC, so test bench check approaching is repeated at itself. The test bench role is to provide the input pulse, according to the stable pulse, and verify the conversion results, which describe the subtraction between them in the digital terms. Each step is increased the input pulse length in 500 ps, the average value of one cell propagation delay. In other words, the variable pulse length is met the next criteria:

$$Stable\ Pulse \leq Pulse\ length \leq Stable\ Pulse + 31 \times 500\ ps \qquad (3.6)$$

An exception of the minimum, and the maximum ranges have been described, as minimum value, and maximum values, or 0 and 31, according to 5 output bits. In simulation results in Fig. 3.17, each pin behavior can be observed.

- ADC Result – sample result;
- Resistor to Not – variable input pulse, each step is increased the length at 500 ps.;
- Stable Pulse – stable input pulse, which is determined the bias point;
- Pulse Before Delay – subtraction result between the Stable pulse, and the Variable pulse, as an output function of the first buffer;
- Pulse After Delay – subtraction result between the Stable pulse, and the Variable pulse, as an output function of the last buffer.

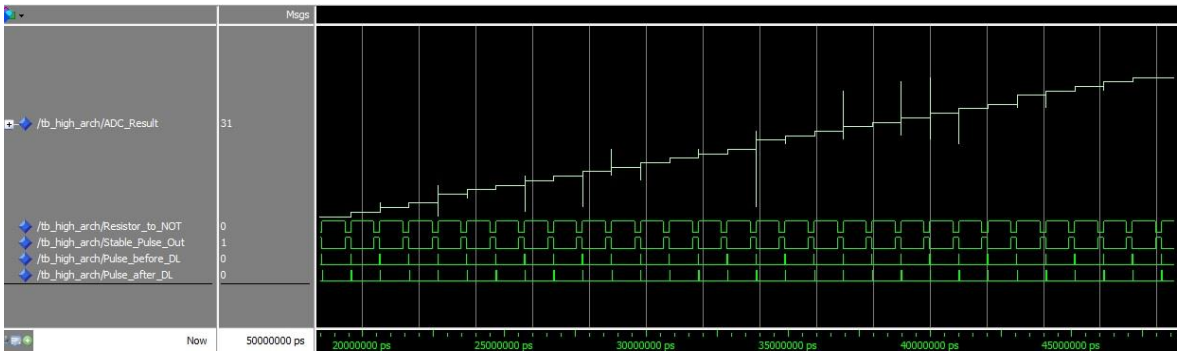

Fig. 3.17 Results of window ADC – gate level simulation

The saw tooth behavior has been achieved, as a result of the linear variability of the incoming pulse. As expected, the output result range is varied between 31, and 0 value. At zoomed simulation in Fig. 3.18, the final result of all the pins is allowed to be observed, when the sample result value is varied, as the function of incoming pulse.

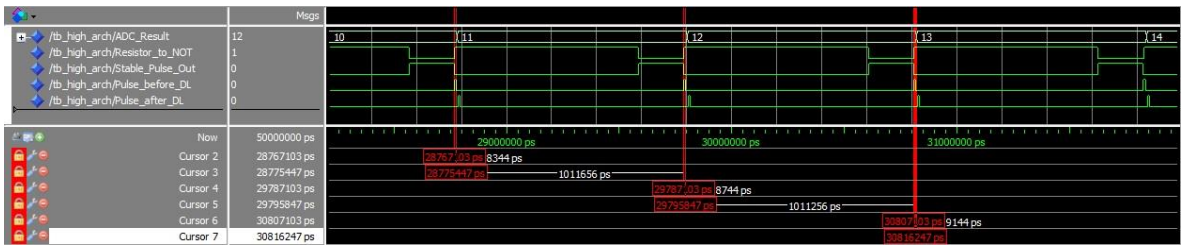

Fig. 3.18 Zoomed results of window ADC – gate level simulation

4. DPWM based on ring oscillator

As it has been described before, the static, and dynamic output voltage regulation capabilities are depended on the characteristics of the ADC resolution, the discrete set of duty ratios, and, ultimately, the discrete set of achievable output voltages is depended on the DPWM resolution. If the resolution of ADC and DPWM is not, sufficiently, high, an undesirable limit-cycle oscillation may be occurred. The requirement for the high-resolution ADC and DPWM is the important consideration in the realization of the digitally controlled low-power high-frequency SMPS. Thanks to the advanced CMOS technologies, the challenge of speed and resolution of the ADC is becoming a less important issue.

The high resolution DPWM is, then, the key module to restrain the undesired limit cycle. Several alternative solutions have already been proposed in recent years for the high-resolution low-power DPWM architectures reviewed, such as, the hardware methods: delay-line, hybrid delay-line, segment delay-line, ring oscillator, segment ring-oscillator, and Delay Locked Loop (DLL), and the soft methods: digital dither, and Δ-Σ modulator. So, all these architectures can be increased the DPWM resolution to some extent, however, they either, entirely, rely on the hardware method, such as, the most advanced, and expensive CMOS technologies for the tight delay-cell/, or ring-oscillator, or, completely, are depended on the soft method, such as, the digital dither, and Δ-Σ modulator.

4.1.Proposed architecture of the DPWM module based ring oscillator

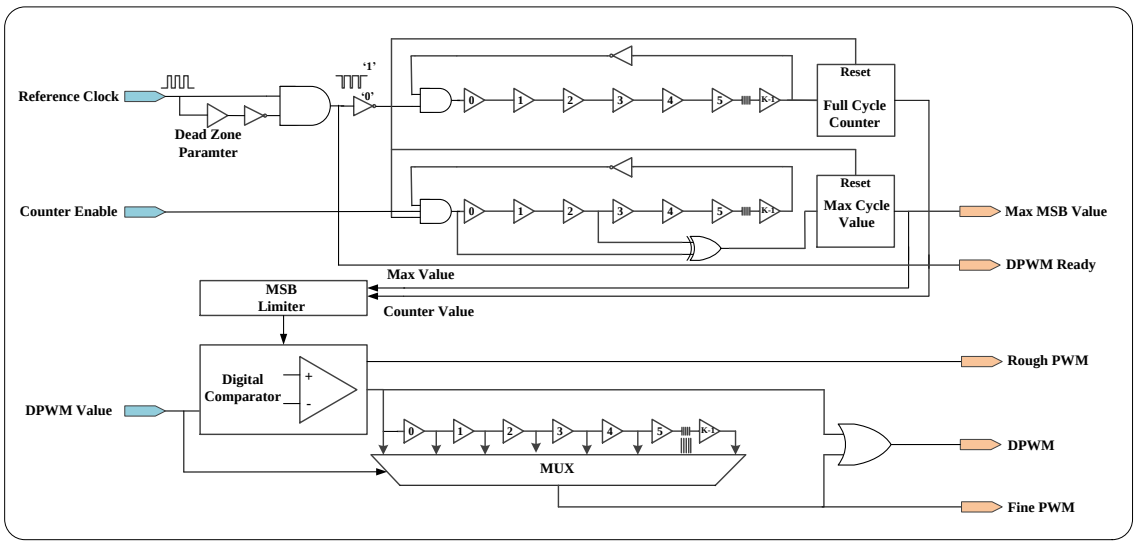

Fig. 4.1 Proposed DPWM architecture based ring oscillator

This DPWM approach provides the solution for the reference pulse quantization in the resolution of one delay cell, and it consists of some primary modules (see Fig. 4.1), which described below.

DPWM based on ring oscillator

4.1.1. Priniciples of DPWM operation

The PWM module, as followed, is allowed the calibration settings for variable frequencies. Similar to the Ring ADC, its operating mode is based on the ring oscillator concept. In order to operate, properly, it is required to provide the reference clock, the DPWM value, and enable discrete, when the reference frequency is determined the DPWM frequency. The primary module target is to divide input frequency, and to reach resolution of single delay element, which the propagation time is determined, in accordance with the production technology, or the FPGA family.

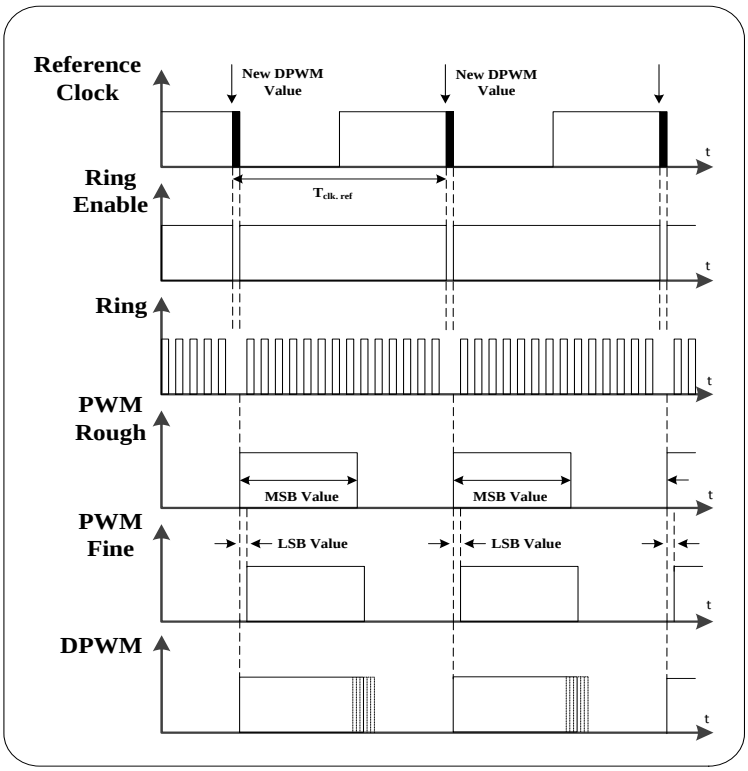

Fig. 4.2 Proposed DPWM architecture based ring oscillator expected results

The reference frequency has been provided to module, which is responsible for the signal producing, with duty cycle close to 100%, when '0' value length has to be, approximately, the same, as the signal propagation time through the delay line. Having obtained the high duty cycle, the signal will be constituted, as the "working window" of the ring oscillator, and '0' value is responsible for the entire ring value reset, in order to be allowed the next cycle of the ring to start at same point, as the previous one. During the work, the counter block will count full delay line transitions of ones, or zeros. Dual edge, or rising, and falling edge sampling are not supported by synthesis tools, so the frequency multiplier is needed, and which is based on the XOR gate. The DPMW input value consists of the MSB and LSB values for the "rough PWM", and "fine PWM" producing, respectively. The MSB value determines, how many ring oscillator cycles '1' of the logical value will be held. In order to

get a resolution of one delay element, the "rough PWM" has been provided to the additional delay line, which is proportional to the previous one. In parallel to delay the line has been connected to the MUX unit, which specifies delay element to be connected to the output pin. The decision has been performed, with the LSB value.

Updating of the new DPWM value is being allowed only at the end of the period. As it has been mentioned before, the module is equipped, with its limiter block, which is responsible for the DPWM input limiting, in case of an exceeding from the maximum allowed value, which has been determined by the reference frequency. If this situation is occurred, '1' logic value outputs, until the new DPWM value has not been provided. So, the supported reference frequency range is between 10 kHz to 1 MHz, approximately. The expected results are described in Fig. 4.2.

4.1.2. DPWM – gate level simulation

In order to verify the proposed DPWM module performance, the built test bench has been optimized for the DPWM work environment. During the simulation, linearly changing duty cycle values have already been entered, in other words, each new DPWM value has been based on the previous one, having increased by one. As a result, the duty cycle value has been changed in the form of the saw tooth. As it has been mentioned before, the DPWM module supports the various range of then reference frequency, which can be changed in the real time. Thus, four different reference frequencies have been provided (see Fig. 4.3), which are 100 kHz (Fig. 4.4), 200 kHz (see Fig. 4.5), 300 kHz (see Fig. 4.6), and 400 kHz (see Fig. 4.7). Each reference frequency has got the similar range of the DPWM value, where the ratio between them is determined the rising slope, according to the formula:

$$\begin{cases} DPWM\ Value < Max\ DPWM\ Value : Max\ DPWM\ Value \downarrow \xrightarrow{yields} DPWM\ Slope \uparrow; \\ DPWM\ Value \geq Max\ DPWM\ Value : DPWM\ Slope = 0 \\ DPWM\ Value = 0 : DPWM\ Slope = 0 \end{cases} \tag{4.1}$$

It can be concluded, that:

$$DPWM\ Values\ range \downarrow when\ Max\ DPWM\ Value \downarrow \tag{4.2}$$

$$where \begin{cases} DPWM\ Values\ Range = (DPWM_1, DPWM_2, DPWM_n) \\ Max\ DPWM\ Value \sim 1/Reference\ Frequency \end{cases} \tag{4.3}$$

In other words, the Max DPWM Value decreasing for the same group of the values is, practically, caused the slope increasing. In simulation results, the primary pin behavior can be observed:

DPWM based on ring oscillator

- Reference Clk – reference clock, which has been determined the DPWM frequency;
- DPWM Value – parameter, which has been determined the duty cycle;
- Enter the New DPWM – module is ready to get the new DPWM value;
- Max DPWM value – the maximum DPWM Value, which is described 100% duty cycle, has been determined, in accordance with the Reference Clk;
- Duty Cycle –the DPWM value calculation, and the Period Length value ratio;
- Period Length – the Reference Clk period time.

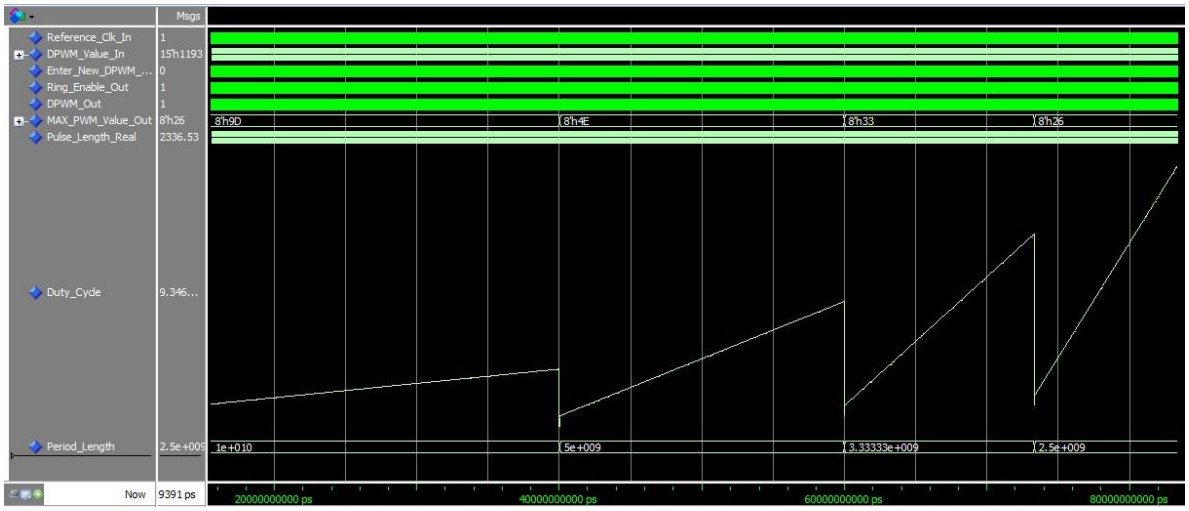

Fig. 4.3 DPWM extended simulation, with range of frequencies, as follows: 100kHz; 200kHz; 300kHz, and 400kHz

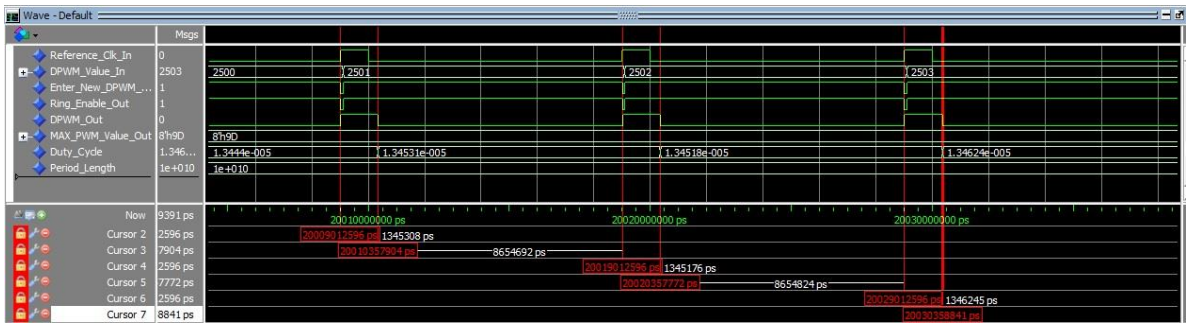

Fig. 4.4 Enlarged simulation result, with reference frequency of 100kHz

Fig. 4.5 Enlarged simulation result, with reference frequency of 200kHz

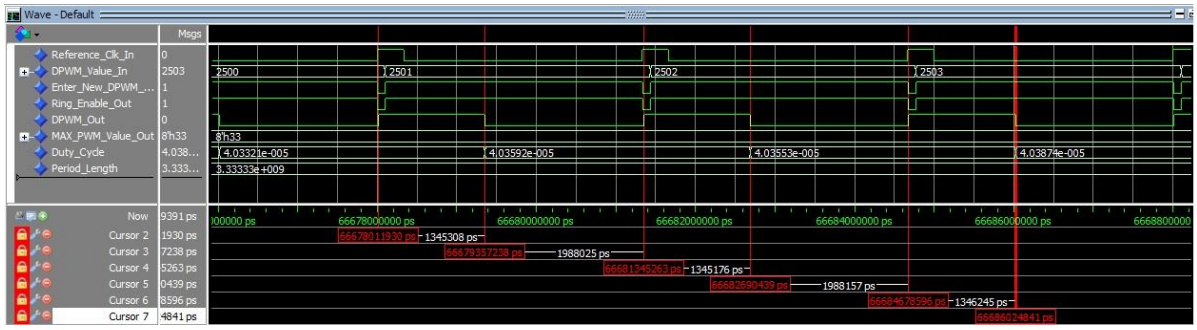

Fig. 4.6 Enlarged simulation result, with reference frequency of 300kHz

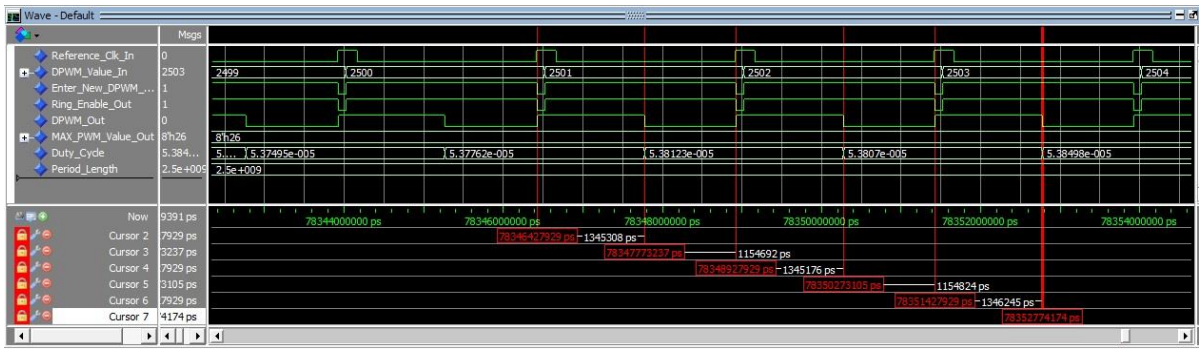

Fig. 4.7 Enlarged simulation result, with reference frequency of 400kHz

During the simulation, the difference between calculated and simulated results has been achieved, the effect is, due to the hardware implementation. Simulation results described in TABLE IV

TABLE IV. CALCULATED RESULTS VERSUS SIMULATED RESULTS

Duty Cycle, calculation result (%)	Duty Cycle, simulation result (%)	Max DPWM Value	Reference Frequency (kHz)	DPWM Value
13.3316	13.4518	18600	100	2502
26.6936	26.9035	9373	200	
39.9477	40.3553	6232	300	
52.5420	53.8070	4672	400	

5. On-chip ADC modules implementation

5.1.Silicon implementation flowchart

The digital implementation of the DL-ADC into IC has been done by the digital logic design developing, which is based only on the vendor's standard digital components, without any custom cells, or the complex analog circuits. The complete block diagram of the digitally implemented DL-ADC, shown in Fig. 5.1, includes four primary modules: the one-shot timer, DL counter, Wallace tree conversion unit, and the high architecture. Thus, they are responsible for the all sub-components interconnection.

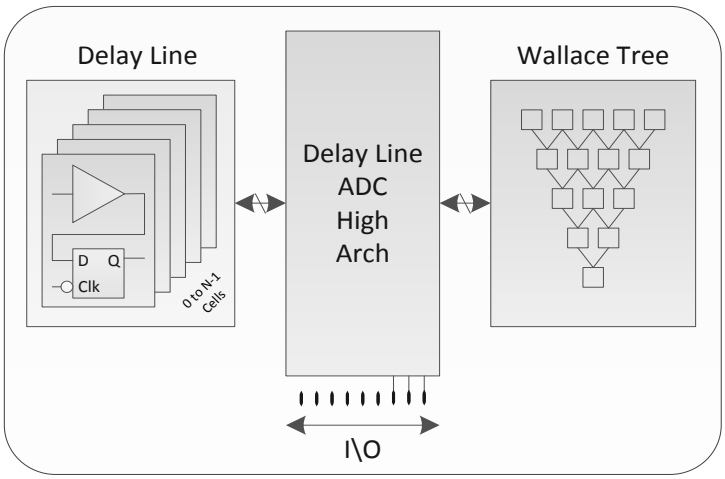

Fig. 5.1 Delay-line ADC high architecture for silicon implementation

The digital implementation is carried out through three main steps. First, the sub-components, and the high architecture are defined in the hardware description language (e.g. VHDL), and they are synthesized by the vendor's standard-cell gates, having used the Synopsys synthesis, and the timing verification tools [2]. The static conversion results are described in Fig. 5.2.

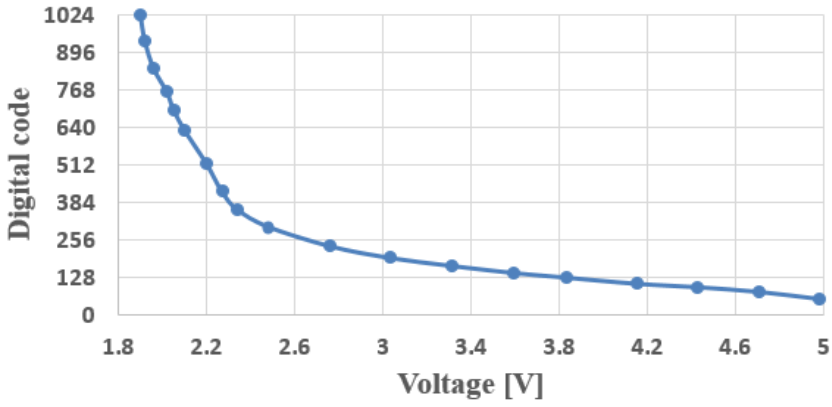

Fig. 5.2 Satatic conversion characteristic of the implemented delay-line ADC

Next, the digital and mixed-signal simulations are carried out, having used the numerical simulation tools such, as Cadence. Finally, the layout is produced by the automated CAD place, and the route (e.g. P&R) tools.

The two 10-bit DL-ADCs have been implemented in the TS18PM platform to verify the study. The produced DL-ADCs' layout are sized at 0.38mm² of the effective silicon area for the basic straightforward version, and 0.05mm² for the ring oscillator, having based on the DL-ADC design approach, as shown in Fig. 5.3 (a,b).

Both ADCs, shown in Figure, have been implemented by the same design procedure, with the key characteristics, having summarized in TABLE V.

TABLE V. COMPARISON OF THE IMPLEMENTED DELAY-LINE ADC

Uncompressed	Compressed	Architecture
ts18pm	ts18pm	Technology
2Mbps	4Mbps	Sampling rate
2v-5v	2v-5v	Input range
10 bit	10 bit	Resolution
5v	5v	Supply voltage
1023	127	Delay elements
10-bit	7-bit	Wallace Tree output register
1066	209	Total logic elements
0.38mm²	0.05 mm²	Silicon area

5.2.Post layout simulation – macro's level

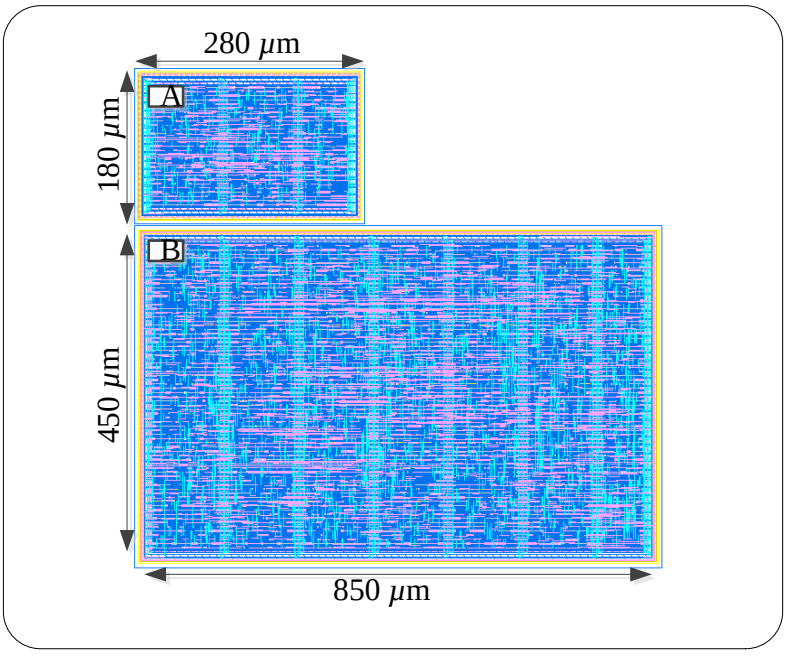

Fig. 5.3 Layout of (a) ring oscillator based delay-line ADC; (b) basic delay cells string based delay-line ADC

To demonstrate the functionality of the implemented ring oscillator based 10-bit DL-ADC, the post-layout simulations had been performed with the simple RC net components, where their values were calculated.

Post-layout simulation results, as shown in Fig. 5.4, have been illustrated the DL-ADC behavior in the transient mode, including the sampled voltage, sample rate, one-shot timer output, ring oscillator output, and the DL-ADC conversion result. The sampled voltage is a generated ramp signal, with a variable range between the threshold voltage, and the supply voltage (e.g. high limit). In addition, to show the conversion step, with sufficient intervals amongst samples, the sample rate has been reduced down to 1.6Msps. It can be observed, that, as the sampled voltage has been increased, the pulse width of the output signal from the one-shot timer is narrowed, and, as a result, there are less complete propagations through the ring. The DL-ADC result, normally, having represented, as a binary word, is displayed in Figure, as the unsigned decimal value for its readability. The insets had been illustrated the expected results, that were discussed before.

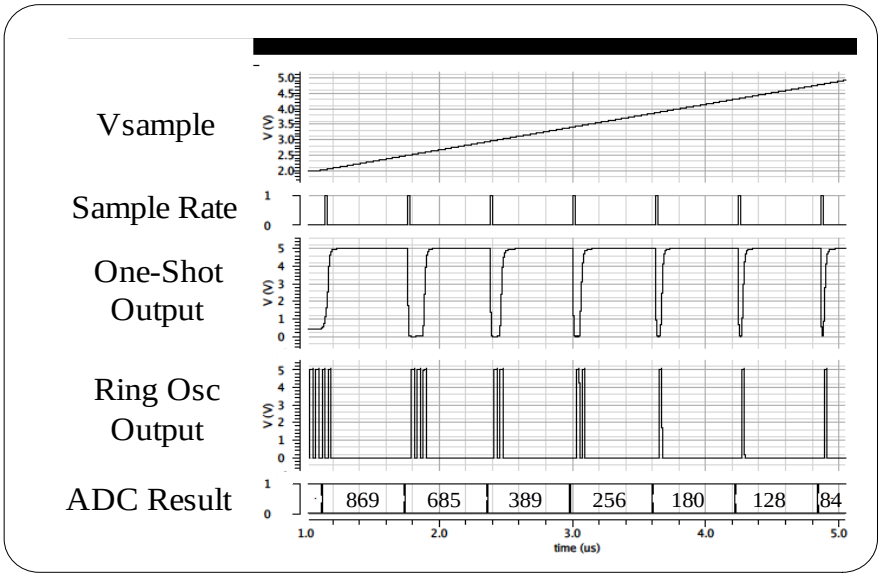

Fig. 5.4 Post layout simulation results of the implemented delay-line ADC

5.3. On-chip implementation – system level

The goal of this work was the macro-modules development and implementation, having described above on the ASIC. The technology, having used in the chip design, is a TOWER 0.18µPM CMOS process, with its 3 metal layers. The physical design, and package selection balances maximum isolation, and matching, with practical size limitations. Care needs to be taken to keep the blocks, as well matched, and as isolated as possible for the optimal performance. The digital ADC layouts are surrounded by guard rings, and arranged in the

column. The digital block placement is critical to minimize the routing to the timing calibration.

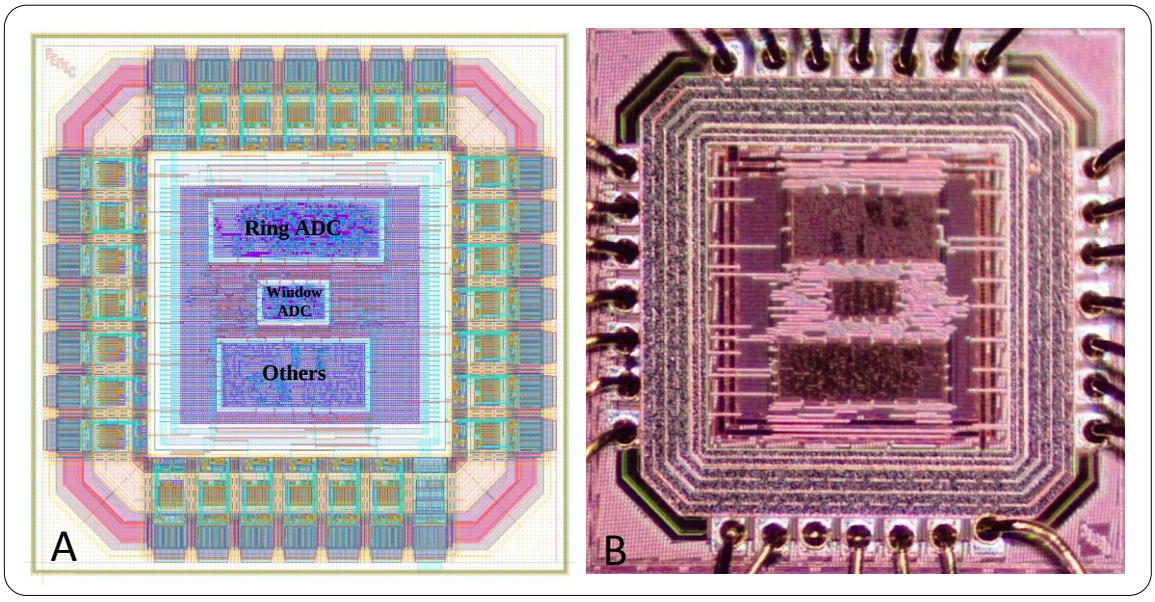

Fig. 5.5 Chip architecture: (a) chip layout; (b) micrograph picture

The chip architecture is based on three primary macros, as it has been described in Fig. 5.5 (a). Working mode, according to the TABLE VI, is allowed the specific macro enabling, or disabling. In the Fig. 5.5 (b) showed the ASIC micrograph picture. The chip package based on 28-pin low profile quad flat pack. The TABLE VII contains the pin list, including all the internal pins, and their main functions.

Two primary chip modes have been tested: Ring ADC, and Window ADC. It can be observed, that the on-chip simulation results are quite similar to the expected, and experimental ones. The Ring ADC simulation behavior is described in Fig. 5.6, and Window ADC simulation results are described Fig. 5.7. All the simulations are based on the external one shot circuit calibrated to the effective sampling of the supported voltage range according to output result word and includes the RC parasitic instructions.

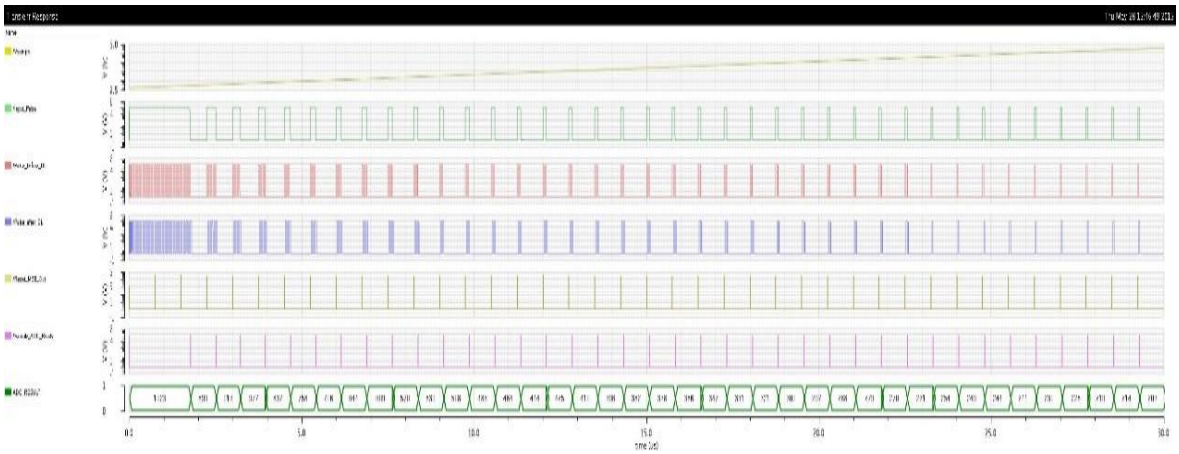

Fig. 5.6 ADC based on ring oscillator on-chip simulation, RC parasitic instruction

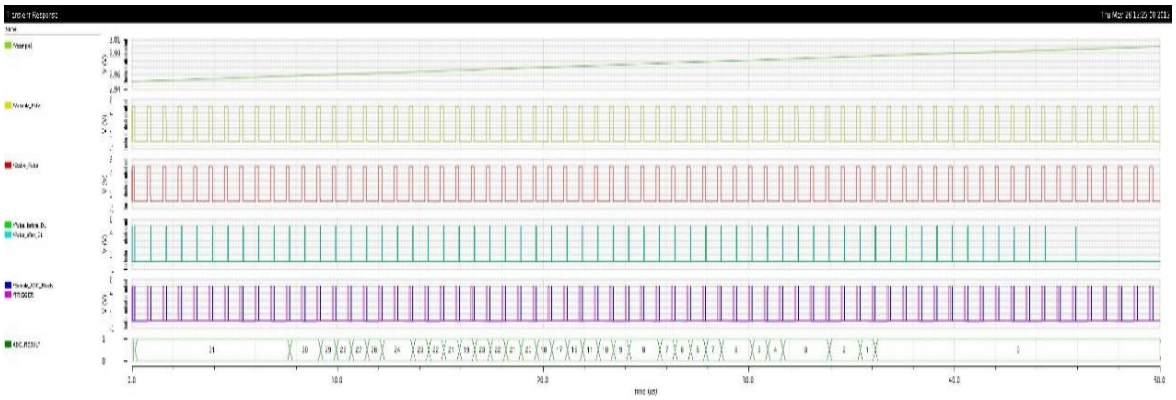

Fig. 5.7 ADC based on window on-chip simulation, RC parasitic instruction

5.3.1. On-chip experimental results

In order to verify the chip performance, the test environment board (see Fig. 5.8) has been developed, which is allowed to check each module separately, and as full system, with wide test point's collection, which are connected to the dedicated chip I\Os having depended on the working mode (see TABLE VI).

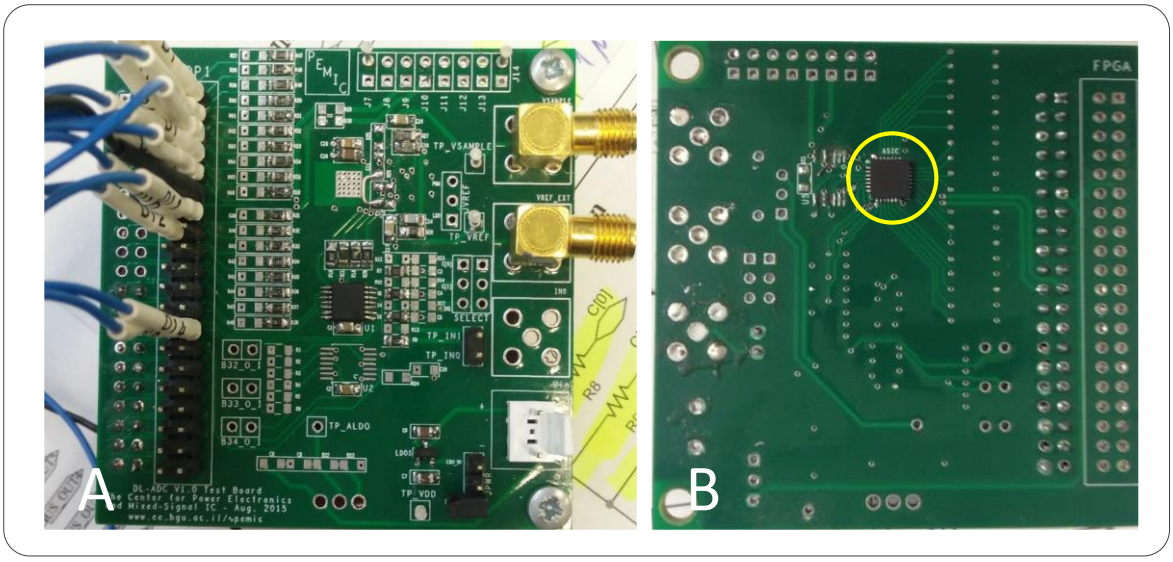

Fig. 5.8 The ASIC development board with dedicated peripherals; a). up side, b). bottom side.

This chapter describes the experimental performance of the two primary modules: the Ring ADC, and the Window ADC. As it has been pointed out before in Paragraph 3, the sample process is separated into two independent steps: the analog-to-time conversion, and the time-to-digital conversion. In Fig. 5.9 it can be seen the one shot circuit's behavior, which is responsible for the analog-to-time conversion, or in other worlds, it is being produced the output pulse, in accordance with input voltage, when the conversion has been performed, in inverse the relationship, according to (3.1). The low voltage (e.g. about the process threshold value), 1.7V, having produced the long pulse (e.g. 160ns) can be effectively sampled (see Fig. 5.9 (a)), and the high voltage, 5V, having produced the short pulse (e.g. 40ns)

(see Fig. 5.9 (c)). The output pulse must be adjusted for the ADC topology, in order to get the optimal effective sampling range. The pin collection has been dedicated to one shot circuit, which is connected to the external digital buffer, in order to be increased the produced pulse stability.

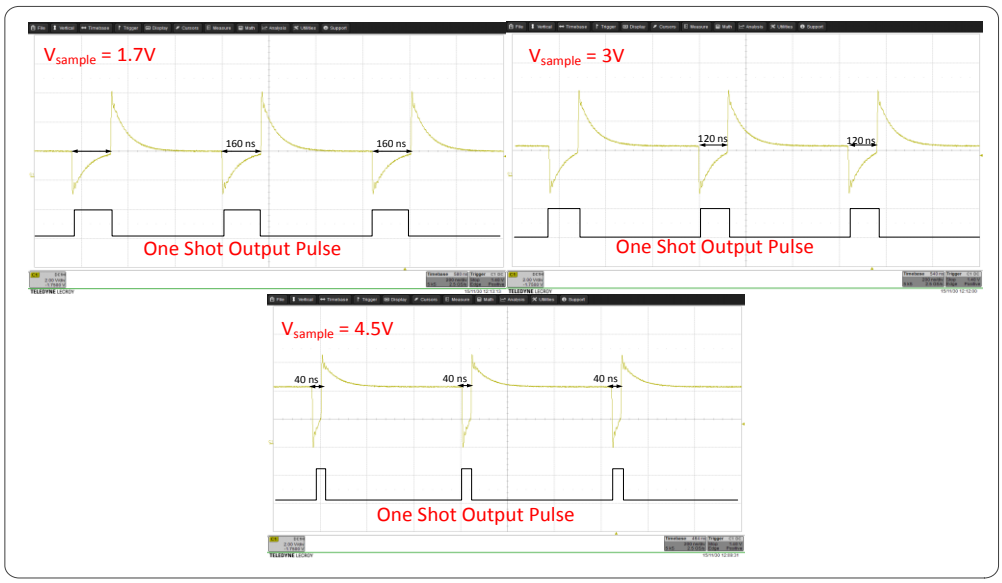

Fig. 5.9 One shot output pulse behaviour, as a result of the input voltage; a). The input voltage = 1.7V, b). The input voltage = 3V, c). The input voltage = 4.5V.

5.3.2. *The Ring ADC experimental results*

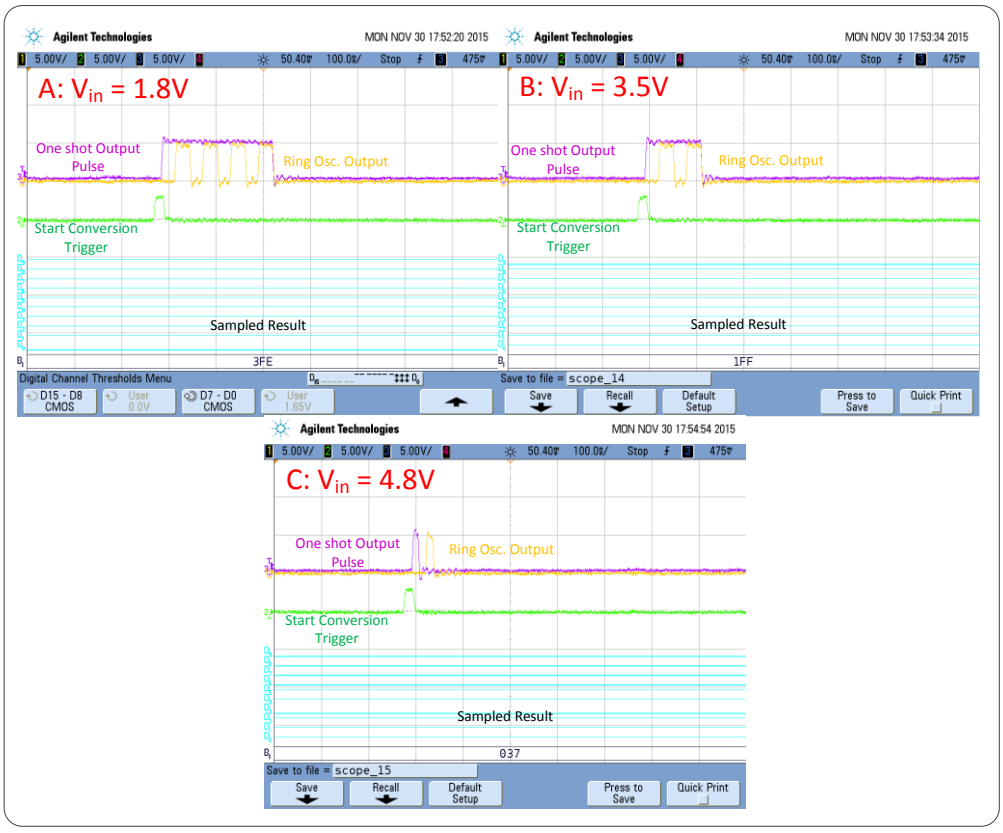

Fig. 5.10 The Ring ADC behavior, as a result of the one shot's output pulse; a). The pulse is compatible to 1.8V, b). The pulse is compatible to 3.5V, c). The pulse is compatible to 4.8V.

In order to verify the Ring ADC correct behavior, the experimental results have to be the similar to the expected results, having described in Fig. 3.6. In Fig. 5.10 the conversion process has been described, where the one shot circuit is produced the output pulse, respectively, the sampled analog voltage level. The output pulse length is responsible for the ring oscillator enabling which is fed the low resolution counter. During the falling edge of the one shot pulse, the sample result is carried out by result unification of, as the low, well as the high resolution counters. The sample result word has been described the Ring ADC conversion result.

The mathematical model of the ADCs based on one shot circuit, according to (3.1), has the ln-function behavior. In Fig. 5.11, the calculated results comparison had been described (e.g. the pulse length variability, according to provided voltage from 1.5V to 5V), and had been sampled results, which were converted to the terms of time by the sample value multiplying on the single buffer propagation delay.

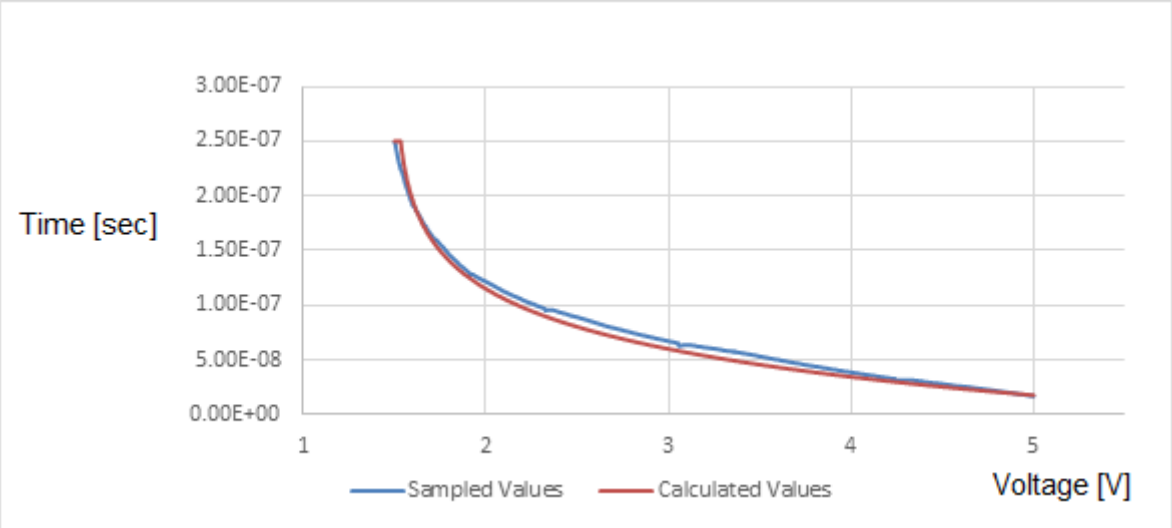

Fig. 5.11 The Ring ADC - sampled versus calculated values comparison.

The full effective sample range has been verified by the two different analog signals providing, like sinus and ramp (see Fig. 5.12 and Fig. 5.13). These signals' properties are the following: the amplitude has been varied between 1.5V – 5V and the frequency has been 100Hz. In Fig. 5.13 the well-defined ln-function effect on the sampled signal can be also observed.

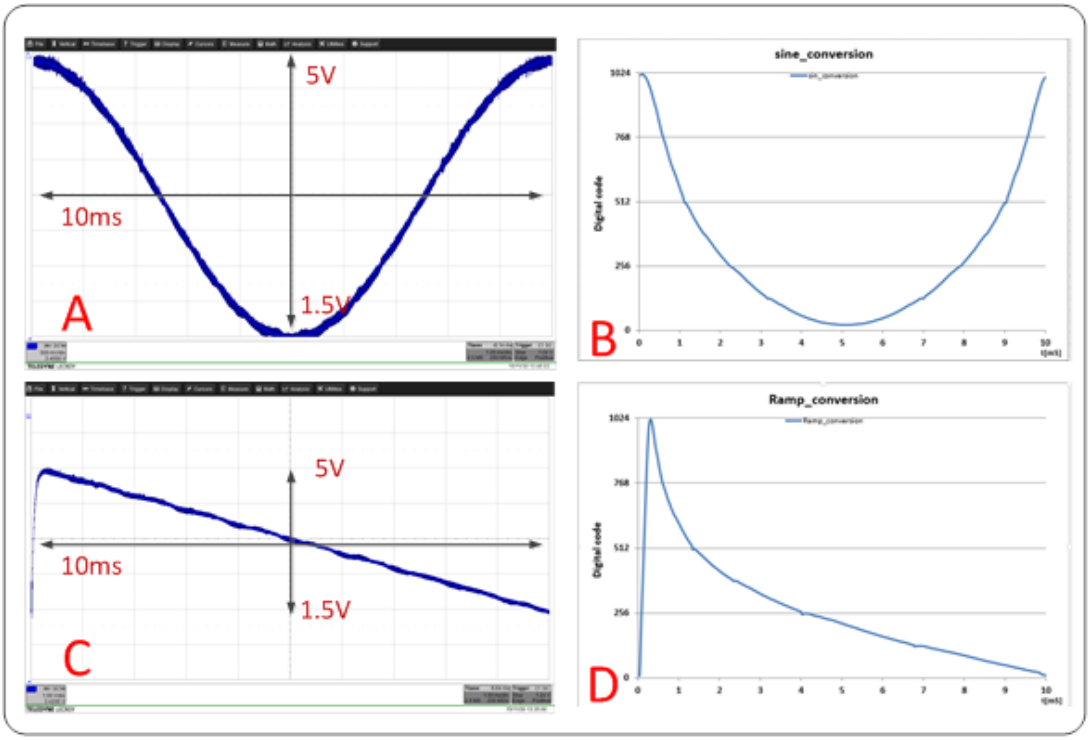

Fig. 5.12 The Ring ADC sampled value (e.g. normalized) versus the input analog signal; a). the analog input Sin@100hz, b). the sampled output Sin@100hz, c). the analog input Ramp@100hz, b). the sampled output Ramp@100hz.

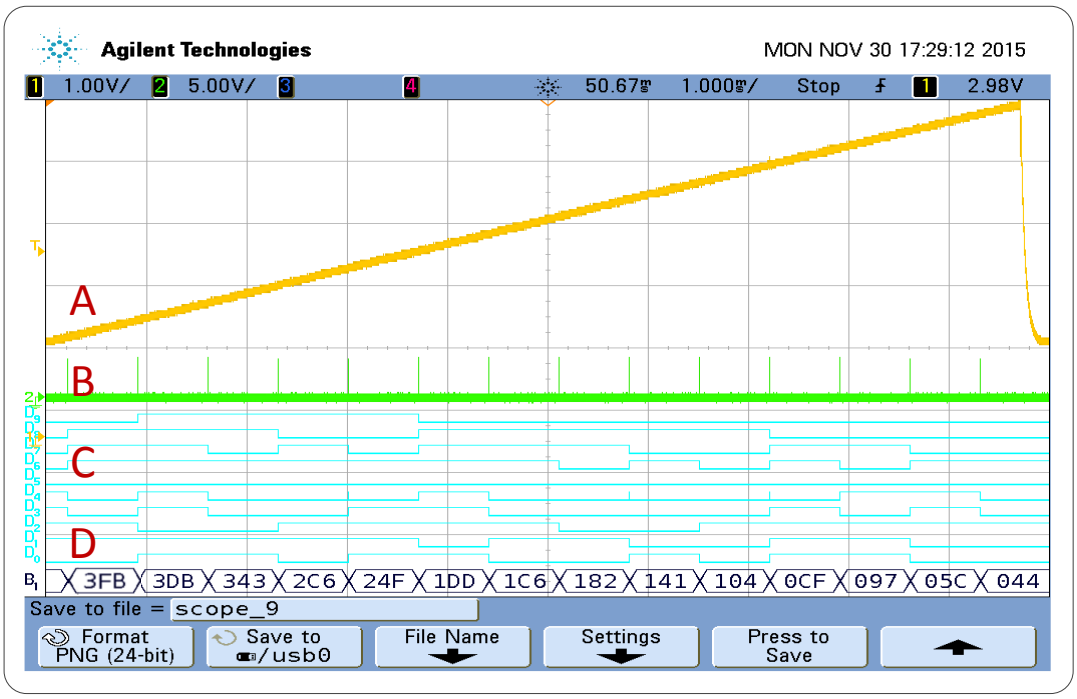

Fig. 5.13 The Ring ADC full effective scale sampling (e.g. normalized); a).the analog input signal Ramp@100Hz (e.g. 1.5V – 5V), b).the sample ready trigger, c).the sample result in the binary representation, d).the sample result in the hexadecimal representatrion.

In contrast to the Ring ADC, which is working at the wide-effective sample range between V_{th} and V_{dd}, the Window ADC is working around pre-defined bias, and it's sample range is, significantly, shorter. In order to verify the Window ADC performance, the bias

level has been set to 3.66V, and the effective sample range has also been varied between 3.67V, and 3.99V (ΔV=320mV). The bias value has been chosen, according to the locally-linear ln-function behavior. The sample result value has the unsigned representation. The experimental results have been observed as in Fig. 5.15, well as in Fig. 5.15.

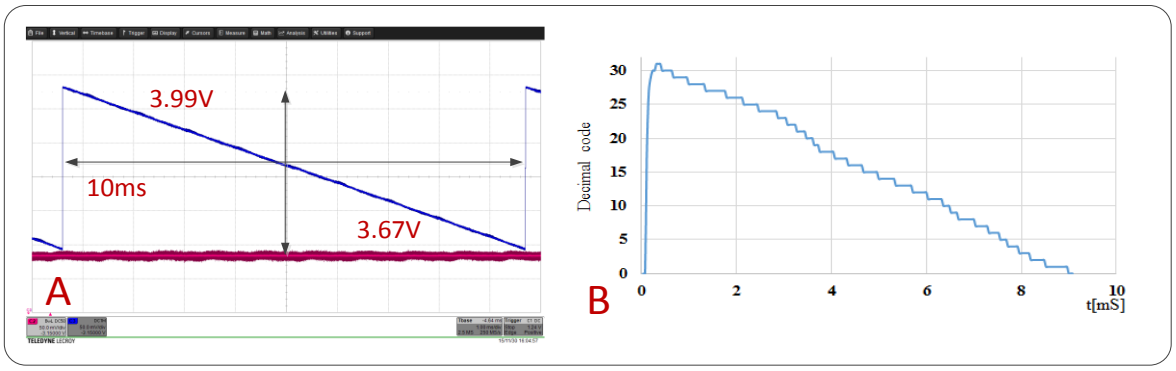

Fig. 5.14 The Window ADC – the output sampled signal (e.g. normalized) versus input analog signal; a). analog input Ramp@100hz, b). sampled output Sin@100hz

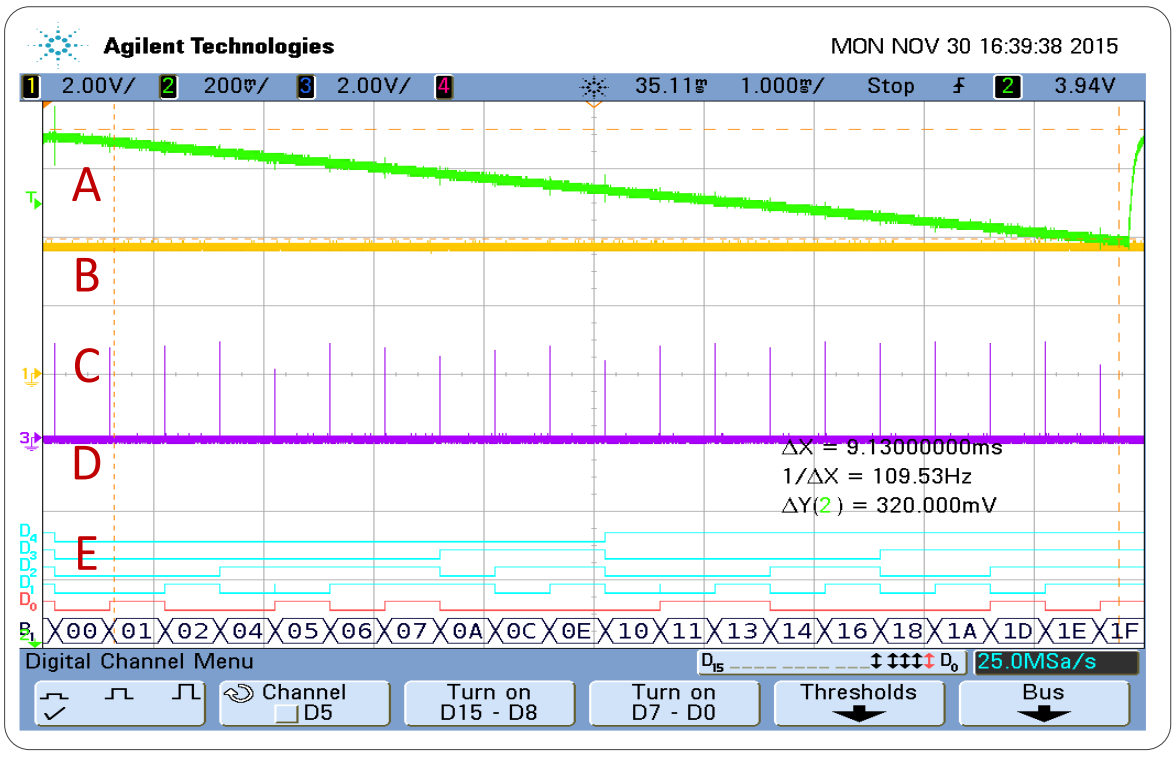

Fig. 5.15 The Window ADC – full effective scale sampling; a). the analog input signal Ramp@100Hz (e.g. 3.67V – 3.99V range), b). the maximum voltage level – 3.99V, c). the sample ready trigger, d). the sample result in the binary representation, e). the sample result in the hexadecimal representation.

In this paragraph described the on-chip experimental performance of the two ADC different architectures. The results obtained had been shown, that the IC implementation didn't harm to the sampling process, compared to the FPGA, but also further improved the whole-module performance, in terms of, as the sample rate, well as the power consumption.

6. Experimental application based on ADC and DPWM

6.1. The PWM/CPM controller with integrated high resolution delay-line ADC

The objective of this design is to be presented the FPGA design, and the PWM/CPM digital controller implementation, that includes the integrated DPWM, and the ADC peripherals (using an all-digital realization), and reduces the auxiliary components number. The introduced controller architecture is depicted in Fig. 6.1. It follows the classical two-loop CPM design, with a fully digital outer voltage loop, while for the inner current loop, an analog comparator i_{cmp} is utilized.

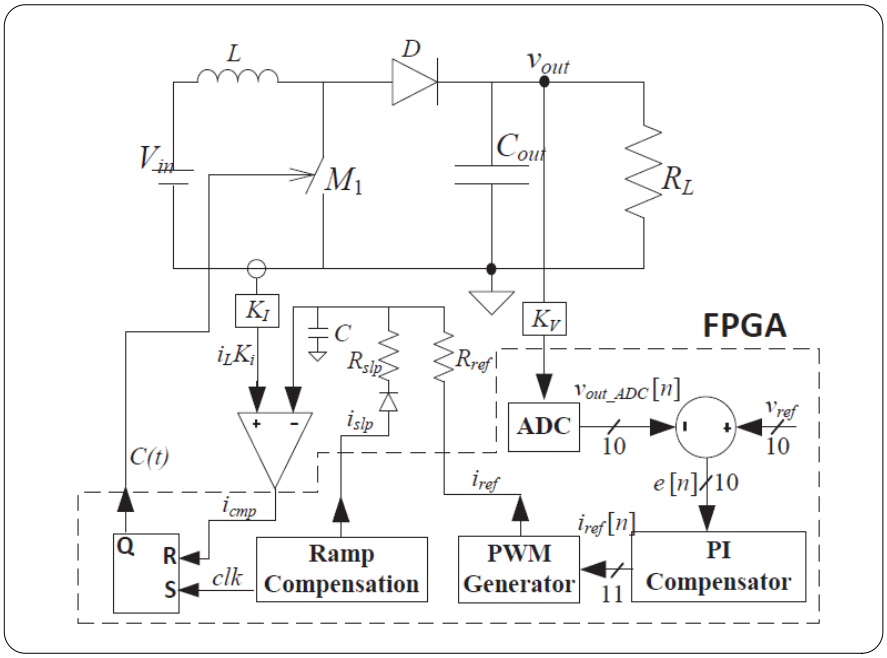

Fig. 6.1 Architecture of the CPM controller based FPGA

The voltage loop creates a digital reference for the peak current value $i_{ref}[n]$, that is, then, converted into an analog equivalent, with a digital-to-analog converter (DAC), that is realized by a simple RC filter, that is fed by a high-frequency high-resolution (11bit @ 1.6 MHz) DPWM unit, has been developed in this study. The current reference is calculated, with a PI compensator, having based on the error signal of the voltage loop e[n], and the resulting output of the DAC is compared to the sensed value of the inductor current $i_L K_I(t)$, with the comparator i_{cmp}. The output of the comparator is, then, sent to the S-R latch, and a pulse width modulated signal c(t) is created.

The output voltage is sensed, having used a modified delay-line (DL), based the ADC, has also been developed in this study. To allow the CPM operation at duty ratios above 0.5, and avoid of the subharmonic oscillations, an additional DPWM signal (at lower frequency)

is generated, and summed, with the generated current reference, to create the artificial slope for compensation.

In the Fig. 6.2 can be observed the ADC configuration that has been developed. The time counter delay string is implemented, having used the asynchronous buffers, which in the current design feature a relatively fixed propagation delay of 300ps per cell. To achieve 10bit resolution, 1023 buffers are used. To facilitate a simple voltage-to-time conversion, having used the digital architecture and the FPGA, a simple monostable multivibrator (i.e. one-shot timer) has been employed by adding two additional gates. To complete the circuit functionality, the initial time constant is created, having used the auxiliary RC network that is connected to the FPGA ports. The sensed voltage is connected to the resistor R, having created the analog link.

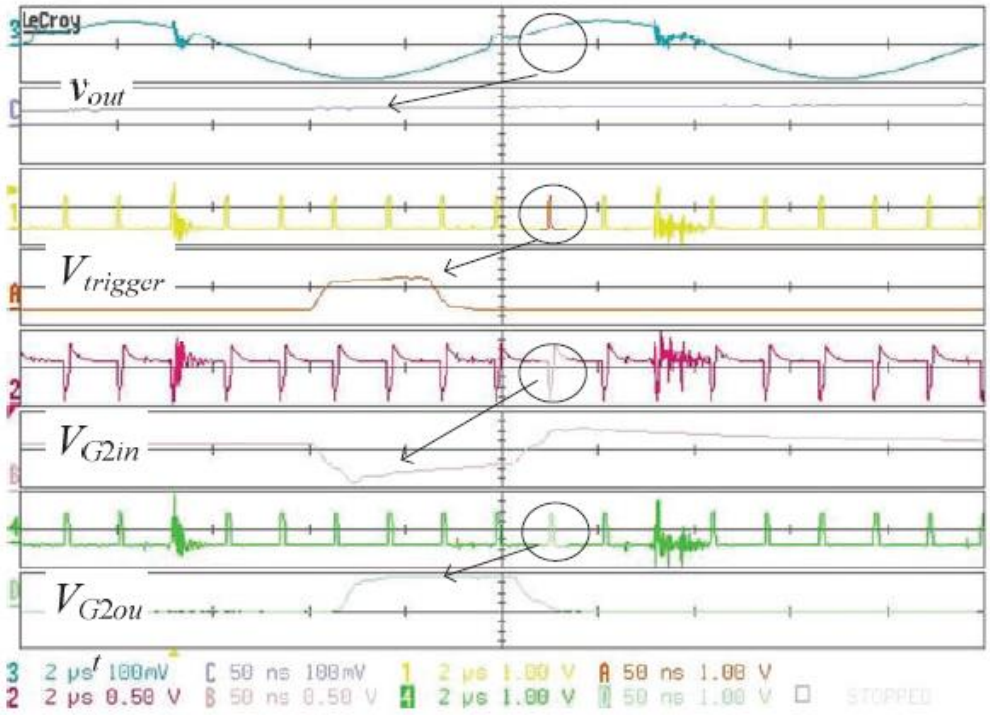

Fig. 6.2 Experimental results of the delay-line ADC; V_{out}:output voltage, $V_{trigger}$: one-shot circuit enable, V_{G2in}:voltage on one-shot capacitor, V_{G2out}:delay-line output pulse;

The description of the DL-ADC operation is assisted by the timing diagram of Figure, which shows the experimental waveforms of the converter. A start-of-conversion, i.e. trigger signal, activates the one-shot. The resultant pulse length, T_{pulse}, as a function of the sensed voltage is expressed, and is described in the formula.

The output signal of the one-shot timer ($G_{2\text{out}}$) contains the required data of the voltage level, and also provides the start, and stop signals to the counter. The edge detector generates a start-of-conversion signal, with the rising edge of G_2 out, and a stop-of-conversion, and capture signal, with its falling edge. The resulting thermometer code is, then, converted into

a digital value by summation of 2's complement based algorithms. It can be also observed from Figure, that power transistors switching action, introduces noise on the sensed signal, which may be resulted in an erroneous measurement. This, however, does not affect the closed-loop operation of the system, which relies on a single sample per switching cycle.

The experimental prototype has been built, according to Figure. A 12V to 48V, 100W, boost converter, that operates at switching frequency of 100 KHz, has been examined (L=150uH, C_{out}=75uF). For the target converter, 8 bits ADC resolution has been found sufficient, having resulted in, approximately, 10mV resolution. The CPM operation, having used a 12bit current reference signal, and slope compensation has been verified. The controller has been implemented on a Cyclone IV FPGA – Altera (EP4CE115F29C7), and it requires only 6500 logic elements (for the entire controller design, as described throughout the paper), having allowed its implementation, with only a 7% of the resources of the low cost FPGA system.

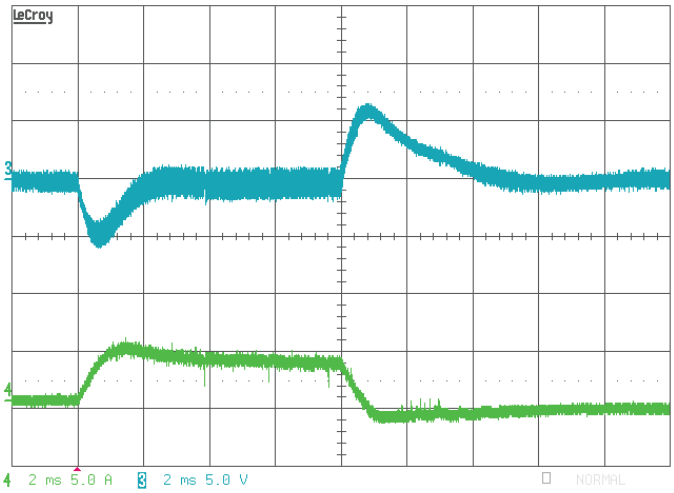

Fig. 6.3 Experimental load transient response (25 W to 90 W to 25 W) of the CPM controlled boost converter, having used the new controller. Ch.3(e.g. upper trace): the ac component of the output voltage, 5V/div;Ch.4 (e.g. bottom trace): inductor current

The response of the experimental CPM controlled boost converter to 25W to 80W to 25W load transient showed in Fig. 6.3. As can be observed, a well-regulated response has been obtained, with the dynamic performance, that is comparable to other reported CPM controllers, with as well the advantages of fully digital design, with as very low gate count realization. The full paper version can be observed in [3].

6.1.SC-buck converter with hybrid controller based on window ADC

The Window ADC has been used, as a sample module in the experiment that explores the large-signal, and small-signal dynamics of a series-capacitor (SC) buck type converter, and introduces an optimal closed-loop control scheme to accommodate both the steady-state and

transient modes. As opposed to a conventional buck converter, where the time-optimal control is realized by a single on-off cycle' in the SC-buck topology, there is a need to distribute the switching phases to satisfy the charge-balance of the flying capacitor. The new control method hybrids a voltage-mode of the small-signal controller for the steady-state operation, and non-linear, state-plane, having based on the transient-mode control scheme for the load transients. The operation of the controller is, experimentally, verified on the $12W$ $12V-to-1.5V$ converter, having demonstrated the voltage-mode control operation, as well as the time-optimal response for the load transients.

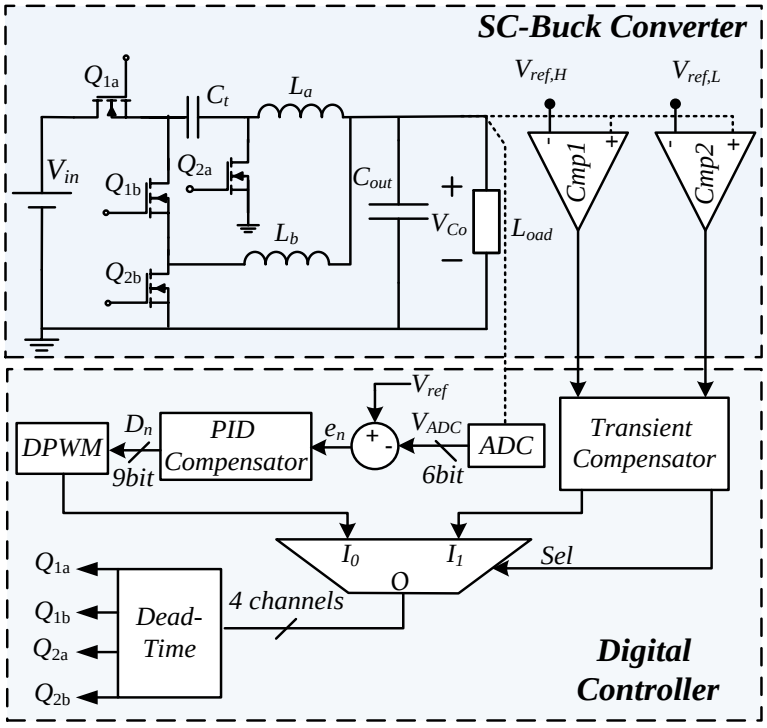

Fig. 6.4 SC-buck converter with hybrid controller based on window ADC

To validate the operation of both the small-signal compensator, and the time optimal controller, a $12V-to-1.5V$ SC-buck converter prototype has been built, and tested (see Fig. 6.4). The experimental converter operates with the Window ADC 6 bit output resolution and sample rate of $10Msps$, its work concept has been described in the previous section. Having achieved the switching frequency $1.25MHz$ and the main components are assigned as: $L_a = L_b = 5\,\mu H;\ C_i = 50\,\mu F;\ C_o = 100\mu F$. The digital controller comprises the steady-state voltage compensator as shown in the Fig. 6.5. The controller has entirely been realized entirely on the Altera Cyclone IV FPGA, including the custom design of all related peripherals, with the all-digital Window ADC, and the digital PWM as described in [1],[2],[4].

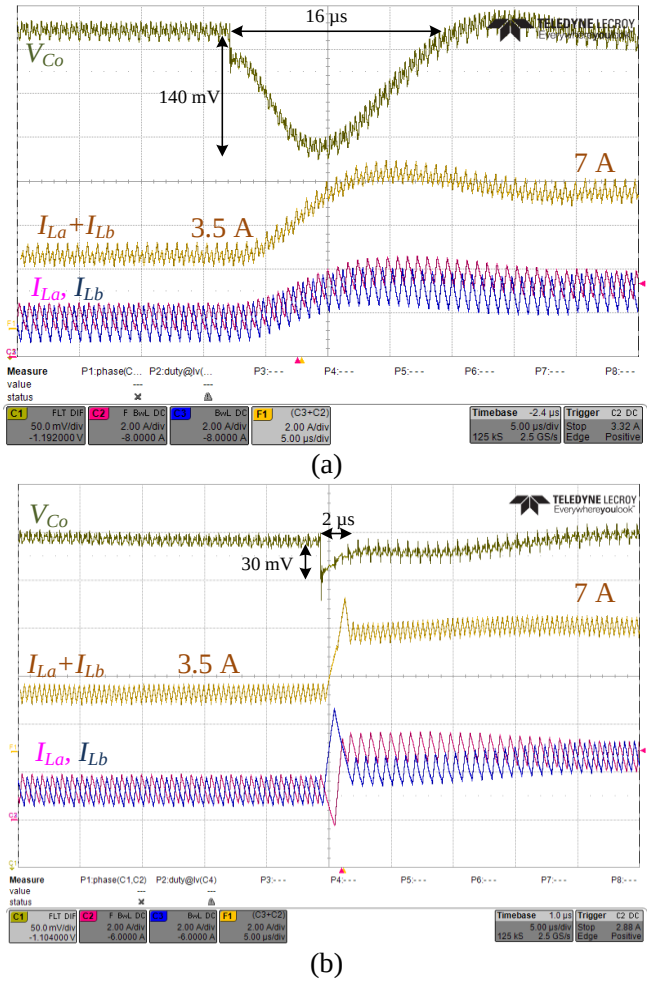

Fig. 6.5 Experimental results for loading transient response from 1.75A to 3.5A by (a) voltage-mode control (500mV/div, 50µs/div), time-optimal control (200mv/div, 5µs/div)

In this study, an optimal closed-loop controller based on all digital components for a SC buck converters has been presented. Two control laws have been implemented by the same digital components. The full paper version can be observed in [4].

7. Discussion

Digital control of high-frequency low-power switching-mode power converter has received significant research attention. Potential advantages include programmability and flexibility, improved system interface, reduced design time, scalability and cost advantages of standard digital CMOS process, as well as the ability to implement more sophisticated system control and management techniques. While most of the advantages of the digital control have been recognized and incorporated in high complexity applications that operate at low switching-frequency and high-power level, high switching-frequency and low-power portable systems such as phones, PDAs and music/video players are still mainly designed with analog PWM control inside the voltage regulator blocks. It should be noted that broader acceptance of digital techniques in low-power DC-DC applications is still hampered by practical problems of the combination of cost issues, trade-off of performances and power consumption. The research interest of the thesis is to explore practical ways of incorporating advantages of digital control in practical realizations, which is considered for the size miniaturization of high-frequency low-power SMPS. Two main objectives of this work are to implement high-resolution high-frequency DPWM and high-resolution ADC in an FPGA and ASIC based realization.

In this concluding chapter, are summarized the major contributions of this research work and discuss the possible future work.

7.1. Contribution of the research

First of all, it enhances understanding of current practical implementation issues of high-frequency low-power digitally controlled SMPS. Issues such as resolution requirements of ADC and DPWM (quantization effects) and limit cycles were reviewed. The thesis presents an analysis of the technical difficulties associated with implementation of digital control at high switching frequency. The performance-related requirements of high speed and high resolution of the key controller building blocks, including ADC and DPWM, must be met together with important practical constraints of low complexity, power consumption and cost. The analysis of these technical obstacles and limitations of conventional DSP digital solutions leads into the main part of the thesis where new hardware and software solutions are proposed to enable successful practical implementations of high-performance digital controllers.

In continuation, the thesis presents the results of our research concerning the practical implementation of the digital controllers, where described two kinds of ADCs: 10-bit Ring

ADC architecture and 5-bit Window ADC architecture and DPWM based ring oscillator approach. All work and development were carried out using digital circuitry methods based on FPGA (module and system implementation) and partially on ASIC (module implementation). The developed prototypes are investigated and supposed to be an alternative choice for SMPS realization. This is done in the hope of providing strong justification to how the digital controllers may be better in some aspects than the analog controlled systems, and to prove that not only the digital control implementation is very possible now in the area of high-frequency low-power SMPS, but also that by using the digital control significant improvements of switching converters characteristics can be achieved.

7.2.Suggestions for future research

As the preliminary research work for the project, the experiment here is only dedicated to validate the functional performance of independent macro modules of ADC and DPWM in FPGA and IC. But the design modules are implemented in fully synthesizable in RTL code and willing to be part of the overall SOC (System-on-Chip) design. However, the ASIC implementation of the proposed digital control blocks as a part of the whole system is a necessary procedure. There are several reasons to address this point. Firstly ASIC chip enables the much higher speed, performance operations and optimization properties. Secondly ASIC implementation offers the vehicle for energy consumption measurement and comparison between the simulation of power consumption and experimental measurement. In fact this work has already started lately in a subsequent project. The ASIC implementation is the only reasonable technology to quantify the energy performance of digital control and lead to conclusive comments with respects to analog-control.

8. Appendix

8.1.Chip working modes

TABLE VI. FOUR AVAILABLE WORKING MODES

Comments	Mode Description	Mode Number (MSB → LSB)
All modules disabled	Shut Down	00
Window ADC module enabled, others disabled	Window ADC	01
Ring ADC module enabled, others disabled	Ring ADC	10
Full adder module enabled, others disabled	Full adder	11

8.2.External pin placement

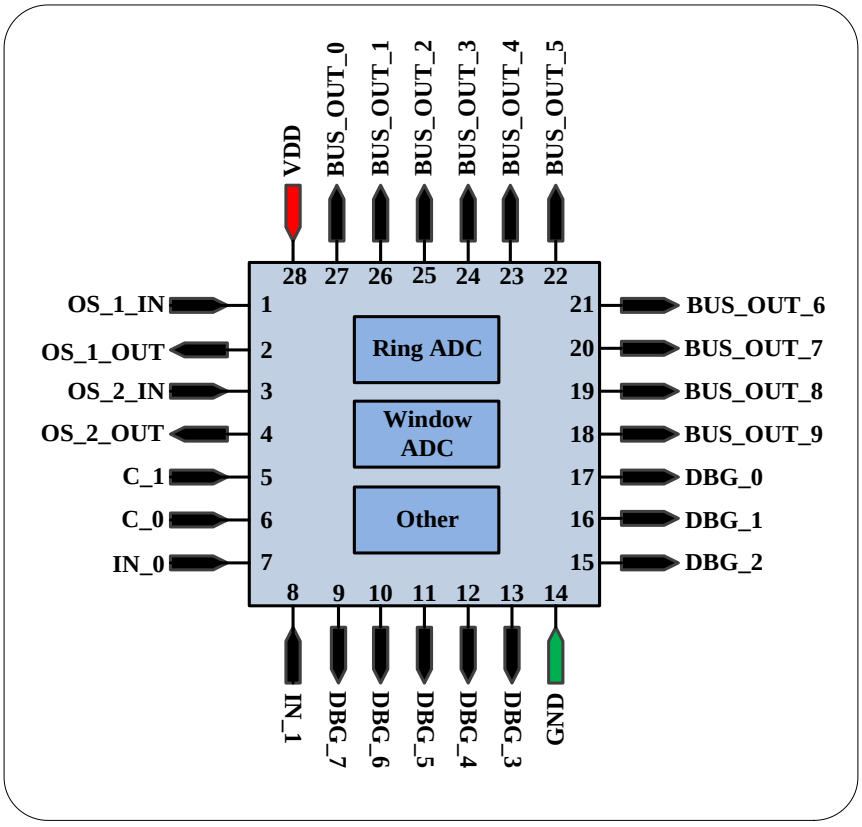

Fig. 8.1 Chip pin placement

8.3. Chip architecture – module level

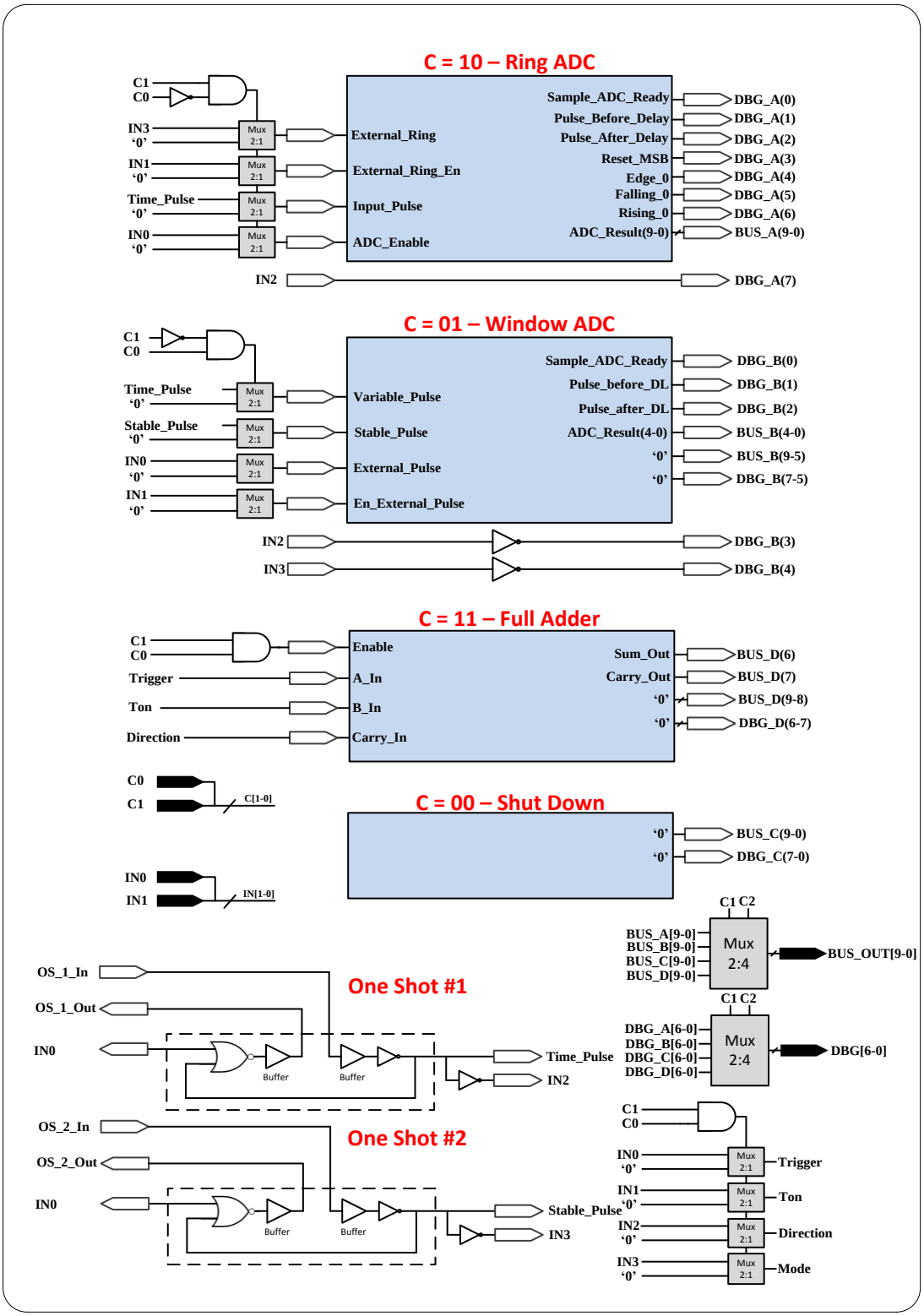

Fig. 8.2 Chip architecture – block level

8.4.Internal pin functionality description

TABLE VII. INTERNAL PINS FUNCTIONALITY DESCRIPTION

Pin Purpose	Pin Type	Pin Name	Logic Module
External oscillator	Input	External_Ring	Ring ADC
Enables external oscillator	Input	External_Ring_En	
Pulse provided by one shot circuit	Input	Input_Pulse	
Enables Ring ADC	Input	ADC_Enable	
Ring ADC result ready	Output	Sample_ADC_Ready	
Delay line first buffer output	Output	Pulse_Before_Delay	
Delay line last buffer output	Output	Pulse_After_Delay	
Reset MSB counter	Output	Reset_MSB	
Debug pin	Output	Edge_0	
Debug pin	Output	Rising_0	
Debug pin	Output	Falling_0	
Ring ADC sample result	Output	ADC_Result	
Variable pulse provided by one shot circuit	Input	Variable_Pulse	Window ADC
Stable pulse provided by one shot circuit	Input	Stable_Pulse	
Artificial external pulse	Input	External_Pulse	
Enable artificial external pulse	Input	En_External_Pulse	
Window ADC result ready	Output	Sample_ADC_Ready	
Delay line first buffer output	Output	Pulse_Before_Delay	
Delay line last buffer output	Output	Pulse_After_Delay	
Window ADC sample result	Output	ADC_Result	
Enable module	Input	Enable	Full Adder
First bit input	Input	A_In	
Second bit input	Input	B_In	
Carry bit input	Input	Carry_In	

Full adder sum result	Output	Sum_Out	
Full adder carry result	Output	Carry_Out	

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