Modeling and Behavioral SPICE Simulation of a Self Adjusting Current-Fed Push-Pull Parallel Resonant Inverter (SA-CFPPRI)

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***Abstract*—A modeling methodology that can be applied to power systems that include non-linearities and phase lock loops was developed and used to model and investigate the properties of a Self Adjusting Current-Fed Push-Pull Parallel Resonant Inverter (SA-CFPPRI). This topology is based on the Push-Pull Parallel Resonant Inverter in which a controlled variable inductor is incorporated to keep the system at resonant frequency over a given frequency range and under a non-constant reactive load. The analytical expression and SPICE models developed in this study were found to be in good agreement with experimental results. PSPICE/ORCAD (Cadence, USA) files (Evaluation version 9.2) of the system under study are available for download from http://www.ee.bgu.ac.il/~pel/download.htm.**

I. INTRODUCTION

As Power Electronics circuits are getting more complex, higher level modeling and simulation is becoming a crucial tool for designing and verifying the performance of such systems in open and closed loop configurations. This is particularly important when a system is highly non-linear and includes a multitude of signals types: voltages, currents, frequency and phase. A case in point is a recently described power oscillator [1] that is based on the Current-Fed Push-Pull Parallel Resonant Inverter (CFPPRI) [2,3] in which a controlled variable inductor is incorporated to keep the system at resonant frequency over a given frequency range and under a non-constant reactive load. The system includes two feedback loops: an inner current loop and an outer phase-lock loop that is used to track the control frequency. Possible applications of the Self-Adjusting CFPPRI (SA-CFPPRI) include: driving piezoelectric motors and transformers [4, 5] and as a power source for an AC distributed power management system [6].

The objective of this study was two fold: (a) to develop a modeling methodology that can be applied to power systems which include non-linearities and phase lock loops as found in the Self Adjusting Current-Fed Push-Push Parallel Resonant Inverter (SA-CFPPRI) as well as in other systems, and (b) to apply these tools to investigate the properties of the SA-CFPPRI. The proposed modeling approach is primarily aimed at the development of a SPICE compatible model that can be run on modern circuit simulators such as PSPICE/ORCAD (Cadence, USA). In this approach, nonlinear subsystems are described by large-signal behavioral dependent sources that emulate the functional relationships of the elements [7]. To model the SA-CFPPRI there was a need to develop three new behavioral models for: (a) a Buck type current regulator, (b) a phase comparator (as part of the phase lock loop control), and (c) a non-linear inductor.

II. THE SA-CFPPRI

Since a description of the SA-CFPPRI was presented earlier [1], we repeat here, for the sake of brevity only the essential details of this topology. The SA-CFPPRI is built around a self-oscillating CFPPRI (Fig. 1a) that comprises two switches (Q1, Q2) and a Soft Switching Control (SSC) assembly. The SSC keeps the inverter at the resonant frequency by switching the gate drive polarities (V_{GS1},V_{GS2}, in Fig. 1a) whenever the center tap voltage (V_{tap}) reaches zero. This control method is based on the concept used in the IC design of Texas Instrument's (originally Unitrode) controller UC3872 [8, 9]. When locked, the SSC ensures zero voltage switching of the SA-CFPPRI (Fig. 1b) while the frequency of operation is determined by the equivalent capacitance and inductance of the resonant tank (L_r, C_2, C_3). Changing the inductance of L_r can thus change the operating frequency while still maintaining soft switching. This is accomplished in the SA-CFPPRI by incorporating a variable inductor T1 (Fig. 1a) that is controlled by a bias current [10, 11]. This current is stabilized, in present design, by a Buck type converter that operates in closed loop around the amplifier A1. Frequency tracking of the SA-CFPPRI is then assured by incorporating a phase detector that generates an error signal as a function of the phase difference between the control frequency F_{in} and the running frequency of the PPRI. A phase deviation will change the bias current of the variable inductor and hence cause F_β to follow F_{in} (Fig. 1a).

This paper addresses primarily the aspects of model developments (SPICE and small signal) rather than the issue of hardware or control design. Some aspects of these are presented in [1].

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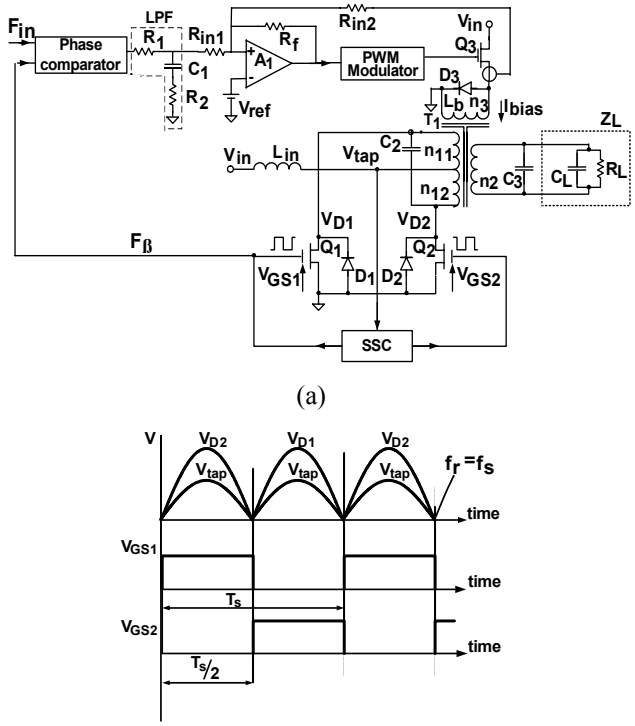

Figure 1. The SA-CFPPRI system (a) and key waveforms under locked condition (b).

III. MODEL DEVELOPMENT

The proposed modeling methodology will be demonstrated by considering the building blocks of the SA-CFPPRI and showing how each block is modeled. Considering the description of the SA-CFPPRI given in the previous section, the SA-CFPPRI large signal block diagram includes two major low frequency control loops (Fig. 2a): an inner current loop of the inductor's bias and the outer phase loop that is responsible for the frequency tracking. An additional feedback loop, the SSC (Fig. 1a), has a fast response (in the order of the operating frequency) and can thus be considered transparent to the low frequency response, which is under investigation here.

The methodology used in this study to develop the SA-CFPPRI model was to first extract the large-signal, non-linear SPICE compatible modules and then to leave the linearization, required for small signal analysis, to the simulator. Verification was carried out by cross checking the results against analytical small signal expressions that were also derived in this investigation and finally cross checking the large and small signal simulation results against experimental data.

The functional relationships in the simplified block diagrams (Fig. 2) are divided into two groups: (a) linear transfer functions (TF): where the output equals the input multiplied by the TF value, and (b) non-linear TF: where the output is derived as a non-linear function of the input signal. The non-linear TF are denoted as Y(X) where Y (capital letter) is the function and X is driving signal. The linear,

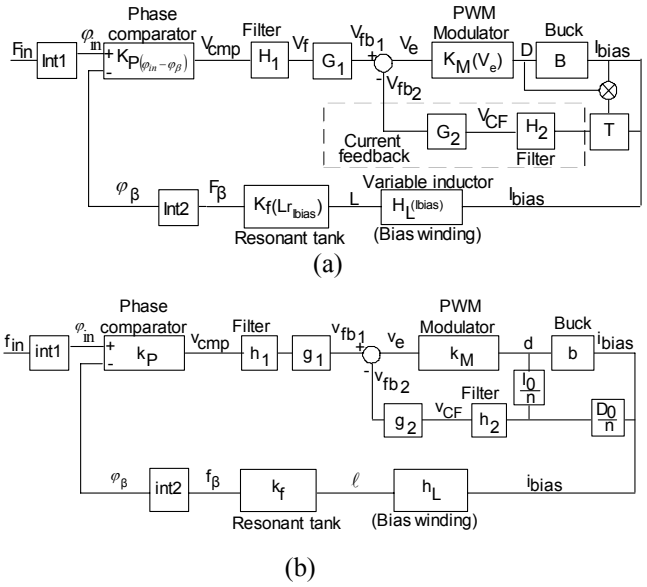

Figure 2. Simplified control block diagram of the SA-CFPPRI. (a) large signal, (b) small signal.

small signal transfer function, denotes as 'y' (small letter), were obtained by taking the derivative Y(X) with respect to X.

For SPICE simulation, the filters and amplifiers can be left as-is while the special and nonlinear devices need to be transformed into a behavioral model. In the behavioral SPICE compatible equivalent circuits, the following variables are coded into voltages: Frequency $1V \equiv 1Hz$; Inductance $1V \equiv 1H$; Phase $1V \equiv 1rad$; Duty cycle $1V \equiv (D = 1)$.

Phase Comparator. (a) Large Signal Model. The inputs to the Phase Comparator (PhC) are two frequency signals (F_{in}, F_β) while the output is a linear function of the phase difference between the two signals (Int1, Int2 and Kp(φ_{in}-φ_β) in Fig. 2a). Consequently, the PhC can be described as a module that includes two integrators at the input and a gain block (Fig. 2a). The PhC output signal V_{cmp} can be expressed as [12]:

$$V_{cmp} = K_p(\varphi_{in} - \varphi_\beta) = V_{sup}(\varphi_{in} - \varphi_\beta) + \frac{V_{sup}}{2} \quad (1)$$

where, φ_{in} is the phase of the input frequency, φ_β is the phase of the output frequency and V_{sup} is the supply voltage of the PhC.

(b) Small Signal Model. Taking the derivative of V_{cmp} with respect to (φ_{in}- φ_β) around the operating point and after some manipulations, the small signal TF of the PhC, k_p is expressed as:

$$k_p = \frac{V_{cmp}}{\varphi_{in} - \varphi_\beta} = V_{sup}. \quad (2)$$

Integrators. In SPICE realization of a PhC, the integrators that transform the frequencies (F_{in}, F_β) into the phases $(\varphi_{in}, \varphi_\beta)$ could be realized by an ELAPLACE behavioral dependent source defined by the expression 1/s. It was found, however, that this approach causes convergence

problem at the bias point calculation (when 's' is assumed to be zero). This problem was not alleviated even after adding a small number to 's' to keep the denominator from approaching zero. The problem was eventually remedied by emulating the integrators as two low pass RC networks followed by a differential amplifier block that was realized by a behavioral dependent source (Fig. 3):

$$\mathrm{int}_1 = \mathrm{int}_2 = \frac{1}{\mathrm{sRC}+1} \qquad (3)$$

where, int1, int2 are the integrators TF of Fig. 2b. Being a linear TF this representation is valid for both the large signal and small signal models.

The time constant RC was chosen to be equal to unity, far below the frequency of interest. This solves the convergence problem at low frequency' while at high frequencies (beyond the break point) the network behaves as an ideal integrator (1/s).

Phase Comparator Output Filter. The PhC generates an error signal that represents the phase mismatch between the inputs for every switching cycle of the inverter.

The output network, H_1 that filters out the pulsed output of the PhC is designed as a lag-lead network (Fig. 4) that can be expressed as:

$$H_1 = h_1 = \frac{R_{in1}}{R_1 + R_{in1}} \frac{(sC_1R_2 + 1)}{sC_1R_T + 1} \qquad (4)$$

where, R_{in1} is input resistance of the summing amplifier A1. R_1, R_2, C_1 are the filter network components (Fig. 1a) and $R_T = R_1 \parallel R_{in1}$.

For SPICE realization the filter can be simulated as a passive lag-lead network as described in Fig. 4.

Resonant Tank Inductor. (a) Large Signal The inductor of the resonant tank L_r is controlled by the bias current [1, 9], and the large signal TF is expressed as:

$$L_r = H_{Lr}(I_{bias}) \qquad (5)$$

where, L_r is the inductor value and I_{bias} is the bias current (Fig. 1a). The relationship $H_{Lr}(I_{bias})$ was obtained by experimental measurements (Fig. 5). The measured values of H_{Lr} (L_r as a function of I_{bias}) were inserted into a Table in a SPICE compatible behavioral dependent voltage source (ETABLE in CADENCE PSPICE) (Fig. 6). This module can be used as-is in large and small signal simulation. The input to the module is the bias current that is passing through a zero voltage sense source (V_Ibias) and the output is a voltage that represents the running value of the inductance (ind) . In AC analysis, the simulator will apply the derivative around the operating point as the gain of the module.

(b) Small Signal Model. Since $H_{Lr}(I_{bias})$ is constructed from a finite set of measurements, a local linearization around the operating point will determine the small signal TF of the non-linear inductor, h_{Lr}:

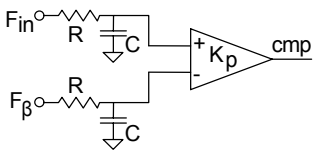

Figure 3. Behavioral SPICE compatible model of phase comparator.

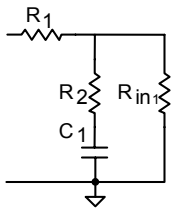

Figure 4. Phase comparator output filter.

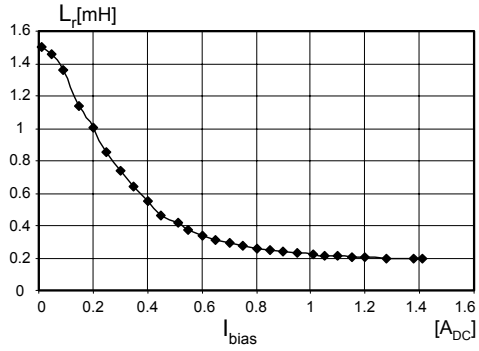

Figure 5. Inductance of resonant inductor as a function of the bias current.

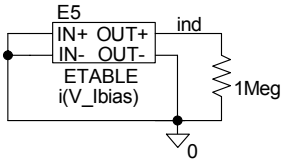

Figure 6. SPICE compatible module of controlled non-linear inductor (Fig. 5).

$$h_{Lr} = \frac{dL_{r(I_{bias})}}{dI_{bias}} = \frac{H_{Lr}(I_{bias0}) - H_{Lr}(I_{bias0} + \Delta I_{bias})}{\Delta I_{bias}} \qquad (6)$$

where, I_{bias0} is the nearest measured value of the bias current for a given operating point (denoted by the subscript 0) and ΔI_{bias} is the increment between the two nearest measured values of the bias current around the operating point.

Resonant Tank. (a) Large Signal Model. The frequency of the SA-CFPPRI that is controlled by the SSC is a function of C_r and $L_{r(Ibias)}$. Since the bias current now controls the resonant inductor, the frequency will shift accordingly. Assuming that the response of the inductance change to a step in the bias current is fast, and that the corresponding frequency correction will be done within one high frequency cycle, F_β can be assumed to follow I_{bias} with no delay and thus the large signal transfer function is given as:

$$K_f(L_r) = f_r = \frac{1}{2\pi \cdot \sqrt{L_{r(I_{bias})} C_r}} \qquad (7)$$

where, f_r is the resonance frequency of the PPRI, $L_{r(Ibias)}$ is the resonant inductance value and C_r is the capacitance reflected to the secondary ($C_2(n_2/2n_1)^2 + C_3 + C_L$). The block $K_f(L_r)$ (Fig. 2a) can thus be defined as behavioral dependent voltage source (Fig. 7). Notice that in the SPICE realization $L_{r(Ibias)}$ is emulated by the voltage of the node 'ind' (V(ind), Fig. 6) as was described previously at the non-linear inductor section.

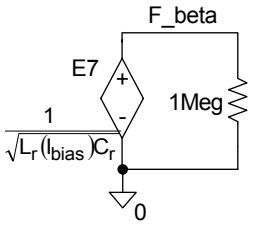

Figure 7. Behavioral model of the resonant tank.

(b) Small Signal Model. A derivation of $K_f(L_r)$ around the operating point (considering $L_{r(Ibias)}$ constant) yields the small signal transfer function of the resonant tank, k_f:

$$k_f = \left.\frac{df_r}{dL_r}\right|_{L_{r(Ibias0)}} = -\frac{1}{2L_{r0}} f_r \qquad (8)$$

where L_{r0} is the resonant inductor value around the operating point (denoted by the subscript 0) which was determined by the bias current.

Current Loop. The inner current feedback is built around the buck converter (B in Fig. 2a) to reduce the order of the system to a first order. The feedback is implemented by sensing the switch current of the buck converter with a current transformer, filtering the signal by an R-C network and feeding the signal back to the summing amplifier A1 (Fig. 1). The current loop was thoroughly investigated earlier [1] for both large and small signals, here we focus on the SPICE realization of the current feedback components.

Pulse Width Modulator. (a) Large Signal Model. The on-time of the buck converter is determined in every switching cycle by comparing the error signal, V_e to a saw-tooth waveform (Fig. 8a), therefore the large signal duty cycle, D is determined by the function $K_M(V_e)$:

$$D = K_M(V_e) = \frac{V_e - V_1}{V_2 - V_1} \qquad (9)$$

where, V_1 and V_2 are the saw-tooth wave boundaries which can be obtained from datasheet [8].

The block $K_M(V_e)$ can be realized in SPICE as a behavioral dependent voltage source (Fig. 8b) and can be used as is for both large and small signal simulation.

(b) Small Signal Model. Taking the derivative of $K_M(V_e)$ around the operating point and after some manipulations, the small signal TF of the PWM, k_M, is expressed as:

$$k_M = \frac{d}{v_e} = \frac{1}{V_2 - V_1} \qquad (10)$$

Buck Converter. (a) *Large Signal Model.* The converter is used to feed the bias winding of the variable inductor to achieve changes in the resonance frequency [1]. It is realized in SPICE by compatible behavioral average model [7] (Fig. 9a) and the TF of interest is the bias inductor current which is given by:

$$I_{bias} = D \cdot B \qquad (11)$$

where, D is the duty cycle and B is the large signal TF of the buck converter (Fig. 2a).

Furthermore, one has to take into account that the value of the inductance of the bias winding L_b (Fig. 1a), that is, the Buck inductor, is changing as a function of the bias current. This was taken into account by making the inductor a function of the bias current (Fig. 9) [13]. The expressions of the dependent source that emulate the non-linear inductor of the bias winding are:

$$E6 = V_{pr} \frac{1}{f(I_{bias})} \qquad (12)$$

$$G2 = I_{sec} \qquad (13)$$

where, I_{sec} and V_{pr} are as marked on Fig. 9b and $f(I_{bias})$ is the dependence of the inductance on the bias current (given as a table in ETABLE).

(b) Small Signal Model. The small signal TF of the buck converter is:

$$b = \frac{i_{bias}}{d} = \frac{V_{in}}{sL_{b0}} \qquad (14)$$

where, V_{in} is the input voltage of the buck converter and L_{b0} is the inductance of the bias inductor at the operating point.

In these analytical expressions we assume that L_b is constant around the operating point. This is, we neglect the second order effect on 'b' resulting from the fact that a perturbation around the operating point will also generate a small signal L_b that will affect 'b'.

Pulse Transformer and Feedback Filter. The feedback is designed to close the loop on the bias winding current regulator in order to stabilize the current loop and thus to reduce the overall order of the system [1]. The filter (H_2, Fig. 2a, h_2, Fig. 2b) is implemented in SPICE by a paralleled RC network fed by a behavioral dependent current source (Fig. 10).

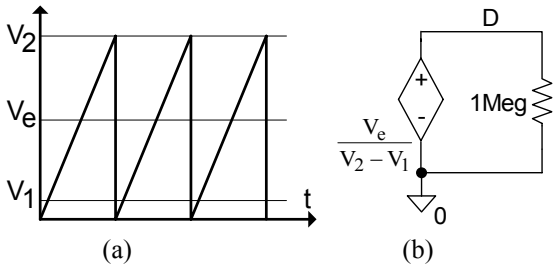

Figure 8. PWM operation. (a) cycle-by-cycle and (b) behavioral model.

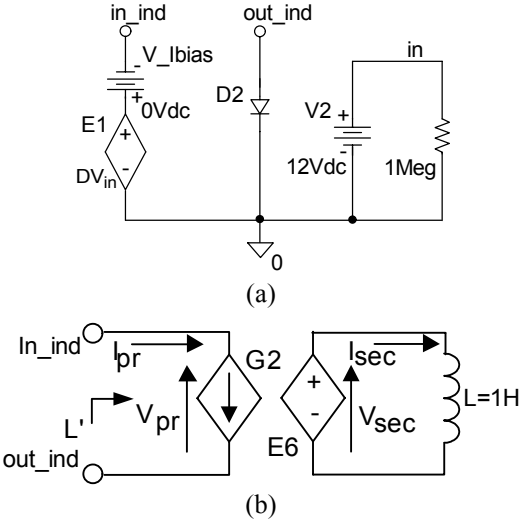

Figure 9. Behavioral average model of the Buck converter (a) that includes a variable inductor (b).

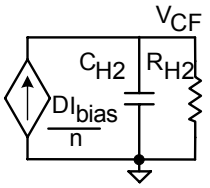

Figure 10. The current feedback circuitry including the current transformer.

The current source represents the current of the buck converter which in this case is sensed at the switch branch via a pulse transformer (T, Fig 2a) and thus the additional TF of $D*I_{bias}/n$ (duty cycle, D, times the inductor current, I_{bias}, and divided by the pulse transformer turns ratio, n) is included in Fig. 10. The filter R_{H2}, C_{H2} replicates the actual network of the circuit.

The considerations for the time constant selection of the RC network were discussed earlier in [1].

IV. ANALYTICAL, SIMULATION AND EXPERIMENTAL VERIFICATION

The simplified small signal block diagram of the SA-CFPPRI that is shown in Fig. 2b is achieved as a result of local linearization and derivation over the large signal block diagram (Fig. 2a) as described in the previous chapter. After the relations of every module were established, the expressions for the closed loop transfer functions of the system may be realized. The current feedback closed loop transfer function is expressed as:

$$A_{CF\_CL}(s)=\frac{i_{bias}}{v_f}=\frac{g_1 k_M b}{1+g_2 k_M cf} \qquad (15)$$

where, g_1 and g_2 are the gains of the summing amplifier A_1 (Fig. 1), k_M is the PWM transfer function, b is the transfer function of the buck converter and cf [1] is the transfer function of the buck converter in series with its output filter h_2 and the current transformer T, which is given by:

$$cf(s)=\frac{v_{CF}}{d}(s)=\left[\frac{V_{in}}{sL_{b0}}\right]\left[\frac{D_0 R_{H2}}{n}\left[s\left(\frac{L_{b0}I_{bias0}}{V_{in}D_0}\right)+1\right]\frac{R_{H2}}{sC_{H2}R_{H2}+1}\right] \qquad (16)$$

where, R_{H2}, C_{H2} are the network component of the current feedback filter H_2 of Fig. 10, D_0 and L_{b0} are the duty cycle and bias inductance for a given operating point, respectively.

After some manipulations [1], the current feedback closed loop can be expressed as a first order system with a bandwidth of ω_{CL}:

$$A_{CF\_CL}(s)=\frac{A_{CL0}}{1+s/\omega_{CL}} \qquad (17)$$

where

$$A_{CL0}=\frac{n}{D_0 R_{H2}},$$

$$\omega_{CL}=g_2 k_M \frac{D_0 R_{H2}}{n}\frac{V_{in}}{L_{b0}}$$

Equation (17) implies that for the frequency range $\omega<\omega_{CL}$, the current feedback has transformed the buck converter (from error signal to bias current) to a zero order system. If the current loop is set that the bandwidth ω_{CL} is larger than the bandwidth of the overall system then the closed loop response of the system f_β/f_{in} $A_{PF\_CL}(s)$ can be expressed as:

$$A_{PF\_CL}(s)=\frac{f_\beta}{f_{in}}(s)=\frac{1}{s}\frac{A_{PF}}{1+\beta_{PF}A_{PF}} \qquad (18)$$

where

$$A_{PF}=k_p h_1 g_1 A_{CF\_CL} k_f h_L$$

$$\beta_{PF}=\frac{1}{s}$$

After some manipulation the closed loop transfer function of the system can be shown as a first order system of bandwidth ω_0:

$$A_{PF\_CL}(s)=\frac{1}{1+s/\omega_0} \qquad (19)$$

where

$$\omega_0=k_p h_1 g_1 A_{CF\_CL} k_f h_L$$

The SPICE compatible simulation model was compared to the results of the analytical expressions derived in this study. The excellent agreement that was obtained is demonstrated by comparing the inner (current) loop gain (Fig. 11) and the overall loop gain obtained by applying the analytical equations and by simulation (Fig. 12). To facilitate comparison between simulation and analytical results, the theoretical calculations were carried out by SPICE. This was accomplished by defining behavioral dependent sources in the frequency domain of ELAPLACE type, an example for ELAPLACE realization is shown in Fig. 13.

A very good agreement was also found between the simulation results and laboratory measurements on an experimental SA-CFPPRI for two cases of the closed loop response: (a) ac response, f_β/f_{in}, (Fig. 14) and (b) a step response (Figs. 15 and 16).

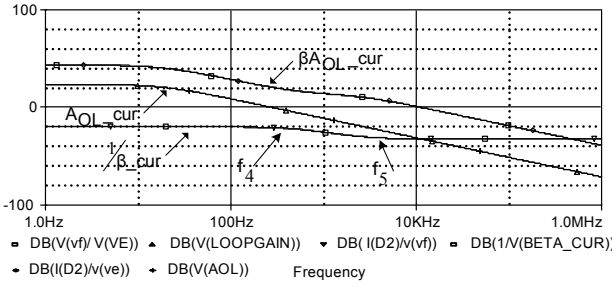

Figure 11. Simulated and calculated inner (current) loop gain (the two sets results coincide).

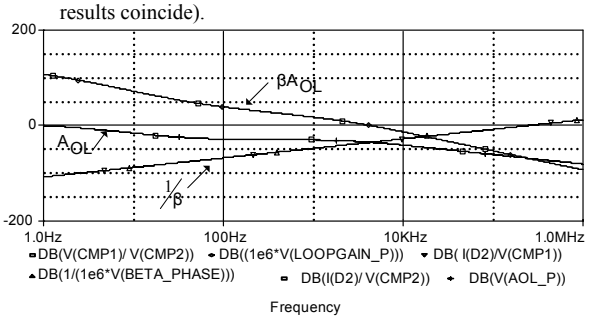

Figure 12. Simulated and calculated outer loop gain (the two sets results coincide).

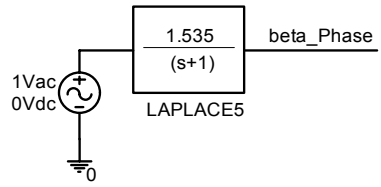

Figure 13. SPICE realization of the expression derived for the phase feedback of Fig. 11.

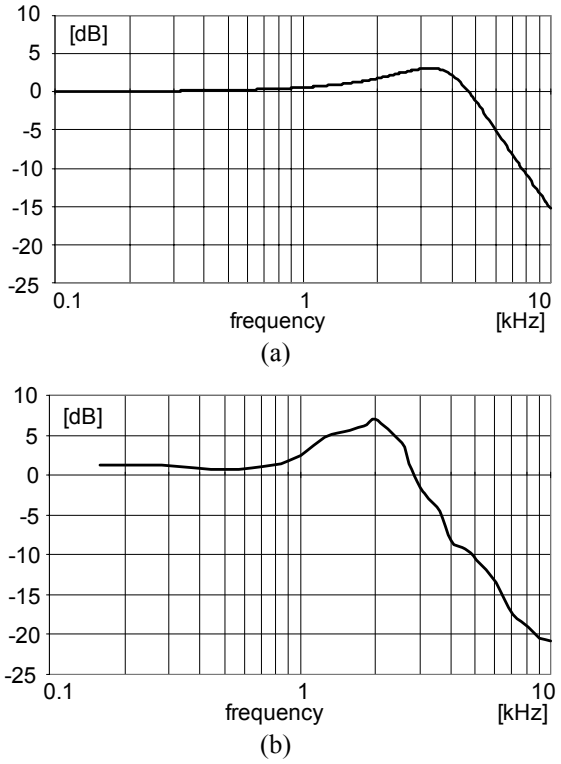

Figure 14. Calculated (a) and measured (b) overall closed loop response (f_β/f_{in}).

V. DISCUSSION AND CONCLUSIONS

The high level modeling methodology explored in this study is based on the powerful features of modern electronic circuit simulators and in particular behavioral dependent sources that include data driven sources such as ETABLE. The built-in linearization feature, that is transparent to the user, simplifies considerably the development of models for non-linear systems such as found in Power Electronics. The method was demonstrated on the SA-CFPPRI that includes a multitude of signals and non-linear elements such as current controlled inductors. It was shown that the behavior of a complex system such as the SA-CFPPRI could be easily obtained by emulating each non-linear section by a behavioral model that is based on dependent sources.

This study introduces a few new SPICE compatible models for modules that are often used in Power Electronics: phase comparator, a controlled non-linear inductor, resonant network that includes a controlled inductor and a Buck converter with current feedback via a pulse transformer that senses the switch current.

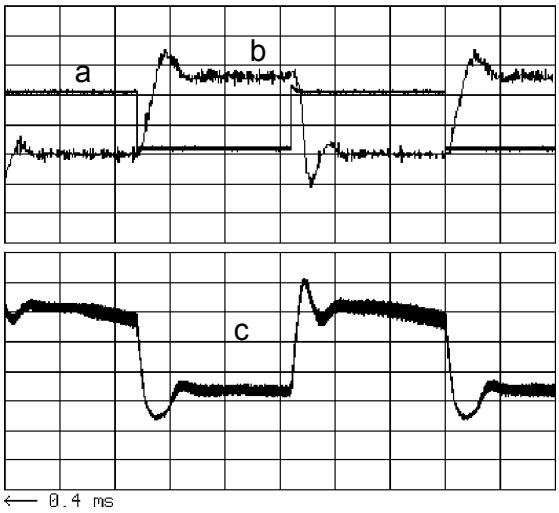

Figure 15. Measured response of experimental unit to a step in input frequency around 93 KHz (with output capacitance of 2.1 nF). (a) Modulating signal. (b) Output frequency change (1.56 kHz/div), was measured by the frequency jitter (Jfreq)feature of the Lecroy WaveRunner digital oscilloscope. (c) Error signal at the output of phase detector filter (H1) of Fig. 2a (20.5 mV/div). Horizontal scale: 1 (ms/div).

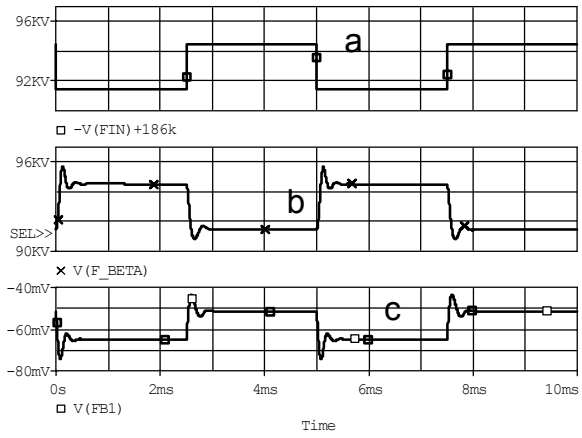

Figure 16. Simulated response of experimental unit to a step in input frequency around 93 KHz (with output capacitance of 2.1 nF). (a) Modulating signal. (b) Output frequency change. (c) Error signal at the output of phase detector filter (H1) of Fig. 2a.

The excellent agreement between the simulations, analytical calculations and experimental results suggest that the proposed method could be beneficial to the designers and researchers in Power Electronics.

It should be noted that the proposed model for the phase comparator is exact for modeling dynamic responses (time or frequency domain). For zero frequency (bias point calculation) the error signal at the input of the gain block of the phase comparator is a frequency difference rather than a phase difference. This is due to the fact that the input filter network is transparent to signal of low frequencies (below the break point of RC). However, since the gain factor of the comparator is large the steady state error signal will be small albeit, from the theoretical point of view, incorrect.

The present investigation further suggests that SA-CFPPRI can be controlled to follow a frequency under

(reactive) load variation. The design of the experimental unit demonstrated zero frequency error under a locked condition and a fast dynamic response of about 3kHz bandwidth that is ample in the intended applications of a piezoelectric motor driver [4,5]. PSPICE/ORCAD files (Evaluation version 9.2) of the system under study are available for download from http://www.ee.bgu.ac.il/~pel/download.htm**.**

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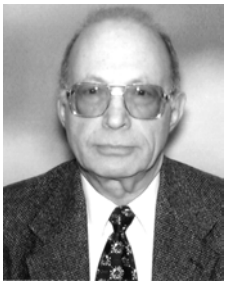

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