Time domain design of digital compensators for PWM DC-DC converters

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***Abstract*- A time-domain design method for digital controller of PWM DC-DC converters that was developed, tested by simulations and verified experimentally. The proposed approach is based on the fact that the closed-loop response of a digitally controlled system is largely determined by the first few samples of the compensator. This concept is used to fit a digital PID template to the desired response. The proposed controller design method is carried out in the time domain and thus, bypasses errors related to continuous to discrete domain transformation and discretization. Digital PID controllers for a Buck and Boost type converters were implemented experimentally on a TMS320LF2407 DSP core. The measured closed-loop attributes were 3.5KHz bandwidth and phase margin of 40° for the Buck converter, and 1.6 KHz and 40° for the Boost. Good agreement was found between the design goals and the experimentally determined response.**

I. INTRODUCTION

As digital control of PWM converters is turning to be more relevant, the need for effective and convenient design procedures for digital compensators is becoming apparent. Two general approaches have been described hitherto to tackle this task. The most popular one is the frequency domain based method [1]. Another design scheme proposes the use of MATLAB in a trial and error procedure based on pole-zero location in the z plane [2]. In as much that there is a theoretical relationship between the frequency domain and the sampled data domain (via the various transformation algorithms), a digital compensator operates, in reality, in the sampled data domain and the notions of phase margin, bandwidth and the like are alien to the finite difference equation algorithm that is implemented on the digital platform. The digital compensator, in fact, handles in each computational event only few samples of error signals and previous results, so basically all relevant information is short lived around the sampling instance. One can find an analogy between this situation and the frequency domain case. In the latter, the relevant feedback information is around the cross over frequency of the loop-gain. In the time domain case, all relevant feedback data is around each sampling event. That is, in the frequency domain case, the behavior of the system at frequencies that are higher or lower than the cross over frequency, is unimportant to a large extent. Analogously, in the time domain case, information at times other than the vicinity of the sampling instance is irrelevant. Putting it in other words, the digital compensator handles only a handful of adjacent data points and is blind to all other samples prior to the sampling event. It follows then, that the algorithm of the compensator (that is implemented as finite difference equations) can be based on the short-term time response of the system rather than on the full response, which in many design procedures is derived from the frequency domain response.

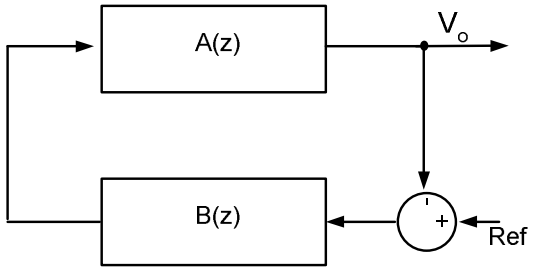

Figure 1. Basic feedback system.

The objective of this work was to test the above conjecture by developing and testing a design procedure of a digital compensator for PWM DC-DC converters that is based on the short-term time responses of the system. The motivation for this effort stems from the underlying assumption that such digital compensator design methods could provide not only a more natural and streamlined approach, but could lead to better designs and improved performance of the system in closed loop.

II. THEORETICAL CONSIDERATION

The precursor of proposed design method is the Ragazzini-Franklin method [3] - [4] in which the compensator B(z) is derived form the known open loop response of the plant (A(z)) and the desired closed loop response ($A_{CL}(z)$) [5]. This is demonstrated by considering the basic feedback system of Fig. 1. Since

$$A_{CL}(z) = \frac{A(z)B(z)}{1 + A(z)B(z)} \tag{1}$$

then

$$B(z)_{ideal} = \frac{A_{CL}(z)}{1 - A_{CL}(z)} \frac{1}{A(z)} \tag{2}$$

The disadvantage of this method is that it may end up with a high order compensator (poles and zeros) that would translate into many terms in the compensator's difference equation and hence a long computation time.

Another issue that needs to be resolved is the specification of (ACL(z)). In most DC-DC converters the relevant closed loop response is the step response rather than the frequency domain transfer function from which (ACL(z)) is normally derived by say, s to z transformation. Here we propose to extract ACL(z) from the time domain response. The proposed procedure includes two steps. The first is to specify the characteristic equation of (ACL(z)) through time domain parameters. This could be achieved by considering the typical response of a closed loop system with phase margin smaller than 500. The closed loop response in this case will behave like a second order system (see for example [6]). The denominator (characteristic equation, CE(s)) can be described by the conventional template

$$CE(s) = \frac{s^2}{\omega_n{}^2} + \frac{s}{\omega_n Q} + 1 \tag{3}$$

where ω_n is the angular resonant frequency and Q is the quality factor. For this dynamic system, the rise time t_r and the overshoot M_p can be expressed as [3]

$$t_r \approx \frac{1.8}{\omega_n} \tag{4}$$

and

$$M_p = e^{\frac{\pi}{2Q}\Big/\sqrt{1-\frac{1}{4Q^2}}}. \tag{5}$$

That is, the angular resonant frequency and the quality factor can be expressed as

$$\omega_n \approx \frac{1.8}{t_r} \tag{6}$$

$$Q = -\frac{\sqrt{1+\left(\frac{\ln(M_p)}{\pi}\right)^2}}{2\frac{\ln(M_p)}{\pi}} \tag{7}$$

Equations (6) and (7) provide a way to define the characteristic equation of $A_{CL}(s)$ as a function of the desired rise time and overshoot. Once the time domain response of A_{CL} is set, the denominator of $A_{CL}(z)$ can be obtained by one of the s to z transformations. The second step of the $A_{CL}(z)$ derivation procedure is to set the numerator such that the closed loop response will be of a second order nature [3], [7]. That is, to obtain the form of $A_{CL}(z)$ such that the closed loop system will: (a) be casual, (b) have zero error in steady state to step perturbation and (3) have a constant error to a ramp signal. This set of rules is commonly known as "Truxal-rules" [3], [7] and can be obtained by the followings constraints

$$A_{CL}(z)\big|_{z=\infty} = 0 \tag{8}$$

$$A_{CL}(z)\big|_{z=1} = 1 \tag{9}$$

$$\frac{dA_{CL}(z)}{dz}\bigg|_{z=1} = \frac{1}{K_V} \tag{10}$$

Following the above procedure one can derive from (2) the transfer function of the compensator B(z) that will yield the desired rise time t_r and over shoot M_p (i.e. $A_{CL}(z)$) for a given power stage A(z)). The compensator that will be derived is an "ideal" compensator in the sense that will reproduce the exact ($A_{CL}(z)$) that was prescribed.

Examination of the step response of a typical B(z) compensator (Fig. 2) suggest that many function, aside from the ideal B(z) would do the job. The reason is (as already pointed out in the Introduction section) that in reality, the compensator is concerned only with the data points around the sampling instance. Hence, the behavior of the compensator after more than, say, 3 steps is irrelevant. This implies that any transfer function that will reproduce the first few samples of the step response of the ideal B(z) will also be capable of reproducing the same (or at least close to) $A_{CL}(z)$. This concept was pursued in the proposed compensator design method.

III. The Proposed Method

The proposed design procedure follows three basic steps:

1. Deriving the ideal compensator from the specified rise time t_r and overshoot M_p based on knowledge of A(z). Namely, deriving B(z) from (2) after the closed loop response was set by following Eqs. (3) to (10).
2. Obtaining the step response of the ideal B(z).
3. Curve fitting a given compensator's template to the first few samples of the step response.

Among the possible templates of compensators for PWM DC-DC converter, the popular PID comes to mind as a candidate that has a long proven track record. This was the approach adopted in this study.

Applying the matched pole-zero method [3] the continuous template of the PID compensator

$$\frac{V_c(s)}{V_e(s)} = \frac{\frac{s^2}{\omega_c{}^2} + \frac{s}{\omega_c Q} + 1}{s} \tag{11}$$

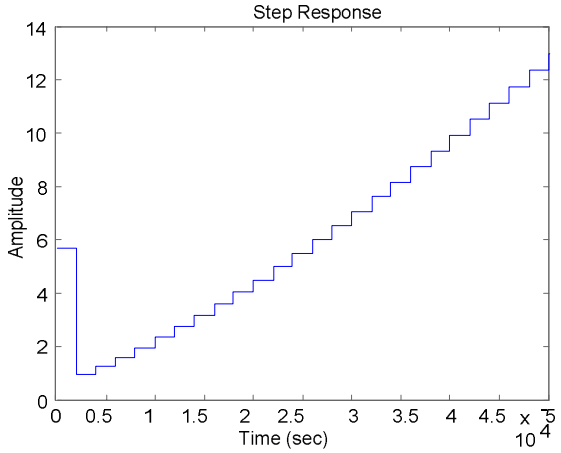

Figure 2. Step response of the 'ideal' B(z) compensator

is translated into the discrete z domain transfer function

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{z^{-1} - z^{-2}} \tag{12}$$

In sampled-data systems, the time interval between sampling the output and updating the control signal (V_c) which, in the case under study is the duty-cycle command, depends on: A/D acquisition time, conversion period and computational delays. This time interval can be approximated to one sampling cycle delay [1], [2], [5], [11] (i. e. Z^{-1}) and is taken into account when combined with (12)

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}} \tag{13}$$

This relationship can be described by the difference equation

$$V_c[n] = V_c[n-1] + aV_e[n] + bV_e[n-1] + cV_e[n-2] \tag{14}$$

The three coefficients (a, b, c) can now be calculated by indexing and solving (14) for the first three samples

$$\begin{bmatrix} V_c[0] & -0 \\ V_c[1] & -V_c[0] \\ V_c[2] & -V_c[1] \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{15}$$

where the indices, 0, 1, 2 stand for the first three samples of the output of the ideal B(z) compensator for the step input: 1, 1, 1.

IV. Example

The following example illustrates the proposed digital compensator design method. Assuming:

A. A Buck type converter power stage described by

$$A(s) = \frac{3.333 \cdot 10^8}{s^2 + 2500\,s + 1.333 \cdot 10^8} \tag{16}$$

B. Required closed loop time domain performance

t_r=100μS ; M_p=10%

The first step would be to transform A(s) to A(z) by the ZOH transformation

$$A(z) = \frac{0.06548\,z + 0.06459}{z^2 + 1.908z + 0.96} \tag{17}$$

It should be noted that in practical sampled-data systems, the acquisition of the feedback signal which is in present design the output voltage, is obtained by sample and hold operation and an A/D converter. Also, the duty-cycle command is held throughout the sampling interval and is updated (if needed) only at the beginning of a new command cycle. Thus, the appropriate transformation method to be used for A(z) is ZOH.

Next, t_r and M_p are used to calculate ω_n and Q (by (6), (7)) that define the characteristic equation of $A_{CL}(s)$ (3)

$$CE(s) = 3.086 \cdot 10^{-9}\,s^2 + 1.1 \cdot 10^{-3}\,s + 1 \tag{18}$$

To properly specify the closed loop response in the discrete domain ($A_{CL}(z)$), we follow the rules of section II. The discrete equivalent of (18) is extracted by applying one of the s to z transformations (here we used the normalized matched p-z [3])

$$CE(z) = z^2 - 1.401\,z + 0.4933 \tag{19}$$

The reason that either of the transformation methods is applicable at this point is that, as opposed to (17), the form or values of CE(z) are not restricted by the design and thus, does not need to be further approximated to any sampled signal. That is, since the entire compensation operation (from error to control) is obtained in the discrete domain, the mathematical manipulations to extract B(z) are free from practical constraints as long as the conditions set by (6) and (7) are satisfied. In the event that the parameters of CE(z) change, either due to specifications changes or due to different transformation, the values of the derived compensator will vary accordingly.

The second step of $A_{CL}(z)$ derivation is extracting the numerator. For proper design, the order of the numerator must not exceed the order of CE(z) [3] thus $A_{CL}(z)$ will be of the form

$$A_{CL}(z) = \frac{n_0 z^2 + n_1 z + n_2}{z^2 + d_1 z + d_2} = \frac{n_0 z^2 + n_1 z + n_2}{z^2 - 1.401\,z + 0.4933} \tag{20}$$

where d_1 and d_2 are the denominator coefficients extracted in (19), and n_0, n_1, n_2 are the numerator coefficients to be found by applying (8) to (10).

Eq. (8) forces causality by dictating that the system will not contain zeros at infinity. Setting n_0 to zero will satisfy this term.

In order to extract n_1 and n_2 we apply (9) and (10) on (20) and solve

$$\begin{matrix} n_1 + n_2 = 1 + d_1 + d_2 \\ n_1 + 2n_2 = (1 + d_1 + d_2)(1 + d_1 + 2d_2) \end{matrix} \rightarrow \begin{matrix} n_1 = 0.5067 \\ n_2 = -0.4148 \end{matrix} \tag{21}$$

The resulting discrete closed loop transfer function, $A_{CL}(z)$, is

$$A_{CL}(z) = \frac{0.5067\,z - 0.4148}{z^2 - 1.401\,z + 0.4933} \tag{22}$$

A(z) and $A_{CL}(z)$ are then used to express B(z) (2)

$$B(z) = \frac{0.5044z^3 - 1.375\,z^2 + 1.271z - 0.3958}{0.06548\,z^3 - 0.1249\,z^2 + 0.05945\,z} \tag{23}$$

This expression can now be used to obtain the step response of the ideal compensator. This could conveniently be done by MATLAB using the function: [Vc_data] = step(B). Since B(z) was already assigned to the step function as a discrete function, the time steps are automatically adjusted to the sampling period (20μS) [8].

Once the vector of the response (Vc_data) is evaluated, the PID coefficients (a, b, c) are calculated to be:

a= 3.4; b=-6.15 ; c= 2.93

Comparison between the step responses of the proposed compensator and that of the ideal compensator shows (Fig. 3) a good fitting for the first three steps, which was the objective of the fitting. More importantly, the system's closed loop step response with the proposed compensator is very close to the response with the ideal compensator (Fig. 4).

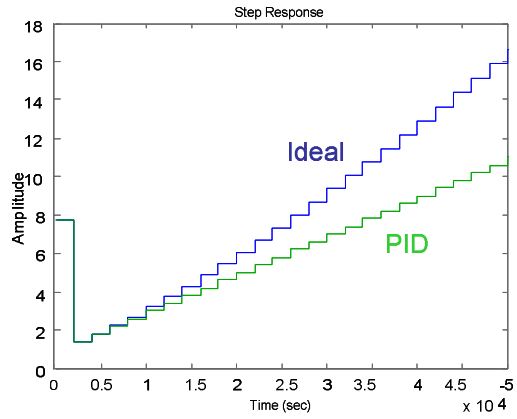

Figure 3. Step responses of the 'ideal' compensator and the proposed PID compensator.

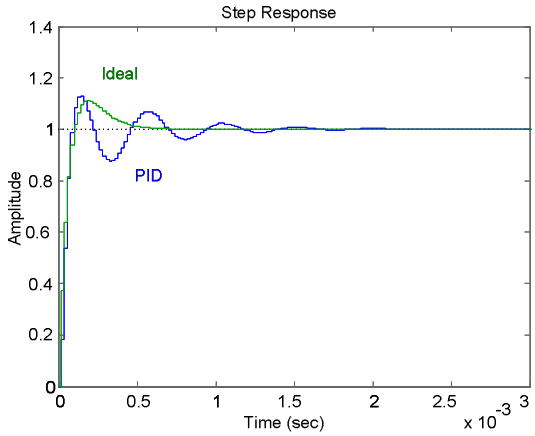

Figure 4. Closed loop step responses of a system controlled by 'ideal' compensator and proposed PID compensator.

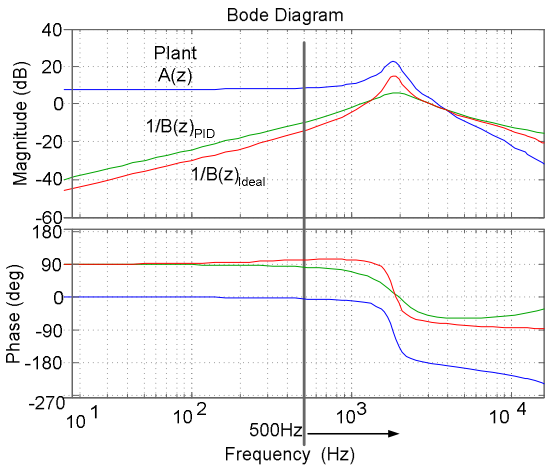

Figure 5. Frequency response of plant, 'ideal' compensator and PID compensator.

An interesting insight into the performance of the proposed compensator can be obtained by reconstructing the frequency domain of the responses (Fig. 5). It can be observed that $1/B(z)_{PID}$ crosses A(z) nearly at the same frequency as $1/B(z)_{ideal}$. However, the phase of the PID network is slightly lagging with reference to the ideal compensator. This implies that for a given set of design specifications, systems that are controlled by either the ideal compensator or by PID will have the same bandwidth, but with modest phase margin when controlled with PID. In time domain terms, both system will produce the same overshoot and respond with the same rise time, however, the PID controlled system will decay somewhat slower, yet still acceptable, as can be observed in Fig. 4.

V. Experimental

The experimental converter (Fig. 6) was controlled by a TMS320F2407 DSP evaluation board (Texas instruments) [9] - [10]. Input voltage was 15V, output voltage 5V, sensing gain 1/7, and switching frequency and sampling rate were 50KHz. The A/D resolution was 6.4 mV/bit; the resolution of the DPWM was 9 bits. Following the proposed design procedure, the digital PID compensator was derived for two cases. A relatively slow response $B_S(z)$: tr=500μS; M_p= 0; and a faster response $B_F(z)$: tr=100 μS; M_p=10%. The compensators were found to be

$$B(z)_S = \frac{1.52 - 2.81z^{-1} + 1.38z^{-2}}{1 - z^{-1}} \tag{24}$$

and

$$B(z)_F = \frac{3.4 - 6.15z^{-1} + 2.93z^{-2}}{1 - z^{-1}} \tag{25}$$

Figs. 7 and 8 show a very good agreement between experimental closed loop responses and simulation results. The experiment objective was to change the reference values from 110 to 130 (digital values), such that the output voltage is changed from 5V to 6V, respectively. The responses to a load step change from 1A to 1.5A are given in Figs. 9, 10. The loop-gain of the system with the "Fast" compensator design was measured with a HP4395A network analyzer (resolution measurement of 10Hz). The measured loop-gain (Fig. 11) was found to match the one predicted by simulation (Fig. 5). The measured bandwidth and phase margin were 3.5KHz and 40^0 respectively.

The proposed compensator design method can be improved by applying an experimentally derived small signal model of the Buck and Boost converters rather than using the theoretical response that may not include all the parasitic effects. This was accomplished by applying a newly developed time domain based parametric identification procedure.

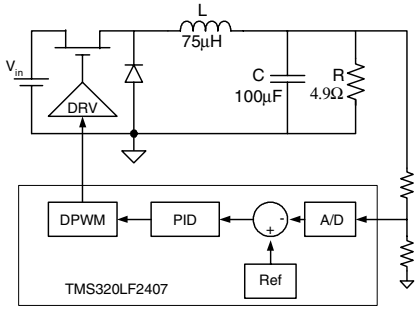

Figure 6. Experimental setup

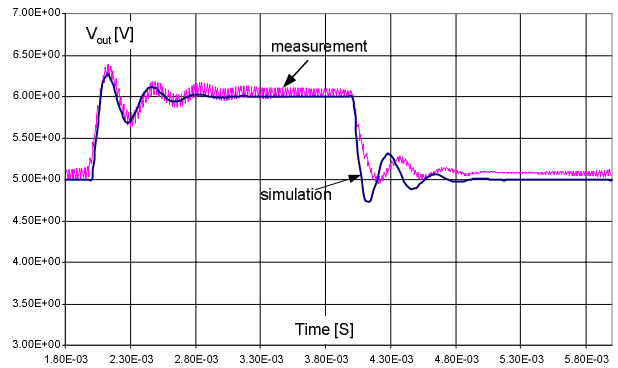

Figure 7. Comparison of simulation and experimental output voltage step response for a step in reference (5V to 6V). Faster compensator ($B(z)_F$).

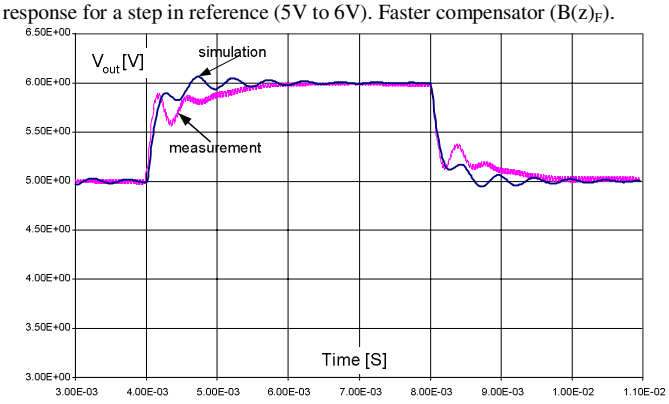

Figure 8. Comparison of simulation and experimental output voltage step response for a step in reference (5V to 6V). Slower compensator ($B(z)_S$).

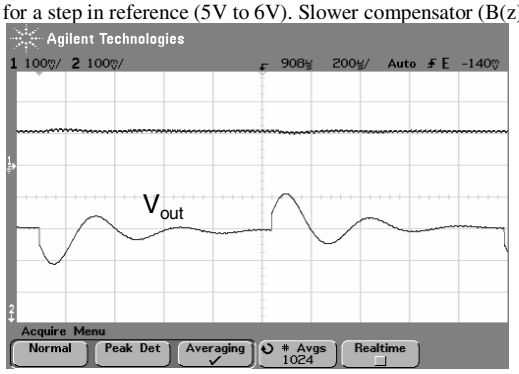

Figure 9. Experimental result of output voltage response to a load step (1A to 1.5A). Closed loop Buck converter with the faster compensator ($B(z)_F$). V_{out} (100mV/div). Horizontal scale (200µS/div)

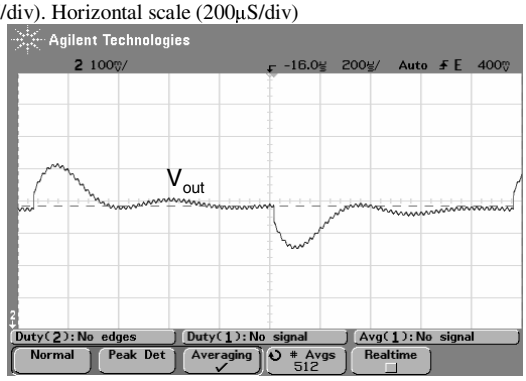

Figure 10. . Experimental result of output voltage response to a load step (1A to 1.5A). Closed loop Buck converter with the slower compensator ($B(z)_S$). V_{out} (100mV/div). Horizontal scale (200µS/div)

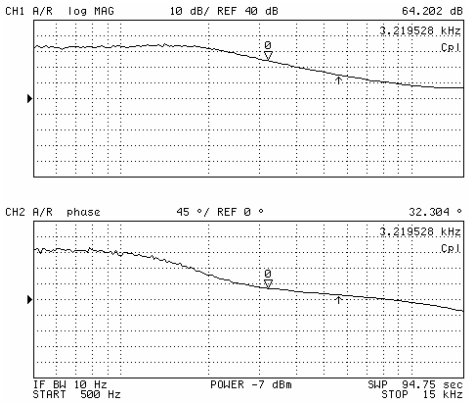

Figure 11. Experimental Loop gain of the system when controlled by the faster compensator ($B(z)_S$).

The features of this identification method are: that is a straightforward, one stage, procedure with no need for further data manipulation or transformation, it requires a relatively small number of data samples for successful identification and it utilizes a generic template for all PWM topologies. A complete description of the identification method is beyond the scope of this paper and will be detailed in subsequent publication.

The parameters of the Buck stage were: Input voltage: 15V, output voltage: 5V, sensing gain: 1/7, load current: 1ADC, switching frequency and sampling rate: 50 KHz, L=75µH (R_L=250mΩ), C=100µF (ESR=300mΩ), switch-on resistance (IRF640): 0.18Ω, diode forward voltage (1N5822): 0.5V. The identified discrete time Buck transfer function ($A_{Buck\_ID}(z)$) was found to be

$$A_{Buck\_ID}(z) = \frac{0.04285z - 0.01426}{z^2 - 1.753z + 0.8028}. \quad (26)$$

Two PID compensators were designed to achieve: a relatively slow response (t_r=500µS, Mp=0)

$$B(z)_{Buck\_S} = \frac{3.74 - 6.357z^{-1} + 2.85z^{-2}}{1 - z^{-1}} \quad (27)$$

and a faster response PID (t_r=150µS, Mp=10%)

$$B(z)_{Buck\_F} = \frac{14.683 - 22.962z^{-1} + 9.692z^{-2}}{1 - z^{-1}} \quad (28)$$

Figs. 12 and 13 show the experimental closed loop step responses compared with simulation results. The reference values were changed from 110 to 130 (digital values), such that the output voltage was stepped from 5V to 6V. Very good agreement is observed.

The parameters of the Boost stage were: Input voltage: 10V, output voltage: 16V, sensing gain: 1/7, load current: 0.3ADC, switching frequency and sampling rate: 20 KHz, L=300µH (R_L=350mΩ), C=100µF (ESR=300mΩ), switch-on resistance (IRF640): 0.18Ω, diode forward voltage (1N5822): 0.5V. The identified discrete time Boost transfer function ($A_{Boost\_ID}(z)$) was found to be

$$A_{Boost\_ID}(z) = \frac{0.2526z - 0.197}{z^2 - 1.866z + 0.8844}. \quad (29)$$

The slow closed-loop response PID controller (t_r=1000μS, Mp=0) was

$$B(z)_{Boost\_S} = \frac{1.91 - 3.379z^{-1} + 1.528z^{-2}}{1 - z^{-1}} \quad (30)$$

and the faster response PID (t_r=400μS, Mp=10%) was found to be:

$$B(z)_{Boost\_F} = \frac{2.287 - 3.122z^{-1} + 1.03z^{-2}}{1 - z^{-1}}. \quad (31)$$

The excellent agreement between the experimental closed loop step responses and simulation results for both controller cases is depicted in Figs. 14 and 15. The reference values were changed from 350 to 400 (digital values), to cause a change from 16.3V to 18.7V at the output.

VI. Discussion and Conclusions

The proposed design procedure of a digital compensator for a PWM DC-DC converter follows the concept, developed in this study, of local behavior of discrete compensators. The basic idea behind this concept is that the system's closed loop response is largely determined by the first few samples of the step response of the compensator. Based on this conjecture, many templates can be fitted to approximate the 'ideal' compensator (as defined in this paper). In this study we explored the possibility of applying a PID template in proposed design procedure. The proposed compensator derivation method relies entirely on the discrete domain and does not involve any transformation-related approximations. Thus, the extracted compensator can be considered more accurate in the sense that it produces the exact design specifications that were prescribed.

The simulation and the experimental results confirm the viability of the proposed design method. The proposed method can thus be a good candidate for an alternative approach to the design of digital compensators for PWM DC-DC converters.

The (continuous) average model of the converter can be used to model the open loop small signal response of the plant A(z). When transformed into the z domain, it will be corrupted by the fact that inherent inaccuracy of the transformation as well as numerical errors such truncation errors. An alternative way to obtain A(z) is by a system identification procedure that applies experimental data. By doing so, all parasitic effects (e. g. R_L, ESR, R_{ds_on}, V_{Don}, etc.), quantization gains (A/D and DPWM) and delays are taken into account and do not need to be estimated. Hence, it should lead to a more accurate controller design.

Comparison between PID controllers derivation based on average models and identified models of the plant, supports the above conjecture. It was found that PID compensators that were extracted based on the identification produce better dynamic results in closed loop, especially in the slow rise time (i. e. low BW) cases and the resulted closed loop responses were found to be emulated more accurately by simulation.

Comparison between the simulated performances of the ideal compensator and the PID shows that the latter might suffers from slightly longer settling periods. This is probably due to the modest gain obtained by the integrator part at lower frequencies. On the other hand, it was made worth-while to avoid the practical drawbacks of the 'ideal' compensator such as: complicated compensator implementation, long computational intervals and potential steady state ringing due to staggering zeros.

It should also be noted that due to the relatively low switching frequency (and sampling rate) used in the experimental part of this paper, the absolute closed loop attributes of the results may seem modest when compared to other published digital control examples where the switching frequency were in the region of hundreds of KHz to over 1MHz. Obviously, the proper criterion for evaluating the performance is the ratio between the crossover frequency and the switching frequency that, in present design, is measured to be 1:12.5, which is compatible with the majority of digital feedback designs that were carried out by other methods [1], [11], [12].

The potential advantages of the proposed method are the fact that it is carried out in the time domain (and hence bypasses some of the errors due to the s to z transformation) and that it is does not involve a trial and error procedure.

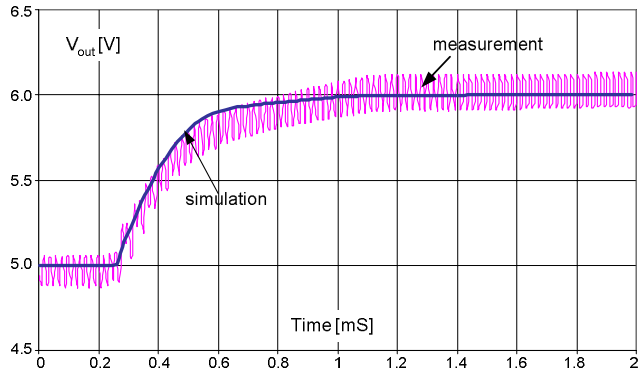

Figure 12. Comparison of simulation and experimental closed loop Buck converter response a step in reference voltage (5V to 6V). Controller design was based time domain identification of the plant's response. Slower compensator ($B(z)_{Buck\_S}$).

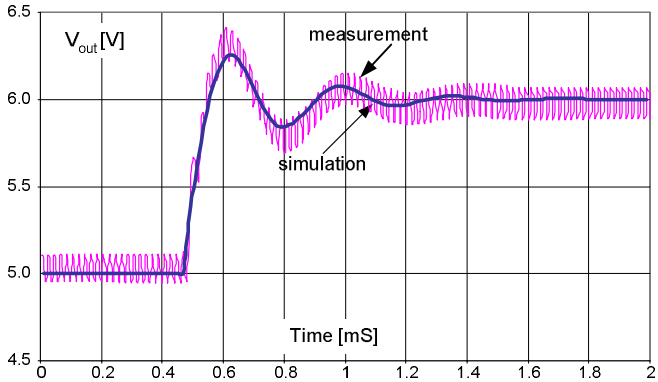

Figure 13. Comparison of simulation and experimental closed loop Buck converter response a step in reference voltage (5V to 6V). Controller design was based time domain identification of the plant's response. Faster compensator ($B(z)_{Buck\_F}$).

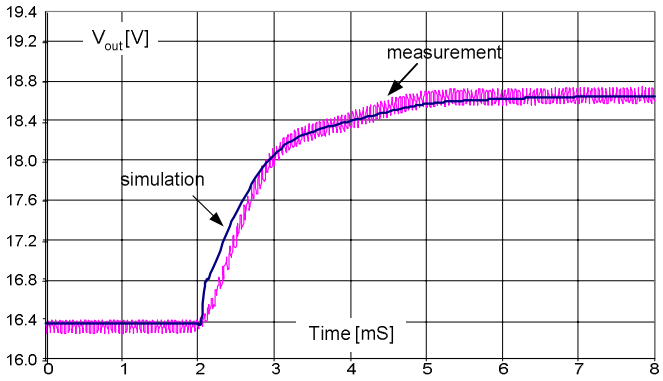

Figure 14. Comparison of simulation and experimental closed loop Boost converter response a step in reference voltage (16.4V to 18.7V). Controller design was based time domain identification of the plant's response. Slower compensator ($B(z)_{Boost\_S}$).

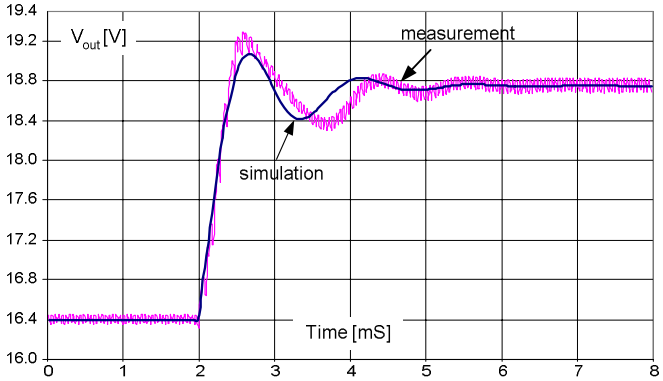

Figure 15. Comparison of simulation and experimental closed loop Boost converter response a step in reference voltage (16.4V to 18.7V). Controller design was based time domain identification of the plant's response. Faster compensator ($B(z)_{Boost\_F}$).

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