A Novel Time-Domain Based Design of PWM Controllers for Switch-Mode Converters and its Implementation by the C2000 DSP Family

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Abstract

A new time-domain design method for digital controller of PWM DC-DC converters that was developed, tested by simulations and verified experimentally. The proposed approach is based on the fact that the closed-loop response of a digitally controlled system is largely determined by the first few samples of the compensator. This concept is used to fit a digital PID template to the desired response. The proposed controller design method is carried out in the time domain and thus, bypasses errors related to continuous to discrete domain transformation and discretization. Digital PID controllers for a Buck and Boost type converters were implemented experimentally on a TMS320LF2407 DSP core. The code for the proposed PID control law was realized by assembly code to minimize the run time of the controller. Good agreement was found between the design goal, simulation and the experimentally determined response.

1. Introduction

Switch-mode power systems normally operate in closed-loop to achieve a regulated desired output, stable operation and desired dynamic performance [1]. Currently, the majority of applications apply analog controllers mostly due to its cost-effectiveness. Following the rapid growth of digital technology and the resulting lower cost of digital control and computation power, the integration of digital controllers in power applications has become a viable alternative. Also, modern power management systems are likely to include a digital platform (microcontroller or DSP) for data logging, user interfacing, communication and other 'house-keeping' tasks. Thus it would be highly advantageous to incorporate the compensation into the already existing digital platform. To facilitate this, a simple control algorithm, with reasonable consumption of memory space and computation resources would be advantageous, to leave sufficient computation time for the DSP to perform the other auxiliary chores.

The traditional approaches used to design a digital controller are based on the frequency domain and involves trial and error procedure [2-4]. That is, known control transfer functions are transformed from analog (linear) into a digital equivalent using one of the s to z transformations. This approach has two severe disadvantages: at best, the performance of the digital controller will approach that of the analog one (and will not be better) and secondly, to achieve a comparable control bandwidth one would need extremely high clock frequencies which will make the digital controller prohibitive economically.

In as much that there is a theoretical relationship between the frequency domain and the sampled-data domain, a digital compensator operates, in reality, in the time domain. The notations related to the frequency domain, such as phase margin and bandwidth, are artificial in the context of the finite difference equation algorithm that is implemented on the digital platform. In fact, the digital compensator handles only few samples of the error signals and previous results in each computational event (sampling instance) and hence, all the relevant information is short lived around the sampling instance.

In the light of the above observation, this study proposes a new direct digital design method that is based on short term responses, characterized by time domain parameters and simplifies the controller implementation on the digital platform by cutting down a large portion of the computational resources needed to perform the control algorithm.

2. The Proposed Method

The precursor of the proposed design method is a direct extraction method [4, 5] in which the compensator B(z) is derived form the known open loop response of the plant (A(z)) and the desired closed loop response ($A_{CL}(z)$) [6]. This is demonstrated by considering the basic feedback system of a compensator B(z) which is in series with a plant A(z) and closed by a unity feedback. Since:

$$A_{CL}(z) = \frac{A(z)B(z)}{1 + A(z)B(z)} \qquad (1) \qquad \text{then} \qquad B(z)_{ideal} = \frac{A_{CL}(z)}{1 - A_{CL}(z)} \frac{1}{A(z)} \qquad (2)$$

The resultant compensator is referred to as 'ideal' in the sense that it will reproduce the exact closed loop response that was prescribed. The major shortcoming of this procedure is that the derived compensator would be of high order (poles and zeros) that in turn translates into many terms of the difference equation and hence, long computation time and memory space to store the computation records, and that the compensator's template will depend of the system. Examination of the step response of a typical B(z) compensator (Fig. 1) suggests that many other controller templates aside from the ideal B(z) can generate a similar response. This conjecture is based on the fact, already pointed above, that the compensator is primarily concerned with data points around the sampling instance. That is, the behavior of the compensator beyond its highest order is presumably less significant, and thus any transfer function that will reproduce the first few samples of the response of the ideal B(z) might be considered a good candidate for reproducing the same as (or at least close to) the desired $A_{CL}(z)$. Among the possible templates of compensators for PWM DC-DC converter, the popular PID comes to mind as a candidate that has a long proven track record. This was the approach adopted in this study. Based on the above, the proposed design procedure follows three basic steps:

1. Extracting the ideal compensator from the given specification of the power stage and the desired closed loop response.
2. Obtaining the step response of the ideal B(z).
3. Curve fitting the PID template to the first few samples of the ideal compensator.

The discrete z domain template of the PID compensator (taking into account the sampling delay) can be described as

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}} \tag{3}$$

or by the difference equation

$$V_c[n] = V_c[n-1] + aV_e[n] + bV_e[n-1] + cV_e[n-2] \tag{4}$$

The three coefficients (a, b, c) can now be calculated by indexing and solving (4) for the first three samples

$$\begin{bmatrix} V_c[0] - 0 \\ V_c[1] - V_c[0] \\ V_c[2] - V_c[1] \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{5}$$

where the indices, 0, 1, 2 stand for the first three samples of the output of the ideal B(z) compensator for the step input: 1, 1, 1.

Another issue that needs to be resolved is the specification of ($A_{CL}(z)$). In most DC-DC converters the relevant closed loop response is the step response rather than the frequency domain transfer function from which ($A_{CL}(z)$) is normally derived by say, s to z transformation. Here we propose to extract $A_{CL}(z)$ from the time domain response. The proposed procedure includes two steps. The first is to specify the characteristic equation of ($A_{CL}(z)$) through time domain parameters. This could be achieved by considering the typical response of a closed loop system with phase margin smaller than 50^0. The closed loop response in this case will behave like a second order system (see for example [1]). The denominator (characteristic equation, CE(s)) can be described by the conventional template

$$CE(s) = \frac{s^2}{{\omega_n}^2} + \frac{s}{\omega_n Q} + 1 \tag{6}$$

where ω_n is the angular resonant frequency and Q is the quality factor. For this dynamic system, the angular resonant frequency and the quality factor can be expressed as [4]

$$\omega_n \approx \frac{1.8}{t_r} \tag{7}$$

$$Q = -\frac{\sqrt{1 + \left(\frac{\ln(M_p)}{\pi}\right)^2}}{2\frac{\ln(M_p)}{\pi}} \tag{8}$$

Equations (7) and (8) provide a way to define the characteristic equation of $A_{CL}(s)$ as a function of the desired rise time and overshoot. Once the time domain response of A_{CL} is set, the denominator of $A_{CL}(z)$ can be obtained by one of the s to z transformations. The second step of the $A_{CL}(z)$ derivation procedure is to set the numerator such that the closed loop response will be of a second order nature [4], [7]. That is, to obtain the form of $A_{CL}(z)$ such that the closed loop system will: (a) be casual, (b) have zero error in steady state to step perturbation and (3) have a constant error to a ramp signal: This set of rules is translated into the followings constraints:

$$A_{CL}(z)|_{z=\infty} = 0 \quad (9) \qquad A_{CL}(z)|_{z=1} = 1 \quad (10) \qquad \frac{dA_{CL}(z)}{dz}_{|z=1} = \frac{1}{K_V} \tag{11}$$

Following the above procedure one can derive from (2) the transfer function of the compensator $B(z)_{ideal}$ that will yield the desired rise time t_r and over shoot M_p (i.e. $A_{CL}(z)$) for a given power stage A(z).

3. Design Example

The following example illustrates the proposed digital compensator design method. Assuming:

A Buck type converter power stage described by

$$A(s)=\frac{3.333\cdot 10^{8}}{s^{2}+2500\,s+1.333\cdot 10^{8}} \tag{12}$$

Required closed loop time domain performance

t_r=100μS ; M_p=10%

The first step would be to transform A(s) to A(z) by the ZOH transformation

$$A(z)=\frac{0.06548\,z+0.06459}{z^{2}-1.908z+0.96} \tag{13}$$

Next, t_r and M_p are used to calculate ω_n and Q (by (7), (8)) that define the characteristic equation of $A_{CL}(s)$ (6)

$$CE(s)=3.086\cdot 10^{-9}\,s^{2}+1.1\cdot 10^{-3}\,s+1 \tag{14}$$

To properly specify the closed loop response in the discrete domain ($A_{CL}(z)$), we follow the rules of section 2. The discrete equivalent of (14) is extracted by applying one of the s to z transformations (here we used the normalized matched p-z [4])

$$CE(z)=z^{2}-1.401\,z+0.4933 \tag{15}$$

The second step of $A_{CL}(z)$ derivation is extracting the numerator. For proper design, the order of the numerator must not exceed the order of CE(z) [4] thus $A_{CL}(z)$ will be of the form

$$A_{CL}(z)=\frac{n_0z^{2}+n_1\,z+n_2}{z^{2}+d_1\,z+d_2}=\frac{n_0z^{2}+n_1\,z+n_2}{z^{2}-1.401\,z+0.4933} \tag{16}$$

where d_1 and d_2 are the denominator coefficients extracted in (15), and n_0, n_1, n_2 are the numerator coefficients to be found by applying (9) to (11). The resulting discrete closed loop transfer function, $A_{CL}(z)$, is

$$A_{CL}(z)=\frac{0.5067\,z-0.4148}{z^{2}-1.401\,z+0.4933} \tag{17}$$

A(z) and $A_{CL}(z)$ are then used to express B(z) (2)

$$B(z)=\frac{0.5044z^{3}-1.375\,z^{2}+1.271z-0.3958}{0.06548\,z^{3}-0.1249\,z^{2}+0.05945\,z} \tag{18}$$

This expression can now be used to obtain the step response of the ideal compensator. This could conveniently be done by MATLAB using the function: [Vc_data] = step(B). Since B(z) was already assigned to the step function as a discrete function, the time steps are automatically adjusted to the sampling period (20μS) [8].

Once the vector of the response (Vc_data) is evaluated, the PID coefficients (a, b, c) are calculated to be: a= 3.4; b=-6.15 ; c= 2.93

Comparison between the step responses of the proposed compensator and that of the ideal compensator shows (Fig. 1) a good fitting for the first three steps, which was the objective of

the fitting. More importantly, the system's closed loop step response with the proposed compensator is very close to the response with the ideal compensator (Fig. 2).

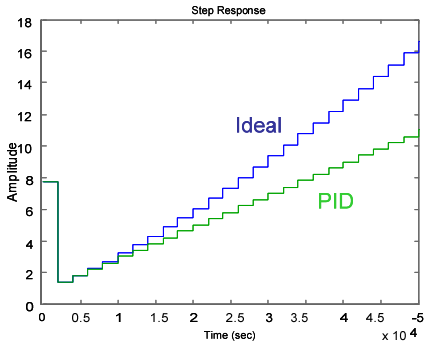

Figure 1. Step responses of the 'ideal' compensator and the proposed PID compensator.

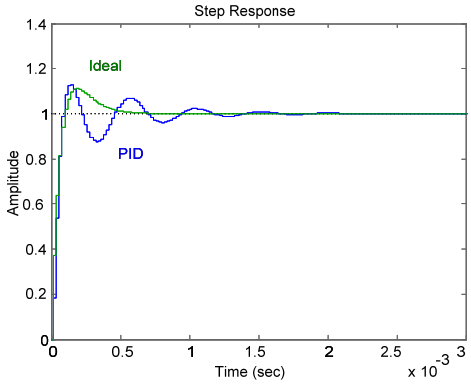

Figure 2. Closed loop step responses of a system controlled by 'ideal' compensator and proposed PID compensator.

An interesting insight into the performance of the proposed compensator can be obtained by reconstructing the frequency domain of the responses (Fig. 3). It can be observed that loopgain of a system controlled by the proposed PID crosses the 0dB point nearly at the same frequency as the system controlled by the ideal compensator. However, the phase of the PID network is slightly lagging with reference to the ideal compensator. This implies that for a given set of design specifications, systems that are controlled by either the ideal compensator or by PID will have the same bandwidth, but with a somewhat smaller phase margin when controlled with PID. In time domain terms, both system will produce the same overshoot and respond with the same rise time, however, the PID controlled system will decay somewhat slower, still acceptable yet, as can be observed in Fig. 2.

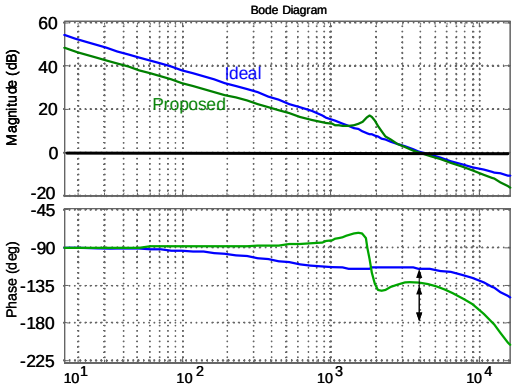

Figure 3. Loopgain frequency responses of systems controlled by the 'ideal' compensator and the PID compensator.

4. Implementation by the C2000 DSP family

The C2000 DSP family offers variety fixed-point microcontrollers dedicated to real-time control purposes (GPIO/PWM ports, A/D inputs and communication peripherals). The 24x series belong to the older generation of relatively low clock frequency and 16bit controllers, but with the nice addition of a 32bit accumulator to increase calculation accuracy. The 28x series of DSPs are the more advanced version of 32bit fixed-point, fast controllers with high-resolution PWM capability.

The proposed PID controller (Eqs. 3 and 4) consumes only a small portion of the controller's resources. It requires (for each computational event, sampling instance) only three memory spaces for data storage and short computation time. So it can be operated with all the C2000 DSPs. The only limitation of the device selection would be on the basis of the sampling rate selection and the duty cycle resolution that is required to avoid undesirable oscillations.

The realization of the PID control law of (4) on the digital platform is quite straightforward. It involves the algebraic summation of error samples (current and two previous) and the previous value of the duty command. Many open literature references offer C-code examples of this law, or with some modifications. In fact, in the TI's motor control library one can find application notes and code examples of PID compensation for motion, speed and torque control. Lacking however, are assembly code examples that can be better optimized in terms of code run time, and compatibility to simpler cores such as the F2407 DSP.

It should also be noted that PID structures, and the extracted coefficients which are found in the literature are based on frequency domain methods, and thus suffer from the limitations discussed earlier. The main focus of this work was to present a controller design method that is based on the time domain and thus bypasses these limitations, and provide a more streamlined design procedure.

4.1 Software realization

The proposed PID compensator was implemented on the F2407 DSP. To improve the run time and to overcome the lack of compilation capabilities, the code was written in assembly language. The program algorithm is detailed in the flowchart of Fig. 4. It should be noted that the control operates in constant frequency PWM with one sampling per switching cycle. The object is to change the duty-cycle command to facilitate regulation, stability and the desired performance goals.

The program starts with the initialization of fixed PWM frequency (timer register TxPR), initial duty-cycle (compare register CMPRx) and four, fixed-point scaled, constants for the PID coefficients and the reference output signal. Then the program enters idle mode and awaits the interrupt. The ADC interrupt is programmed by the timer compare register (TxCMPR) to be just before the end of period to obtain 'interference free' measurement, as much as possible, of the output signal. The timer Interrupt Service Routine (ISR) handles the calculations of the PID control law as described by the finite difference equation of (4). A limiter is added to the numerical calculation to maintain the duty cycle command within the physical limits (0 – 1). The resulting value is stored to be used in the next calculation. Upon return from the ISR, the new (limited) duty cycle command is loaded to the timer compare register (CMPRx) and is programmed to be updated with the beginning of a new timer period count.

One should be aware of some practical implementation issue when translating the control algorithm that was derived by a floating-point software tool (e.g. MATLAB) to a fixed-point

code. This transfer normally calls for multiplication of the floating-point parameters by large scaling factors and rounding. Once the calculation on the scaled integers is done, there is a need for rescaling to generate the correct output values. It follows then that a 16bit based controller, may not be capable of retaining the accuracy of the control. It was found however, that with the proper use of a 32bit accumulator (as in the F2407) one can get s sufficient latitude required for this control algorithm.

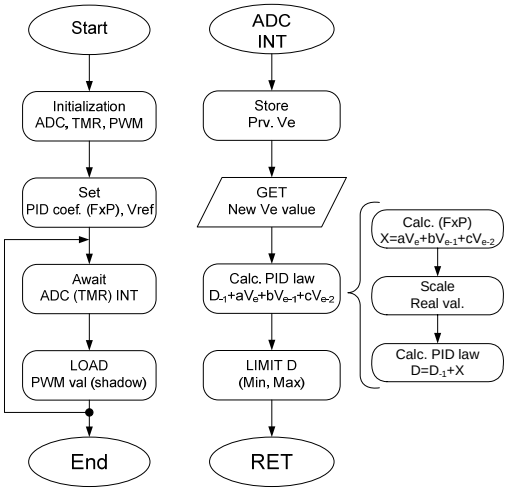

Figure 4. Flowchart of PID control realization on C2000 DSP.

5. Experimental verification

Digital PID controllers for a Buck and Boost type converters were implemented experimentally on a TMS320LF2407 DSP core (Texas Instruments) (Fig. 5) [9, 10]. The sampling rate (and switching frequency) was set to 50KHz for the Buck and 20KHz for the Boost. The A/D resolution was set to 8bit to avoid limit-cycle oscillations. The measured closed-loop attributes were 3.5KHz bandwidth and phase margin of 40^o for the Buck converter, and 1.6 KHz and 40^o for the Boost. Good agreement was found between the design goals and the experimentally determined response. Fig. 6 demonstrates the very good agreement that was obtained between the closed loop response and simulation results.

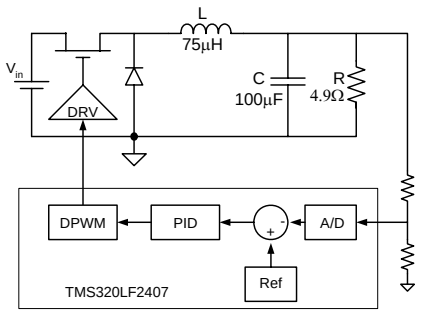

Figure 5. Experimental setup for a Buck converter

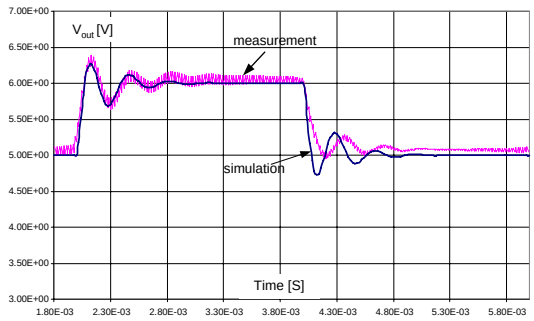

Figure 6. Comparison of simulation and experimental output voltage step response for a step in reference for a Buck type converter (5V to 6V).

6. Discussion and Conclusions

The proposed design procedure of a digital compensator for a PWM DC-DC converter follows the concept, developed in this study, of local behavior of discrete compensators. The basic idea behind this concept is that the system's closed loop response is largely determined by the first few samples of the step response of the compensator. The simulation and the experimental results confirm the viability of the proposed design method. The proposed method can thus be a good candidate for an alternative approach to the design of digital compensators for PWM DC-DC converters.

Comparison between the simulated performances of the ideal compensator and the PID shows that the latter might suffers from slightly longer settling periods. However, slight performance deterioration is considered an acceptable pay off to avoid the practical drawbacks of the 'ideal' compensator such as: complicated compensator implementation, long computational time and system dependent template.

It should also be noted that although executed on a 16bit fixed-point DSP, with relatively low clock frequency, the proposed control method performed accurately considering the limitation of the switching frequency. The use of new DSP versions such as the 28x series will allow higher switching frequencies and hence higher bandwidth settings thanks to their higher clock frequency, faster A/D conversion and code execution time.

The potential advantages of the proposed method are the fact that it is carried out in the time domain (and hence bypasses some of the errors due to the s to z transformation) and that it does not involve a trial and error procedure.

7. References

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