Resonant Binary and Fibonacci Switched-Capacitor Bidirectional DC-DC Converter

Eli Hamo, Mor Mordechai Peretz, and Shmuel (Sam) Ben-Yaakov

Power Electronics Laboratory, Department of Electrical and Computer Engineering
Ben-Gurion University of the Negev
P.O. Box 653, Beer - Sheva, 84105 Israel
eliham@walla.com; morp@ee.bgu.ac.il; sby@ee.bgu.ac.il
Website: www.ee.bgu.ac.il/~pel/

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Abstract - **A resonant step-up/step-down Binary and Fibonacci Switched capacitor bi-directional converter is proposed for the medium power range. The resonant operation is achieved with only one air core inductor or by using the stray inductance. This approach reduces the power losses by reducing the switching losses together with increasing the number of target voltages. A 100W prototype with 100V input and 13 conversion ratios, operating at 45-55 kHz switching frequency is built and tested experimentally. A simple, an isolated gate driver was also developed. It features wide switching frequency duty cycle ranges of 30kHz - 350kHz and 0.1-0.9, respectively, and rise and fall times of about 200ns.**

Index Terms - **Resonant Switched-Capacitor, Binary/Fibonacci, generic equivalent model, bidirectional switches, isolated drivers.**

I. INTRODUCTION

Switched capacitor converters (SCC) are becoming attractive alternative in many applications ranging from low to high power. These include voltage regulators for mobile electronic systems, voltage equalizers for batteries and capacitors, for solar photovoltaic (PV) modules, and for automotive applications [1], [2]. As opposed to conventional switch mode DC/DC converters that include bulky inductors to process and store energy, SCC require only capacitors and MOSFET switches. The use of small ceramic capacitor makes them very compact, light and suitable for high temperature environments. In order to increase the efficiency, reduce the switching losses, voltage spikes and EMI, several zero current switching topologies have been proposed. These are realized by inserting small inductors in series with the capacitors.

In many applications there is a need to maintain a constant output voltage under input voltage variation or to provide different output voltages. Fig. 1 describes the generic equivalent circuit model [3] for SCC, in which losses are conveniently described as a function of the load current by R_{eqT}. The efficiency can be expressed as -

$$\eta = \frac{V_o}{V_{\text{Target}}} = \frac{R_o}{R_o + R_{eqT}}, \quad V_{\text{Target}} = M_n \cdot V_{in} \qquad (1)$$

where M_n is the no-load voltage transfer ratio. Equation (1) implies that high efficiency can be reached if M_n is controllable with high resolution. An effective way to realize many target voltages is using the Binary/Fibonacci SCC that exhibit a high resolution. Previous Binary/Fibonacci SCC were implemented by hard switched SCC topologies and were limited to low power devices [4].

The objective of this study was to examine the behavior and the performance of a resonant Binary/Fibonacci converter with single air core inductor or stray inductances, for medium power range. For n capacitors the number of target voltages in such converters will be 2^n-1with a resolution of $1/2^n$ in the Extended Binary (EXB) codes and the Signed Fibonacci (SFN) codes exhibit additional 2n target voltages [4].

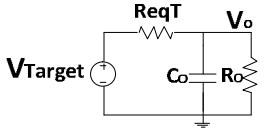

Fig. 1: SCC generic equivalent circuit.

II. PROPOSED CONVERTER AND OPERATIONAL PRINCIPLE

Fig. 2 shows the proposed topology for a step down resonant Binary/Fibonacci SCC. The precursor of this approach was the hard-switched case presented [4, 5]. In this study, Zero Current Switching (ZCS) is obtained by a single air core inductor, L_s (Fig. 2). Step up conversion can also be achieved by swapping the input and output stages as depicted in Fig. 3. With three capacitors, n=3 the converter can provide 13 conversion ratios - {1/8,1/5,1/4,1/3,3/8,2/5,1/2,3/5,2/3,5/8,3/4,4/5,7/8}.

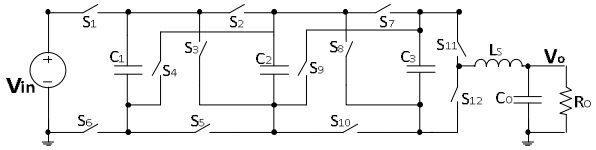

Fig. 2: Resonant Binary/Fibonacci switched capacitor step-down converter, example for n=3.

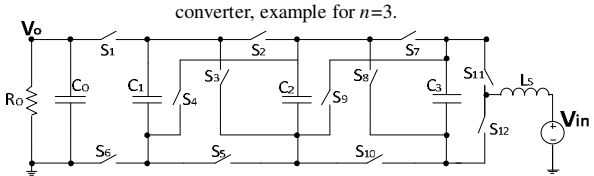

Fig. 3: Resonant Binary/Fibonacci switched capacitor step-up converter, example for n=3.

The analysis is performed on a step-down resonant SCC as shown in Fig. 2. The connection of V_{in} is defined by the coefficient A_0 in each of the EXB/SFN codes for a given conversion ratio - M_n. All flying capacitors are always connected serially according to the coefficients A_j. We can summarize the rules of the topological interconnections of V_{in}, C_j and C_o as follows:

1. If $A_0 = 1$, then V_{in} is connected.
2. If $A_0 = 0$, then V_{in} is not connected.
3. If $A_j = -1$, then C_j is charged.
4. If $A_j = 0$, then C_j is not connected.
5. If $A_j = 1$, then C_j is discharged.

For example, a case of M=5/8, will result in the EXB codes as presented in Table 1a, that is translated to the corresponding resonant SCC topologies of Table 1b . Thus, each EXB code leads to specific series of high-order RCL circuit in every state. The specific topologies are depicted in Fig. 4.

TABLE 1a
THE EXB CODES FOR M=5/8.

A_0	A_1	A_2	A_3
1	0	-1	-1
1	-1	1	-1
0	1	1	-1
1	-1	0	1
0	1	0	1

TABLE 1b
THE SWITCHES STATE ACCORDING TO THE EXB CODES.

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	1	0	0	0	0	0	0	1	0	0	1
1	0	0	0	1	0	1	0	0	0	0	1
0	0	1	0	0	1	1	0	0	0	0	1
1	0	0	0	1	0	0	0	0	1	1	0
0	0	1	0	0	1	0	0	0	1	1	0

For a simplification of the mathematical analysis on the topologies depicted in Fig. 4, a steady-state operation and very light output load are assumed. Kirchhoff's Voltage Law (KVL) can be obtained for each topology for the average voltages. Furthermore, at steady-state, $\hat{V}_{Ls} = 0$ for each of the sub circuits. This leads to system of five linear equations and four unknown.

$$\begin{cases} V_{in} + 0 - V_{C2} - V_{C3} = V_{Co} \\ V_{in} - V_{C1} + V_{C2} - V_{C3} = V_{Co} \\ 0 + V_{C1} + V_{C2} - V_{C3} = V_{Co} \\ V_{in} - V_{C1} + 0 + V_{C3} = V_{Co} \\ 0 + V_{C1} + 0 + V_{C3} = V_{Co} \end{cases} \quad (2)$$

Grouping the unknowns in (2) at the left hand side and normalizing it to V_{in} yields to (3). Solving the system of (3) we obtain the voltages across the flying capacitor and the output stage : V_{C1}=(1/2)V_{in} , V_{C2}=(1/4)V_{in} , V_{C3}=(1/8)V_{in} , V_{Co}=(5/8)V_{in}. Since this is the unique solution [6] there is no need for any control system to assure that the capacitors have stabilized at their corresponding nominal voltages.

$$\overbrace{\begin{bmatrix} 0 & -1 & -1 & -1 \\ -1 & 1 & -1 & -1 \\ 1 & 1 & -1 & -1 \\ -1 & 0 & 1 & -1 \\ 1 & 0 & 1 & -1 \end{bmatrix}}^{A} \overbrace{\begin{bmatrix} V_{C_1}/V_{in} \\ V_{C_2}/V_{in} \\ V_{C_3}/V_{in} \\ V_{C_o}/V_{in} \end{bmatrix}}^{X} = \overbrace{\begin{bmatrix} -1 \\ -1 \\ 0 \\ -1 \\ 0 \end{bmatrix}}^{b} \quad (3)$$

Parallel connection of two flying capacitors must be avoided when transitioning between two sub circuits. This is done to eliminate the large current spike that may damage the system.

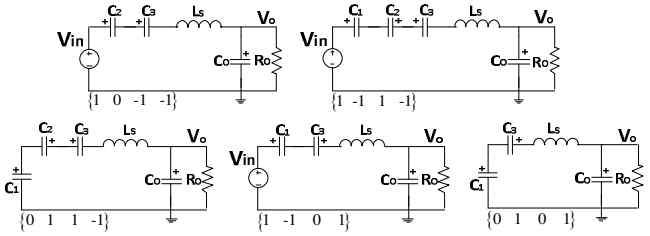

Fig 4: Resonant SCC topologies configured from the EXB codes of M=5/8.

III. Switches And Isolated Gate Drivers

The Resonant SCC of Fig. 2 is experimentally implemented with twelve bidirectional switches. Every switch includes two N - channel power MOSFETs with common source and common gate as depicted in Fig. 5. This is done to avoid reverse current flow that may create undesired when the switches are off.

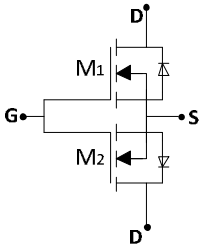

Fig. 5: Bi- directional switch using N - channel power MOSFETs.

Fig. 6, 7 describes the structure and the operation principle of the floating driver for the bidirectional switches. The structure consists of a 1:1 pulse transformer for isolation, a DC blocking capacitor C_1 to prevent the DC content of the gate drive from passing through the pulse transformer, C_2 and D_2 to restore the DC level at the secondary side, capacitor C_3 acts as an independent supplier and NPN and PNP transistors connected push-pull configuration. Assuming that the voltages across C_2, C_3 are stable, the operation of the gate driver may be described as follows:

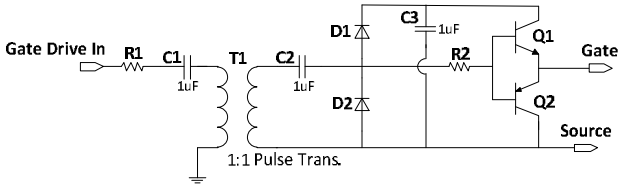

Fig. 6: The Isolated Gate Driver.

On State: *Vp* positive with regard to the ground, D_1 is forward biased and C_3 partially discharges through Q_1 that is saturated, and charging C_{GS} turning on the MOSFET, (Fig. 7a). Then, C_3 recharges through C_2 and D_1. The independent supplier C_3 provides a quick charging of C_{GS} and therefore, the rise time is relatively fast.

Off state: *Vp* is negative, D_2 is forward biased, C_2 now charges in the opposite way through D_2. C_{GS} discharges through Q_2 that is saturated, turning off the MOSFET, (Fig. 7b). R_2 damps potential overshoots that may occur due to stray inductances and influences the fall time.

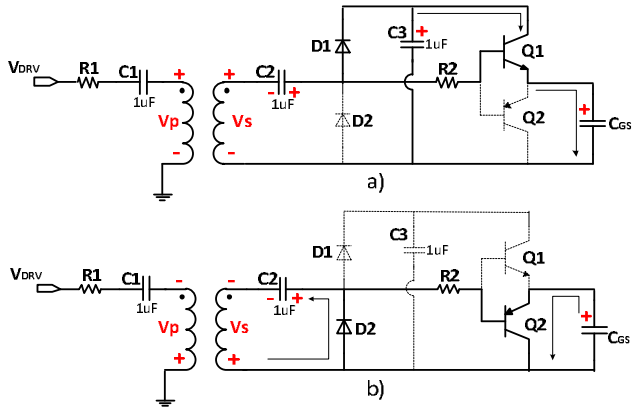

Fig. 7: Operation modes: a) ON state - C_{GS} charging.

b) OFF state - C_{GS} Discharging.

The experimental prototype implemented with six MIC4427, dual 1.5A driver, twelve gate drive transformers GT03-111-110-A, and twenty four JE170 and JE181 transistors. The floating drivers have a switching frequency range of 30kHz-350kHz, and a wide duty cycle range of 0.1-0.9, with rise time and fall time of about 200ns.

IV. Converter Performance Analysis

Each stage for all EXB/SFN codes use four switches in 'on' state. Therefore the total parasitic loop resistance for every state includes eight $R_{DS(on)}$-s, ESR of the total equivalent capacitance and the resistance of the inductor and wires.The total equivalent resistance R_{eqT} of the generic model depicted in Fig.1, can be expressed in term of all sub circuits quality factor Q_i [7]:

$$R_{eqT} = \sum_{i=1}^{n} k_i^2 \frac{2Q_i^2 \pi R_{t_i}}{df_i \sqrt{4Q_i^2 - 1}} \tanh\left(\frac{\pi}{2\sqrt{4Q_i^2 - 1}}\right) \qquad (4)$$

where df_i is the ratio between the switching frequencies to the damped resonant frequencies, k_i is the proportional coefficient between the average flying capacitor current and output current, R_{t_i} is the total loop resistance for each state. From the equivalents RCL circuit depicted in Fig. 4, we can write the effect of each flying capacitor on the average output current. Capacitors currents lead to system of four linear equations and five unknown. The system consists of average currents for each phase I_1-I_5, taking into account that the average current through each capacitor for a time period must be zero. The last equation expresses the sum of all current states.

$$\begin{cases} 0 - I_2 + I_3 - I_4 + I_5 = 0\ ; & C_1 \\ -I_1 + I_2 + I_3 + 0\ + 0 = 0\ ; & C_2 \\ -I_1 - I_2 - I_3 + I_4 + I_5 = 0\ ; & C_3 \\ I_1 + I_2 + I_3 + I_4 + I_5 = I_o\ ; \end{cases} \qquad (5)$$

Assuming a particular solution for (5) when I_4=*0,* yields: I_1=(1/4)I_o , I_2=(3/8)I_o , I_3=(-1/8)I_o , I_5=(1/2)I_o. Furthermore since the value of the flying capacitors are equal and always connected in series, the total equivalent capacitance C_{t_i} can be found from the number of non-zero coefficients A_j. It should be noted, however, that the simplified model described in Fig. 1 does not include the losses due to the gate drives and the parasitic effects. This can be estimated by:

$$P_{Gate\_loss} = V_{GS} Q_{gate} f_S \qquad (6)$$

where V_{GS} is the drive voltage, f_s - switching frequency, and Q_{gate} is the total gate charge of the MOSFET.

V. Design Guidelines

The guidelines to design the Resonant Binary/Fibonacci SCC were derived based on the generic equivalent modeling approach [3, 7].

A. R_{eq} and The Quality Factor

The conduction losses of each sub circuit are linearly proportional to the equivalent resistances R_{ei}, as implied from (1). Since the transistors' on resistances are significantly larger than the rest of the resistive components of the sub circuit, R_{t_i} is approximated to eight $R_{DS(on)}$-s. It is also assumed that R_{t_i} is equal for all sub circuits. For In every voltage ratio - $L_{t_i} = L_s$ and in the case of M=5/8, C_{t1}=C_{t4}=C/2, C_{t2}=C_{t3}=C/3. This leads to $Q_1 = \sqrt{2/3} \cdot Q_2$ and $df_2 = (2/3) \cdot df_1$. Numerical analysis was carried out using MATLAB for the normalized equivalent resistance of all sub circuits (7), derived from (4), regarding to Q_1 and df_1, in order to examine the worst case.

$$\frac{R_{eqT}}{R_{t_i}} = k_1^2 \frac{2Q_1^2\pi}{df_1\sqrt{4Q_1^2-1}} \tanh\left(\frac{\pi}{2\sqrt{4Q_1^2-1}}\right) + k_2^2 \frac{9Q_1^2\pi}{2df_1\sqrt{6Q_1^2-1}} \tanh\left(\frac{\pi}{2\sqrt{6Q_1^2-1}}\right)$$
$$k_3^2 \frac{9Q_1^2\pi}{2df_1\sqrt{6Q_1^2-1}} \tanh\left(\frac{\pi}{2\sqrt{6Q_1^2-1}}\right) + k_4^2 \frac{2Q_1^2\pi}{df_1\sqrt{4Q_1^2-1}} \tanh\left(\frac{\pi}{2\sqrt{4Q_1^2-1}}\right) \qquad (7)$$

Fig. 8 shows the dependence of the normalized equivalent resistance of all RCL sub circuits on the quality factor and the ratio df_1. It can be observed that for quality factor higher than 3, any further reduction of the normalized resistance is minor. High quality factor can results in a large inductor or very small capacitors. Whereas low quality factor, Q<*1* increases the conduction losses. Furthermore, df_1=0.6 is the preferable value for lower conduction losses. Given these tradeoffs, a good choice for the case of M=5/8 will be $Q_1 \approx 1.25$. Once Q has been selected, and given the value of the flying capacitors and the parasitic inductances, one can calculate the upper boundary for $R_{DS(on)}$. For a given power level, this value should be selected as the lower resultant $R_{DS(on)}$ between the one extracted from the efficiency expression of (1) and the worst-case value of $R_{DS(on)_{MAX}} = \left(\sqrt{L/C_t}\right)/8Q$. This calculation should take into account a worst-case C_t, that is, the largest equivalent

capacitance that can be obtained among all sub circuits for a given voltage ratio M_n.

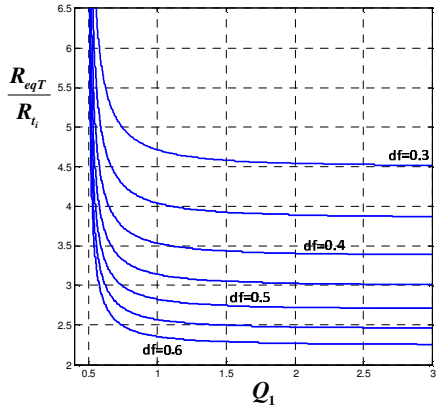

Fig. 8: Dependence of the normalized equivalent resistance on the Quality factor (Q_1) and the frequency ratio, (df_1).

B. The Flying Capacitor

For capacitors type, the ESR inversely proportional to the capacitance. Low capacitance may lead to large voltage ripple and even to opposite charge flow of the flying capacitors. High capacitance may lead to larger converter dimensions and higher conduction losses. A good practice would be to use several MLCC (ceramic) capacitors connected in parallel for low ESR and small dimensions. Therefore capacitance of several or even tens of μF, that can fit to the switching frequency and the quality factor that have already been selected. The flying capacitor value is calculated from the resonant frequency or by the quality factor by:

$$C = 1/4\pi^2 L f_s = L/Q^2 R^2 \qquad (8)$$

C. Inductance

The circuit layout should be carefully designed to allow high frequency operation and symmetrical operation of the sub circuits. This can be done by limiting the stray inductance to the range of tens or even few hundreds of nH and making the current paths equal for each sub circuit. Symmetry in the sub circuits also simplifies the control method. In case of small stray inductance, a small air inductor in the input or at the output stage may be added.

D. Switching Frequency

Zero current switching is achieved when the 'on' time of each equivalent RCL circuit matches the half period of the resonant current. This can be achieved by inserting only one inductor or to use the stray inductances in the circuits as depicted in Fig. 2. Therefore for N sub circuits the switching frequency of the converter can be express as:

$$f_s = 2/\left(1/f_{o1} + 1/f_{o2} + ... + 1/f_{oN}\right) = 1/\left(\pi \cdot \sum_{j=1}^{N} \sqrt{L_{total_j} C_{total_j}}\right) \qquad (9)$$

For cases of small mismatches between the stray inductances of the sub circuits or capacitance changes due to different voltage stress on the flying capacitors, a simple duty cycle adjustment can be obtained with respect to the shortest or the longest resonant period by - $\delta = D_{ref}/D_j$. Another consideration for the upper frequency bound is to prevent the pulse transformer from saturation and increased gate drive losses.

VI. Simulation And Experimental Results

The simulations and the experimental set-up were done on the circuit of Fig. 2. Fig. 9, 10 shows PSIM simulation results of the Resonant Binary SCC at: M=5/8, V_{in}=$100V$, P_{out}=$100W$, air inductor L_S=$200nH$, all flying capacitors C_j=$9.4\mu F$, and switching frequency f_s=$90kHz$. S9, S5 are the normalized switch gate-source control voltages, I_C1,2,3 are the currents through the flying capacitors C_1, C_2 and C_3. I_Ls is the inductor current at the output stage, and Iout is the load current. V_C1,2,3 are the capacitor voltages across the flying capacitors and AVG(V_C1,2,3) are the average voltages.

The $100W$ Resonant Binary SCC Prototype was realized using the stray inductance in the circuit alone without adding an additional inductor. The switching frequency was adjusted correspondingly to the equivalent RCL circuit, in every stage. The test parameters of the prototype were V_{in}=$100V$ and $f_s \approx 53kHz$. The resonant capacitors are two $4.7\mu F$, $100V$, MLCC capacitors C5750X7R2A475K (TDK) connected in parallel. Output capacitor were ten 4.7μF, $100V$, capacitors connected in parallel and nominal R_o=39Ω. The bidirectional switching devices are two $100V$ power MOSFETs with 'on' resistance around $45m\Omega$ each. Microcontroller DsPic33J12GP202 was used for timing the frequency and the duty cycle respectively.

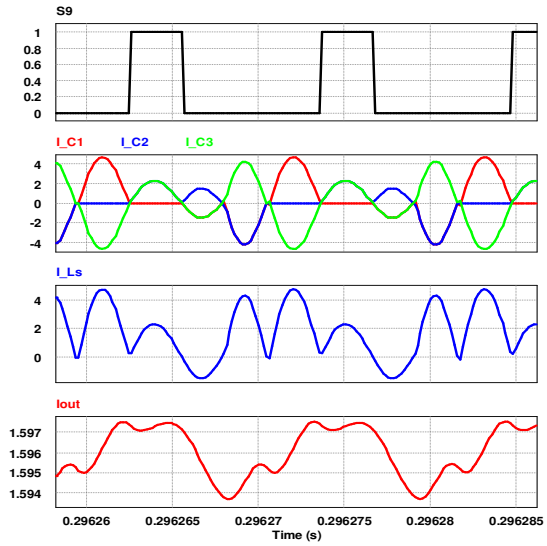

Fig. 9: Capacitors and output stage current waveforms, M=5/8.

The calculated stray inductance were approximately L_{t1}=$680nH$, L_{t2}=$358nH$, L_{t3}=$866nH$, L_{t4}=$484nH$. Taking into account the capacitance change due to the change of the average voltages and that the total parasitic loop resistance in every state about $360m\Omega$, the quality factor were calculated to be Q_1=1.08, Q_2=1.12, Q_3=1.68, Q_4=1.05. Furthermore the frequency ratio df_1=0.58, df_2=0.32, df_3=0.48 and df_4=0.42.

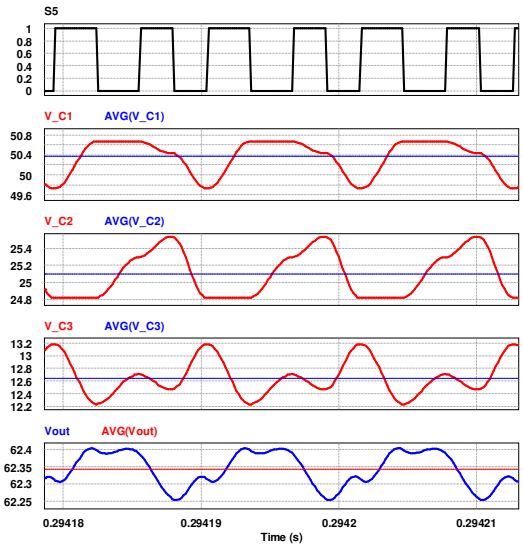

Fig.10: Capacitors and output voltages waveforms, M=5/8.

Fig. 11, 12 and 13 show the experimental waveforms of the Resonant Binary SCC prototype with the components mentioned above. Fig. 11, 12 show the current at the output stage for V_{in}=80V and V_{in}=100V at M=5/8 respectively and Fig. 13 for V_{in}=60V at M=3/8.

Fig. 14 shows the efficiency of various input voltages and loads. It is clear from the generic equivalent circuit model described in Fig. 1 that for higher target voltages the RMS current values will be smaller for a constant P_o and hence the power loss on R_{eqT} will decrease. The calculated values of R_{eqT} according to (4) for the 5/8 case were 1.2Ω while the experimentally evaluated values were about 1.3Ω.

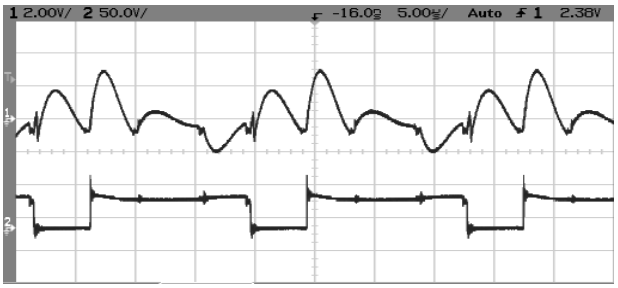

Fig. 11: I_{out} and $V_{DS}(S6)$ at V_{in}=100V, P_{out}=136W, M=5/8.

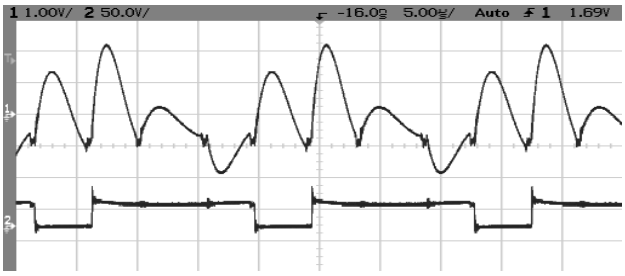

Fig. 12: I_{out} and $V_{DS}(S6)$ at V_{in}=80V, P_{out}=100W, M=5/8.

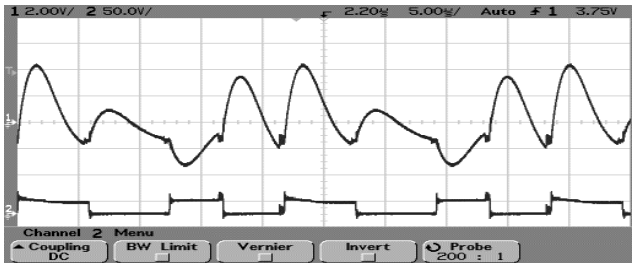

Fig. 13: I_{out} and $V_{DS}(S6)$ at V_{in}=60V, P_{out}=69.89W, M=3/8.

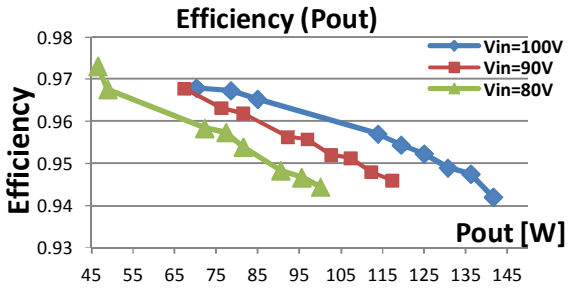

Fig. 14: Efficiency of step-down, Resonant Binary SCC, *M=5/8.*

VII. Conclusions

A resonant binary and Fibonacci step-up/down converter was introduced in this paper. Soft switching method based on inserting one air core inductor or the use of the parasitic inductance and adjusts all the duty cycle respectively to the RCL sub circuits created from the EXB/SFN codes. The method can implement with the most of switch capacitor topologies for reducing the conduction losses and the EMI noises. Furthermore, the converter reducing the power losses by increasing the number of target voltage. Low quality factor, $Q<1$, can leads to low efficiency. The simulation and the experimental results confirm the theoretical analysis and showed that the proposed converter is a viable approach for medium step-up/down power systems despite of the large number of switches.

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