Full FPGA-Based Design of a PWM/CPM Controller with Integrated High-Resolution Fast ADC and DPWM Peripherals

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Abstract - This paper introduces the design and implementation of a full FPGA oriented PWM/CPM controller. The controller realization has been enabled by newly developed ADC and high-resolution DPWM peripheral units based on delay line technology that has been specially modified to FPGA design and constrains. The new ADC is capable of converting a sample with resolution of 10 bits within 300ns. The DPWM has demonstrated capability of producing 11bit signal at 1.6MHz. CPM operation is verified on a 12-48V, 100W boost converter.

I. INTRODUCTION

In recent years, digital control has established a dominant role as efficient regulator for switch-mode power supplies (SMPS). Voltage-mode digital PWM (DPWM) controllers have been widely and effectively demonstrated on low-cost microcontrollers and FPGAs [1]-[3]. This has been enabled by the advancement of two main peripherals: high-resolution DPWM units and a fairly fast (at the switching rate) analog-to-digital converter (ADC). On the other hand, many applications that require peak current mode control (CPM) for its inherent cycle-by-cycle current protection and improved dynamics are still realized by analog means. This is due to the fast sampling of the current and complex processing that is required by CPM. As a workaround, various current-mode concepts that require only single sampling of the current per-cycle, have been developed such as the average [4],[5], predictive [6]-[7], and dead-beat [8]-[9]. The introduction of low resolution current ADC in [5] or the integration of simple comparator and DAC into the digital platform [10], have established good foundations for implementation of CPM by digital means. These are the precursors of this study.

Present-day digital controllers, excluding IC design, are implemented on either DSP cores or FPGAs. For operating frequencies in the range of several hundred kHz, DSPs with specialized integrated peripherals (DPWM, ADC, etc.) are available. For higher operating frequencies and more advanced control schemes (e.g. CPM or time-optimal control) [22]-[24], FPGA design is the preferred option. There, however, additional auxiliary components are required for peripherals which, to some extent, limit the capabilities of the controller. It would be highly advantageous if the main peripheral units that are required could be integrated into the FPGA, and are made configurable. In this way, the optimization and evaluation process of the controller operation are eased as well as providing a straightforward platform for IC integration via synthesis tools.

The objective of this paper is to present an FPGA design and implementation of a PWM/CPM digital controller that includes integrated DPWM and ADC peripherals (using an all-digital realization) and reduces the number of auxiliary components. The introduced controller architecture is depicted in Fig. 1. It follows the classical two-loop CPM design with a fully digital outer voltage loop while for the inner current loop, an analog comparator *i_cmp* is utilized [12], [25]-[27]. The voltage loop creates a digital reference for the peak current value $i_{ref}[n]$ that is then converted into an analog equivalent with a digital-to-analog converter (DAC) that is realized by a simple RC filter that is fed by a high-frequency high-resolution (11bit @ 1.6 MHz) DPWM unit, developed in this study. The current reference is calculated with a PI compensator based on the error signal of the voltage loop $e[n]$, and the resulting output of the DAC is compared to the sensed value of the inductor current $i_L K_I(t)$ with the comparator *i_cmp*. The output of the comparator is then sent to the S-R latch and a pulse width modulated signal $c(t)$ is created.

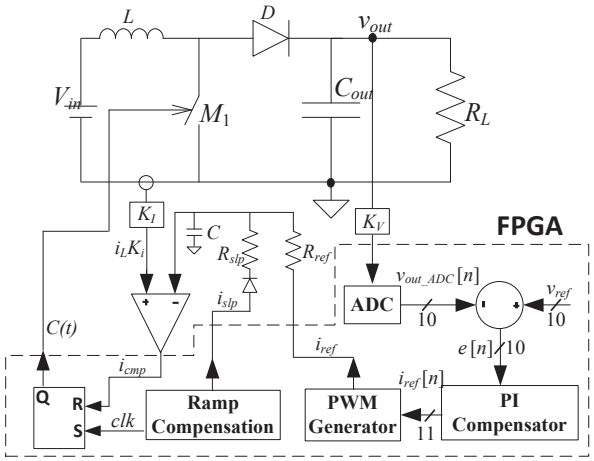

Fig. 1. Architecture of the FPGA-based CPM controller.

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The output voltage is sensed using a modified delay-line (DL) based ADC, also developed in this study. To allow CPM operation at duty ratios above 0.5 and avoid sub-harmonic oscillations [11],[12], an additional DPWM signal (at lower frequency) is generated and summed with the generated current reference, to create the artificial slope for compensation.

The rest of the paper is organized as follows: Section II presents the implementation of the modified DL-ADC. The realization of the high-resolution DPWM and the generation of the slope compensated current reference are described in Section III. The compensator design and a detailed description of the system gains are provided in Section IV. Experimental results for CPM operation on a 48V, 100W boost converter are given in Section V.

II. On-FPGA Delay-Line ADC

In contrast to conventional ADCs where voltage levels are compared, delay line based ADC (DL-ADC) compare the time difference between traveling signals [13]. As a result, DL-ADCs feature high noise immunity, lower power consumption, configurable conversion time, does not require sample-and-hold circuitry, and their construction primarily relies on digital architecture [14].

There are two main approaches to realize a DL-ADC. The first method is based on a string of voltage-controlled delay cells. Since the propagation delay of a logic gate depends on the supply voltage (by inverse proportion), the length of the propagation along the delay line serves as a measure of the gates supply [15]-[16]. The second approach follows a two-step conversion, that is, a voltage-to-time converter that is followed by a delay line based counter. The latter is facilitated using a string of digital buffers with fixed propagation time. Similar to the first method, the digital representation of the voltage is obtained by the count of active cells within the pulse length. Since this method does not require variable supply voltage, it is more suitable for FPGA implementation and therefore adopted in this study.

Figure 2 shows the ADC configuration that has been developed. The time counter delay string is implemented using asynchronous buffers, which in the current design feature a relatively fixed propagation delay of 300ps per cell. To achieve 10bit resolution, 1024 buffers are used. To facilitate a simple voltage-to-time conversion using digital architecture using FPGA, a simple monostable multivibrator (i.e. one-shot timer) has been employed by adding two additional gates. To complete the circuit functionality, the initial time constant is created using an auxiliary *RC* network that is connected to the FPGA ports. The sensed voltage is connected to the resistor *R*, creating the analog link.

The description of the DL-ADC operation is assisted by the timing diagram of Fig. 3 which shows experimental waveforms of the converter. A start-of-conversion, i.e. trigger signal, activates the one-shot. The resultant pulse length, T_{pulse}, as a function of the sensed voltage is expressed as:

$$T_{pulse} = RC\ln\left(\frac{V_{DD}}{V_{sample} - V_{threshold}}\right), \qquad (1)$$

where V_{DD} is the supply voltage to the FPGA, $V_{threshold}$ is the transition voltage of the or gate (typically ½ of V_{DD}) and $V_{sample}=K_v v_{out}$ is the value of the sensed signal. As can be observed, the voltage range is limited from ½ V_{DD} to V_{DD}. For cases that a range of 0 to ½ V_{DD} is of interest, the sensed signal can be offset by -½ V_{DD} using a simple resistive divider.

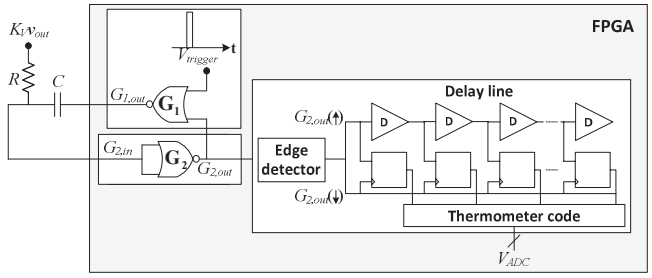

Fig.2. FPGA implementation of a delay-line ADC

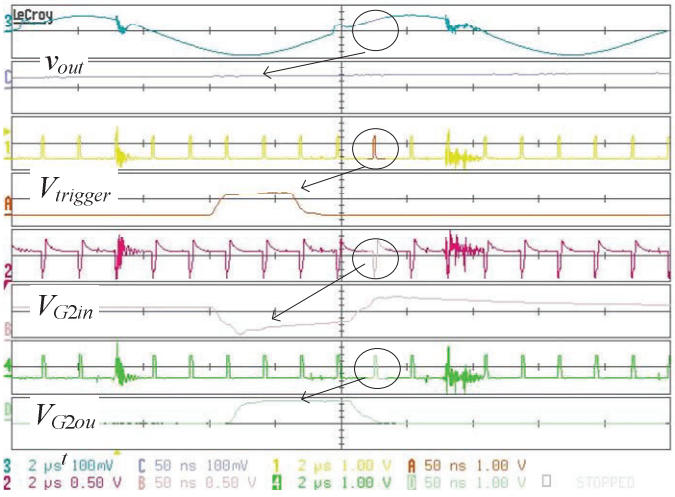

Fig.3. Operation of the experimental DL-ADC

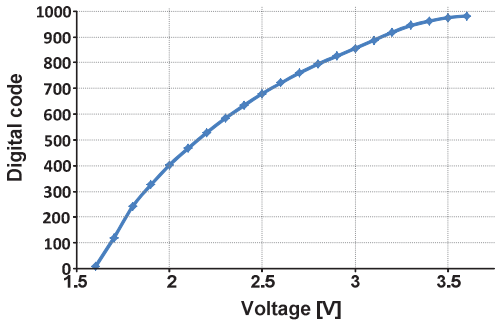

Fig.4. The static conversion characteristics of the experimental DL-ADC

The output signal of the one-shot timer (G_{2out}) contains the required data of the voltage level and also provides the start and stop signals to the counter. The edge detector generates a start-of-conversion signal with the rising edge of G_{2out} and a stop-of-conversion and capture signal with its falling edge. The resulting thermometer code is then converted into a digital value by summation of 2s-complement based algorithms. It can also be observed from Fig. 3 that power transistors switching action introduces noise on the sensed signal which may result in an erroneous measurement. This however, does not affect the closed-loop operation of the system which relies on a single sample per switching cycle.

The static conversion characteristics of the experimental DL-ADC are shown in Fig. 4. As can be observed and also foreseen from (1), since the voltage-to-time conversion is based on a simple RC one-shot timer, the static conversion curve has exponential characteristics as opposed to the desired linear one. However, in the context of voltage regulation, this has negligibly small effect on the performance of system in closed-loop since the operation is around a steady-state point and the deviations from that point are minor, compared to the entire range of the ADC. Therefore, within the vicinity of the steady-state, the exponential curve can be fairly approximated to a linear one. For cases that a general-purpose ADC with linear conversion curve is required, a post-conversion look-up-table linearization unit can be added based on the known deviation of exponential curve of (1) from a linear one.

III. Delay-Line DPWM and Current Reference Generator and Slope Compensation

High-resolution (HR) correction signal is essential to avoid undesirable limit cycle oscillations [17]. Commercial microcontrollers typically offer HR DPWM peripherals using frequency multipliers in the range of 32 times the core frequency, resulting in approximately 1ns effective resolution. An alternative approach to realize a HR DPWM is on the basis of delay cells [18]. This has been pursued in this study.

The construction and operation of the FPGA-based HR DPWM is illustrated in Figs. 5 and 6, respectively. To facilitate a variable digital pulse width with a resolution equals to the propagation delay of a single gate, three major components are constructed: a ring oscillator realized using DL, N cells multiplexer, and a xor gate.

The ring oscillator is constructed using a chain of buffers, creating a fixed frequency signal with 50% duty ratio. The frequency out of the ring oscillator is programmable by selecting the number of delay cells, and is expressed as:

$$f_{ring\_osc} = \frac{1}{2Nt_{pd}}, \qquad (2)$$

where N is the number of buffers in series, t_{pd} is the propagation delay of a single cell (approx. 300ps in the current design).

A controlled duty ratio signal is achieved by a xor operation between the first input buffer of the ring oscillator (X[0]) and the n^{th} cell of the ring oscillator (X[n]). Access to n^{th} cell is obtained by a shift register vector that controls the selection bits of the mux. For example, to generate a signal with 30% duty ratio out of 1000-cell string, a xor operation between X[0] to X[300] is carried out. It should be noted that due to the xor action the effective output frequency is twice of f_{ring_osc}.

To facilitate CPM operation, the current reference to the comparator, i_{ref}, is generated by filtering out the high frequency component of the DPWM signal using a simple RC network as depicted in Fig. 1. Since high-resolution can be obtained at relatively high frequencies (e.g. 11bit at 1.6MHz), the low-pass reconstruction using an RC network can be set above the system dynamics without introducing additional pole in the effective frequency range of the system. To avoid sub-harmonic oscillations under steady-state operation for cases that d>0.5, a lower frequency (at the switching frequency) DPWM signal is generated and summed onto the current reference signal using attritional resistor as depicted in Fig. 1. The experimental timing diagram of the current reference DPWM and the resultant slope-compensated reference are shown in Fig. 7.

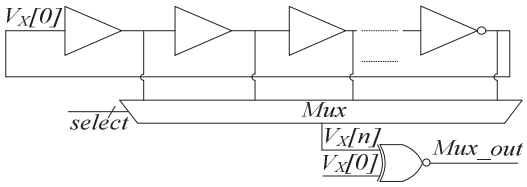

Fig.5. Construction of the FPGA-based HR DPWM

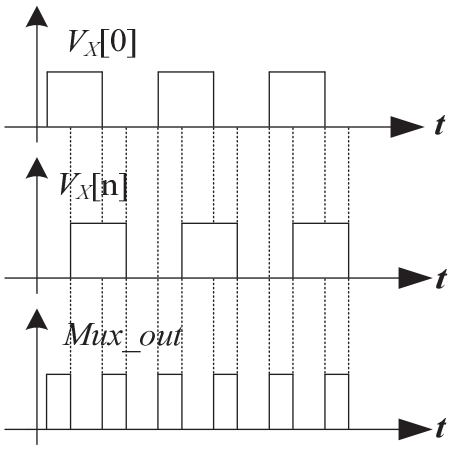

Fig.6. Operation of the FPGA-based HR DPWM

To assure linearity of the relatively long chain of delay elements, the synthesis tool has been assigned with specific timing and placement constraints such that each delay cell has a fixed time-delay throughout the chain. In this particular design, the type of cells that have been utilized as delay elements are of L-type [28].

IV. PI Controller Realization

To complete the controller implementation, a voltage-loop compensator is required. In this study, the compensation scheme has been realized under the assumption that the inner current loop has wider bandwidth than the desired loop dynamics, and that sampling of the output voltage is obtained once per cycle. Under CPM operation, the power stage control-to-output transfer function, taking into account all of the system gains, can be expressed as:

$$A_{OL} = \frac{K_V K_I K_{ADC} K_{PWM} R_L}{sC_{out} R_L + 1} \qquad (3)$$

where K_V and K_I are the voltage and current sensing gains (Fig. 1), respectively, K_{ADC} and K_{PWM} are the gains of the ADC and the DPWM, R_L is the load resistance, and C_{out} is the output capacitance. In this study, a PI compensation scheme has been realized based on the functional diagram of Fig. 8. The discrete-time representation of the PI compensation can be expressed as:

$$v_C = v_{C-1} + K_1 v_e - K_2 v_{e-1}, \qquad (4)$$

where K_1 and K_2 are the PI gains.

V. Experimental Results

An experimental prototype has been built according to Fig. 1. A 12V to 48V, 100W, boost converter that operates at switching frequency of 100KHz has been examined (L=150µH, C_{out}=75µF). For the target converter, 8 bits ADC resolution has been found sufficient, resulting in approximately 10mV resolution. CPM operation using a 12bit current reference signal and slope compensation has been verified. The controller has been implemented on a Cyclone IV FPGA – Altera (EP4CE115F29C7) [28], and requires only 6500 logic elements (for the entire controller design as described throughout the paper) allowing its implementation with only a 7% of the resources of a low-cost FPGA system.

Figure 9 shows the response of the experimental CPM controlled boost converter to 25W to 80W to 25W load transient. As can be observed, a well regulated response is obtained with dynamic performance that is comparable to other reported CPM controllers, with the advantages of fully digital design with very low gate count realization.

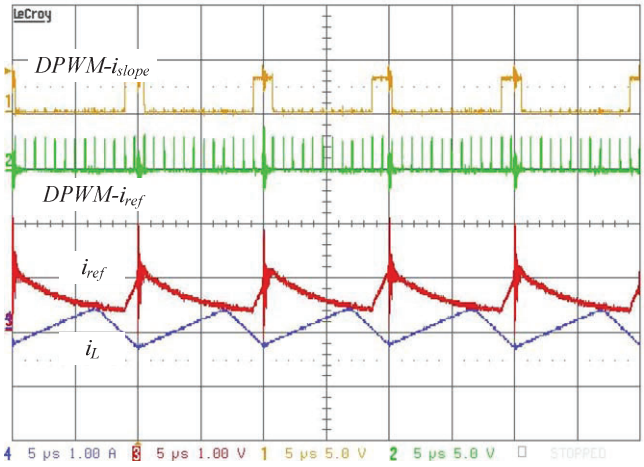

Fig.7. Operation of the experimental slope-compensated current reference signal generation

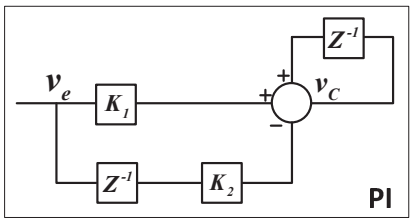

Fig.8. PI compensation scheme.

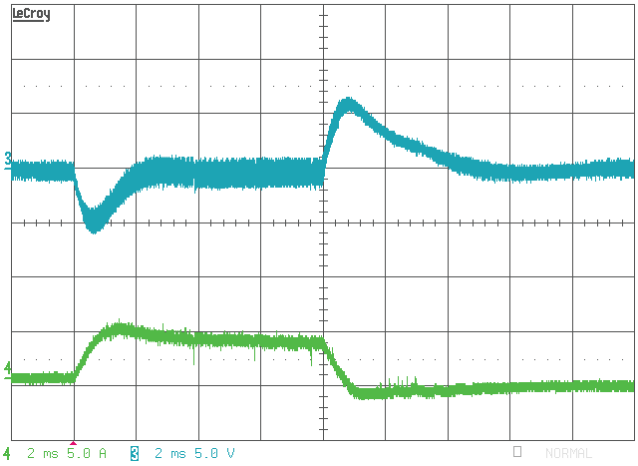

Fig.9. Experimental load transient response (25 W to 90 W to 25 W) of the CPM controlled boost converter using the new controller. Ch.3(upper trace): the ac component of the output voltage, 5V/div; Ch.4 (bottom trace): inductor current, 5A/div. The time scale is 2 ms/div.

VI. Conclusion

An FPGA-based PWM/CPM digital controller with newly developed peripherals that are suitable for FPGA implementation was developed. A new DL-ADC design has been presented with verified performance of 10bit and conversion rate of 300ns. The HR DPWM has been constructed based on a delay line architecture as well, producing 300ps with the current FPGA implementation.

The entire controller realization (compensator and peripherals) requires a relatively modest amount of logic elements, allowing a cost-effective CPM solution.

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