

Improving Loading and Unloading Transient Response of a Voltage Regulator Module Using a Load-Side Auxiliary Gytrator Circuit

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Abstract— This paper introduces a new voltage regulator module (VRM) that hybrids a highly efficient switched-inductor converter as the main unit with a load-side switched-capacitor based converter to assist during load transient events. The resulting hybrid-VRM exhibits improved dynamic performance for both loading and unloading transient events, while maintaining a compact design with reduced stress of the components. The hybrid controller that has been developed allows operation based on output voltage measurement alone, further reducing the circuit complexity. The operation of the VRM is verified on a 30W, 12V-to-1.5V prototype, demonstrating a near-ideal transient recovery.

Index Terms— Voltage regulation module, switch-mode power supply, improved transient-response, optimal control, digital control, auxiliary circuit

I. INTRODUCTION

In recent years there has been a sharp rise in interest and demand for more compact, light, energy efficient and economical voltage regulation solutions. In particular, tighter output voltage regulation, faster response times and lower volume are of major concern in the design of present-day voltage-regulator modules (VRM). For processing power from fractions of a watt to several tens of watts with fast transient performance, multi-stage interleaved converters combined with analog controllers have been predominantly used [1]-[5]. There, fast response is usually achieved by designing a wide bandwidth control loop.

The advancement in hardware-efficient digital controllers [6]-[9] enabled the implementation of advanced nonlinear control methods that improve the dynamic performance and, as a consequence, drastically reduce the size of the output capacitor. Among them, time-optimal control (TOC) [10]-[16] and minimum-deviation [17] controllers have demonstrated transient response with virtually the smallest possible voltage deviation, restricted only by the inductor's slew-rate. In VRM applications, this limitation has a major effect on the output voltage deviation for the case of an unloading transient event, primarily due to the high input-to-output conversion ratio. Another weakness of the classical time-optimal approach is the relatively higher current stress, beyond the steady-state value, that is required to restore the lost charge of the output capacitor during the recovery time [16],[18]. As a result, the overall power processing efficiency is impacted from consecutive transients, when compared to steady-state.

State-of-the-art solutions that exceed the performance of the time-optimal control method propose several circuit extensions to the original buck converter in order increase the inductor's slew-rate [19]-[22]. For example, extensions have

been presented by addition of a fast auxiliary converter in parallel to the main converter with smaller inductance [23] or with active region current injection circuit [24]. However, it comes at the cost of an increased input filter since the load transient is reflected to the input. This is partly resolved by compensating only for half of the current mismatch, which does not increase transient time [25].

Recent studies have reported improved loading and unloading transient performance, obtained using an auxiliary converter connected to the output side [26]. An independent energy bank is used, eliminating the impact on the input. Although the solution requires additional sensors to regulate the auxiliary operation and is limited by switching frequency to mid-range output voltages, it provides a new concept to improve the performance of VRMs and, therefore, is adopted in this study.

A recently-developed resonant switch-capacitor based gyrator converter (GRSCC) presented in [27] demonstrated an ultra-compact voltage regulator solution which obtains ideal transient response [28]. However, a modest efficiency (around 85%) at steady-state is achieved due to high rms currents. Nonetheless, its main advantage is that no magnetic element is required, allowing on-chip integration.

The objective of this study is to introduce a new compact VRM solution that *hybrids a buck converter with a resonant switched-capacitor auxiliary circuit that is connected at the load side*, as detailed in Fig. 1. By incorporating a new control concept, the auxiliary circuit effectively mimics increased capacitance during loading and unloading transient events,

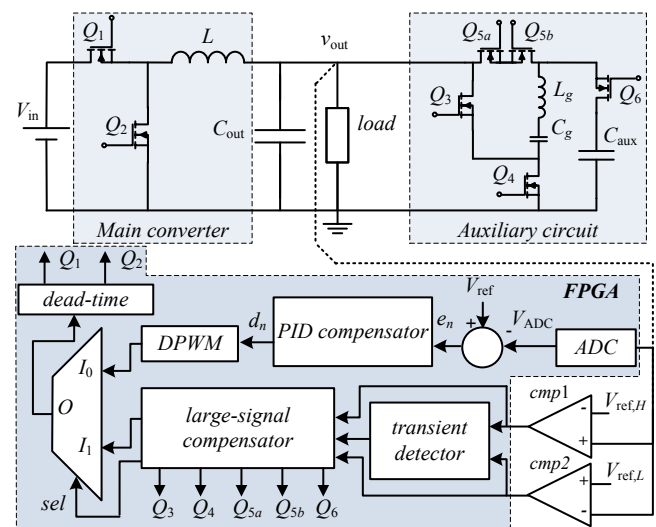


Fig. 1 Hybrid-VRM with load-side GRSCC auxiliary circuit. The area within the bottom box is implemented within an FPGA.

reducing the burden on both the input and output filters, and reduces the current stress. In addition, the hybrid-VRM presented in this study *requires indication from the output voltage alone*, making this solution simple and cost-effective.

The paper is organized as follows: Section II describes the effect of different auxiliary current profiles on the transient-recovery performance, Section III discusses the improvement in power-processing efficiency. The implementation of the GRSCC as an auxiliary circuit is delineated in Section IV. Next, the details of the control scheme for the hybrid-VRM are detailed in Section V. Experimental results and conclusions are then provided in Sections VI and VII, respectively.

II. TRANSIENT RECOVERY BY A LOAD-SIDE AUXILIARY CIRCUIT

A key factor for assisting the recovery of the main converter from a load transient is the capability of the auxiliary circuit to rapidly sink or source the current mismatch between the new load state and the main inductor current. To analyze the required behavior and control mechanism of the auxiliary unit, an idealized bi-directional current source that is connected to the output terminals of the voltage regulator can be assumed as depicted in Fig. 2.

The analysis is aided by Fig. 3 which shows average waveforms for different sinking patterns of the current source to a current unloading step of ΔI_{out} . It is further assumed that a time-optimal-like control is implemented for the main converter to maximally expedite the recovery phase.

To eliminate any deviations of v_{out} from the steady-state value, V_{out} , the auxiliary circuit is to mimic infinite capacitance, i.e. mirror the mismatch between i_{buck} and i_{load} . As shown in Fig. 3(a), the auxiliary current, i_{aux} , is triangular, ramping down from ΔI_{out} and reaching zero when i_{buck} equals i_{load} . In this case, the total transient time, T_{tr} , is governed by the main inductor's slew-rate and current mismatch, and can be expressed as:

$$T_{tr,\text{loading}} = \frac{L}{V_{\text{in}} - V_{\text{out}}} \Delta I_{\text{out}}, \quad T_{tr,\text{unloading}} = \frac{L}{V_{\text{out}}} \Delta I_{\text{out}}, \quad (1)$$

where L is the main inductor value and V_{in} is the input voltage. This case produces a significantly shorter transient time than obtained using classical time-optimal control approach since no additional discharging is required to drain excess charge from C_{out} .

Realization of an auxiliary unit as described by Fig. 3(a), rated for the peak load current is, to some extent, overly designed. It requires higher stress-rating components to accommodate for stress that exists for slight fractions of the transient time. Furthermore, an ideal response with zero voltage deviation is not an objective of a VRM. Since some amount of voltage deviation is still tolerable by standard, even in tight VRM applications [29], a more conservative approach can be taken. As shown in Fig. 3(b), improved unloading transient recovery, provided some allowed deviation margins, can be achieved by a constant current sinking profile of $I_{\text{aux}} = \Delta I_{\text{out}}/2$. It can be seen that although v_{out} initially deviates from V_{out} , it is fully restored at T_{tr} . In the aforementioned cases the current source sinks an identical charge within T_{tr} , meaning that initial under-current is ultimately balanced by over-current at the second half of the transient. Considering a maximum allowable overshoot of ΔV_{out} and the greatest possible load change ΔI_{max} , C_{out} can be sized as follows:

$$C_{\text{out}} = \frac{\Delta I_{\text{max}}^2 L}{8 \Delta V_{\text{out}} V_{\text{out}}} \quad (2)$$

When compared to TOC, the shorter transient times and the smaller initial current mismatch are in favor of a hybrid-VRM, resulting in C_{out} which is four times smaller.

The method shown in Fig. 3(b) reduces the complexity of the auxiliary circuit compared to the method in Fig. 3(a), however, it requires a fairly accurate estimation of the load current. To overcome this obstacle, a recovery pattern as shown in Fig. 3(c) is suggested. In this method the auxiliary

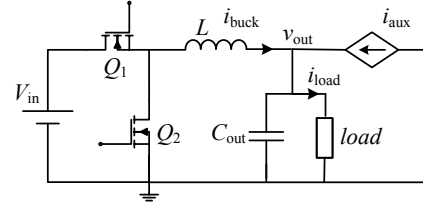


Fig. 2 Simplified circuit with the auxiliary circuit modelled as a controlled current source, demonstrating the current relationships towards the load.

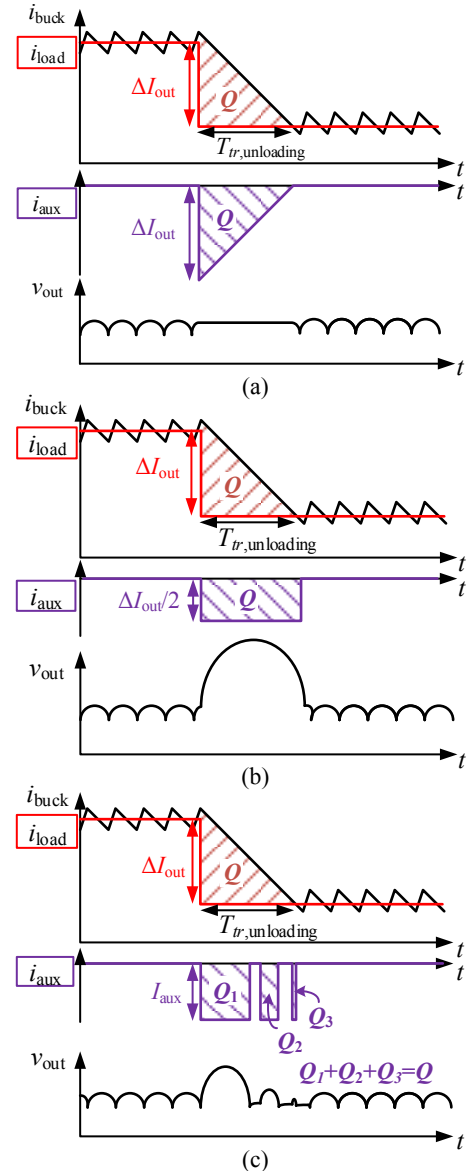


Fig. 3 Schematic response waveforms of the hybrid-VRM to an unloading step of ΔI_{out} for different auxiliary behaviour. (a) $i_{\text{aux}} \approx i_{\text{load}} - i_{\text{buck}}$, (b) $I_{\text{aux}} = \Delta I_{\text{out}}/2$, (c) $I_{\text{aux}} > \Delta I_{\text{out}}/2$, segmented to match the overall charge Q .

current is set to $I_{aux} = \Delta I_{max}/2$ (by design) while the instantaneous ΔI_{out} is unknown. As long as $I_{aux} \geq \Delta I_{out}/2$, the resultant total transient time remains T_{tr} , governed by the main inductor's slew-rate.

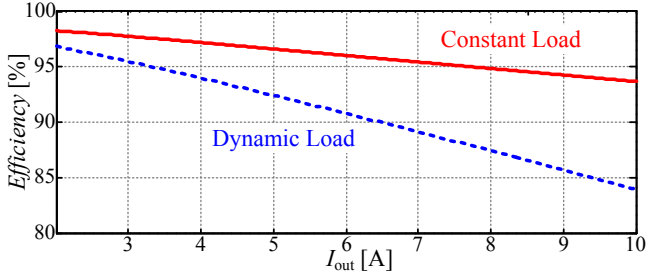


Fig. 4 Power processing efficiency of a buck converter connected to a constant load, versus a 50kHz dynamic load with the same average current, 50% load duty-cycle (see Fig. 5). Series resistance is 10m Ω .

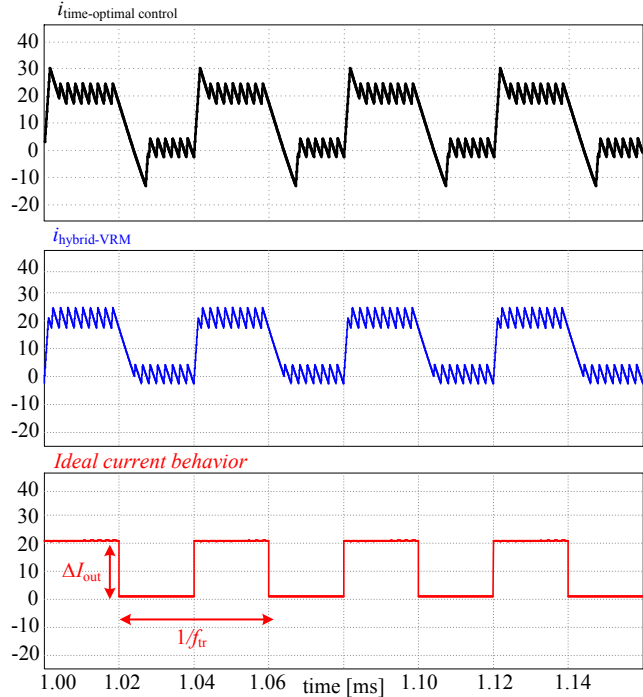


Fig. 5 Inductor current waveforms for time-optimal control (top), hybrid-VRM (middle) and ideal inductor behavior (bottom)

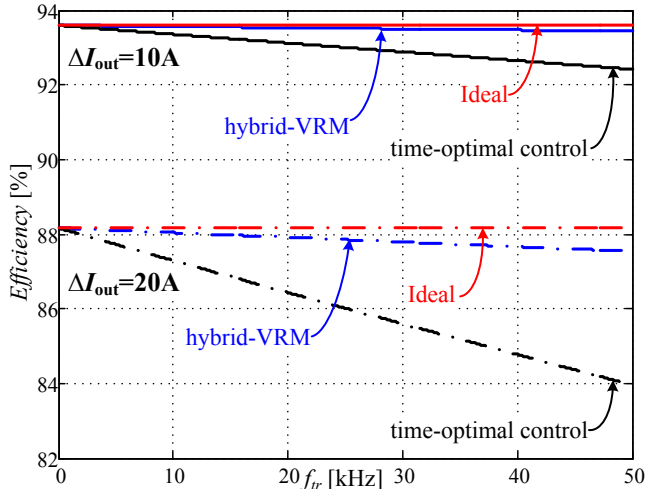


Fig. 6 VRM efficiency as a function of load transient rate for two load-step magnitudes. $R_{loss}=10m\Omega$, switching losses are not considered.

The design of an auxiliary source that compensates for $\Delta I_{max}/2$ provides two main advantages: 1) the transient controller can be realized based purely on sensing the output voltage and without additional current sensing, and 2) the conditions for the end-of-transient are within the main inductor's slew-rate for any given transient, without the need for extra time to reestablish the steady-state voltage.

III. POWER PROCESSING EFFICIENCY

Present-day efficiency estimations for dc-dc converters are performed with general assumption of steady-state operation as the dominant working condition, defined here as static conversion efficiency. Neglecting switching losses and assuming steady-state operation, the main contributor for the conduction losses is the average inductor current since the rms current of the ripple component is negligibly small [30].

These estimations for the efficiency are relatively accurate for most applications in which the load is static or mostly-static. However, for modern applications with continuously varying loading conditions, the static conversion efficiency estimation might fail to predict the actual losses and as a consequence the required thermal design of the system. Fig. 4 shows comparison of a typical static efficiency curve compared with a dynamic loading one, for a similar average output power. As can be observed, the deviation of the static efficiency estimation from actual one significantly increases with the load repetition rate. It should also be noted that the situation worsen for applications with relatively high conversion ratios, such as the VRM case.

To analyze the converter efficiency under varying load conditions, three cases are compared as shown Fig. 5: an ideal inductor current behavior, time-optimal control [11] and beyond time-optimal one [18] which is adopted in this study. To focus on the difference between the controllers types, it is assumed that all methods are governed by an identical steady-state control law.

Without loss of generality, the analysis to obtain the rms value of the inductor current for all cases is carried out under the assumption of a repetitive load transient with magnitude of ΔI_{out} and repetition rate of f_{tr} and duty ratio of 50%. For the time-optimal control case, the rms value of the inductor current can be expressed as (3), where I_{min} is the load current at light load, $I_{min} + \Delta I_{out}$ is the load current at heavy load, ΔI_{ripple} is the inductor's steady-state current ripple and D is the steady-state duty cycle, i.e. $D = V_{out}/V_{in}$.

Applying the hybrid-VRM control, the peaks, over and under the steady-state value are eliminated, the transient time is reduced, resulting in an rms current of:

$$I_{RMS,hybrid-VRM} = \quad (4)$$

$$\sqrt{\left(I_{min} + \frac{\Delta I_{out}}{2}\right)^2 + \left(\frac{\Delta I_{out}}{2}\right)^2 + \frac{\Delta I_{ripple}^2}{12} + \frac{\Delta I_{out} L (\Delta I_{out}^2 - \Delta I_{ripple}^2)}{12D(V_{in} - V_{out})} f_{tr}}$$

Comparison of the resultant efficiency curves of (3), (4) and the ideal current waveform as a function of the load transients rate is shown in Fig. 6. As can be observed, the elimination of the additional restoration current, i.e. peaks, reduces the overall rms inductor current that in turn increases

$$I_{RMS-TOC} = \sqrt{\left(I_{min} + \frac{\Delta I_{out}}{2}\right)^2 + \left(\frac{\Delta I_{out}}{2}\right)^2 + \frac{\Delta I_{ripple}^2}{12} - \frac{\Delta I_{ripple}^2 \Delta I_{out} L (1 + \sqrt{D} + \sqrt{1-D})}{12D(V_{in} - V_{out})} f_{tr} + \frac{\Delta I_{out}^3 L}{12} \left(\frac{(1 + \sqrt{D})^3 + \sqrt{1-D}^3}{V_{in} - V_{out}} + \frac{\sqrt{D}^3 + (1 + \sqrt{1-D})^3}{V_{out}} \right) f_{tr}} \quad (3)$$

the power processing efficiency.

In addition, another design concern is the inductor sizing. As derived in [16], time-optimal control results in current overshoot of $\Delta I_{\text{out}} \sqrt{D}$ and undershoot of $\Delta I_{\text{out}} \sqrt{1-D}$ during loading and unloading transients of ΔI_{out} , respectively. Since these are eliminated by the hybrid-VRM approach, the sizing of the main inductor reduces as well.

IV. GYRATOR RESONANT SWITCHED-CAPACITOR CONVERTER AUXILIARY CIRCUIT

The GRSCC topology has been recently presented in [27], based on the concept of a resonant switched-capacitor converter, but with the capability to maintain high efficiency over a wide and continuous step-up/down conversion ratio. Thanks to its soft-switching resonant nature it is applicable at high frequencies, and as a consequence, does not require a magnetic element. Furthermore, it has a bi-directional current sourcing behavior and is able to react *immediately* to create current step response with bandwidth of up to half its maximal switching frequency [28].

A voltage doubling variation of the GRSCC has been implemented in this study and is shown as the auxiliary circuit of Fig. 1. It is structured relying on a voltage multiplying resonant switched capacitor converter topology, shifting the GRSCC's optimal efficiency point from V_{out} to $V_{\text{aux}} = 2V_{\text{out}}$. The main reason for the selection of this topology is to increase the power density of the auxiliary storage capacitor C_{aux} by increasing its rated voltage, but without adding voltage stress to the transistors. Another advantage of the doubling realization is that the desired load-side current, i.e. $\Delta I_{\text{max}}/2$, can be obtained by a higher characteristic impedance of the resonant network. This implies that higher target efficiency of the GRSCC can be obtained for a given loop resistance.

The GRSCC is resonant in nature and can be completely halted at zero-current after each cycle. As a result, the nominal current can be resumed within one cycle. In the context of this study, this zero-order step capability enables the GRSCC to be used as the auxiliary current source unit. Moreover, there is no limitation to scalability, the resonant tank values can be determined for any desired V_{out} and operating frequency with further option of interleaved operation. The bridge configuration also guarantees that the maximum stress on any given switch will be around V_{out} , which translates into small area requirements of the power switches.

To further reduce the overall volume of system and enhance the auxiliary circuit efficiency, it is realized in this

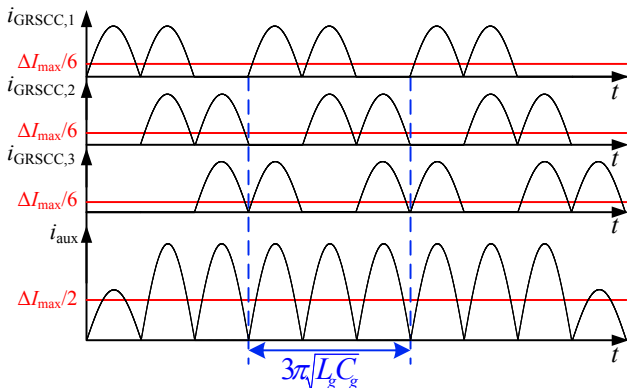


Fig. 7 Distribution of the auxiliary current between three interleaved GRSCCs operating at maximum frequency with half-resonance phase delay.

study using three small interleaved GRSCC modules, each designed to output $\Delta I_{\text{max}}/6$, operating with phase delay of half-resonance period, as demonstrated in Fig. 7. By doing so, the auxiliary circuit rms current is reduced by a factor of $(2/3)^{0.5}$, when compared to a single-converter equivalent since much smaller pulses are evenly distributed over the transient phase, for the same average current. This configuration also increases the accuracy and resolution as a current source. Furthermore, lower current is required per module, allowing higher impedance of the resonant network.

V. HYBRID-VRM CONTROLLER

The configuration of the hybrid-VRM controller is divided into two main units as shown in Fig. 1, a steady-state voltage-mode controller that is entirely implemented on FPGA [31] and a transient-mode controller.

To facilitate fast transient detection and end-of-transient phase, the latter is assisted by two auxiliary comparators with two thresholds, well below the maximum allowed voltage deviation, to determine both loading and unloading events.

A. Principle of operation

The description of the hybrid-VRM controller operation is assisted by Fig. 8 which provides in-detail the response for an unloading transient event.

At $t < t_0$ the controller operates the buck converter with a voltage-mode steady-state compensator whereas the GRSCCs are idle. A load step at t_0 creates current mismatch between i_{buck} and i_{load} resulting in a rise of v_{out} . At t_1 , when v_{out} crosses $V_{\text{ref,H}}$, an unloading event is detected by *cmp1* (Fig. 1) and a transient mode is initiated: Q_2 is turned on to ramp i_{buck} down with the highest slew-rate available. Simultaneously, the GRSCCs are activated to sink excess current and are set to $I_{\text{aux}} = \Delta I_{\text{max}}/2$. Since $\Delta I_{\text{out}} < \Delta I_{\text{max}}$, at instance t_2 , v_{out} returns within the steady-state range below $V_{\text{ref,H}}$, the GRSCCs' operation is halted while Q_2 remains on, however, i_{buck} is still larger than i_{load} . This results in the output voltage rising over $V_{\text{ref,H}}$ at t_3 which re-triggers the GRSCCs. When v_{out} is within the steady-state range at t_4 , i_{buck} approximately equals to i_{load} . The end of the transient phase (t_5), in this case, is due to v_{out} crossing $V_{\text{ref,L}}$, detected by *cmp2*.

The information on the end-of-transient is derived, in this study, from the output voltage measurement by observing the comparator states. However, the information that is obtained from the output voltage indicates on the current charge state of the output capacitor and not directly on the current mismatch

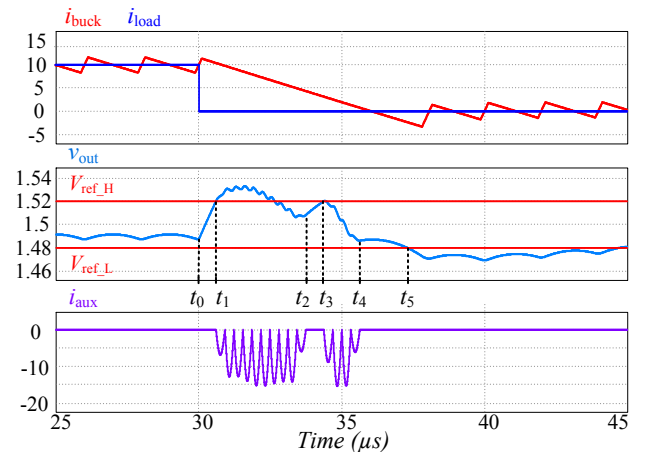


Fig. 8 Simulation results for the response of the hybrid-VRM to an unloading event.

between i_{buck} and i_{load} . Given the example of Fig. 3(c), it can be observed that the output voltage is momentarily restored to the steady-state value without reaching the point that i_{buck} equals i_{load} . The reason for this is that the charge balance has been achieved by the aid of the auxiliary circuit.

To overcome the problem of premature indication on the end-of-transient, without additional current sensors, a state-machine algorithm described by the flowchart of Fig. 9, was developed. The controller monitors the output voltage by observing the comparator states. When v_{out} returns within the steady-state thresholds, the GRSCCs are immediately halted whereas the buck converter remains in transient mode. In case that a current mismatch still exists, the output voltage is shifted back beyond the boundaries, and the auxiliary circuit is re-triggered. A true end-of-transient indication (i.e., i_{buck} is in the vicinity of i_{load}) is verified by either one of the necessary conditions: (a) the comparators state has been inverted from the original transient-mode trigger, or (b) a preset time has elapsed since the auxiliary circuit was halted without change in the comparator states.

B. Comparators thresholds settings

A finite voltage difference between the comparators thresholds is required to prevent the controller from falsely entering or exiting the transient mode. To prevent false entry, it is sufficient to satisfy that the voltage difference between the thresholds is well above the steady-state voltage ripple and accounting for additional noise errors (e.g. ESR, switching noise, and measurement errors). However, to prevent a false indication of the comparators state and an early return to the steady-state mode, the difference between thresholds should be set such that the largest voltage deviation generated from a single discharge cycle of the auxiliary circuit is kept within the threshold boundaries. The largest value for this deviation occurs when current mismatch is small ($i_{\text{buck}} \approx i_{\text{load}}$), that is:

$$V_{\text{ref,H}} - V_{\text{ref,L}} \geq Q_g / C_{\text{out}} = 4V_{\text{out}} C_g / C_{\text{out}}, \quad (5)$$

where Q_g is the charge delivered from the auxiliary circuit during a single discharge cycle and C_g is the GRSCC resonant tank capacitor. Selection of the voltage detection window according to (5) assures that the voltage-drop due to a single gyrator pulse is contained within threshold levels.

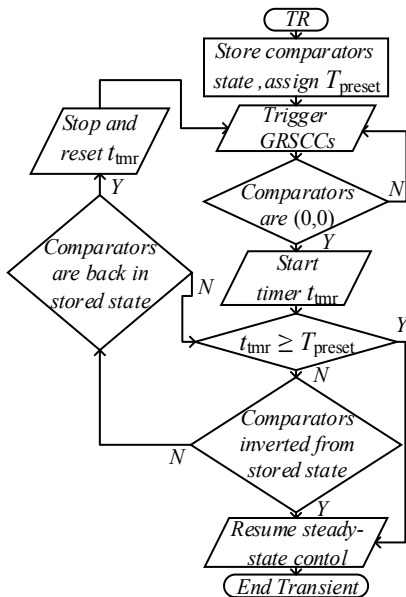


Fig. 9 Flowchart of the end-of-transient algorithm

C. Auxiliary circuit halt time - T_{preset}

As described earlier, steady-state operation may be resumed by either inversion of the comparators state or after specific time has elapsed since the auxiliary circuit was halted (T_{preset} in Fig. 9). Given the controller sequence when steady-state is resumed, and an estimation on the range of error for the buck inductor current at that instance, the preset time can be set to assure that the steady-state operation is restarted without creating additional oscillations. In this study, it is defined that the first switching action of the steady-state controller is the opposite of the one obtained in the non-linear mode, i.e. resuming from an unloading event starts with an on state, whereas an on state during a loading event is followed by an off state. This implies that the preferred instance to switch back to the steady-state is when the inductor current has passed the target load current value since less error in the inductor current is accumulated by the following switching action. The ideal case would be at the point that the inductor current is beyond the load value by $\Delta I_{\text{ripple}}/2$, then the steady-state current is already within the target margins within the first switching action. Since this case cannot be guaranteed by voltage sensing alone, it is essential to map the range of the possible error in the current with respect to the preset halt time.

Fig. 10 shows a zoomed-in view to the preset instance, describing i_{buck} within two worst-case scenarios. The time index, t_{last} , indicates the instance of the last trigger event of the auxiliary circuit. The lower boundary of the inductor current is characterized as the condition when the inductor current reached the load current at t_{last} , given by:

$$i_{\text{buck,min}}(t_{\text{last}} + t) = I_{\text{load}} + at, \quad (6)$$

where a is the slope of the buck inductor current during the transient, given by:

$$\begin{aligned} a &= -V_{\text{out}}/L, & \text{unloading} \\ a &= (V_{\text{in}} - V_{\text{out}})/L, & \text{loading} \end{aligned} \quad (7)$$

The upper boundary of the inductor current is due to an additional charge injection by the auxiliary circuit, Q_g , at the instance of t_{last} , given by:

$$i_{\text{buck,max}}(t_{\text{last}} + t) = I_{\text{load}} - a \sqrt{\frac{2Q_g}{|a|}} + at. \quad (8)$$

Equating (8) to I_{load} and solving for t , yields the necessary condition to assure that the worst-case inductor current has

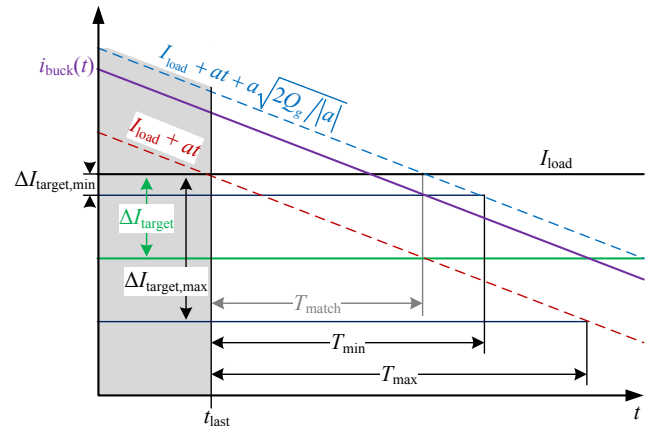


Fig. 10 Possible range of the buck inductor current around the T_{preset} instance.

reached the load current, that is:

$$T_{\text{match}} = \sqrt{2Q_g / |a|}, \quad (9)$$

namely, the auxiliary circuit has completed its operation for the particular transient mode.

To further reduce the error of the inductor current to the allowed range of $\{\Delta I_{\text{target,max}}, \Delta I_{\text{target,min}}\}$, a target time range for return to steady-state is specified, as shown in Fig. 10. Equating (6) to the lower current boundary and (8) to the upper one, yields the margin criterion, T_{min} and T_{max} , for T_{preset} as:

$$\begin{aligned} T_{\text{min}} &= \Delta I_{\text{target,min}} / |a| + \sqrt{2Q_g / |a|} \\ T_{\text{max}} &= \Delta I_{\text{target,max}} / |a| \end{aligned} \quad (10)$$

It should be noted that it is required to assure that the defined T_{preset} satisfies the conditions in (10) and the minimum time condition in (9), that is,

$$\max(T_{\text{min}}, T_{\text{match}}) \leq T_{\text{preset}} \leq T_{\text{max}} \quad (11)$$

Furthermore, to avoid dependence of T_{preset} on the converter parameters and present dependence on the design considerations alone, (9) and (10) can be reorganized as:

$$\begin{aligned} T_{\text{min}} &= \frac{\Delta I_{\text{target,min}} (1-D)}{KI_{\text{nom}} f_s} + \sqrt{\frac{\Delta I_{\text{max}}}{KI_{\text{nom}} f_s f_g}} \\ T_{\text{max}} &= \Delta I_{\text{target,max}} (1-D) / KI_{\text{nom}} f_s \\ T_{\text{match}} &= \sqrt{\Delta I_{\text{max}} / KI_{\text{nom}} f_s f_g} \end{aligned} \quad (12)$$

where f_s is main converter switching frequency and f_g is the GRSCC maximal frequency, I_{nom} is the nominal load current at steady-state, and $K = \Delta I_{\text{ripple}} / I_{\text{nom}}$ is the proportionality factor between the ripple and nominal currents. The criterion for a loading event can be extracted in a similar manner.

D. Auxiliary Capacitor Voltage Reset

The amount of energy that is processed by the auxiliary circuit during a transient event depends on the conversion ratio of the buck converter. In this study of a 12V to 1.5V converter, during an unloading transient more charge is processed by the auxiliary circuit than during a loading transient of a similar magnitude. To maintain the ability to sink or source sufficient current from the output capacitor, prevent C_{aux} from overcharging, and restore excess energy, a reset procedure for the

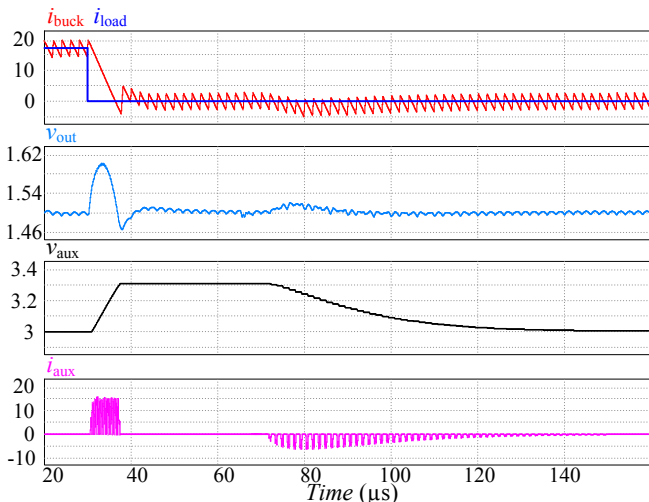


Fig. 11 Simulated unloading transient followed by a reset of v_{aux} back to $2V_{\text{out}}$

independent auxiliary capacitor is essential.

A key consideration in the design of the reset procedure is to avoid interference with the desired steady-state operation of the main converter, i.e., that the reset procedure will not cause a significant change of the output voltage. This implies that the auxiliary circuit reset current has to sink or source sufficiently small amount of charge per pulse and to be distributed over a longer period of time compared to the total load transient time. To this end, in this study, one of the three GRSCC modules is further employed during the steady-state phase to balance the auxiliary charge and reset the capacitor voltage back to its target value. Since the output voltage is well-regulated by the steady-state controller, the module is allowed to operate as a classical open-loop resonant switched-capacitor converter, forcing the auxiliary capacitor to converge to $2V_{\text{out}}$, without any additional sensors. To limit the average current injected by the module during the reset phase, the effective operating frequency can be reduced by additional time delay between RSCC cycles [32].

Fig. 11 can be used to demonstrate the reset procedure. It shows an unloading transient that causes v_{aux} to rise due to the current sinking operation. It is then followed by a reset performed using one GRSCC module operating as a RSCC at lower effective frequency which restores v_{aux} back to the target value of $2V_{\text{out}}$. It can also be observed that the voltage-mode control law maintains v_{out} within its steady-state margins.

VI. EXPERIMENTAL VERIFICATION

In order to validate the operation of the hybrid-VRM, a 30W 12-to-1.5V prototype was built and tested, with a measured peak efficiency of 90%. The auxiliary circuit was realized by three interleaved GRSCCs as described in Section III. Table I lists the component values and parameters of the experimental prototype. The digital controller comprises a steady-state voltage-mode control and a transient-mode control and was realized on an Altera Cyclone IV FPGA [33]. Steady-state control is assisted by integrated high-performance ADC and DPWM on-FPGA realizations as described in [31]. Load transient signals were also generated by the FPGA, independently, without synchronization to the controller.

TABLE I – EXPERIMENTAL PROTOTYPE VALUES

Component	Value
Input voltage V_{in}	12 V
Output voltage V_{out}	1.5 V
Main inductor L	0.5 μH
Output capacitor C_{out}	200 μF
Buck converter switching freq. f_s	500 kHz
GRSCC maximal switching freq. f_g	~1 MHz
Auxiliary capacitor C_{aux}	30 μF
GRSCCs resonant tank capacitor C_g	0.5 μF
GRSCCs resonant tank inductor L_g	~20 nH
Number of GRSCC stages	3

Fig. 12 shows the system's response to various loading and unloading transient events of 10A and 15A, in comparison to a buck converter operating under TOC, using same transient detection circuit. Fig. 12(a) shows the system's response to an unloading transient event of 10A (15A to 5A). The performance of the system results in output voltage overshoot of 60mV and settling time of 4μs, compared with 150mV and 8μs using TOC as shown in Fig. 12(b). The system response to a larger, 15A unloading step (20A to 5A), is given in Fig. 12(c). A voltage overshoot of 100mV and a total transient time

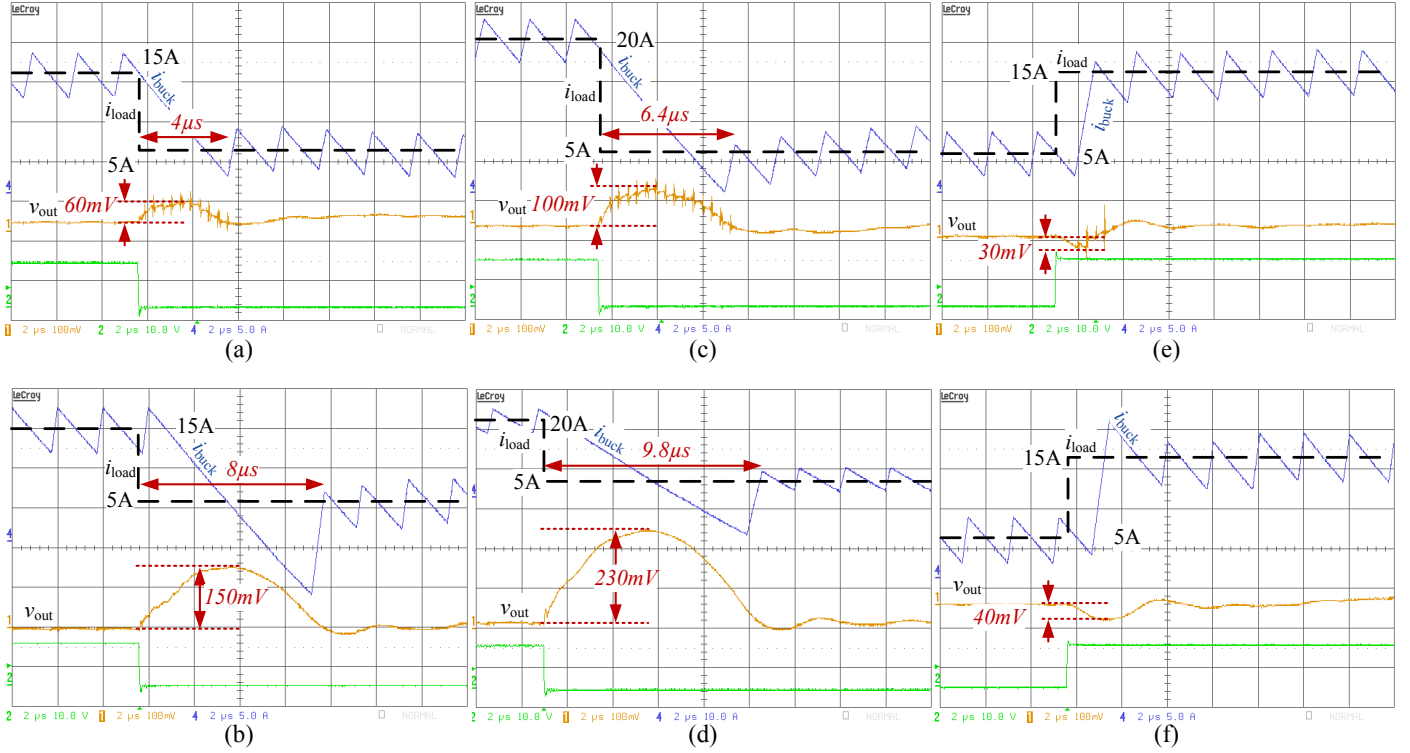


Fig. 12 Experimental results showing transient response of the hybrid-VRM [(a),(c),(e)], versus TOC [(b),(d),(f)]. Signals from top to bottom: i_{buck} (5A/div, dashed line marks the output current step), v_{out} (100mV/div.), and load-step signal. Time scale is 2µs/div. (a),(b) 15-5A unloading event, (c),(d) 20-5A unloading [for (d) i_{buck} is 10A/div], (e),(f) 5-15A loading.

of 6.4µs are measured, compared to 230mV and 9.8µs using TOC, as depicted in Fig. 12(d). A loading transient event of 10A (5A to 15A) is depicted in Fig. 12(e). As can be observed, the voltage undershoot of 30mV is mainly dominated by the inherent delay added by the transient detection circuit. It should be noted that in the loading event, the auxiliary GRSCCs were operated synchronously rather than phase-delayed due to the large conversion ratio of the VRM, resulting in a higher slew-rate of the inductor current. The same loading event using TOC results in a similar undershoot of 40mV, again, due to the delay of the transient detection circuit delay.

Fig. 13 shows the system's response to a consecutive loading-unloading event of 10A (5A to 15A to 5A). The resulting overshoot and undershoot are similar to the specific cases presented by Fig. 12(a) and Fig. 12(c), respectively. Fig. 14 shows the auxiliary reset procedure, confirming its capability to balance the charge of the auxiliary capacitor without affecting the steady-state operation.

VII. CONCLUSIONS

A voltage regulator module with improved loading and unloading transient response has been presented. The improvement has been achieved by the addition of a load-side auxiliary circuit that comprises three interleaved converters, implemented using a recently presented GRSCC topology. This VRM has the potential to be space conserving and cost-effective when implemented into an IC design. The output capacitance is significantly reduced at the cost of small additional semiconductors and few capacitors, and does not require ferromagnetic elements.

The experimental results exemplify the performance of the design for both loading and unloading events, reducing output overshoots by up to 60% and transient time by up to 50% compared to time-optimal control, without affecting the input side. In particular for the relatively high conversion ratio case,

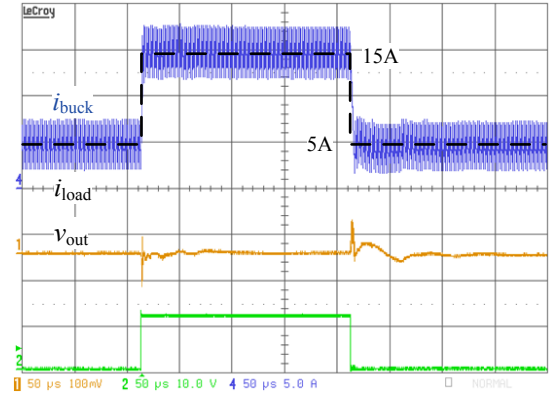


Fig. 13 Screenshot demonstrating the hybrid-VRM's response to a loading followed by an unloading transient event of 5-15-5A. Signals are consistent to as in Fig. 11, with a time-scale of 50µs/div.

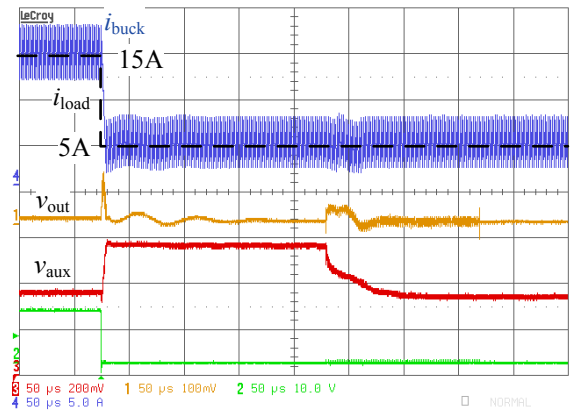


Fig. 14 Experimental results showing an auxiliary reset procedure that follows an unloading transient. Signals from top to bottom: i_{buck} (5A/div, dashed line marks the output current step), v_{out} (100mV/div.), v_{aux} (200mV/div.), and load-step signal. Time scale is 50µs/div.

significant improvement has been demonstrated in the response to an unloading event, compensating for the moderate current slew rate of the buck inductor.

The hybrid-VRM operates autonomously with reduced circuit complexity, i.e. no additional current-sense circuitry or pre-transient information is required. In addition, since no complex mathematical estimations are needed, the complete FPGA implementation for the control (Including the ADC and DPWM peripherals) sums less than 8000 logic elements, providing a cost-effective and simple controller solution.

REFERENCES

- [1] E. A. Burton, G. Schrom, F. Paillet, J. Douglas, W. J. Lambert, K. Radhakrishnan, M. J. Hill, "FIVR — Fully integrated voltage regulators on 4th generation Intel® Core™ SoCs," *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, pp.432,439, 16-20 March 2014
- [2] S. Abedinpour, B. Bakkaloglu, and S. Kiaei, "A multistage interleaved synchronous buck converter with integrated output filter in 0.18 μ m SiGe process," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2164–2175, Nov. 2007.
- [3] G. Schrom, et al., "A 100 MHz Eight-Phase Buck Converter Delivering 12 A in 25 mm² Using Air-Core Inductors," in *Proc. 22nd Annu. IEEE Applied Power Electronics Conf.*, 2007.
- [4] L. P. Dong, D. K. Cheng, M. H. Chow, and Y. S. Lee, "Interleaved three phase forward converter using integrated transformer," *IEEE Trans. Ind. Electron.*, vol. 52, no. 5, pp. 1246–1260, Oct. 2005.
- [5] P.-L. Wong, P. Xu, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 499–507, Jul. 2001.
- [6] P. Midya, P. T. Krein, and M. F. Greuel, "Sensorless current mode control-an observer-based technique for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 16, pp. 522 – 526. 2001.
- [7] Z. Lukić, N. Rahman, and A. Prodić, "Multi-bit Σ - Δ PWM digital controller IC for DC–DC converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron.*, vol. 22, pp. 1693–1707, 2007.
- [8] S. Saggini, P. Mattavelli, G. Garcea, and M. Ghioni, "A mixed-signal synchronous/asynchronous control for high-frequency dc-dc boost converters", *IEEE Transactions Power Electron.*, vol. 55, no. 5, 2008.
- [9] B. Patella, A. Prodić, A. Zirger and D. Maksimović, "High-frequency digital PWM controller IC for DC/DC converters," *IEEE Trans. Power Electron.*, Vol.18, no. 1, pp. 438-446, 2003.
- [10] A. Babazadeh, D. Maksimović, "Hybrid digital adaptive control for fast transient response in synchronous buck DC–DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2625 – 2638, 2009.
- [11] L. Corradini, A. Costabeber, P. Mattavelli, and S. Saggini, "Parameter-independent time-optimal digital control for point-of-load converters," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2235–2248, Oct. 2009.
- [12] A. Babazadeh, L. Corradini, and D. Maksimović, "Near time-optimal transient response in DC-DC buck converters taking into account the inductor current limit," in *Proc. 1st IEEE Energy Convers. Conf. Expo.*, Sep. 2009, pp. 3328–3335.
- [13] V. Yousefzadah, A. Babazadeh, B. Ramachandran, E. Alarcon, L. Pao, and D. Maksimović, "Proximate time-optimal control for synchronous buck DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 2018–2026, Jul. 2008
- [14] L. Corradini, A. Babazadeh, A. Bjeletić, and D. Maksimović, "Current-limited time-optimal response in digitally controlled dc–dc converters," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2869–2880, Nov. 2010
- [15] Pitel, G.E.; Krein, P.T., "Minimum-Time Transient Recovery for DC–DC Converters Using Raster Control Surfaces," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp.2692 - 2703, 2009.
- [16] E. Meyer, Z. Zhang, Y-F. Liu, "An optimal control method for buck converters using a practical capacitor charge balance technique", *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1802-1812, Jul. 2008.
- [17] A. Radić, Z. Lukić, A. Prodić, and R. de Nie, "Minimum deviation digital controller IC for single and two phase dc–dc switch-mode power supplies," in *Proc. 25th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2010, pp. 1–6.
- [18] P.S. Shenoy, P.T. Krein, S. Kapat, "Beyond time-optimality: Energy-based control of augmented buck converters for near ideal load transient response," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE*, pp.916-922, 6-11 Mar. 2011
- [19] D. D. Lu, J. C. Liu, N. K. Poon, and M. H. Pong, "A single phase voltage regulator module (VRM) with stepping inductance for fast transient response," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 417–424, Mar. 2007.
- [20] A. Stupar, Z. Lukić, and A. Prodić, "Digitally-controlled steered-inductor buck converter for improving heavy-to-light load transient response," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2008, pp. 3950–3954.
- [21] S. Ahsanuzzaman, A. Parayandeh, A. Prodić, and D. Maksimović, "Load-interactive steered-inductor dc-dc converter with minimized output filter capacitance," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE.*, Feb 2010, pp. 980–985.
- [22] W. Jing, A. Prodić, W. T. Ng, "Mixed-Signal-Controlled Flyback-Transformer-Based Buck Converter With Improved Dynamic Performance and Transient Energy Recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 970-984, Feb. 2013
- [23] Y. Wen and O. Trescases, "DC–DC converter with digital adaptive slope control in auxiliary phase for optimal transient response," in *Proc. IEEE Appl. Power Electron. Conf.*, Mar. 2011, pp. 331–337.
- [24] V. Svikovic, J. A. Oliver, P. Alou, O. Garcia, and J. A. Cobos, "Synchronous buck converter with output impedance correction circuit," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3415–3427, Jul. 2013.
- [25] E. Meyer, Z. Zhang, and Y. F. Liu, "Controlled auxiliary circuit to improve unloading transient response of buck converters," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 806–819, Apr. 2010.
- [26] Z. Shan, S. C. Tan, and C. K. Tse, "Transient mitigation of dc-dc converters for high output current slew rate applications," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2377–2388, May 2013.
- [27] A. Cervera, M. Evzelman, M.M. Peretz, and S. Ben-Yaakov, "A High Efficiency Resonant Switched Capacitor Converter with Continuous Conversion Ratio," *IEEE Trans. Power Electron.*, in press.
- [28] A. Cervera, M. M. Peretz, "Resonant switched-capacitor voltage regulator with ideal transient response," *Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE*, March 2014, pp. 867-872.
- [29] Voltage regulator module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.0, Intel Corp., Hillsboro, OR, USA, Sep. 2009.
- [30] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer, 2001.
- [31] Y. Halihal, Y. Bezdenezhnykh, I. Ozana, M. M. Peretz, "Full FPGA-Based Design of a PWM/CPM Controller with Integrated High-Resolution Fast ADC and DPWM Peripherals," *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)* 2014.
- [32] M. Evzelman, *Topologies, Losses, and Applications in Switched Capacitor Converters*, PhD dissertation, Ben-Gurion University of the Negev, Beer-Sheva, Israel, Sep 2013.
- [33] DE2 Development and Education Board user manual, Altera Corporation, 2006.