Optimal Design of a Voltage Regulator Based Resonant Switched-Capacitor Converter IC

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***Abstract* — This paper details efficiency analysis and characteristics of a gyrator resonant switched-capacitor converter (GRSCC) operating as a voltage regulator. Following the efficiency analysis, this paper introduces an optimal size-efficiency design procedure for IC realization of the converter. In area-sensitive applications, the optimization method combined with the converter's benefits present an attractive approach for better power delivery concepts for point-of-load (PoL) applications. Based on the optimization principles detailed in this study, an on-chip bridge GRSCC topology has been implemented in 0.18µm 5V CMOS process. The analysis has been verified by post-layout analysis and measurements of the fabricated IC. Neglecting the package limitations, the prototype operation is demonstrated with 10 MHz switching frequency, up to 3A, 4.5 W with 3V input voltage, and the efficiency is measured to be 87%. The study has been extended to survey on effects of the package on the performance. The experimental measurements of the manufactured IC have been found to be in very good agreement with the theoretical analysis and optimization process, as well as to accurately estimate the package contribution to the system performance. In addition, a fully monolithic control system to regulate the output voltage is described and implemented on-chip by an automated synthesis process and place-and route tools.**

I. INTRODUCTION

Present-day microprocessors and other high-performance ICs require an accurate, dynamically scalable supply voltage in the range of 1V and total current of 10s A/chip. In addition to the tight voltage regulation requirements, the area-efficiency factor of the Point-of-Load (PoL) converter is of key importance to assure the desired performance and to be considered reasonable for commercialization. Improvements of the area-efficiency factor of the PoL converter may enable 3-D power delivery architectures [1] where the converter is integrated with the load, significantly enhancing dynamic power delivery capabilities.

Conventional approaches to reduce the total volume of voltage-regulator modules (VRMs) are carried out by increasing the operating frequency to the 100 MHz range [1]-[2]. By doing so, the integration of magnetics and the decoupling capacitors is more convenient. However, the efficiency and total power that can be processed is limited by the static power consumption at high frequencies. Another area saving concept can be facilitated by resonant-mode converters [3]-[6]. By employing soft-switching features, the converter's efficiency is not compromised by the high-frequency operation.

Present-day switched-capacitor technology demonstrated superior power density over switched-inductor converters [7]-[8]. However, it lacks the capability of accurate voltage regulation without the penalty of introducing losses, and its transient characteristics are limited [9]-[12].

A solution that overcomes these challenges is presented in [13]. There, an additional switching state has been added to balance the charge difference between the input and output rather than introducing losses for voltage regulation, creating a *gyrator mode resonant switched-capacitor converter (GRSCC) that disengages the efficiency of the system from the voltage gain*. Utilizing such approach allows on-chip integration at operating frequencies in the range of 10MHz without sacrificing the dynamic performance, further improving the power conversion efficiency.

Classical design of the power processing components for VRMs, considers the converter's mode of operation and especially the conversion ratio to optimize the peak efficiency point to the target parameters. E.g., in a 12V to 1.5V buck VRM, the lower transistor of the synchronous rectifier would be much larger in size than the top transistor to assure higher efficiency at the target voltage. In switched-capacitor converter (SCC) technology on the other hand, symmetry of the power transistors is typically assumed since the output voltage is in proximity to the target one. Based on the existing design tools for SCC, the efficiency characteristics of a GRSCC as a voltage regulator will be in-par with other switched-inductor based candidates since it has not been optimized to the target operation [14].

The objective of this study is to present an *optimal size-efficiency design procedure* for the GRSCC when operating as a voltage regulator (VR), and to define the required sizing of the power transistors (and resonant network) based on the target operating point. It is a further objective of this study to present a fully monolithic GRSCC based voltage regulator that is realized by simple constant on-time Pulse Density Modulation (PDM) control (Fig. 1). The new VR scheme with an optimized power converter demonstrate a reasonably sized

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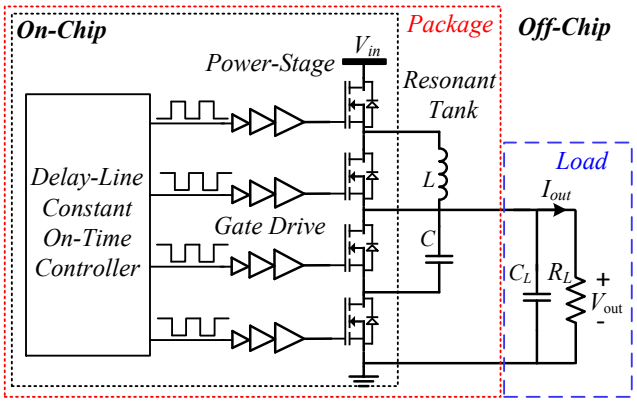

Fig. 1 Circuit diagram of a bridge gyrator mode resonant switched-capacitor converter.

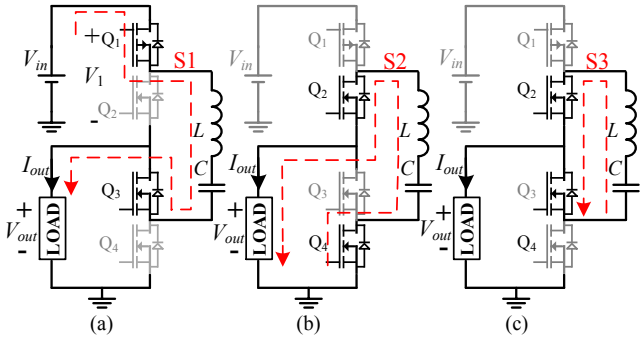

Fig. 2 Bridge GRSCC configuration and operation principle: (a) charge, (b) discharge, and (c) charge balancing.

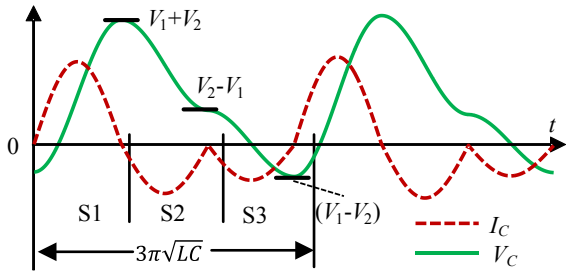

Fig. 3 Typical waveforms of the GRSCC.

solution at much lower operating frequencies and requires virtually no physical inductors, which may be found beneficial for many applications and enable smoother transition towards the 3-D power delivery approach.

The rest of the paper is organized as follows: Section II briefly surveys the GRSCC operation. Section III presents a generalized loss analysis oriented to a desired target conversion ratio. A design procedure and IC implementation are delineated in Section IV. The monolithic delay-line based constant on-time controller is detailed in Section V. Post-layout validation of the converter IC is provided in Section VI. Section VII concludes the paper.

II. Bridge GRSCC Principle of Operation

The GRSCC-based VR, presented in [14], has evolved from the conventional soft-switched resonant SCC configuration [15]-[17]. As in the common bridge design of a voltage dividing SCC [18], the topology includes four switches and a resonant tank. In addition to the classical complementary switching states, demonstrated by Fig. 2a and 2b, a third state is added which introduces a zero-voltage resonant current path (Fig. 2c). This state is used to balance the residual charge of the flying capacitor, i.e. restore the flying capacitor's voltage to its original state by reversing its polarity. The mechanism of polarity reversal (charge balance) lays the foundations to break the rigid connection of input/output voltage and efficiency dependency. Controlling the sequence of the switches governs power flow direction, hence bidirectional operation.

The operation of the converter shown in Fig. 2 is described for one steady-state charge/discharge/balance cycle and is assisted by Fig. 3 that illustrates the capacitor voltage, V_C, and the resonant tank current, I_C, for an arbitrary case of an uneven voltage ratio. By turning Q_1 and Q_3 on, a charge state (S1) is commenced, in which the resonant tank connects to V_{in} while in series with V_{out}, resonantly charging the flying capacitor from a voltage potential of $V_1 = V_{in} - V_{out}$. After a half-resonant cycle, i.e. at zero current, the switches are turned off and followed by the complementary pair, Q_2 and Q_4 (state S2). At this point, the resonant tank connects in parallel to the output and discharges the flying capacitor onto the potential of $V_2 = V_{out}$. In this example $V_2 > V_1$, so when completing S2 after another half-resonant cycle only a portion of the charge is delivered to the output. This results in V_C that is different from its voltage at the starting point of S1. By turning Q_2, Q_3 on (S3), the resonant tank is short-circuited. This creates the required charge-balance and reverses the flying capacitor voltage polarity such that the voltage at the end of S3 equals the voltage at the beginning of S1.

The relationship between I_{out} and V_{in} follows a gyrator behavior [13] and can be expressed as:

$$I_{out} = 2V_{in}fC\,, \tag{1}$$

where f is the repetition frequency of S1-S3. Voltage regulation is obtained by introducing time-delay between consecutive sequences, i.e. PDM [19]-[22], meaning that f can be of any value below the resonant limitation, f_{max}, of:

$$f_{max} = \left(3\pi ZC\right)^{-1} \quad , \quad Z = \sqrt{L/C}\ . \tag{2}$$

III. Loss Analysis

In previous studies, derived from the precursor resonant SCC foundation, symmetrical loop resistances were assumed for all three switching states. While appropriate for most discrete-component realization, in area-sensitive applications and in particular for IC implementation, higher attention should be given to the desired resistance per-loop to obtain the target efficiency. Given a typical operation as described earlier for a case that all three switching phases are dominant, where the inner switches conduct twice per cycle, it may appear that a different organization of the switches' on-resistances results in a higher efficiency from which would be obtained by symmetrical on-resistance organization. An expansion to the loss analysis is detailed in this study.

Assuming a relatively high ratio between the circuit's characteristic impedance to the loop resistance (i.e., quality factor $Q=R_S/Z \gg 5$) of the resonant network, constant output current I_{out}, and neglecting the output voltage ripple, the relationship between the states' rms currents and the average I_{out} can be expressed as

$$\begin{cases} I_{rms,S1} = \left(\sqrt{A\pi R_L/4Z}\right) I_{out} \\ I_{rms,S2} = \left|\sqrt{A\pi R_L/4Z} - \sqrt{A^{-1}\pi R_L/4Z}\right| I_{out} \\ I_{rms,S3} = \left|2\sqrt{A\pi R_L/4Z} - \sqrt{A^{-1}\pi R_L/4Z} - 1\right| I_{out} \end{cases}, \quad \left\{ A = \frac{V_{out}}{V_{in}} \right. \quad (3)$$

where A is the conversion ratio and R_L is the load resistance.

Since the converter operates under ZCS conditions, the dominant contributors to the power dissipation are the conduction losses. To individually identify the per-transistor contribution to these losses, the rms current of the transistors can be written as a function of (3) as:

$$\begin{cases} I_{rms,Q1} = I_{rms,S1} \\ I_{rms,Q2} = \sqrt{I_{rms,S2}^{\ 2} + I_{rms,S3}^{\ 2}} \\ I_{rms,Q3} = \sqrt{I_{rms,S1}^{\ 2} + I_{rms,S3}^{\ 2}} \\ I_{rms,Q4} = I_{rms,S2} \end{cases} \quad (4)$$

As detailed in [23], uniform current distribution results in minimum losses per-area due to even power dissipation. Thus, to minimize losses each transistor should be sized based on the rms current through it. The factor ψ_i defines the required ratio for a transistor's on-resistance (R_{Qi}) with respect to symmetrical operation as:

$$\psi_i = R_{Qi}/R_{sym} = \Sigma I_{rms,Qi}/4I_{rms,Qi} \quad , \; i = 1,2,3,4 \; , \quad (5)$$

where R_{sym} is the nominal resistance at symmetrical partition of the switches.

Assuming the transistors' on-resistances, R_{Q1} through R_{Q4}, are the dominant resistances in each loop, the total loss of the converter as a function of the conversion ratio is derived by summation of the losses [24] as presented in (6) below. Substituting (4) and (5) into (6), and after some manipulations, the efficiency of the converter η as a function of A, R_{sym} and ψ can be expressed as (7).

Fig. 4a shows the resulting efficiency versus conversion ratio curves of (7), for several cases of on-resistance selection and compares symmetrical sizing with an optimized one. As can be observed, in the vicinity of the target voltage ($A=0.5$) where charge-balance of resonant SCC is naturally obtained, the results of both sizing methods coincide. However, as predicted by the initial conjecture, as the conversion ratio deviates from center, a significant efficiency improvement can

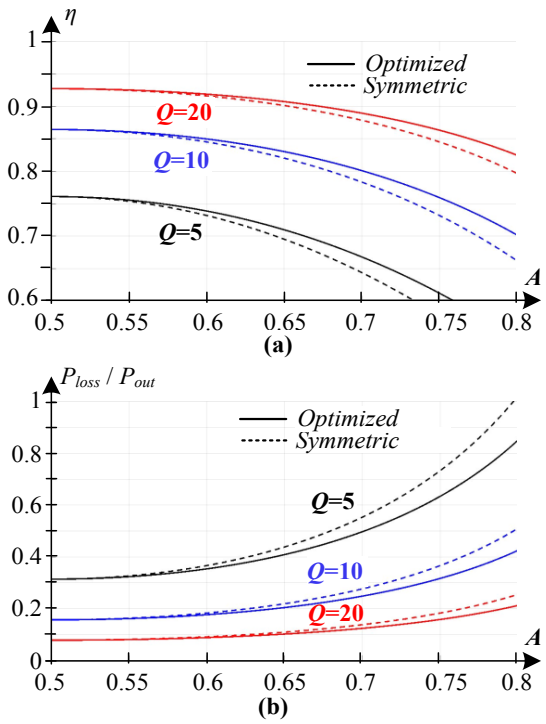

Fig. 4 Theoretical efficiency and losses curves both symmetrical (dotted lines) and optimized (solid lines) partition as a function of A, for various values of Q: (a) efficiency, (b) P_{loss} vs P_{out}.

be observed in favor of the optimized sizing method. An even more interesting is the power losses factor that is depicted in Fig. 4b, showing the possible power saving as a result of better area distribution between the transistors. For example, in conversion ratio of 0.75, $Q=10$ and output power of 10W, 0.5W of the losses can be trimmed down for the same total area. Alternatively, this implies that if certain power dissipation is allowed, the converter can be further reduced in size.

IV. Design Procedure and IC Implementation

Using the above analysis and observations, generalized IC design guidelines of a voltage regulator GRSCC are provided and then followed by practical power-stage IC sizing and realization. The procedure is as follows:

a. Given target values for $V_{in,min}$, $I_{out,max}$ and operating frequency, f_{max}.

b. Calculate the resonant network parameters C and L by:

$$C = I_{out,max}/2V_{in,min}f_{max} \; , \; L = \left[\left(3\pi f_{max}\right)^2 C\right]^{-1} \quad (8)$$

c. From the desired efficiency η and conversion ratio A,

$$P_{loss} = \frac{\pi R_L}{4Z} I_{out}^2 \left[\left(R_{Q1} + R_{Q2} + 2R_{Q3}\right)\frac{A}{1-A} + \left(R_{Q4} + 2R_{Q2} + R_{Q3}\right)\frac{1-A}{A} - 2\left(R_{Q2} + R_{Q3}\right) \right] \quad (6)$$

$$\eta = \left[1 + \frac{\pi R_{sym}}{4Z} \left(\left(\psi_1 + \psi_2 + 2\psi_3\right)\frac{A}{1-A} + \left(\psi_4 + 2\psi_2 + \psi_3\right)\frac{1-A}{A} - 2\left(\psi_2 + \psi_3\right) \right) \right]^{-1} \quad (7)$$

calculate the symmetrical sized resistance R_{sym}:

$$R_{sym} = \frac{\left(\eta^{-1}-1\right)}{\frac{\pi}{4Z}\left[\left(\psi_1+\psi_2+2\psi_3\right)\frac{A}{1-A}+\left(\psi_4+2\psi_2+\psi_3\right)\frac{1-A}{A}-2\left(\psi_2+\psi_3\right)\right]} \quad (9)$$

d. Calculate ψ_i from (5) and determine the optimized on-resistances by:

$$R_{Qi} = \psi_i R_{sym} \quad (10)$$

e. The individual silicone width per transistor can be directly derived from R_{Qi}:

$$W_i = K' L_g / R_{Qi}, \quad (11)$$

where K' can be found by the values that are given by the vendor's process design kit (PDK) and L_g is the gate length. The total transistors' silicone width is obtained by summing W_i.

A design procedure example is demonstrated by 0.7W GRSCC with target values of: $V_{in,min}$=3V, V_{out}=0.7V, $I_{out,max}$=1A, f_{max}=10MHz, η=80%. The resonant network values are calculated as $C \approx$ 17nF and $L \approx$ 6.7nH. The required resistances are: R_{sym}≈17.5mΩ; or R_{Q1} through R_{Q4}: 53mΩ, 11mΩ, 18.5mΩ, 14.5mΩ. Given a 0.18µm CMOS process, $K' \cdot Lg$≈3mΩ, the resulting total width is $W \approx$ 685,700µm. Fig. 5 depicts an efficiency prediction for the design example. It can be observed that for the same silicon area efficiency improvement by approximately 3% can be obtained at nominal input voltage of 3.3V. A more noticeable benefit can be viewed in terms of size, where 20% less silicon area is required to obtain the same efficiency.

A. On-Chip Power-Stage Implementation

The selection of the transistor type depends primarily on the driver type. Assuming a conventional ground-referenced driver and that the input voltage is limited to the technology voltage V_{DD}, a pMOS is used for Q_1, while nMOSs are used for Q_2, Q_3, and Q_4, based on the required gate-source threshold voltage to activate the transistor.

To increase current handling capabilities of a 5V CMOS process transistor, paralleled multiple unit cells are realized, as shown in Fig. 6. The size of the device with multiple unit cells is typically defined in terms of the gate boundary $W_i = N_{fi} W_g$, where N_{fi} is the number of fingers for a transistor Q_i, and W_g is the gate width. N_{fi} can be expressed as:

$$N_{fi} = R_{on} A_{eff} / W_g L_g R_{Qi} \quad (12)$$

Given the PDK W_g and L_g constraints, an accurate and efficient quadrilateral layout of the power-stage can be applied. It should be noted that the transistors are connected via a top metal pad, resulting a relatively low parasitic resistance of the conduction and is neglected for the design.

B. Driver Circuitry Implementation

A fully integrated circuit based buffers with the ability to drive transistors with large gate width is implemented. Buffers logic implementation is realized by logical effort technique, including a network of three custom designed buffers for each switch. The ratio between the pull-up network and the pull-down network is $\beta = 1.5$. In the context of driving power transistors, the buffers sizing should also be considered due to the relatively higher input capacitances of the buffers chain. To assure a non-distorted input gate signal, the first inverter of the chain has been matched in size to the analog input unit. Fig. 7 shows in detail a sized example of a driving stage, where $W_{g,P} = 1.5 \cdot W_{g,N}$. It should be further emphasized that the sizing characteristics such as gate capacitances are technology-dependent, which should be taken into account to assure proper drive signal.

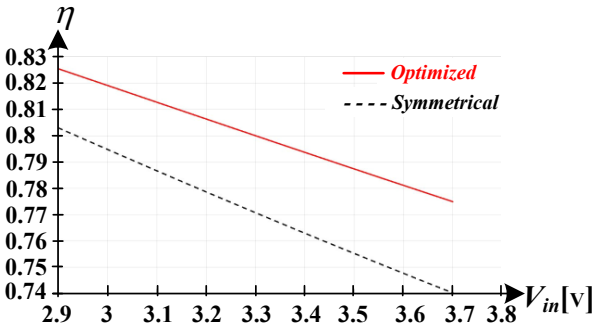

Fig. 5 Efficiency curve of GRSCC as function of V_{in} symmetric and optimized partition, with the target parameters: V_{out}=0.7V, $V_{in,min}$=3V, $I_{out,max}$=1A, f_{max}=10MHz.

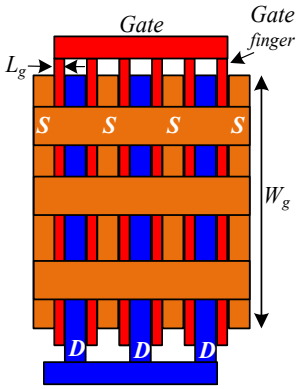

Fig. 6 Simplified structure of a device with paralleled multiple cells.

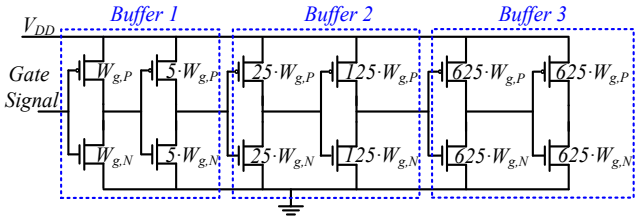

Fig. 7 Schematic of the implemented IC drive circuitry.

Explained above, since the driver stage is integrated and the control signals are all ground referenced (with gate voltage swing between 0 to 5V), neither isolation nor level shifters are required. Even for a worst case scenario where $V_{in} = V_{DD}$, the driving circuit is still functional.

C. Package and Bonding Wires Limitations

On-Chip interconnections ultimately connected to the board level via IC packaging. Bond wires technique is extensively used in IC packaging designs, because of its relatively lower

cost and simple implementation [25]. Bond wires usually consist of copper, aluminum, gold and silver, while each material has its own electrical and physical characteristics. The bonding is usually farther away from the substrate and therefore has less coupling and loss at high frequencies, still bonding wires can be a major limiting factor in IC design, in particular for high current ICs. The thin and narrow bonding wires are a significant penalty to the conduction losses. In the context of a soft-switched converter, these are the dominant contributors to efficiency reduction. Advances in power semiconductor technology further highlight the limitations of bond wires packaging technology, since the losses contribution by resistances and parasitics of the package and the bond wires exceed those of the silicon die [26]. Performance improvement solutions by means of packaging were detailed in [26]-[29]. However, these technologies require high cost specialized resources and processes. It should be noted that the packaging and bonding wires implementation are beyond the scope of this study.

V. Monolithic Delay-Line Based Constant On-Time Controller

A fully monolithic internal controller has been designed to regulate the output voltage. As described in [14], regulation is facilitated using a single comparator which compares the output voltage to an internal value and triggers the GRSCC when needed. Fig. 8 shows the main components of the control unit. A flip-flop based state-machine (SM) synchronically dictates the active state and out of six options: The three switching states (S1-S3), two intermediate dead-time states (D2, D3) necessary to prevent shoot-through between complementary switches, and an inactivity state (S0). The state-machine is clocked by a configurable delay-line (DL), which enables an individual predefined time length for each state. Once triggered by a comparator (unmasked only at state S0 when inactive for a predefined time value), the DL is activated and triggers the SM to produce the required logic sequence for the GRSCC. Fig. 9 shows a measured experimental gate logic sequence operating at ~3MHz produced from the monolithic DL controller.

VI. Post Layout and Experimental Verification

Following the design procedure, an IC prototype that implements the bridge GRSCC voltage regulator has been designed and fabricated. To demonstrate the operation of the IC GRSCC and to verify the theoretical analysis, the Post-Layout design of the power-stage and driver circuitry was verified using Cadence Spectre simulator in 0.18µm 5V CMOS process. R_{on} of the power transistors was designed to value of ~20mΩ (layout shown In Fig. 10). The chip consists of 11-pins and connects to a resonant tank of 2.25nH, 50nF. With the ability to operate at 10MHz, the GRSCC can produce up to 4.5W (1.5V, 3A) from a 3V input. The gate signals are transmitted through an analog input unit and buffers matching network to obtain the desired drive voltage for the converter's power-stage. The timing controller was implemented by an automated synthesis process and place-and route tools, directly from the VHDL representation. Fig. 11 shows the flying capacitor current and voltage waveforms and the gate logic signals that were obtained by cycle-by-cycle post-layout

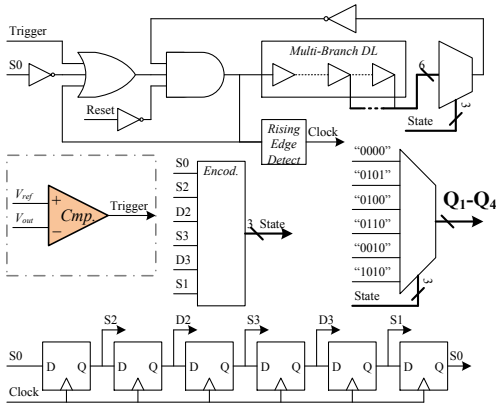

Fig. 8 Schematic of a delay-line based constant on-time controller.

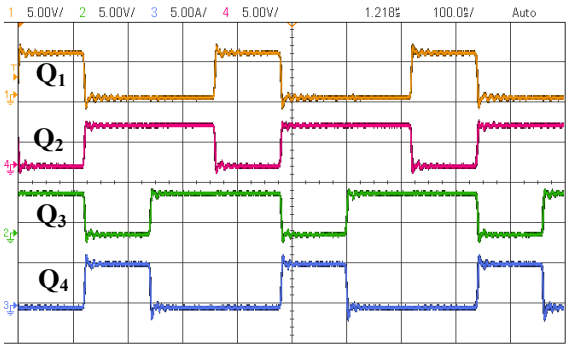

Fig. 9 Experimental gate signals produced from the monolithic controller.

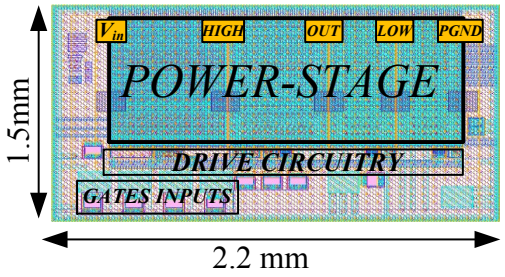

Fig. 10 Chip layout 2 mm x 1.5 mm.

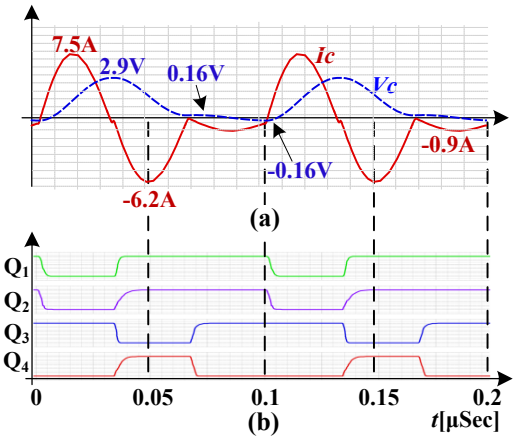

Fig. 11 (a) Flying capacitor voltage and current waveforms. The circuit parameters are V_{in}=3V, V_{out}≈1.5V, R_{loop}≈40mΩ, C=50nF, L=2.25nH; and (b) gate logic signals

simulation. The system has been tested under open-loop conditions and the waveforms verify operability of the design. The efficiency is measured to be 87% (excluding drive losses). Operating under the above specifications, the converter IC is capable to output power up to 4W. These results are in very good agreement with the theoretically predicted efficiency of 85%-90%.

The fabricated IC prototype was packaged using 24-pin 4x4mm QFN package, where 11 pins were in use for the GRSCC. A chip micrograph is depicted in Fig. 12a. The chip connects to a resonant tank of C=100nF and L=6nH. The inductance is realized by stray inductances by the connection and interconnections from the chip to the flying capacitor, Fig. 12b depicts the IC prototype on PCB.

Experimental measurements of the packaged IC converter resistances resulted in approximately 160mΩ per loop, or effective R_{on} of a single transistor is ~80mΩ. Kelvin resistance measurements to cancel out the package effect resulted in resistance of 20mΩ per transistor. These measurements clearly exhibit the bond wires and package limitation, in this case by four times than the targeted R_{on}. Considering these limitations, the best-case experimental results were obtained at maximum switching frequency of 4.5 MHz producing up to 2.25W. The actual quality factor is measured to around 2 and the resulting efficiency is measured to be 67%. Table I summarizes the IC prototype experimental measurements. Fig. 13 shows open loop measured and post-layout simulated results of the capacitor current and voltage.

Efficiency curve of the converter IC as function of V_{in} is depicted in Fig. 14. The experiment was carried out by varying the input voltage and manually compensating with the frequency, such that the output power and the input voltage, 2.25W and 1.5V, respectively, were kept constant. The experimental measurements tightly follow the results obtained by the simulation as well as the theoretical predictions. As can be observed, lower efficiency can be obtained for higher input voltages. This is primarily due to higher conduction losses at higher conversion ratios. Fig. 15 shows the efficiency of the converter IC as a function the output current, I_{out}. As can be seen, in light-load operation there is a discrepancy between the experimental and simulation results from the theoretical analysis, this is due to the resonant characteristics of the three states that are not identical, which was not taken into the theoretical model analysis. The experimental measurements also highlighted the advantage of the GRSCC operating at light loads, at 20mA the efficiency drops only at 4%.

TABLE I – SUMMARY OF IC PROTOTYPE EXPERIMENTAL MEASUREMENTS

Specifications	***Value / Type***
Package	4x4 QFN - MLP
V_{in}	3V
R_{on}	~80mΩ
V_{out}	1.5V
I_{out}	1.5A
Off Chip resonant tank	6nH, 100nF
Switching Frequency	4.5MHz
Quality Factor Q	~2
Efficiency	67%

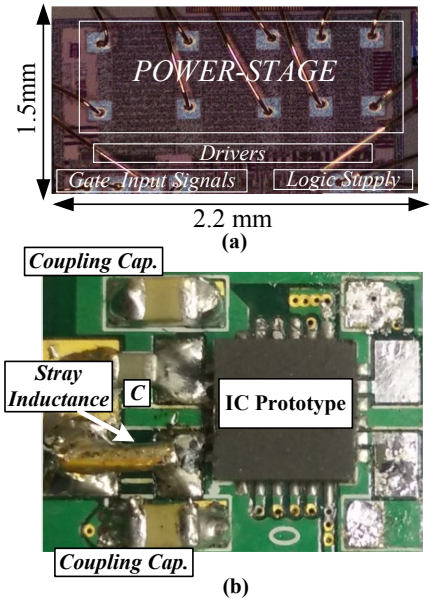

Fig. 12 (a) Chip micrograph of Bridge GRSCC, (b) IC prototype on PCB.

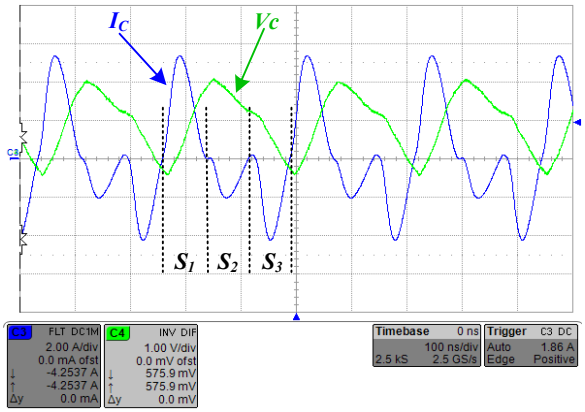

Fig. 13 Flying capacitor voltage and current waveforms including the packaging limitations. (a) Experimental ,(b) Post-Layout.

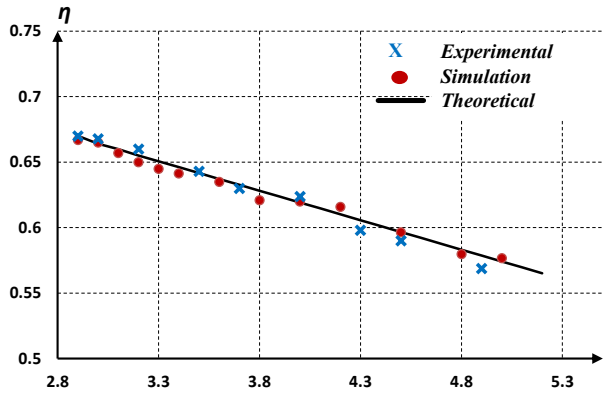

Fig. 14 IC GRSCC efficiency as a function of input voltage, V_{in}, while R_{loop}=160mΩ.

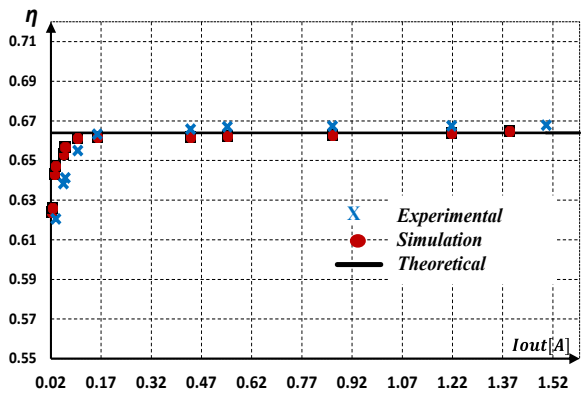

Fig. 15 IC GRSCC efficiency as a function of load current, I_{out}, while R_{loop}=160mΩ.

VII. Conclusion

A bridge gyrator resonant-switched capacitor converter IC and optimization methodology have been presented. The detailed efficiency analysis and characteristics of the GRSCC operating as a voltage regulator have been explored. An optimal size-efficiency design procedure and considerations based on the target values of operation are introduced. The effectiveness of the design procedure is verified with a fully monolithic GRSCC fabricated in 0.18µm CMOS process, the analysis was meticulously verified by post-layout simulations and the results are in very good agreement with the theoretical predictions and the efficiency is measured to be 87%. In addition, a fully monolithic control system is described and implemented on-chip to regulate the output voltage of the converter IC.

The experimental results highlighted the significance of packaging and bonding wires limitations. Due to the additional parasitic resistances of the packaging, the experimental tests were slightly different than the targeted. For the given package limitations the obtained measurements from the manufactured converter IC are in very good agreement with the presented optimization procedure. The experimental measurements also further strengthen the advantages of the GRSCC ability to maintain virtually constant efficiency curve for load variations, in particular when operating at light loads. At 20mA loading, the efficiency drops only at 4%. Future work direction would include packaging and wiring optimization to assure absolute certainty of final design.

Significant area saving highlights the benefit of the optimization method, providing a simple and efficient procedure to improve the size-efficiency factor based on the target operating conditions. Combined with the topology benefits, a GRSCC voltage regulation scheme presents an attractive alternative to the switch-inductor converters, in particular in area sensitive application, and establishes the foundations for better power delivery concepts for PoL applications.

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