Closed-Loop Design and Time-Optimal Control for a Series-Capacitor Buck Converter

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***Abstract*— This paper explores the large-signal and small-signal dynamics of a series-capacitor (SC) buck-type converter and introduces an optimal closed-loop control scheme to accommodate both the steady-state and transient modes. As opposed to a conventional buck converter, where time-optimal control is realized by a single on-off cycle, in the SC-buck topology there is a need to distribute the switching phases to satisfy the charge-balance of the flying capacitor. The new control method hybrids a voltage-mode small-signal controller for steady-state operation and a non-linear, state-plane based transient-mode control scheme for load transients. A detailed principle of operation of the SC-buck converter is provided and explained through an average behavioral model and state-plane analysis. The operation of the controller is experimentally verified on a 12W 12V-to-1.5V converter, demonstrating voltage-mode control operation as well as time-optimal response for load transients.**

Keywords— Time-optimal control, state-space control, dc-dc converters, voltage regulation

I. Introduction

In recent years, a significant effort is made to enhance the performance of voltage regulator modules (VRMs) for high-performance ICs that operates with low supply voltage and high current. Tighter voltage regulation, high efficiency, and accommodating load transient are key factors in the design of the switch-mode power supplies (SMPS), in particular for high step-down conversion ratio applications. Several converter topologies and circuit extensions have been discussed in the literature to minimize the size of passives and improve the dynamics of the VRM. One direction of VRM implementation is based on multi-phase interleaved converters, allowing high frequency operation and size reduction at the cost of complex control for current sharing [1]-[2]. Another approach is by multi-level converters where the lower component stress allow better sizing of the components and efficiency improvements [3].

The series capacitor (SC) buck converter, also known as a double step-down two-phase buck converter, originally presented in [4] and recently revised in [5]-[6], merges an interleaved buck converter with a switched-capacitor front-end and by doing so allows high-frequency operation in the MHz range and better system dynamics with reduced stress on the components. Additional attractive features of the SC-buck converter are natural current balancing between phases and effectively doubles the pulse width, which make it suitable for large conversion ratio applications.

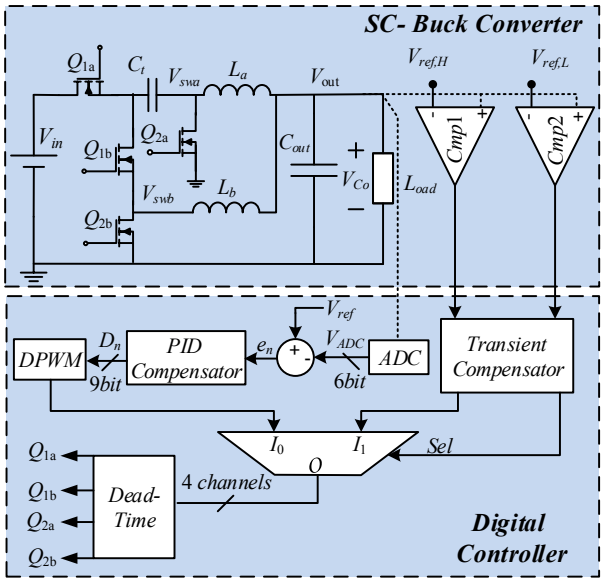

Fig. 1. SC-buck converter and a hybrid controller

Recent studies have quantified the attributes of the SC-buck topology at high frequency [7] and demonstrated improved light load efficiency when operating in DCM [8]. Further extensions presented a two-phase, four-inductor, converter which emphasizes its current balancing feature when the power is distributed between multiple phases [9]. In spite of all the major benefits for this topology, neither closed-loop operation nor dynamic analysis for controller design have been investigated to-date. It would be further advantageous to examine the converter suitability for time-optimal controller assignment in order to be considered attractive for VRM applications.

The objective of this study is therefore to investigate the dynamic features of a SC-buck converter and *to introduce an optimal closed-loop controller that hybrids a small-signal controller for steady-state operation and a time-optimal control scheme for load transient*, as detailed in Fig. 1. In this study, two modeling approaches are presented, the first by an average-behavioral model to examine the control-to-output response and design a small-signal voltage-mode controller. The second technique is to obtain a state-space representation which will be the basis for the design of a non-linear time-optimal controller for loading transient. The latter is

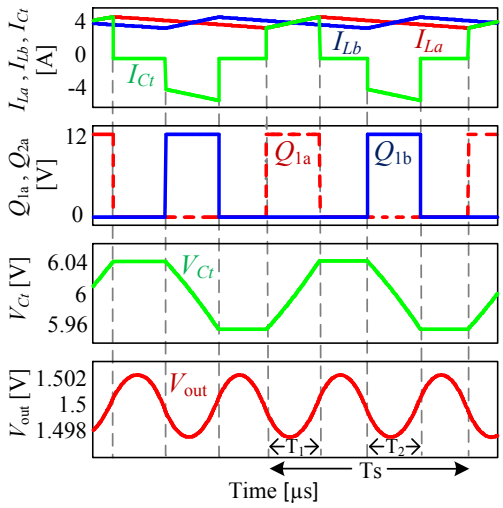

Fig. 2. Typical waveforms of a SC-buck converter. Case study of 12V-1.5V.

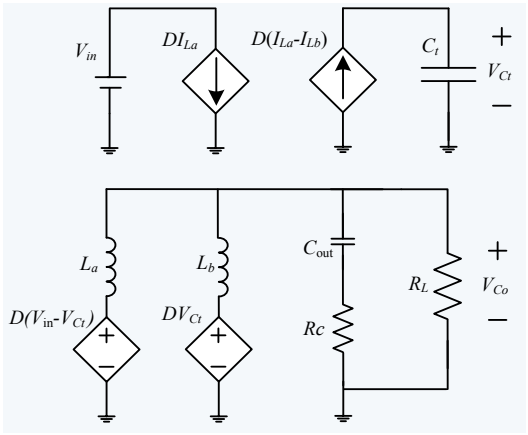

Fig. 3. Average-behavioral model of the SC-buck converter

significantly more challenging in the context of the SC-buck converter since it involves combined operation of two pseudo-balanced converters.

The rest of the paper is organized as follows: Section II describes the steady-state operation of the converter, extracts an average-behavioral model representation, and provides a design procedure of a small-signal voltage-mode compensation scheme. Section III provides a state-space analysis and a time-optimal control of the SC-buck converter. Experimental validation is presented in Section IV. Section V concludes the paper.

II. Steady-State Operation and Voltage-Mode Controller

The description of the SC-buck converter is assisted by topology and typical waveforms, as shown in Fig. 1 and 2, respectively. The steady-state operation is similar to that of an interleaved, two-phase buck converter with a slight difference that the back-end converter is fed by a flying capacitor C_t that is charged to approximately $V_{in}/2$. The duty ratio for both phases (a and b) is identical and each phase is time-interleaved with a 180-degree phase delay. As a result, four switching-states are identified. State-1, Q_{1a} and Q_{2b} are on, resulting in V_{swa} equals $V_{in}/2$ and the inductor current I_{La} ramps up with a slope of $(V_{in}/2\text{-}V_{Co})/L_a$ and I_{Lb} ramps down with a slope of $-V_{Co}/L_b$. In state-2, Q_{1a} is turned off, Q_{2a}, Q_{2b} are on, and the operation resembles a conventional buck converter in off state. In state-3 Q_{2a} and Q_{1b} are on, the flying capacitor C_t, acts as the source, and the inductor current I_{Lb} ramps up with a slope of $(V_{in}/2\text{-}V_{Co})/L_b$ while I_{La} ramps down with a slope of $-V_{Co}/L_a$. State-4 is identical to state-2. Charge balance of C_t is naturally maintained by this operation allowing both charge and discharge action per cycle [4], this naturally stabilizes V_{Ct} to half the input voltage.

Following the switching sequence and assuming CCM operation, the behavioral operation of the converter is obtained by averaging [10]-[11]. The average voltage across the inductors, $\langle v_{La} \rangle$, $\langle v_{Lb} \rangle$ and the average capacitor current $\langle i_c \rangle$ can be expressed as:

$$\langle i_c \rangle = D_1 i_{La} - D_2 i_{Lb}, \quad (1)$$

$$\langle v_{La} \rangle = D_1 (V_{in} - V_{Ct}) - V_{out}, \quad (2)$$

$$\langle v_{Lb} \rangle = D_2 V_{C_t} - V_{out}, \quad (3)$$

where $D_1=T_1/T_s$ and $D_2=T_2/T_s$ are the duty ratios related Q_{1a} and Q_{2a} conduction time, respectively. V_{out} is the output voltage.

Fig. 3 shows a graphical representation for an average-behavioral model as described by (1)-(3). Assuming that $D_1=D_2$ and applying small-signal linearization, the full control-to-output dynamic expression can be obtained. To simplify the expressions, V_{Ct} is assumed constant by small-ripple approximation [12], resulting in a control-to-output expression of the form:

$$\frac{v_{out}}{d}(s) = \frac{\frac{V_{in}}{2}\left(sC_oR_c+1\right)}{s^2\frac{C_o\left(L_a \parallel L_b\right)}{R_L}\left(R_L+R_c\right)+s\left(C_oR_c+\frac{L_a \parallel L_b}{R_L}\right)+1}. \quad (4)$$

As can be observed from (4), this expression is similar to the control-to-output response of a classical 2-phase buck converter. The frequency response of (4) is presented in Fig. 4 along with the required compensator that its design is detailed in the next sub-section.

Closed-Loop Discrete-Time Compensator Design

To satisfy the requirements for loop-gain stability and high bandwidth, the crossover frequency f_c of the closed-loop system is chosen to be greater than the double pole frequency by approximately 50% while the target phase margin is set above 45°. Based on the control-to-output behavior, the setting of the target parameters in this way guarantees suitability for PID compensation scheme [13]. The extraction of the PID coefficients (a,b,c) is based on the methodology that has been presented in [14] with minor adjustments to a frequency-domain design. The design procedure is as follows:

1) Specify the crossover frequency f_c and the phase margin of the desired closed-loop $A_{CL}(s)$ frequency response based on a knowledge of the control-to-output response $A(z)$.

2) Obtain the denominator of $A_{CL}(z)$ by a pole-zero matching *s*-to-*z* transformation.

3) Derive the numerator of $A_{CL}(z)$ such that the closed-loop response is of second order system [14].

4) Derive the transfer function of an ideal compensator $B_{ideal}(z)$ that yields the desired closed-loop response.

5) Obtain the response of a template PID compensator $B_{PID}(z)$ from the first three samples of the ideal compensator $B_{ideal}(z)$ by evaluation of difference equations.

The designed PID compensator has been validated through Matlab simulations as a full closed-loop system with a 12-to-1.5 V SC-buck converter, operating at 1.25 MHz (L_a=L_b=0.6 µH; C_f=10 µF; C_o=50 µF). The target closed-loop parameters were crossover frequency of 60 KHz and phase margin of 45°. Fig. 4 shows the frequency response of the converter (blue), the *1/B* of the PID compensator (red) and the loop-gain (green). It should be noted that higher bandwidth could be obtained by higher gain settings of the compensator or by different target specifications. However, since large transients are accommodated by an optimal controller, a conservative crossover frequency of 50% beyond the double pole location has been satisfactory for steady-state regulation.

III. State-Space Representation and Time-Optimal Control

To enhance the load transient performance of the SC-buck converter, it is essential to obtain the information of the possible state-trajectories that are available for the converter to recover to the new steady-state operating point after a load transient. Since in this study, a small-signal compensator is assumed for steady-state operation, the objective of the transient controller is to minimize the recovery time of the converter and as a result minimizing the output voltage deviation, i.e. time-optimal control [15]-[18]. Unlike a conventional two-phase buck converter, in the SC-buck converter case, charge balance of the flying capacitor must be satisfied during the transient time to allow smooth transition back to the steady-state operation. This implies that the 'simple' on-off time-optimal cycle as carried out by many applications would not hold in this case and, as a matter of fact, would worsen the overall performance.

To realize the required switching sequence, the first task is to map the behavior of the state-variables with respect to the new loading conditions [19]-[20], then the required switching sequence can be derived from the possible trajectories of the state-variable. The state equations for state-1 can be expressed as:

$$\frac{dV_{C_o}}{dt}=\frac{1}{C_o}(I_{L_a}+I_{L_b}-\frac{V_{C_o}}{R_{\text{out}}}), \tag{5}$$

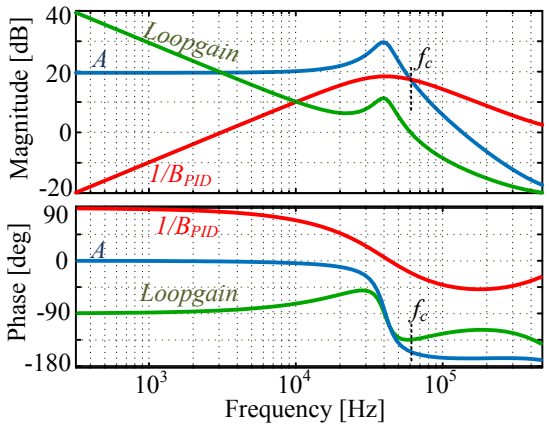

Fig. 4. Frequency responses of: control-to-output A, inverse compensator $1/B_{PID}$, and the Loop-Gain. Crossover frequency is marked f_c.

$$\frac{dI_{L_b}}{dt}=-\frac{V_{C_o}}{L_b}, \tag{6}$$

$$I_{L_a}=I_{L_b}(0)-\frac{L_a}{L_b}\frac{V_{in}/2-V_{c_o}}{V_{c_o}}\left(I_{L_b}-I_{L_b}(0)\right), \tag{7}$$

where $I_{La}(0)$ and $I_{Lb}(0)$ are the inductors currents at the beginning of state-1. As can be seen in (7), the current difference of I_{La} - $I_{La}(0)$ depends on the current difference of I_{Lb} - $I_{Lb}(0)$. Substituting (7) and (6) into (5) yields:

$$\frac{C_o}{3}V_{C_o}{}^3-L_b\frac{I_{L_b}}{R_{out}}V_{C_o}{}^2+\left(I_{L_b}{}^2L_b+I_{L_a}(0)I_{L_b}L_b-I_{L_b}(0)I_{L_b}L_b\right)V_{C_o}+ \\ +C_{\text{onstant}}+L_bV_{in}\left[\frac{I_{L_b}(0)I_{L_b}}{2}-\frac{I_{L_b}{}^2}{4}\right]=0 \tag{8}$$

where C_{onstant} is defined by the initial values of I_{Lb} and V_{Co}. $I_{La}(0)$ and $I_{Lb}(0)$ are the inductors currents at the beginning of state-1. The first solution of this function yields the state-1 trajectories of the converter in the form of V_{Co}=$f(I_{Lb})$ with three initial conditions: $I_{La}(0)$, $I_{Lb}(0)$ and $V_{Co}(0)$.

By symmetry in the operation of state-3 to state-1and proper variable assignment, the state-trajectories are derived from (8). The variables are assigned as: V_{Cf}=V_{in}/2, I_{La} swaps with I_{Lb}, and L_a swaps with L_b. States 2 and 4 are the off states and identical. The states' equations can be expressed as:

$$\frac{dV_{c_o}}{dt}=\frac{1}{C_o}\left(I_{L_a}+I_{L_b}-\frac{V_{c_o}}{R_{\text{out}}}\right), \tag{9}$$

$$\frac{dI_{L_a}}{dt}=-\frac{V_{C_o}}{L_a},\frac{dI_{L_b}}{dt}=-\frac{V_{C_o}}{L_b}, \tag{10}$$

$$I_{L_a}=I_{L_a}(0)+\frac{L_a}{L_b}(I_{L_b}-I_{L_b}(0)), \tag{11}$$

and the state trajectories for each state are obtained by the variable assignment as described earlier.

For example I_{La} can be expressed as:

$$V_c^2 \frac{C_o}{2} - V_c \frac{L_a}{R_{out}} + C_{\text{onstant}} + L_a (I_{L_a}{}^2 + (I_{L_b}(0) - I_{L_a}(0)) I_{L_a}) = 0 \quad (12)$$

Solving (12) yields the trajectories of the converter $V_{Co}=f(I_{La})$ for states 2 and 4.

To summarize, following the above derivations, the state trajectories for the SC-buck converter are defined as a conventional buck converter with two expansions. First, the converter includes two on-states 1 and 3 and two off states 2 and 4. The second expansion is that there are three initials conditions instead of two. As a result, the procedure to obtain the graphical state-space map as presented in Fig. 5 is as follows:

- Horizontal axis variable for all states is the output capacitor voltage V_{Co}.
- For states 1 and 2, the state vertical axis variable is I_{Lb}; for states 3 and 4 use I_{La}. i.e., the state variable is an inductor current in the off state and the progress direction of all the trajectories is down toward the vertical axis.
- Transition on the map between states 1 to 3 is not continuous, but depends on the actual value of the inductors current. As a result of this so-called singularity, it is possible to view the climb-up of the inductor current from a lower point to a higher one.

The above procedure enables to draw a state-space map with two trajectories instead of four, when states 1 and 3 share one trajectory (on) and states 2 and 4 share the other (off). This is facilitated by duplication of the vertical axis such that it represents both I_{La} and I_{Lb} as shown in Fig. 5. The blue trajectories represent an on state; state-1 is monitored by I_{Lb} and state-3 by I_{La}. The red trajectories represent an off state; state-2 monitored by I_{Lb} and state-4 by I_{La}. For an easier view, a single trajectory is depicted in Fig. 6 for a case of loading transient. (full movement along the trajectory is detailed in the next sub-section).

Transient Controller

Observation of the resulting state-space map for the SC-buck converter reveals one of the main differences of this converter topology with respect to a multi-phase buck. As exemplified by Fig. 7 (a), during on state, while one current ramps up, and may satisfy the required charge balance to the output, the other phase's current ramps down and may result in unstable convergence around the new steady-state point. In addition, since only one phase carries the load, the minimum possible deviation is not obtained. It should be noted that for demonstration purposes, the load transient convergence in Fig. 7(a) has been obtained using an extremely overly-sized flying capacitor (1 mF) to hold the charge during the exceeding long on time. The situation worsens when C_f is sized to the steady-state requirements (50 µF) as depicted in Fig. 7(b).

Based on the behavior of the converter and by observing the trajectories map, better results are obtained by distribution of the on periods between the phases. As presented in Fig. 6,

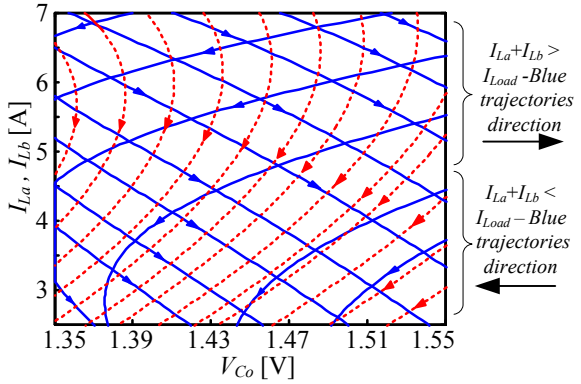

Fig. 5. State-space map for the SC-buck converter. On (states (a) and (c)-solid-blue) and off (states (b) and (d)-doted-red) trajectories.

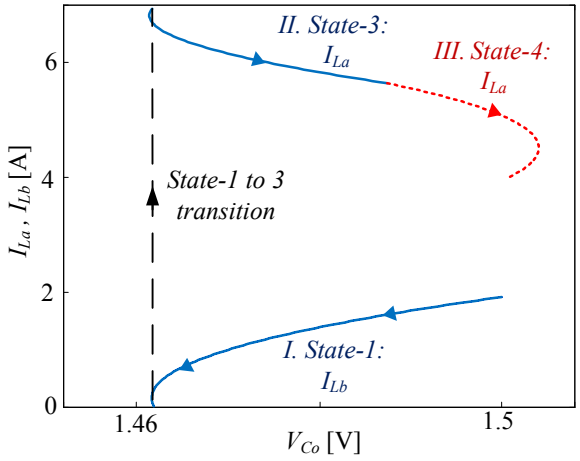

Fig. 6. Optimal trajectories for loading transient: I. First on period of phase a (state-1). II. Second on period of the alternating phase (state-3). III. Off period state-2 or 4. Note the singular transitioning point – monitoring different currents using the same plot.

switching between one on sequence to another, and then applying the off phase, results in a smaller voltage drop down to the minimum deviation of V_{Co} and a time-optimal-like behavior.

A time-optimal switching sequence for the SC-buck converter is as follows (described for loading transient):

- At the detection of a load change, the controller switches to one of the on phases (1 or 3).
- A second on period of the alternating phase is initiated when sum of the currents equals to the new load current. This point is detected by the output voltage minimum [21].
- Third, off state (state-4 or 2) can be initiated based on the charge balance of the output capacitor, which can be achieved by transient time calculation. Q_{charge} and $Q_{\text{discharge}}$, which represents the value of the capacitor charge and discharge, must be equal, as shown in Fig. 9. By assuming that the sum of the inductors current $I_{La}+I_{Lb}$ ramps up with constant slope, $V_{\text{in}}/2\text{-}2V_{Co}/L$, and ramps down with a slope of $-2V_{Co}/L_b$, the second state ends when $T_3=T_1D^{0.5}$ [16]. This assures the desired equilibrium, and can be implemented using counters.

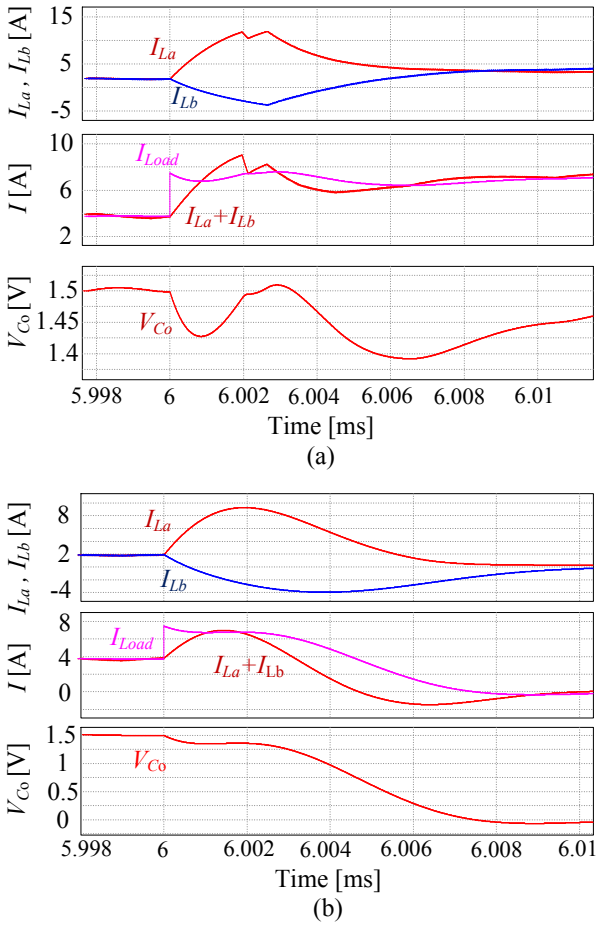

Fig. 7. Attempts of time-optimal recovery from load transient with uneven distribution of the on phases: (a) large flying capacitor (1 mF) and (b) 50µF.

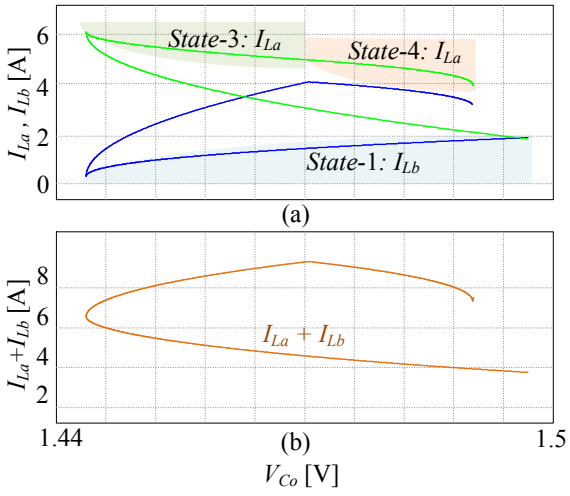

Fig. 8. Simulation results for load step heavy-to-light on the state domain: (a) the inductor currents and (b) for the sum of the inductor currents

To facilitate fast transient detection and end-of-transient phase, the first is assisted by two auxiliary comparators with two thresholds, well below the maximum allowed voltage deviation. This assists in the detection of both loading and unloading events.

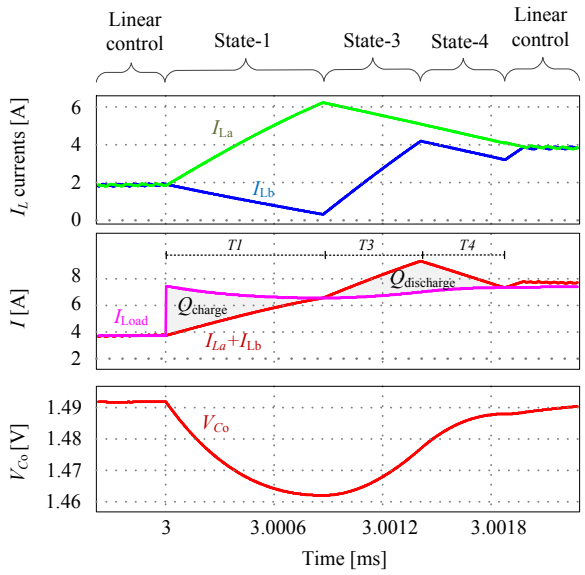

Fig. 9. Time-optimal recovery sequence for loading transient.

Figs. 8 and 9 are used to demonstrate the full sequence procedure for a loading transient, showing the individual inductor currents, sum of the currents and the output capacitor voltage for both in the time-domain and in the state-space. As can be seen, the resulting recovery trajectory of the sum of currents exactly matches a time-optimal behavior for a step load of single-phase buck converter.

To establish that time-optimal response is facilitated, the movement of the state-variables along the trajectories is examined, in the context of load transient, by observation of the output capacitor voltage and the sum of the inductors current, i.e. $I_{La}+I_{Lb}$. As a consequence, the resultant state-plane map (Fig. 8) resembles one of a conventional buck converter. As can be observed in Figs. 8 and 9, the trajectory is the one where the minimal output voltage deviation is obtained, i.e. time-optimal control [22].

IV. Experimental Results

To validate the operation of the small-signal compensator and the time-optimal controller, two 12-to-1.5 V SC-buck converters prototype have been built and tested. One converter has been designed to operate at 200 kHz and the second converter at 1.25 MHz. The main components of both units are listed in Table I. The digital controller comprises the steady-state voltage-mode compensator and the transient mode controller as shown in Fig. 1. The controller has been realized

TABLE I. Experimental Component Symbols and Values

Hardware components parameters		
Parameter	***200 kHz***	***1.25 MHz***
Inductors (L_a, L_b)	5 uH	0.6 uH
Series capacitor (C_t)	20 uF	10 uF
Output capacitor (C_o)	100 uF	50 uF
Output capacitor resistance	10 mΩ	5 mΩ
Input capacitor (C_{in})	100 uF	100 uF

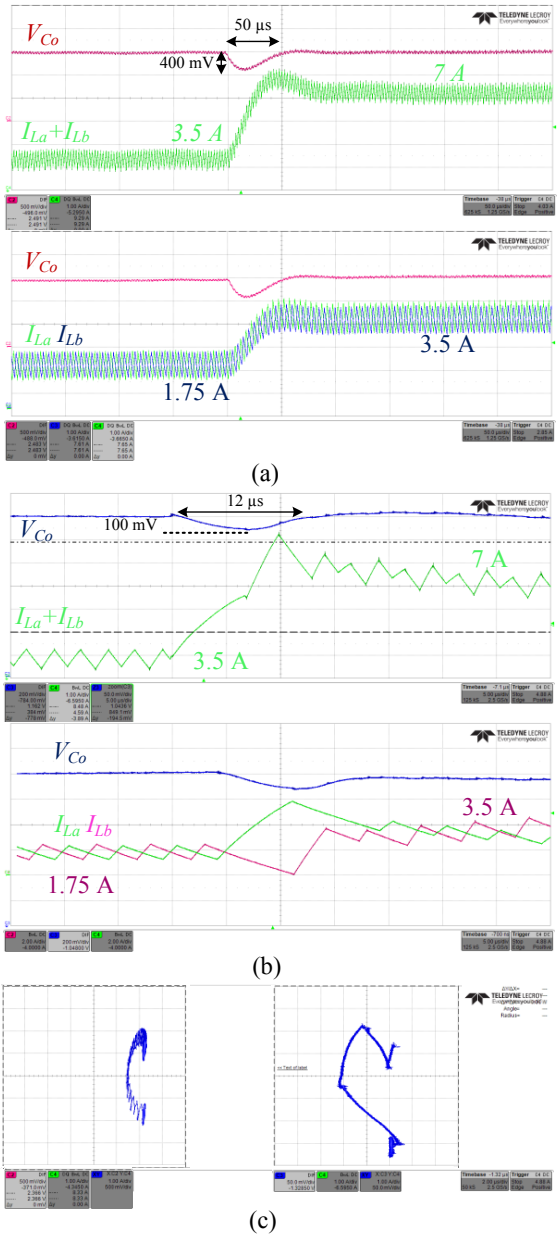

Fig. 10. 200 kHz experimental results for loading transient response from 3.5A to 7A by voltage-mode control (a) (500mV/div, 1A/div. Time scale is 50µs/div) and time-optimal control (b) (200mV/div, 1A/div for the sum of the currents and 2A/div for I_{La} and I_{Lb} . Time scale is 5µs/div), and (c) the state trajectories.

entirely on Altera Cyclone IV FPGA [23], including custom design of all related peripherals with an all-digital delay-line ADC and digital PWM as described in [24]-[25].

Fig. 10 shows the recovery of the 200kHz SC-buck converter from a loading transient of 50%, comparing the operation and performance of a small-signal voltage-mode compensation to time-optimal control scheme that has been developed. Also shown in Fig. 10 are the state-plane trajectories that are obtained using each control method, validating the theoretical analysis. Fig. 11 shows recovery results for the 1.25MHz prototype. A significant improvement

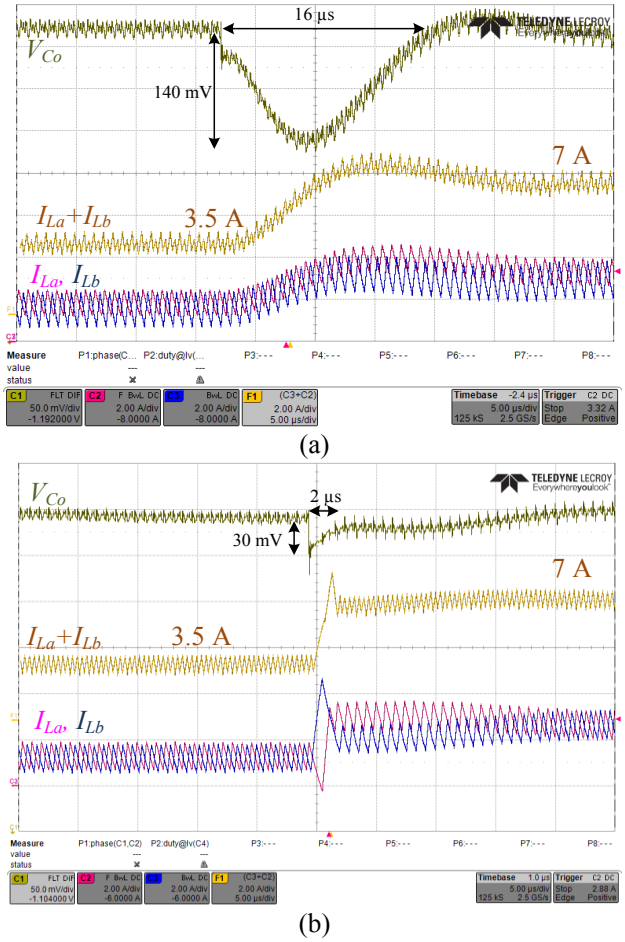

Fig. 11. 1.25 MHz experimental results for transient response from 3.5A to 7A by voltage-mode control (a) and time-optimal control (b). (50mV/div, 2A/div. Time scale is 5µs/div)

of the transient recovery using the time-optimal approach can be observed for both designs. Fig. 10 demonstrates output voltage undershoot of the TOC is 100 mV and settling time of 12 µs, compared to 400 mV and 50µs obtained by small-signal voltage-mode control. In Fig. 11 the undershoot has been trimmed from 140 to 30 mV while the settling time has been reduced from 12 µs to 2 µs.

V. Conclusions

In this study, an optimal closed-loop control scheme for a SC buck converters has been presented. The controller hybrids a voltage-mode small-signal compensator for steady-state operation and a transient-mode time-optimal controller for load transients. In the theoretical analysis, an average-behavioral model as well as state-space representation of the converter have been derived, then an optimal controller has been developed. The analysis revealed that a key factor for recovery of the converter from load transients is the capability of the controller to satisfy the charge-balance of the flying capacitor at all times (including during load transients). As a result, the time-optimal controller developed distributes the on-time period between the phases and by doing so, a smooth transient recovery is obtained. The experimental validation of the controller operations has been found to be in very good

agreement with the theoretical predictions. Also shown are the differences between small-signal voltage mode and time-optimal controls, demonstrating the superiority of the state-variable based approach.

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