Fully-Integrated Digital Average Current-Mode Control 12V-to-1.xV Voltage Regulator Module IC

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***Abstract* — This paper introduces a fully-integrated 12-to-1.xV voltage regulator module IC. A fully synthesizable digital two-loop controller has been realized through HDL tools. Several new IP blocks have been developed: a window delay-line based ADC, two independent PI compensators with shared hardware for calculations, high-resolution digital PWM (HR-DPWM), and a programmable dead-time module. The mixed-signal IC has been fabricated on a 0.18µm 5V CMOS process. It incorporates the digital core and a synchronous rectifier power-stage, including a drive circuitry operating at 1.25MHz with the ability to deliver up to 10W from 12V input. The digital core has been realized by an automated synthesis process and place-and route tools, resulting in effective silicon area of 0.16mm2. Post-layout and experimental results of the fabricated IC operating in closed-loop are provided, demonstrating the performance and benefits of the new controller for meeting the requirements of tight output voltage regulation.**

Keywords - Power management IC, digital control, average current mode control, PWM, dc-dc converters, voltage regulator module.

I. INTRODUCTION

Following the rapid growth in computing power and in particular for portable electronics, the specifications and restrictions on the power delivery have been significantly tighten to assure compact, light, energy efficient, and economical power sources. In voltage regulator module (VRM) and point-of-load (PoL) applications, the requirements also extend to the transient response and to the closed-loop system performance. The efforts to accommodate these challenges range from the selection of the power devices, frequency of operation, through new topologies for switch-mode power supplies (SMPS), controller types and more [1]-[5]. In recent years, the technology for on-chip integration of the power devices with the controller [6], [7] and further advancements for co-packaging of the reactive components [8], [9] have enabled a new generation of compact, efficient and economical VRMs.

In the worldwide trend of integration, digital design is predominant with several advantages such as convenience of the design, flexibility, scalability, and potential performance improvements. However, in power electronics and particularly in VRM applications, analog-oriented integration and analog controllers are the leaders [10], [12].

The main reason is that wide control bandwidth can be obtained without a significant penalty in the die area or power consumption. In order for a digital controller to be attractive and compete with an analog one, a low supply voltage process is preferred. This however introduces a tradeoff for a monolithic design, where the 'real-estate' for the power devices is rather costly, especially for over 5V input. The main limiting factor of digital technology in integrated power processing applications is therefore that the controller architecture has not been optimized to the operation of the SMPS, but uses rather generalized cores to execute very specific tasks. It would be extremely efficient if the digital controller is *specifically tailored to the set of tasks required by the SMPS and can be realized through a simple design flow, with competitive sizing, on a similar process of the power devices* – this has been pursued in this study.

State-of-the-art solutions that present architectures of integrated digital controllers propose several modifications of the two main peripheral units, i.e., the ADC and the DPWM [13], [14]. One of the technology enablers can be identified as the use of delay-lines (DL) as the primary building block for the ADC and DPWM. By doing so, the power consumption and a significant portion of the controller can be trimmed down without compromising performance [4], [7], [14], [15], demonstrating the potential of the digital design. However, in many of the design modifications it is required to custom design the delay cells, converting the design back to the analog domain, and losing some of the scalability features. Operation of digital controllers in either voltage-mode (VM) or mixed-signal peak current mode (CPM) have been demonstrated in variety of approaches [4], [8], [16]. There, the focus has been placed on creating an alternative to the conventional ADC and DPWM peripherals.

Another important compensation type that has been avoided hitherto is the average current-mode (ACM) control [17], [18]. With the rise in popularity of integrated VRMs, the recent evolution of methods for on-line efficiency optimization [14], [19], and current sharing for multi-phase stages, where the information of the average current is essential, the advantages of ACM approach are becoming more apparent. Especially in the case that it can be realized without additional hardware penalty.

The objective of this study is to introduce a new, ultra-compact, digital architecture for average current-mode DPWM control that is entirely realized through hardware description language (HDL), i.e., by pure digital means without additional custom design. It is a further aim of this study to detail the design of the integrated power stage for input voltage range of 12V, and finally, to present a fully monolithic VRM IC as detailed in Fig. 1. The final IC architecture incorporates an integrated synchronous rectifier that is realized by 5V-gated lateral double-diffused MOS (LDMOS) power devices that have been designed to sustain up to 18V and the required bootstrapped drive circuitry. The digital two-loop controller includes two independent discrete time compensators that operate with joint hardware for calculations, a dual-channel 6-bit delay-line based window ADC that is realized without any analog hardware, a custom dual-frequency 12-bit DPWM and system governor, a programmable dead-time unit, and a serial communication interface.

The rest of the paper is organized as follows: Section II describes the principle of operation of the new digital ACM controller. Section III details the architectures for the main units of the controller. The IC implementation of the mixed-signal, with emphasis on power stage design and the digital core are delineated in Section IV. Experimental verification of the VRM IC is provided in Section V. Section VI concludes the paper.

II. Digital Average Current-Mode Controller

Many current-programmed controller architectures reported in the literature or as commercial applications prefer the PCM method over ACM [6], [7], [17], [18], [20]. One of the main arguments for this is that PCM can achieve superior dynamics and offer cycle-by-cycle protection with simpler hardware. With digital implementation, the hardware requirements of ACM are equivalent, or even lower than those of VM control. Adding the fact that no high-speed mixed-signal design is required (as in the case of PCM), since it can be designed entirely by HDL description, ACM control becomes an attractive compensation type.

The principle of operation for the new digital ACM controller that has been realized in this study is described with the aid of Fig. 2 and Fig. 3, which show a conceptual block diagram of the control system and a fundamental timing diagram, respectively. As can be seen in Fig. 2, the controller follows the classical two-loop ACM design with an all-digital outer voltage and inner current loops. The voltage loop creates a digital reference $i_c[n]$ based on the error signal of the voltage loop $v_e[n]$, for the average current value $i_L[n]$. The current error signal $i_e[n]$ is the input to a current loop compensator that generates the duty-command $d[n]$ which is then sent to the DPWM, and a pulse width modulated signal $c(t)$ is created.

As detailed in the next section, each of the fundamental units has been implemented as an asynchronous hardware, using DLs and combinatorial circuits. By doing so, a significant portion of complex and power-hungry hardware for timing and high-speed synchronization is eliminated. Since DPWM is still a synchronized process, a system governor is

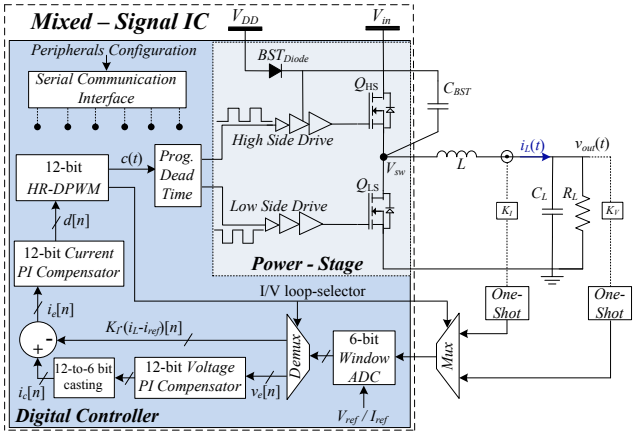


Fig. 1. Monolithic synchronous Buck converter with the fully-digital average current-mode PWM controller.

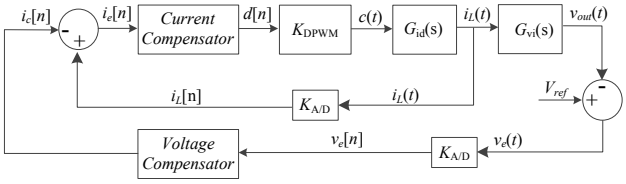


Fig. 2. Conceptual block diagram of the control system.

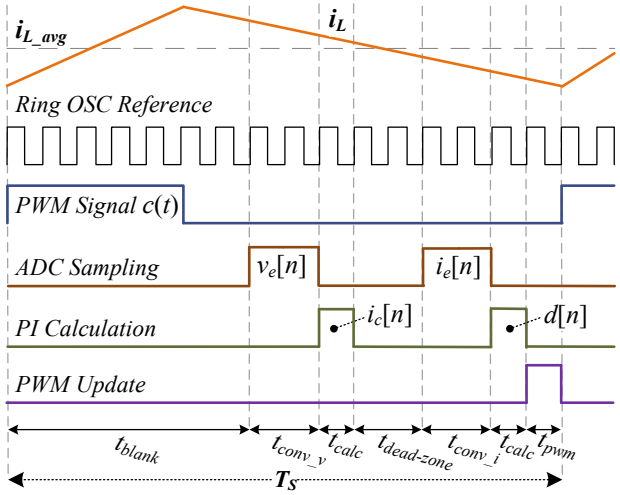


Fig. 3. Timing sequence of a typical steady-state switching cycle for the digital ACM.

employed to trigger the sequential operation of the functional blocks within the switching cycle. As can be seen in Fig. 3, the DPWM signal is sectioned into 16 equal intervals per switching period, which are derived from a DPWM based on an internal ring oscillator.

To facilitate sampling with high signal-to-noise ratio, it is preferred that the sampling event is triggered sufficiently away from the switching action [18], [21]-[22]. Fortunately, within the context of VRMs, the on time takes a relatively small portion of the switching period, allowing noise-clean sample throughout most of the cycle duration. In this study, given a target conversion ratio, a blanking time window t_{blank} (see Fig. 3) is set from the beginning of the cycle to the trigger action of sampling the output voltage. Following a short period of t_{conv_v}

to allow conversion of the ADC, a sample of the output voltage is obtained and a digital error signal $v_e[n]$ is generated. In the following interval t_{calc} the current correction signal $i_c[n]$ is calculated by the voltage compensator.

It should be further emphasized that in the case of a load transient event, or other circumstances that may lead to a significant increment of the on time beyond t_{blank}, the sampling instance may slide onto the switching action. This undesirable case can result in an incorrect, or noisy, sampling. One possible practice to overcome this is illustrated in Fig. 4, which shows an adaptive trimming of t_{blank} so that the sampling event is not allowed in the vicinity of the switching action [21], [22].

Since the same hardware is used for sampling of the inductor current, time-multiplexing is employed. Sampling of the current takes place during the off time and is preceded by the interval t_{dead_zone} to allow the hardware multiplexers to switch between the ADC channels. Following a similar conversion interval t_{conv_i}, a current error $i_e[n]$ is obtained and then the new duty-command $d[n]$ is generated and is ready to be loaded onto the DPWM unit at t_{pwm}, before the beginning of the new switching period. It should be noted that average current sensing can be obtained with or without extra filtering of the inductor current. This is since the current information is obtained through one sample per cycle approach, thus filtering out the ripple information [23], [24].

III. Digital Controller Architecture

The realization of the digital controller, shown in Fig. 1, relies on three key building blocks: 1) a dual-channel 6-bit DL-based window ADC to obtain a sample of both the output voltage and inductor current. 2) a 12-bit PI compensators generating the current correction $i_c[n]$ and duty-ratio command $d[n]$ signals. 3) a 12-bit hybrid HR-DPWM that generates the gate drive signals for Q_{HS} and Q_{LS} with a programmable dead-time option.

A. Voltage and current compensators

As in any classical two-loop control method for PWM converters in which the effect of the state-variables can be decoupled, the computational effort and the hardware complexity of the compensators can be reduced to a first order system, resulting in PI-type compensation [20], [25]. In this study, a digital PI compensation has been realized for both the voltage and current loops with shared hardware (multiplier) on the basis of one-sample-per-cycle [6], [21], [26]. There, a simple hardware realization can be achieved, resulting in reduced power consumption and silicon area. Taking into account a sampling delay of one switching cycle, the compensator can be expressed by the difference equation as [26], [27]:

$$v_c[n] = v_c[n-1] + av_e[n] - bv_e[n-1]. \quad (1)$$

where a, b are the compensator coefficients. Applying a conservative compensation design to assure stability with reasonable dynamics [28]-[30], and under the assumption that the inner loop is with a higher bandwidth than the outer loop the coefficients can be calculated as:

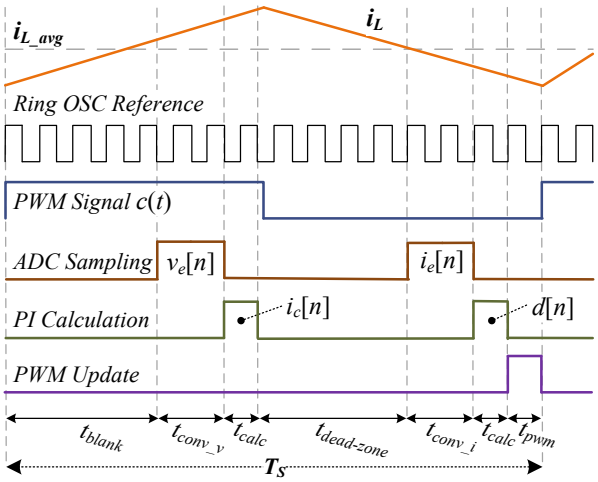


Fig. 4. Timing sequence waveforms of the controller for a possible switching cycle during loading transient. Adaptive tunning of t_{blank} to avoid sampling within the switching instance.

$$a = k_p \quad , \quad b = k_p\left(1 - T_S / T_i\right) \quad (2)$$

where k_p is the PI compensator's proportional gain at the target crossover frequency of the closed-loop system and T_i is the integrator time constant. To satisfy phase margin greater than 45º, $1/T_i$ is set lower than crossover frequency by approximately 50% [31].

The design of the compensators, prior to the implementation, has been validated through Matlab simulations as a full closed-loop system with a 12V-to-1.5V Buck converter, operating at 1.25 MHz (L=2.2 µH; C_o=50 µF). The target closed-loop parameters were: for the inner (current) loop a crossover frequency of 250 KHz and phase margin of approximately 50^0 whereas for the outer (voltage) loop the crossover frequency has been aimed at 120 KHz with phase margin of 80^0.

Since the final IC should function as a stand-alone device, a set of default values for a and b (that are fused-on during fabrication or loaded on startup) have been assigned. It should be noted that the overall gain of the voltage and current loops is affected by the equivalent gains of the ADC, HR-DPWM, and the power-stage's control-to-output transfer function. Since these gains are not equal, each compensator is loaded with its set of values for the compensator's coefficients.

In this study, the compensators' hardware architecture includes a small volatile memory, as a part of the serial communication interface (custom SPI in this study) that is preprogrammed with a set of default values. On startup, the default values can be used or a new set of coefficients can be loaded to the controller through the SPI. Then, the SPI internally communicates with the compensator units and loads the set of values per compensation loop. A benefit of this embedded feature is that the same controller hardware can be used with different power-stage configurations and parameters. Another reason for this feature is to support the next development steps of online auto-tuning and adaptive control [22], [32]-[34].

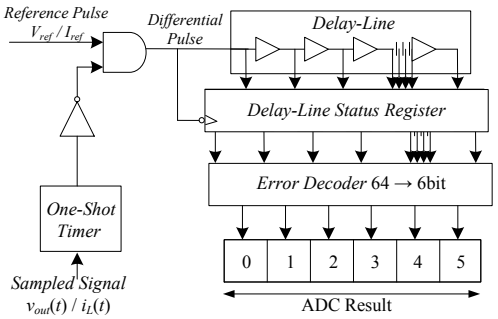


Fig. 5. Simplified architecture of 6-bit Window ADC.

B. Window DL-ADC

To achieve good regulation accuracy, a reliable sensing of the state-variables is essential. In the digital domain, this requirement translates into a relatively high-resolution measurement around the operating point. This has been facilitated in this study by a window-ADC [6], [14], [17], [35], where a small quantizer around the target point provides an accurate measurement with modest hardware. By doing so, the size can be significantly reduced, but more importantly, many of the full span linearity concerns of full-scale ADCs are removed. As oppose to many variations in the literature that use DLs for ADCs [5], [6], [35], the window-ADC of this study has been developed on the basis of standard-cell technology without any modifications.

The on-chip ADC, quantizes the difference between the sensed signal of $v_{out}(t)$ or $i_L(t)$ and an internal constant reference V_{ref} or I_{ref}, respectively. The architecture of the 6-bit window DL-ADC that is shown in Fig. 5, follows a two-step conversion: a voltage-to-time conversion using a one-shot timer [36], followed by time-to-digital conversion (TDC) using DL built of a string of digital buffers with fixed propagation time. The one-shot timer generates a pulse that is duration is inversely proportional to the amplitude of continuous-time (analog) sensed signal [$v_{out}(t)$ or $i_L(t)$]. The relationship between the generated pulse-length, T_{pulse} and the analog input can be expressed as:

$$T_{pulse} = RC \cdot ln\left[V_{DD} / \left(V_{sample} - V_{th}\right)\right] \quad (3)$$

where V_{DD} and Vth are the logic and threshold voltages, respectively. V_{sample} is the value of the sensed signal [$v_{out}(t)$ or $i_L(t)$]. The TDC converts the differential pulse, obtained by the time difference between the reference and generated pulses. At the end of the conversion, the differential pulse triggers the DL status register, which latches synchronously with respect to falling edge of the differential pulse. The residual time is captured as a thermometer code and then translated to a binary value.

C. Hybrid high-resolution digital pulse width modulator

In the context of digitally controlled SMPS, HR-DPWM is essential to avoid undesirable limit cycle oscillations [37]-[39]. The conventional approach to implement HR-DPWM is by a fast-clocked counter-comparator scheme [14], [38], [40]. In this way, n-bit resolution at a switching frequency of f_s requires

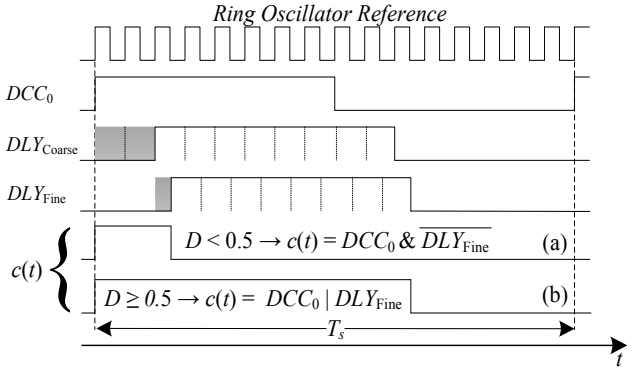


Fig. 6. HR-DPWM operation for a case that: (a) D = 15.5% ; d[11-0] = '**0**01010000000'. (b) D = 65.5% ; d[11-0] = '**1**01010000000'.

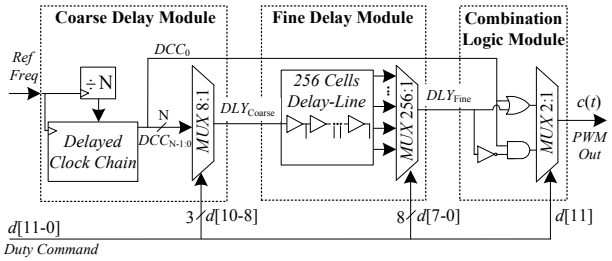


Fig. 7. Simplified architecture of 12-bit HR-DPWM.

a reference clock frequency of $2^n \cdot f_s$. This translates to increased power consumption and more complex design to realize the high-speed circuitry. Another approach to realize a HR-DPWM is based on tapped DL scheme [5], [6], [15]. In this method, the power consumption is reduced, but the required silicon area of the design grows exponentially with the number of resolution bits. Another potential design challenge of the tapped DL method is the design of the delay elements (DEs). In this study, a combination of both methods has been employed, i.e., by incorporating a coarse-counting block and then fine-tuning it to the target delay. This allows a design that is based on compact standard cells, and enables direct synthesis. In addition, the silicon area as well as power consumption are reduced significantly.

A simplistic way to generate a DPWM signal using a time-delay method requires phase-detection type operation between a reference signal and a delayed one. To increase accuracy and reduce the silicon area, the use of short delays (less than half switching cycle) is preferred. An exclusive-or (XOR) operator is a simplistic phase detector, with narrow but sufficient dynamic range of half-cycle (180º), therefore it is an ideal candidate to carry out the task. To accommodate the dynamic range, half-cycle padding is realized based on the duty-ratio command as follows; Assuming a given reference time base DCC_0, and a delayed signal DLY_{Fine}, the DPWM output for D<0.5 can be obtained as:

$$D < 0.5 \rightarrow c(t) = \begin{Bmatrix} DCC_0 \oplus DLY_{Fine}, & t < T_S/2 \\ \text{'0'}, & T_S/2 \leq t < T_S \end{Bmatrix} \Leftrightarrow DCC_0 \,\&\, \overline{DLY_{Fine}} \quad (4)$$

and for D≥0.5 the padding is adjusted as:

$$D \geq 0.5 \rightarrow c(t) = \begin{Bmatrix} \text{'1'}, & t < T_S/2 \\ DCC_0 \oplus DLY_{Fine}, & T_S/2 \leq t < T_S \end{Bmatrix} \Leftrightarrow DCC_0 \mid DLY_{Fine} \quad (5)$$

From (4) and (5), the combined logic is simplified to few basic operators.

The next challenge in generating the DPWM signal is to create a delayed signal from the reference with high-resolution, but with simple hardware. This has been facilitated by a combined coarse-fine digital counter as described in Figs. 6 and 7, which also show the conceptual architecture and timing diagram for the HR-DPWM unit that has been realized in this study. As can be seen, it consists of three functional blocks; a coarse delay module, a fine delay unit, and a logic block. The 12-bit digital word for the duty ratio d[11-0] is distributed within the three modules. The course delay block is fed by a reference clock (generated by a ring oscillator) and 3 upper bits d[10-8], it generates two signals; first is a time-base DCC_0, also used for the switching period. The second is a coarse-delayed version of the time-base DLY_{Coarse} with time intervals derived from the reference clock as prescribed by d[10-8]. The latter is facilitated by a delay clock chain [41]. The fine delay unit is a string of 8-bit long DL that finely adjusts DLY_{Coarse} by the number of DEs as specified by d[7-0], creating the high-resolution delayed signal DLY_{Fine}. The logic block applies the required operation of either (4) or (5) on DCC_0 and DLY_{Fine} based on the MSB d[11]. The switching frequency of the HR-DPWM can be expressed as function of the number of bits and the propogation time $t_{pd,DE}$ of a single delay element (of the fine-delay module) as:

$$f_s = \frac{1}{t_{pd,DE}\,2^{N+M}} \quad ; \quad \begin{cases} \text{N - number of coarse bits} \\ \text{M - number of fine bits} \end{cases} \tag{6}$$

D. Programmable dead-time

To facilitate switching of the power devices without shoot-through, it is necessary to control the gate driving signals with proper dead-time, such that the power transistors Q_{HS} and Q_{LS} (Fig. 1) turn on does not overlap. Another important task of an adjustable dead-time unit is to improve the efficiency of the converter [42], therefore, a programmable dead-time module has been developed. It consists a string of 200 DEs connected to an 8-channels multiplexer. In a similar manner to the compensators' coefficients setup, the dead-time t_{DT}, set within the SPI memory register with initial default value, and can be programmed from 1nSec up to 40nSec.

IV. Mixed-Signal IC Implementation

The mixed-signal IC of the VRM shown in Fig. 1 integrates power, analog and digital circuits on one die. To satisfy proper operation, several layout constraints such as adding guard rings and isolation wells between devices have been employed to reduce coupling noise and undesired holes/electrons injections. This section primarily focuses on IC implementation, design considerations of the power-stage and the digital blocks' implementation procedure.

A. Power-stage implementation

The mixed-signal IC's synchronous rectifier power-stage is constructed by N-channel devices for both the high and low side switches. In this study, these are realized by a 5V-gated LDMOS power device [43]. The use of LDMOS allows higher voltage swing operation of a monolithic DC-DC converter, since its typical breakdown voltage is higher than the standard 5V CMOS device. Each switch has a dedicated driving stage designed with a 5V CMOS, whereas Q_{HS} transistor requires a bootstrap driver and floating level shifter configuration to overcome the limitations of a standard CMOS device breakdown voltage. The architecture and considerations of the HS level shifter is discussed in the next subsection. The driving stages have been realized by four dedicated custom designed buffers with high sinking-sourcing capabilities.

The switches have been designed symmetrically with an on-resistance of 35mΩ. The effective gate width W_g of the switches is 200,000μm, obtained based on the target operating point derived from [44]. Each switch is constructed from 4000 fingers [45], creating a symmetrical quadrilateral layout pattern.

B. High-side level shifter

The HS transistor is driven by a bootstrap configuration to assure proper driving signals of the power-stage. By realizing such approach the voltage drop on the level shifter is potentially a full rail-to-rail voltage swing from V_{in}+5V to ground, damaging the CMOS device. One approach to overcome this issue, is designing the level shifter circuit with LDMOS devices only, which results in a significant larger die-size and higher power consumption. The design approach implemented in this study is shown in Fig. 8. It merges both CMOS and LDMOS, such that several LDMOS devices (DM_1-DM_4) are used only in critical branches for absorbing high voltage drop. A unique feature of the level shifter develop in this study is that it does not require biasing circuitry for its operation and relies on the logic rail alone. This has been accomplished by appropriate sizing of transistors M_1 and M_2 with respect to V_{DD}, creating a self-biased level shifter circuit. The level shifter circuit is divided into three main sub-units. First, an edge detector that triggers the level-shifter whenever the PWM signal changes. Second, the shifting unit constructed by DM_1-DM_4 to absorb the high voltage drop to assure that the stress on M_1-M_4 does not exceed 5V. Finally, a differential pair that saturates the differential change between V_P and V_N, such that the PWM signal voltage levels, V_{DD} and ground, are

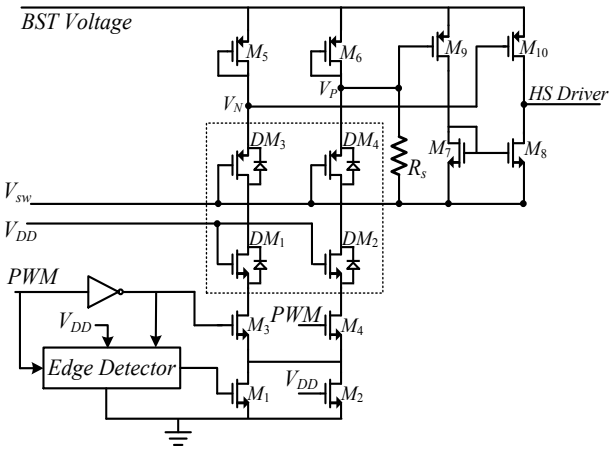


Fig. 8. High voltage level shifter circuit.

shifted to V_{sw} and V_{sw}+5V, respectively. The output signal of the differential pair controls the floating drive circuitry of the HS transistor.

C. Digital implementation of ACM controller

The realization of the digital controller relies on a digital implementation flow, using vendor's standard cells only. The digital implementation is carried out through two main steps. In the first step, the controller's units are described in HDL as standalone units for the simplicity of the verification and behavioral functionality simulations. Then, each unit is synthesized using synthesis and timing verification tools into an optimized gate-level representation, given a set of design constraints (such as skew and jitter, power consumption, etc.). The layout of each unit was generated by an automated place-and-route process. In the second step, all the units have been integrated together onto the higher hierarchy of the digital controller. Finally, the digital controller has been integrated with the power and analog units, creating the finalized digital ACM Buck converter IC. The main characteristics of the digital controller including the digital core active area and current draw are summarized in Table I. It should be further emphasized that the controller's design scales with the technology, such that its overall area and power consumption can be significantly reduced by implementing it to a deeper sub-micron process.

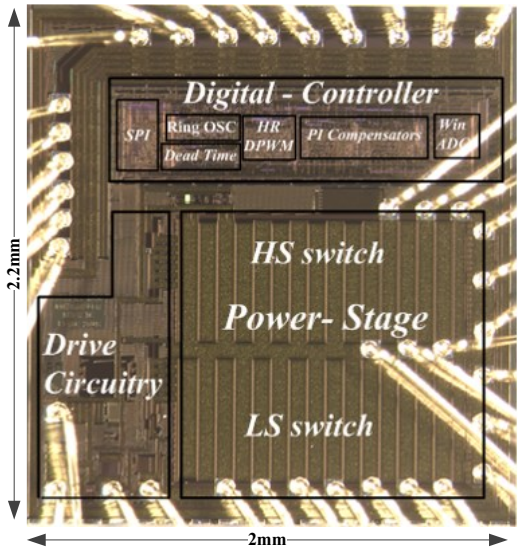
To achieve good PWM regulation with digital control, and to avoid limit-cycle oscillations, it is required that the resolution of the DPWM is sufficiently high with respect to resolution of the ADC [37]-[39]. This translates into a limitation on the maximum switching frequency that can be obtained by the digital controller, which then affects the overall size of the controller and the performance in closed-loop. For a given $t_{pd,DE}$ of a single delay element is 200pSec and the desired DPWM resolution is 12-bit, using (6) the obtained switching frequency f_s is 1.25MHz. From (6) it can be seen that f_s is inversely proportional to DPWM resolution, such that decreasing the resolution by a single bit will increase f_s by a factor of two. For example, 10-bit resolution results in 5MHz operation and vise-versa.

V. Closed-Loop Experimental Verification

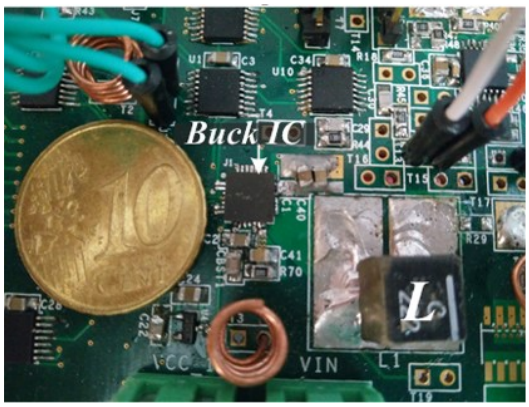
A fully-integrated digital ACM control VRM IC has been designed and fabricated in 0.18µm 5V CMOS process, the chip micrograph is shown in Fig. 9a and Fig. 9b depicts the mixed-signal IC prototype on a PCB. To demonstrate the operation of the digital controller and to validate closed-loop operation, the mixed-signal IC has been verified with experimental results, whereas the IC connects to an external filter of L = 2.2µH, C_{out} = 50µF. The VRM IC operates at 1.25MHz, with the ability to deliver up to 10W from a 12V input. Experimental kelvin resistance measurements of the packaged IC converter report approximately 120mΩ and 200mΩ for the LS and HS switches, respectively. The deviation between the target on-resistances (~35mΩ) and the measured on-resistances can be explained by bond wires and package limitations [46]. Table II summarizes the mixed-signal VRM IC main characteristics, it

TABLE I - Digital Controller Main Characteristics

IC Block / Digital Core	*0.18µm CMOS*
Supply voltage	5V
$t_{pd,DE}$ buffer	200pSec
DPWM resolution	12-bits
DPWM nominal frequency	1.25MHz
DPWM Si area	0.03 mm^2
ADC resolution	6-bit
ADC conversion time	20nSec
ADC Si area	0.022 mm^2
PI calculation time	< 40nSec
PI Si area	0.034 mm^2
Digital core current-draw	58µA/MHz
Effective digital core Si area including Ring-Oscillator, Dead-Time and SPI	0.16 mm^2



(a)



(b)

Fig. 9 (a) Micrograph of the fabricated fully-integrated digital average current-mode control 12V-to-1.xV voltage regulator module IC, (b) Chip prototype on PCB.

should be noted that the current sensing obtained by an off-chip series-sense resistor setup [47].

Fig. 10 shows experimental steady-state waveforms of the closed-loop system, for 12V input at 1.25MHz operation and duty-ratio of 0.125. Smooth low-to-high and high-to-low transitions operation can be observed, validating the proper operation of the high-side level shifter.

TABLE II – SUMMARY OF THE MIXED-SIGNAL IC CHARACTERISTICS

Specifications	*Value*
Package	5x5 QFN - MLP
V_{in}	12V
Power-stage R_{on} LS/HS	~120mΩ, ~200mΩ
V_{out}	1.5V
I_{out}	1.5A
Off Chip L, C	2.2µH, 50µF
Switching frequency f_s	1.25MHz
Total chip Si Area	4.4mm^2

Experimental load transient responses of the VRM IC are shown in Figs. 11 and 12. A loading transient of 1.5A-to-3A and V_{out} = 1.5V with operating frequency of f_s = 1.25 MHz is depicted in Fig. 11. An output voltage undershoot of 40mV has been measured with settling time of 15µs. Fig. 12 shows the response of the converter to 1.5A unloading transient, from 3A to 1.5A. As can be observed, the output voltage overshoot is 40mV and 14µs is the time it takes for the system to set back to the steady-state. Although rapid dynamics were not a primary objective of this study, it can be observed that for both load transients the output voltage is well regulated with reasonable and comparable performance.

VI. CONCLUSION

A fully-integrated digital average current-mode control 12-to-1.xV voltage regulator module IC has been presented. The mixed-signal design incorporates a two-loop digital controller with a monolithic power stage. In the controller design, three main components have been developed: a dual-channel ADC, 12-bit HR-DPWM and two independent PI compensators with a joint arithmetic core. The VRM IC has been designed and fabricated on 0.18µm 5V CMOS process, operates at 1.25MHz, and is capable of handling approximately 10W from 12V input with tight voltage regulation. The controller has been implemented on-chip by pure digital means without additional custom designs, resulting in total silicon area of 0.16mm^2, whereas the total silicon area of the chip is 4.4mm^2. The experimental results of the closed-loop operation demonstrated the performance and benefits of the new digital ACM controller approach, in particular in terms of area and power saving.

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REFERENCES

[1] J. Sun, D. Giuliano, S. Devarajan, J. Lu, T. P. Chow, and R. J. Gutmann, "Fully monolithic cellular Buck converter design for 3-D power delivery," *IEEE Trans. Very Large Scale Integr. Syst.,* vol. 17, no. 3, pp. 447–451, Mar. 2009.

[2] E. A. Burton, G. Schrom, F. Paillet, J. Douglas, W. Lambert, K. Radhakrishnan, and M. Hill, "FIVR-Fully integrated voltage regulators on 4th generation Intel Core SoCs, " in *Proc. IEEE APEC*, pp. 432–439, Mar. 2014.

[3] P.S. Shenoy, O. Lazaro, R. Ramani, M. Amaro, W. Wiktor, J. Khayat, and B. Lynch "A 5 MHz, 12 V, 10 A, monolithically integrated two-phase series capacitor buck converter," in *Proc. IEEE Applied Power Electron. Conf*., March. 2016.

[4] Z. Lukic, N. Rahman, and A. Prodić, "Multibit Σ–Δ PWM digital controller IC for DC-DC converters operating at switching frequencies beyond 10 MHz," *IEEE Trans. Power Electron*., vol. 22, no. 5, pp. 1693–1707, Sep. 2007.

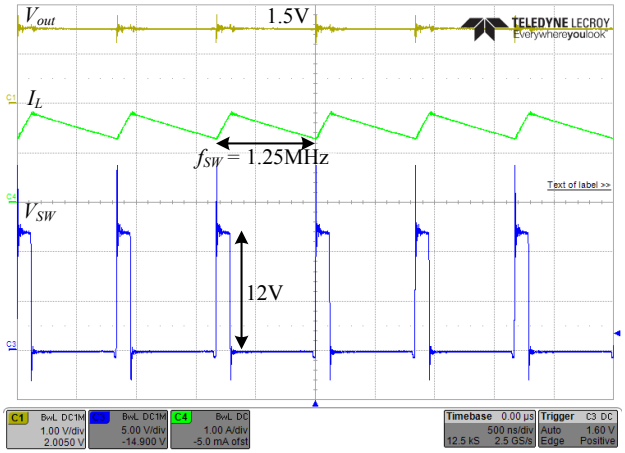

Fig. 10. Experimental steady-state results with a duty-ratio of 0.125 at 1.25MHz. Output voltage (top) 1V/div, inductor current (middle) 1A/div, switching node voltage V_{sw} (bottom) 5V/div. Time scale 500ns/div.

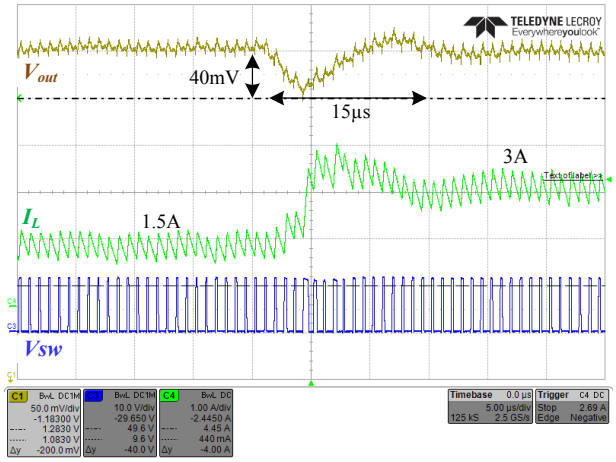

Fig. 11. Experimental results of a 1.5A loading transient response from 1.5A to 3A. Output voltage (top - yellow) 50mV/div, inductor current (middle – green) 1A/div, switching node voltage V_{sw} (bottom - blue) 10V/div. Time scale 5µs/div

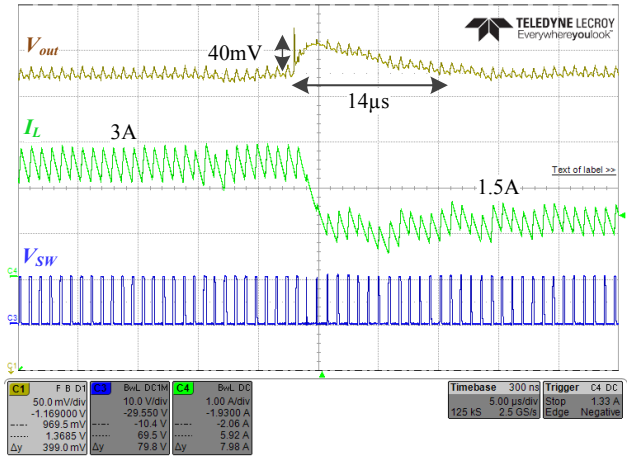

Fig. 12. Experimental results of a 1.5A unloading transient response from 3A to 1.5A. Output voltage (top) 50mV/div, inductor current (middle) 1A/div, switching node voltage V_{sw} (bottom) 10V/div. Time scale 5µs/div.

[5] B. J. Patella, A. Prodić, A. Zirger, and D. Maksimović, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. On Power Electronics*, Vol. 18, No. 1, Pm 11, Jan. 2003.

[6] O. Trescases, A. Prodić, Wai Tung Ng, "Digitally controlled current-Mode DC–DC converter IC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 1, pp. 219-231, Jan. 2011.

[7] J. Xiao, A. Peterchev, J. Zhang, and S. R. Sanders, "A 4-μA quiescent-current dual-mode digitally controlled buck converter IC for cellular phone applications," *IEEE J. Solid-State Circ*., vol. 39, no. 12, pp. 2342–2348, Dec. 2004.

[8] S. M. Ahsanuzzaman, A. Prodić, and D. A. Johns, "An ntegrated high-density power management solution for portable applications based on a multioutput switched-capacitor circuit," *IEEE Trans. Power Electron*., vol. 31, no. 6, pp. 4305–4323, Jun 2016.

[9] S. Sugahara, K. Yamada, M. Edo, T. Sato, and K. Yamasawa, "90% high efficiency and 100-W/cm^3 high power density integrated DC-DC converter for cellular phones," *IEEE Trans. Power Electron*., vol. 28, no. 4, pp. 1994–2004, Apr. 2013.

[10] Y.Qiu, J. Sun, M. Xu,K. Lee, and F.C. Lee, "Bandwidth improvements for peak-current controlled voltage regulators," *IEEE Trans. Power Electron*., vol. 22, no. 4, pp. 1253–1260, Jul. 2007.

[11] N. Keskar and G. A. Rincon-Mora, "Self-stabilizing, integrated, hysteretic boost DC-DC converter," in *Proc. IEEE Ind. Electron. Soc. Annu. Conf*.,2004, vol. 1, pp. 586–591.

[12] Y. Panvo and M. M. Jovanović, "Design consideration for 12-V/1.5-V, 50-A voltage regulator modules," *IEEE Trans. Power Electron*., vol. 16, no. 6, pp. 776–783, Nov. 2001.

[13] G. Wei and M. Horowitz, "A low power switching power supply for self-clocked systems," in *Proc. Int. Symp. Low Power Electron. Design*, ISLPED, pp. 313–317, 1996.

[14] J. Xiao, A. V. Peterchev, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," in *Proc. IEEE Power Electronics Spec. Conf.*, vol. 1, 2001, pp. 38–47.

[15] Y. Halihal, Y. Bezdenezhnykh, I. Ozana, and M. M. Peretz, "Full FPGA-based design of a PWM/CPM controller with integrated high-resolution fast ADC and DPWM peripherals," *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2014.

[16] A. Parayandeh, B. Mahdavikhah, S. M. Ahsanuzzaman, A. Radić, and A. Prodić, "A 10 MHz mixed-signal CPM controlled DC-DC converter IC with novel gate swing circuit and instantaneous efficiency optimization," in *Proc. IEEE Energy Convers. Congr. Expo*., pp. 1229–1235. Sep 2011.

[17] H. Peng and D. Maksimović, "Digital current-mode controller for DC-DC converters," in *Proc. Applied Power Electron. Conf*., pp. 899–905, 2005.

[18] J. Chen, A. Prodić, R. W. Erickson, and D. Maksimović, "Predictive digital current programmed control," *IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 411–419, Jan. 2003.

[19] S. H. Kang, D. Maksimović and I. Cohen, "Efficiency optimization in digitally controlled Flyback DC-DC converters over wide ranges of operating conditions," *IEEE Trans. Power Electron.*, vol.27, no.8, pp.3734- 3748, Aug. 2012.

[20] R. Erickson and D. Maksimović, *Fundamentals of Power Electronics*. Norwell, MA: Kluwer, 2001.

[21] M. M. Peretz and S. Ben-Yaakov, "Time-domain design of digital compensators for PWM DC-DC converters," *IEEE Trans. Power Electronics*., vol. 27, no. 1, pp. 284-293, Jan. 2012.

[22] M. M. Peretz and S. Ben-Yaakov, "Time domain identification of PWM converters", *IET Power Electronics*. Vol. 5, N. 2, 166 - 172, 2012.

[23] D. Maksimović and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron*., vol. 22, no. 6, pp. 2552-2556, Nov. 2007.

[24] R. B. Ridley, "A new small-signal model for current-mode control," Ph.D. Dissertation, Virginia Polytechnic Institute and State University, Nov. 27, 1990.

[25] S. Ben-Yaakov, "Average simulation of PWM converters by direct implementation of behavioral relationships," *International journal of electron*, vol. 77, no. 5, pp. 731-746, 1994.

[26] M. Ilic, D. Maksimović, "Digital average current-mode controller for dc–dc converters in physical vapor deposition applications", in *Proc. IEEE PESC*, pp. 1-7, 2006.

[27] M. M. Peretz and S. Ben-Yaakov, "Revisiting the closed loop response of PWM converters controlled by voltage feedback," in *Proc. Applied Power Electron. Conf. and Expo*, pp. 28-64, Feb. 2008.

[28] R.B. Ridley, B.H. Cho and F.C. Lee, "Analysis and interpretation of loop gains of multiloop-controlled switching regulators," *IEEE Trans. Power Electron*., vol. 3, pp. 489−498, Oct. 1988.

[29] G. F. Franklin and J. D. Powell, *Digital Control of Dynamic Systems*. Reading, MA: Addison-Wesley, 1998.

[30] J. Dannehl, C. Wessels, and F. W. Fuchs, "Limitations of voltage-oriented PI current control of grid-connected PWM rectifiers with LCL filters," *IEEE Trans. Ind. Electron*., vol. 56, no. 2, pp. 380–388, Oct. 2009.

[31] B. Miao, R. Zane, and D. Maksimović, "System identification of power converters with digital control through cross-correlation methods," *IEEE Trans. Power Electron*., vol. 20, no. 5, pp. 1093–1099, Sep. 2005.

[32] A. L. Kelly and K. Rinne, "A self-compensating adaptive digital regulator for switching converters based on linear prediction," in *Proc. IEEE APEC Conf*., 2006, pp. 712–718.

[33] Z. Zhao, H. Lee, A. Feizmohammad, and A. Prodic´, "Limit-cycle based auto-tuning system for digitally controlled low-power SMPS," in *Proc. IEEE APEC Conf*., 2006, pp. 1143–1147.

[34] W. Stefanutti, P. Mattavelli, S. Saggini, and M. Ghioni, "Autotuning of digitally controlled buck converters based on relay feedback," in *Proc. IEEE PESC Conf*., 2005, pp. 2140–2145.

[35] G. Li, Y. M. Tousi, A. Hassibi, and E. Afshari, "Delay-line-based analog-to-digital converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 6, pp. 464–468, Jun. 2009.

[36] R. Jacob Baker, *CMOS Circuit Design Layout and Simulation*, 3rd Edition, John Wiley & Sons, 2010.

[37] A. V. Peterchev and S. R. Sanders, "Quantization resolution and limit cycling in digitally controlled PWM converters," *IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 301–308, Jan. 2003, Special Issue on Digital Control.

[38] H. Peng, A. Prodić, E. Alarcon, and D. Maksimović, "Modeling of quantization effects in digitally controlled dc–dc converters," *IEEE Trans. Power Electron*., vol. 22, no. 1, pp. 208–215, Jan. 2007.

[39] M. M. Peretz and, S. Ben-Yaakov "Digital control of resonant converters: Resolution effects on limit cycles," *IEEE Trans. Power Electron*., vol. 25, no. 6, pp. 1652-1661, 2010.

[40] A. P. Dancy and A. P. Chandrakasan, "Ultra low power control circuits for PWM converters," in *Proc. IEEE PESC Conf*., 1997, pp. 21–28.

[41] J. D. Kershaw *Digital Electronics Logic and Systems*. Wadsworth, Belmont, CA, 1976.

[42] J. A. Abu-Qahouq, H. Mao, H. J. Al-Atrash, and I. Batarseh, "Maximum efficiency point tracking (MEPT) method and digital dead time control implementation," *IEEE Trans. Power Electron*., vol. 21, no. 5, pp. 1273– 1281, Sep. 2006.

[43] K. Sung and T. Won, "High-side N-channel LDMOS for a high breakdown voltage," *Journal of the Korean Physical Society*, vol. 58, no. 5, pp. 1411-1416, 2011.

[44] M. Rodriguez, Y. Zhang and D. Maksimović, "High-frequency PWM buck converters using GaN-on-SiC HEMTs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2462-2473, 2014.

[45] A. Yoo , M. Chang , O. Trescases and W. Ng, "High-performance low-voltage power MOSFETs with hybrid waffle layout structure in a 0.25 μm standard CMOS process," in *Proc. 20th Int. Symp. Power Semicond. Devices & IC's*, pp. 95-98, May 2008.

[46] E. Abramov, A. Cervera, and M. M. Peretz, "Optimal design of a voltage regulator based resonant switched-capacitor converter IC," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, pp. 692-699–920, Mar. 2016.

[47] H. P. Forghani-zadeh, G. A. Rincon-Mora, "Current-sensing techniques for DC–DC converters," in *Proc. IEEE Midwest Symposium. Circuits and Systems*, vol. 2, pp. 577–580, Aug 2002.