Parallel Balancing Converter for Serially Connected Batteries String

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***Abstract* – This paper introduces a new isolated converter topology for parallel balancing of serially connected batteries string. The system uses a low voltage bus capacitor as an energy buffer that is common for all the cells and balancing of the string is achieved by voltage equalizing of the cells. Each converter is in charge of balancing three adjacent cells, reducing the components count of the system. The converter operates in DCM and the current that flows between the cells and the bus is a function of their voltage difference. As a result, the quiescent power loss is minimal since no energy circulates in the system when the cells are balanced. Furthermore, no voltage or current sensors are required, making the implementation of the system simple and cost-effective. Theoretical analysis as well as design guidelines for the construction of the new topology are detailed and validated by experimental results that demonstrate the system's balancing capability.**

I. INTRODUCTION

Batteries have been widely used in various applications as an energy storage element and a power source. To achieve the required high voltage and high power for applications such as electric vehicle (EV) and its derivatives, and due to low cell voltage, large number of batteries cells are connected in series [1]-[5]. Batteries suffer from manufacturing and environmental variances, degradation with aging, charging and discharging, thermal conditions and internal impedance differences. Each of these potential flaws or a combination of them may lead to imbalances in the stored energy of the cells and as a result reduce their lifetime, efficiency and reliability [6]. Therefore, serially connected batteries strings must be assisted by a balancing circuit to minimize imbalances and improve the overall performance [7], [8].

The passive balancing approach is predominant in the majority of commercial batteries balancing applications, primarily due to low cost and simplicity [9]. There, excess energy of each cell is dissipated either through a resistor or transistor, but from an energy efficiency perspective it less attractive due to the inherent power loss. An alternative concept that has been extensively investigated in recent years is the active balancing approach [10]-[27]. Here, power converters are used to evenly distribute the stored energy along the string. Typically, energy is transferred from cells with higher voltage to the lower ones, or in more sophisticated designs by cell's State-of-Charge (SoC) [28], [29]. Active balancing can be realized in a variety of ways, for example using switched-capacitors converters [10]-[12], switched-inductor converters [13]-[24], or multi-winding transformer based converters [25]-[27].

Balancing circuits are further distinguished by power flow architecture, i.e., series balancing and parallel balancing. In series balancing, e.g. as in [11], energy is transferred from one neighboring cell to another using power converters that link between each two adjacent cells. The converters act as a local bypass to the energy flow in case a cell is damaged or has lower energy, but in many cases their operation requires synchronization between the circuits. Parallel balancing is assisted by a small energy storage component, typically a capacitor, and often referred as energy buffer which is used as a link to transfer energy from a charged cell to the cell that needs to be charged. It means that when this type of balancing is used, the energy does not need to be processed through the whole batteries string [30]-[32]. Therefore, an apparent advantage of the parallel balancing approach is the fewer amount of conversions to balance the string, and as a result faster balancing with higher efficiency, especially in large arrays. However, the penalty often comes with large number of components in each balancing circuit and complex control. Practical implementation of active balancing systems is a challenge, mainly due the large number of cells in the string that contribute to the complexity of the system in terms of large component count, high stress components, multi-winding transformers or sophisticated control algorithms. This forces the individual balancing circuit and its controller to be as simple and cost-effective as possible in order to be a competitive solution.

The objective of this study is to introduce a new isolated parallel balancing system with low components count and very simple control. The new system, depicted in Fig. 1, utilizes each of the modules for balancing three adjacent cells. A common bus capacitor for all modules in the string is used as the energy buffer to link between modules. The energy transfer is proportional to the voltage difference between a cell and the bus, resulting in low quiescent power losses since no energy circulates in the system when the cells are balanced. The operation of the balancing modules does not require sensors, neither for current nor for the voltage. In addition, asynchronous operation of the modules is allowed, making the solution simple and cost-effective.

The paper is organized as follows: Section II describes the topology, its principle of operation and the major features of

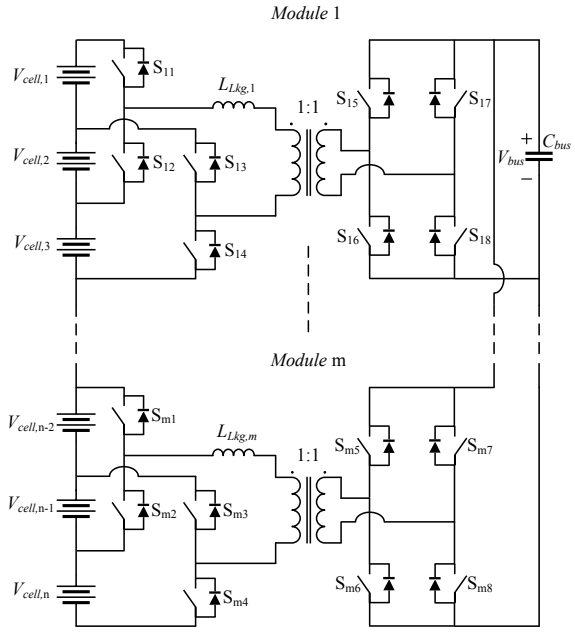

Fig. 1. Batteries balancing system for n serially-connected batteries.

it. Section III delineates the system's implementation and provides design guidelines. Experimental results are then provided in Sections IV, Section V concludes the paper.

II. Principle of Operation

The balancing system, shown in Fig. 1, is divided into $m=n/3$ balancing modules, where n is the number of cells in the string. A single module is in charge of balancing three adjacent cells and the bus capacitor that is common for all the m modules. Each module consists of two half-bridge transistors assemblies at the cells' side (transformer's primary side), a transformer that provides isolation of the cells from the bus capacitor, and a full-bridge transistors assembly at the bus capacitor's side (transformer's secondary side).

The core concept of the balancing system is based on charge equalization by equalizing the voltages of the cells using a converter operating in DCM, where the balancing current is a function of the voltage difference between the cell and the bus. Balancing between the cells is achieved by a bus capacitor that operates as an energy buffer to create a parallel energy path, and each of the cells' voltages is equalized to the bus capacitor voltage.

The basic equalization circuit, shown in Fig. 2, comprises an isolation transformer, with unity transformer ratio (in this study), which is connected between the battery cell and the bus capacitor. The leakage of the transformer is used as a main inductance. The current that flows through this inductance is determined by the voltage difference between the battery cell and the bus voltage, which is V_{primary}–$V_{\text{secondary}}$, In this arrangement, the current naturally flows toward the source with the lower voltage and charges it. For this circuit the current's slew rate is given by

$$\frac{di_L}{dt} = \frac{V_{\text{primary}} - V_{\text{secondary}}}{L_{Lkg}}, \tag{1}$$

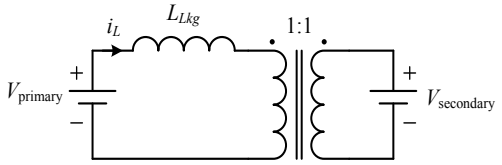

Fig. 2. Voltage equalizing circuit of a battery cell and the bus capacitor.

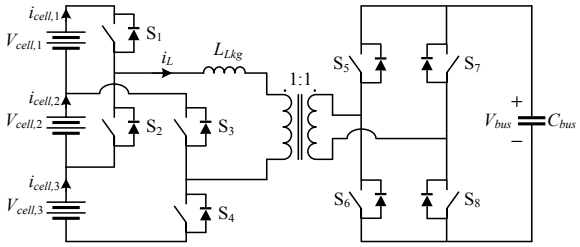

Fig. 3. Balancing module of three adjacent cells.

where L_{Lkg} is the transformer's leakage inductance. Employing this balancing approach for all the cells in the string, the bus capacitor voltage converges to the cells' voltages average value, given by

$$V_{bus} = \frac{1}{n}\sum_{k=1}^{n} V_{cell,k} \tag{2}$$

where $V_{cell,k}$ is the voltage of a single cell in the string (cell number k) and V_{bus} is the voltage of the bus capacitor. Since the bus capacitor is common for the entire string, all the cells are eventually balanced and their voltages are equal to (2).

A. Switching Sequence and Current Paths

A balancing module for three adjacent cells is depicted in Fig. 3. In every switching period T_s a different cell is being balanced. The balancing sequence is exemplified in Fig. 4 for cell no. 1 with the current paths highlighted in red. For this case, switches S_1, S_3, S_5 and S_8 are turned on for a predefined on time T_{on} (further details on setting the on time duration are provided in Section III), the transformer's primary side voltage is $V_{\text{cell,1}}$ and its secondary side voltage is V_{bus} (see Fig. 4(a),(c)). For the off time only switch S_3 remains on whereas S_1, S_5 and S_8 are turned off. Two possible states are recognized: $V_{\text{cell,1}}<V_{\text{bus}}$ and $V_{\text{cell,1}}>V_{\text{bus}}$, as depicted in Fig. 4(b) and Fig. 4(d), respectively. The two states are distinguished by the current direction during the on time and as a consequence, by the current continuity, the body diodes that conduct during the off time. In case that $V_{\text{cell,1}}<V_{\text{bus}}$ the body diodes of S_1, S_6 and S_7 are forward biased, the primary side's voltage is $V_{\text{primary}}=V_{\text{cell,1}}$ and the secondary side's voltage is $V_{\text{secondary}}=-V_{\text{bus}}$. In case that $V_{\text{cell,1}}>V_{\text{bus}}$, the body diodes of S_2, S_5 and S_8 are forward biased, the primary side's voltage is $V_{\text{primary}}=-V_{\text{cell,2}}$ and the secondary side's voltage is $V_{\text{secondary}}=V_{\text{bus}}$. Fig. 5 shows an idealized current waveform for the case that cell no. 1 is being balanced and $V_{\text{cell,1}} > V_{\text{bus}}$. As can be seen, the positive voltage difference between the cell and the bus is applied on the inductance during the on time whereas during the off time the applied voltage is negative with a magnitude that equals the sum of the voltages. This negative voltage ramps the current back to zero.

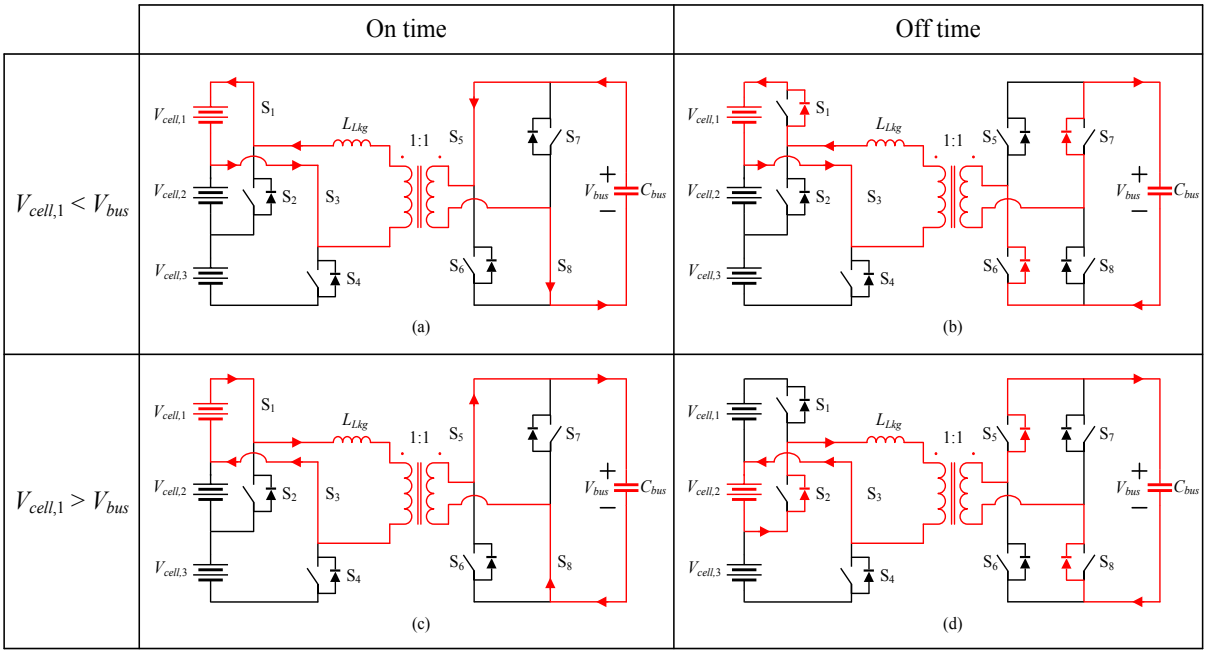

Fig. 4. Balancing operation of cell no. 1 for the case that $V_{cell,1}<V_{bus}$: (a) on time, (b) off time, and for the case that $V_{cell,1}>V_{bus}$: (c) on time, (d) off time. Red arrows mark actual current direction.

TABLE I – SWITCHING SEQUENCE OF A SINGLE BALANCING MODULE

	On time ($0<t<T_{on}$)			**Off time ($T_{on}<t<T_s$)**			
Active Cell	Active Switches	$V_{primary}$	$V_{secondary}$	State	Active Switches	$V_{primary}$	$V_{secondary}$
Cell 1	S_1, S_3, S_5, S_8	$V_{cell,1}$	V_{bus}	$V_{cell,1}<V_{bus}$	S_3	$V_{cell,1}$	$-V_{bus}$
				$V_{cell,1}>V_{bus}$	S_3	$-V_{cell,2}$	V_{bus}
Cell 2	S_2, S_3, S_6, S_7	$-V_{cell,2}$	$-V_{bus}$	$V_{cell,2}<V_{bus}$	S_3/S_2	$-V_{cell,2}$	V_{bus}
				$V_{cell,2}>V_{bus}$	S_3/S_2	$V_{cell,1}/V_{cell,3}$	$-V_{bus}$
Cell 3	S_2, S_4, S_5, S_8	$V_{cell,3}$	V_{bus}	$V_{cell,3}<V_{bus}$	S_2	$V_{cell,3}$	$-V_{bus}$
				$V_{cell,3}>V_{bus}$	S_2	$-V_{cell,2}$	V_{bus}

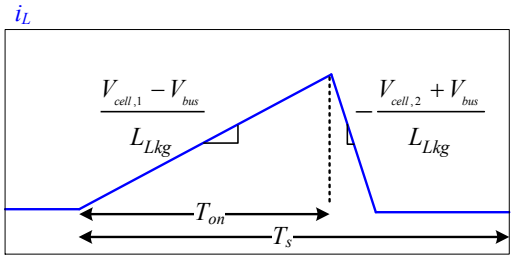

Fig. 5. Idealized current waveform of a single switching cycle for balancing cell no. 1 for the case that $V_{cell,1}>V_{bus}$.

The complete switching sequence of the module for balancing the 3 cells is detailed in Table I. It should be noted that balancing of cell no. 2 has two switching possibilities as explained in the next subsection.

B. Balancing Cycle Sequence

Two switching sequences are possible during the off time while cell no. 2 is being balanced (see Table I). That is, during the on time switches S_2, S_3, S_6, and S_7 are on, but during the off time it is possible to keep either switch S_2 *or* S_3 on, which determines $V_{primary}$ for this period. In case that S_3 is on then $V_{primary}=V_{cell,1}$, and for case that S_2 is on then $V_{primary}=V_{cell,3}$. This implies that during the off time, for the case that $V_{cell,2}>V_{bus}$, cell no. 1 or 3 is being charged. To avoid any undesired charging of only one of cells no. 1 or 3 and to evenly distribute both the stored energy between the cells and the processed power between the switches, cell no. 2 is balanced twice in each balancing cycle. Therefore, a balancing cycle consists of four balancing phases of the cells. In each balancing phase only one cell is being balanced, and the cell's balancing order is 1→2→3→2, as demonstrated in Fig. 6. Of particular interest is a balancing cycle of cell no. 3 ($2T_s<t<3T_s$), shown in Fig. 6 for $V_{cell,3}>V_{bus}$. In this case, the inductor current flows through cell no. 3 during the on time and through the cell no. 2 during the off time, so the voltage at transformer's primary side is clamped to $V_{cell,2}$..

III. IMPLEMENTATION AND DESIGN CONSIDERATIONS

To realize the balancing system of the architecture described in Fig. 1, several practical design challenges need to be addressed. This includes setting of the transistors sequence, design the allowed range of the balancing current to satisfy DCM operation, selection of the bus capacitor, and transformer's design; All need to be defined to ensure proper operation of the system.

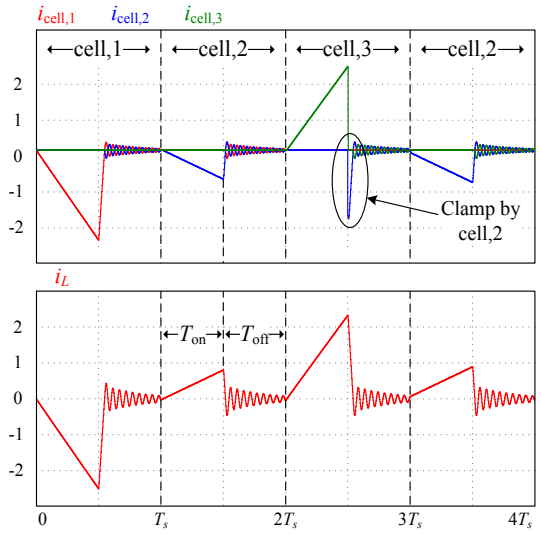

Fig. 6. Currents of the cells (top) and the transformer (bottom) during four switching cycles for the case that $V_{cell,1}<V_{cell,2}<V_{bus}<V_{cell,3}$.

A. *Transformer's Leakage Inductance, Bus Capacitor and Balancing Current Design*

The transformer's leakage inductance in this balancing system is utilized as the main inductor. The current that flows through the transformer in every switching cycle is governed by the on time of the switches T_{on}, the voltage difference between the cell and the bus capacitor ΔV and the inductance value L_{Lkg}. Since the circuit is operated in DCM, the peak inductor current I_{pk} and an inductor current ripple ΔI_L are equal and given by

$$I_{pk} = \Delta I_L = \frac{\Delta V}{L_{Lkg}} T_{on} . \tag{3}$$

After turning off the switches, the time it takes for the current to ramp down back to zero can be expressed as

$$T'_{off} = \frac{\Delta V}{V_{\text{primary}}\big|_{off} - V_{\text{secondary}}\big|_{off}} T_{on} , \tag{4}$$

where V_{primary} and $V_{\text{secondary}}$ during the off time are given in Table I. The average current in a single switching cycle is given by

$$I_L = \frac{\Delta V}{2L_{Lkg}} \left(1 + \frac{\Delta V}{V_{\text{primary}}\big|_{off} - V_{\text{secondary}}\big|_{off}} \right) \frac{T_{on}^2}{T_s} . \tag{5}$$

As can be seen from (5), in case that no voltage difference exists (meaning that the cells are balanced), i.e. ΔV=0 , the current is zero and no energy is processed by the system.

To assure that both leakage and magnetizing currents are zero at the end of every switching period, a sufficiently long off time needs to be allowed. Considering operation at constant switching frequency, this imposes a limitation on the maximum allowed on time. On the other hand, to achieve fast convergence of the cells' voltages, T_{on} should be set as high as possible. Idealized currents waveforms of the magnetization inductance, the leakage inductance and the bus capacitor are shown in Fig. 7. The currents' slew-rates when cell no. 1 is being balanced are detailed in Table II. Under the

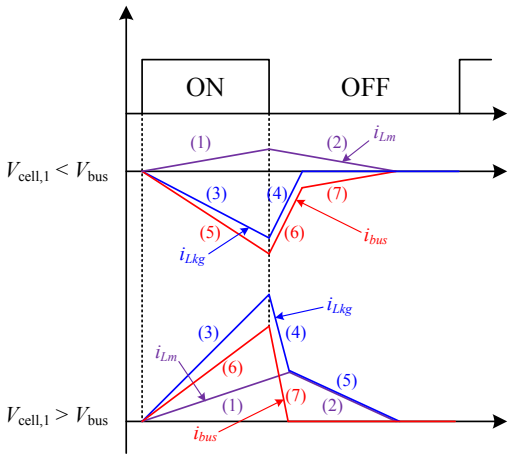

Fig. 7. Idealized currents waveforms of the magnetization inductance, the leakage inductance and the bus capacitor. The currents' slew-rates are detailed in Table II.

TABLE II – CURRENTS SLEW-RATES OF FIG. 7

$V_{cell,1} < V_{bus}$			$V_{cell,1} > V_{bus}$		
di_{Lm}/dt	(1)	$\frac{V_{bus}}{L_m}$	di_{Lm}/dt	(1)	$\frac{V_{bus}}{L_m}$
	(2)	$-\frac{V_{bus}}{L_m}$		(2)	$-\frac{V_{cell}}{L_m + L_{llg}}$
di_{Lkg}/dt	(3)	$\frac{V_{cell,1} - V_{bus}}{L_{Lkg}}$	di_{Lkg}/dt	(3)	$\frac{V_{cell,1} - V_{bus}}{L_{Lkg}}$
	(4)	$-\frac{V_{cell,1} + V_{bus}}{L_{Lkg}}$		(4)	$-\frac{V_{cell,1} + V_{bus}}{L_{Lkg}}$
di_{bus}/dt	(5)	$\frac{V_{cell,1} - V_{bus}}{L_{Lkg}} - \frac{V_{bus}}{L_m}$		(5)	$-\frac{V_{cell,1}}{L_m + L_{llg}}$
	(6)	$\frac{V_{cell,1} + V_{bus}}{L_{Lkg}}$	di_{bus}/dt	(6)	$\frac{V_{cell,1} - V_{bus}}{L_{Lkg}} - \frac{V_{bus}}{L_m}$
	(7)	$\frac{V_{bus}}{L_m}$		(7)	$-\frac{V_{cell,1} + V_{bus}}{L_{Lkg}} - \frac{V_{bus}}{L_m}$

abovementioned constraints, the minimum off time that is required for the magnetizing current to ramp back to zero is $T_s/2$, and therefore the maximum allowed on time, i.e. $T_{on,max}$, is also $T_s/2$. The value of $T_{on,max}$ for balancing cells no. 2 or 3 is the same.

Sizing of the bus capacitor can affect the proper balancing operation. Its voltage should converge to the cells' voltages average value relatively fast and therefore its capacitance should be relatively low. However, it must have sufficiently low voltage ripple so that it can be considered as a near ideal voltage source for each of the balancing phases, which require high capacitance. Therefore, the minimum bus capacitance must satisfy the condition

$$V_{ripple} << \Delta V , \tag{6}$$

where V_{ripple} is the voltage ripple of the bus capacitor. Using (5) and after some manipulations, condition (6) translates into

$$C_{bus} >> \frac{T_{on,\max}^2}{2L_{Lkg}} = \frac{1}{4L_{Lkg} f_s^2} . \tag{7}$$

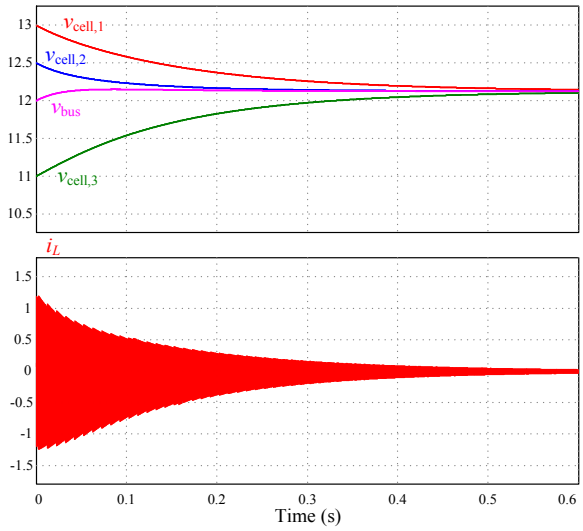

Fig. 8. Simulation results for 4 batteries cells emulated by large capacitors.

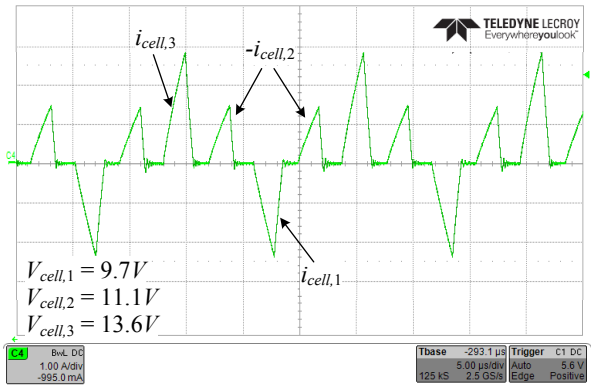

Fig. 9. Transformer's current during unbalanced steady-state operation. C4 – Transformer's current i_L (1A/ div), Time scale is 5µs/div.

To demonstrate the balancing operation of the system, a simulation case study has been carried out and the results are shown in Fig. 8. It depicts the convergence of three cells (emulated by large capacitors to allow timely convergence), each set with different initial voltage, to the cells' average voltage, validating the balancing capability of the system. As can be seen, the current magnitude decays to zero as the cells' voltages converge, in agreement with the theoretical prediction in (5).

IV. Experimental Verification

In order to demonstrate the balancing operation and verify the theoretical analysis and simulation results, several experiments have been carried out using three cells connected in series, built using large capacitors. Table III shows the components types and values of the experimental setup.

Fig. 9 shows the steady-state operation current waveform of the transformer for unbalanced cells with $T_{on}=T_s/2$. The cells' voltages are $V_{cell,1}$=9.7V, $V_{cell,2}$=11.1V and $V_{cell,3}$=13.6V. The differences between the cells' voltages and the bus voltage result in current flowing through the transformer. For this case the voltage relations are $V_{cell,3}>V_{bus}>V_{cell,2}>V_{cell,1}$, and therefore $i_{cell,3} > 0$, $i_{cell,2} < 0$ and $i_{cell,1} < 0$.

TABLE III – Experimental Prototype Values

Component	*Value/Type*
Batteries (emulated by large capacitors)	60 mF
Transformer's leakage inductance L_{Lkg}	1.5 µH
Transformer's magnetizing inductance L_m	700 µH
MOSFETs S_1-S_8	Si4168DY, 30V, 5.7mΩ
Bus capacitor C_{bus}	470 µF
Switching frequency f_s	250 kHz

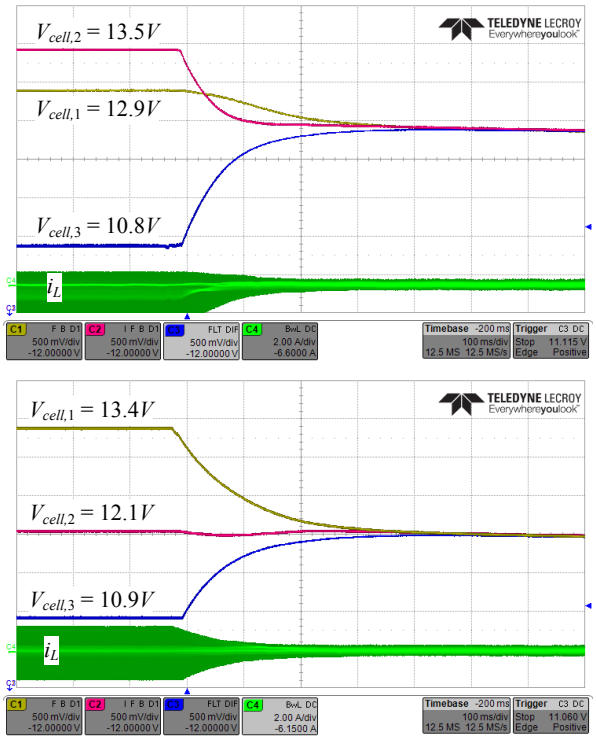

Fig. 10. Convergence of the cells' voltages for the cases that they are pre-charged to different values. C1 – $V_{cell,1}$ (0.5V/div), C2 – $V_{cell,2}$ (0.5V/div), C3 - $V_{cell,3}$ (0.5V/div), C4 – Transformer's current i_L (2A/div). Time scale is 100ms/div.

Fig. 10 shows the cells' voltages and the transformer's current over a long period of time for a case that the cells are pre-charged to different voltages. As can be observed, the voltages of the three cells converge to their average value, in agreement with the theoretical analysis, and the voltage difference between the balanced cells is negligibly small. Also, the current in the transformer decreases as the cells' voltages converge and ΔV decreases, as predicted in (5).

V. Conclusion

In this work, a new isolated balancing topology for serially connected batteries strings has been introduced. Fast convergence of the cells is achieved by using a parallel balancing approach with low voltage bus capacitor that is common for all the cells. Each balancing module is in charge of balancing three adjacent cells and therefore the number of components in the system is low. The DCM operation and the fact that no energy circulates in the system when the cells are balanced result in extremely low quiescent power loss. Control of the modules is very simple and does not require current nor voltage sensors to regulate the operation of the system. The theoretical analysis and the results of the experimental prototype demonstrated fast convergence of the cells to a negligibly small voltage difference.

ACKNOWLEDGMENTS

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