Hardware Efficient Digital Auto-Tuning Average Current-Mode Controller

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Abstract – **This paper introduces a new hardware efficient auto tuning for digitally controlled average current-mode (ACM) controllers. The auto-tuning procedure extracts the required coefficients of the ACM controller to achieve tight voltage regulation as well as closed-loop dynamic performance that may be defined by the end-user. System stability is facilitated for wide operation range under parameters uncertainties and other variations. It is found that information of the change in the state-variables suffice for a successful and accurate closed-loop operation without the need of a detailed extraction of the values of the passive components. The algorithm is applicable upon power up of the SMPS and has been integrated into the soft-start routine of the converter, assuring tight and stable regulation of the output voltage under all scenarios. The effectiveness of the new digital auto-tuning ACM controller is demonstrated on an experimental 500kHz, 12V-to-1.2V digitally controlled synchronous buck converter.**

I. Introduction

In recent years, the use of digital control for power management has gained an important role in technology advancement of high-performance power electronics systems [6]-[7]. Digital control offers potential advantages such as programmability of control and system parameters, flexibility in multitude of tasks that can be set by the user, scalability with semiconductor technology, easier system integration, as well as reduction of the number of the passive components. A benefit that stands out with the integration of digital technology in power management system is simplicity of the design, assuring adequate dynamic performance for wide range of operating conditions, component variations and for aging or temperature. The features are enabled by incorporation of automated or adaptive compensation methods to assure stability and the closed-loop dynamics. This can be achieved in a variety of ways such as multimode compensation [8]-[10], calibration [11]-[13], auto-tuning [14]-[16] and adaptive control [17], [18]. The latter two methods often employ on-line identification of the switch-mode power supply (SMPS) to extract its open-loop response from which the compensation parameters are extracted [19]-[23].

Among the various advantages of the digital approach, fast dynamic performance under load or input voltage changes is of key concern [3]-[6]. One approach to optimize the dynamic performance is to use digital current-programmed mode control [24]-[26]. With the rise in popularity of integrated voltage regulator modules (VRMs) [27], [28], the recent evolution of methods for on-line efficiency optimization, and current sharing for multi-phase stages, where the information of the average current is essential, the advantages of average current-mode (ACM) approach are becoming more apparent. The advantages and streamlined design methodology of ACM is being recognized and gaining popularity in several single and multiphase controllers such as [8]-[10]. There, the compensator is set by the operating conditions [8] and improves on a cycle-by-cycle basis [9], [10].

The objective of this study is therefore to introduce a new hardware efficient auto-tuning procedure specifically developed for integrated digital average-current mode digital pulse-width modulation (DPWM) control. It is a further aim of this study to detail the design of a fully digital auto-tuning ACM controller that follows the classical two-loop ACM design with an all-digital outer voltage and inner current loops as detailed in Fig. 1. The auto-tuning procedure is applicable upon system power up, i.e. through the soft-start routine. It relies on the data acquired by the digital controller of the SMPS (with additional dedicated hardware) to identify the system parameters and derives the compensation coefficients of both loops to meet a desired closed-loop response based on the specified system phase margin and bandwidth.

The rest of the paper is organized as follows: Section II describes the principle of operation and details the algorithm of the auto-tuning procedure for ACM controller. Section III provides an analytical analysis and tuning of the programmable compensators followed by a design example. Practical implementation including the digital architecture of the digital auto-tuning ACM controller are delineated in Section IV. Experimental verification of a prototype utilizing the digital auto-tuned ACM controller is provided in Section V. Section VI concludes the paper.

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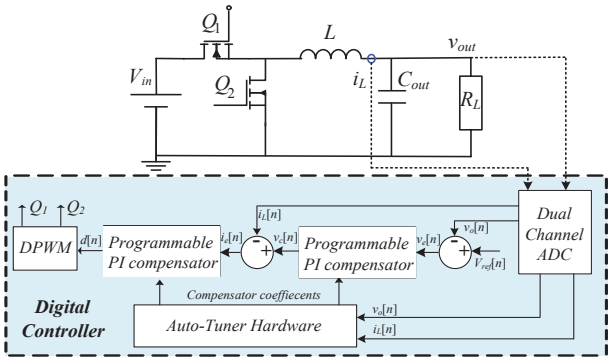

Fig. 1. Simplified diagram of a synchronous buck converter with the digital auto-tuning ACM controller.

II. Auto-Tuning Procedure for ACM Controllers

Many current-programmed controller architectures reported in the literature or as commercial applications prefer the peak current-mode (PCM) control method over ACM [26], [31]-[33]. One of the main arguments for this is that PCM can achieve superior dynamics and offer cycle-by-cycle protection with simpler hardware. With digital implementation, the hardware requirements of ACM are equivalent, or even lower than those of voltage-mode control. Adding the fact that no high-speed mixed-signal design is required (as in the case of PCM), since it can be designed entirely by HDL description, ACM control becomes an attractive compensation type. Adding the flexibility in the compensator design and straightforward approach for current sharing, several commercial applications such as [8]-[10] have been recently implemented digital ACM for voltage regulators, in particular for higher power where dual and multiphase converters are required.

The digital ACM controller that has been realized in this study is described with the aid of Fig. 2, which shows a conceptual block diagram of the control system. As can be seen in Fig. 2, the controller follows the classical two-loop ACM design with an all-digital outer voltage and inner current loops. The voltage loop creates a digital reference $i_c[n]$ for the average current value $i_L[n]$ based on the voltage error signal $v_e[n]$ and the voltage loop compensator. The current error signal $i_e[n]$ is the input to a current loop compensator that generates the duty-command $d[n]$ which is then sent to the DPWM, and a pulse width modulated signal $c(t)$ is created.

Based on the ACM controller architecture, in the context of auto-tuning of the controller, two sets of compensators' coefficients need to be extracted. These are for the inner (current) loop and outer (voltage) loop compensator. As reported in many studies the design of two loops with significantly different bandwidths, i.e. the current loop is with a wider bandwidth than the voltage loop, simplifies the compensators' structure, and a simple PI scheme can be used for both current and voltage loops' compensators [34], [35]. Since each of the loops is tightly regulated using a single state-variable, decoupling of the loops can be assumed, i.e. the coefficients for each controller can be extracted independently and further adjusted without significantly affecting the operation of the other loop.

In this study, it is assumed that the input voltage V_{in} and the nominal load current I_{out} of the power stage are known or can be measured. All the other converter's parameters, with special emphasis on the converter's inductance L and capacitance C_{out}, are unknown and may vary, either by design considerations or as a result of a drift. It is further assumed and justified by the control scheme that the compensators' template is PI-type. Two state-variables measurements in system are used for the output voltage v_{out} and the inductor current i_L, and they are obtained using dual-channel analog-to-digital converter (ADCs). The coefficients are extracted by the information available in the loop, either as a result of natural variation (current ripple) or induced perturbation of the state-variables. The aim of the auto-tuning algorithm is to extract the compensators' parameters to achieve tight output voltage regulation as well as stability over wide range of L and C_{out} values. More precisely, the performance goals are specified to satisfy: a) a minimal phase margin of 45º for both loops; b) control bandwidth as high as possible, derived as a fraction the switching frequency under the assumption that the current loop has higher bandwidth as the voltage loop; c) the output voltage is kept within specified margins.

To assure that stability is achieved within all corners of the variations that have defined the operation range, "artificial" tolerances are added to the design procedure. That is, although a single set of coefficients can achieve the target goal per specified plant, stability verification is embedded in the algorithm to cover the full range that is specified. Naturally, this implies that the dynamic response is optimized to one set of values and would deviate from that point for other values, but as long as the values are within the tolerance range that has been assumed, stability is maintained. The auto-tuning procedure is applicable at running mode, but also during start-up, i.e. when v_{out} has not yet reached its nominal value. This means that with the tuning procedure, the controller must also observe and correct v_{out}. To this end, a voltage-mode integrator-type compensator of low bandwidth (significantly lower than the target) is initially set on power up and is in charge of ramping up the output voltage, i.e. by slowly increasing the reference V_{ref}.

A high-level view of the tuning procedure is illustrated in the flowchart of Fig. 3, which can be divided into two main stages. When the tuning procedure initiated, a default set of pre-loaded coefficients are used to both compensators. These can be obtained from the initial specification of the target application. In case that no information is available on the system, then the values are set to satisfy stability with very low bandwidth that is derived as a fraction of the switching frequency. The tuning operation is conducted per loop. First, the algorithm extracts coefficient for the current loop. This is done by the information obtained from the inductor's current ripple on a basis of sampling twice per switching cycle. Effectively, along with the information of the system voltages, the measurement of the inductor current ripple estimates the inductance value, from which the compensator may be set with a defined crossover frequency. Once the inner current loop tightly regulates the average value of the inductor current, the system is of first order

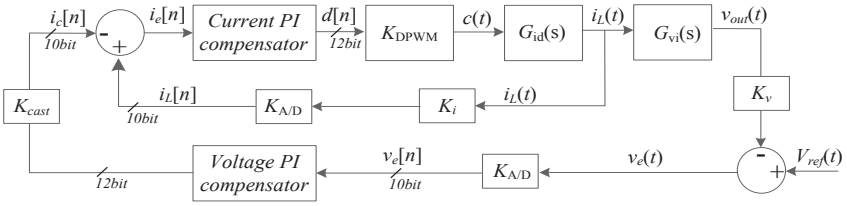

Fig. 2. System block diagram including the buck converter and ACM controller corresponding gains.

and stability is satisfied (but not regulation) [35]. The next stage of the tuning process is to achieve the dynamic performance by extraction of the coefficients of the voltage loop. In this stage, the inner current loop is used as a current source to drive a small current step to the output *RC* network and perturb its voltage from which an estimate of the output capacitance provides the required information to set the coefficients of the second compensator. The analysis and in-detail description of the algorithm are provided next.

III. Extraction of the ACM Controller Coefficients

An established virtue of any two-loop compensation for SMPS is order reduction of the system from a second order into two simpler control loops. Under ACM control scheme, a PWM and in particular a buck converter can be well approximated by a first-order system at frequencies well below the switching frequency f_{sw}, and therefore a PI-type compensator suffice [34], [35]. A conventional PI compensator transfer function in the continuous-time domain can be expressed as

$$G_{comp}(s) = k_P\left(1+\frac{1}{sT_i}\right), \tag{1}$$

where k_p is the compensator's proportional gain and T_i is the integrator time constant which determines the compensator's zero, i.e. $T_i=1/2\pi f_0$. By applying the pole-zero matching method [30] on (1), the discrete-time representation of the template for the PI compensator is given by

$$G_{comp}(z) = \frac{a-b\cdot z^{-1}}{1-z^{-1}}, \tag{2}$$

where a, b are the compensator coefficients, and can be calculated as

$$a = k_p \quad , \quad b = k_p\left(1-T_S/T_i\right), \tag{3}$$

where T_s is the sampling period.

The compensator coefficients are set so that the closed-loop goals are achieved for both phase margin and control bandwidth. The closed-loop response of a first-order system that is controlled by a PI-type compensator has a well-defined behavior. The controller gain with respect to the open-loop response determines the bandwidth while the location of the PI's zero controls the phase margin. From (1) through (3) it can be observed that in this case too, the assignments of the coefficients follows a similar method. The control bandwidth of the proportional gain k_p is set as the gain value at the target crossover

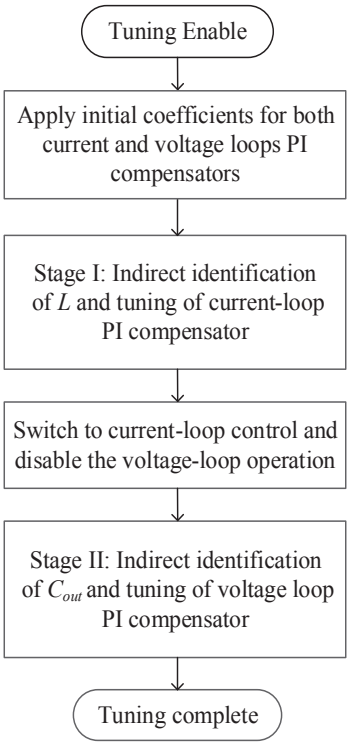

Fig. 3. Flowchart of the controller's tuning procedure.

frequency f_c. Next, to satisfy stability with prescribed phase margin φ_m, the frequency of the compensator's zero f_0 is set using the following expression [35]

$$f_0 = f_c\sqrt{\frac{1-\sin(\varphi_m)}{1+\sin(\varphi_m)}} = \frac{1}{2\pi T_i}. \tag{4}$$

It should be noted that in this study, the crossover frequency is set as a fraction of the switching frequency, typically one-tenth (1/10) to one-eighth (1/8) for the outer voltage loop and approximately one-fifth (1/5) for the inner current loop. By doing so, the tuning procedure does not depend on preceding information or data of the system to facilitate closed-loop operation. Assuming that the power stage is designed according to the frequency range, then the system dynamics are continuously optimized to widest response bandwidth that can be achieved with a steady-state linear-type compensation. In addition, the information of the switching frequency is internally available to the controller, which requires very few resources (or none) to obtain.

A. Current Compensator Design

Given target closed-loop parameters, the tuning task is to extract the integral time constant $T_{i,I}$ and the proportional gain k_{pI} for the inner current loop. As mentioned earlier, the former is determined by (4) to satisfy stability. The latter is inversely proportional to the overall gain of the inner current loop, and with the aid of Fig. 2 can be found as

$$k_{pI} = \frac{1}{G_{id}(s) K_I K_{A/D} K_{DPWM}}, \tag{5}$$

where K_I is the gain due to the current sensing, $K_{A/D}$ and K_{DPWM} are the gains of the peripheral units of the current loop, and $G_{id}(s)$ is the control-to-output transfer function of the inner current loop, in a buck converter is given by

$$G_{id}(s) = \frac{i_L(s)}{d(s)} = \frac{V_{in}}{sL + R_{DCR}} \quad , \tag{6}$$

where R_{DCR} is the dc resistance of the inductor.

By substituting (6) into (5), and setting $s = 2\pi f_{cI}$ at the target crossover frequency of the current loop, (5) can be rewritten as

$$k_{pI} = \frac{2\pi f_{cI} L + R_{DCR}}{V_{in} K_I K_{A/D} K_{DPWM}}. \tag{7}$$

It should be noted that, since R_{DCR} is relatively small, it is therefore neglected during the tuning procedure in this study. From (7), it can be seen that $k_{p,I}$ can be extracted from the information of the input voltage V_{in} (which is known or can be measured) and the inductance L (the peripherals gains i.e. K_I, $K_{A/D}$, K_{DPWM} are known constants). The inductance value can be replaced using the following relationship $\Delta i_L/\Delta t = v_{out}/L$, where Δi_L is obtained by two samples of the state-variable within a cycle and v_{out} can be assumed as non-varying or constant for the measurement timeframe. Rearranging (7) and by transformation from a continuous-time to the discrete-time domain, the current loop proportional gain k_{pI} can be expressed as

$$k_{pI} = \frac{2\pi f_{cI}}{2 f_{sw} V_{in} K_V K_{A/D} K_{DPWM}} \cdot \frac{v_{out}[n]}{\Delta i_L[n]}. \tag{8}$$

As can be seen from (8), the extraction of the proportional gain k_{pI} primarily depends on the (fixed) ratio between the crossover frequency f_{cI} and the switching frequency f_{sw}, the output voltage and the ripple of the inductor current.

B. Voltage Compensator Design

In the second stage of the tuning procedure, the proportional gain k_{pV} for the voltage PI compensator is iteratively tuned such that the specified outer loop-gain bandwidth is satisfied. In a similar manner to the current compensator, with the aid of Fig. 2 K_{pV} is inversely proportional to the overall gain of the outer voltage loop and is given as follows

$$k_{pV} = \frac{1}{G_{vi}(s) K_V K_{A/D} K_{cast} \dfrac{1}{K_I K_{A/D}}}, \tag{9}$$

where K_V is the gain due to the voltage divider on the output voltage, $K_{A/D}$ and K_{DPWM} are the gains of the peripheral units within the voltage loop, and K_{cast} is the gain due to the matching between the bits number of the voltage compensator and the accumulator (See Fig. 2). $G_{vi}(s)$ is the control-to-output transfer function of the outer voltage loop, in a buck converter it is given by

$$G_{vi}(s) = \frac{v_{out}(s)}{v_c(s)} = R_L \frac{sC_{out}R_{ESR} + 1}{sC_{out}R_L + 1}, \tag{10}$$

where R_L is the load resistance and R_{ESR} is the equivalent series resistance of the output capacitor C_{out}. It should be noted that, while R_{ESR} has an important role in the case of electrolytic capacitors, it is neglected in the case of ceramic capacitors. The case of non-negligible equivalent series resistance is beyond the scope of this work, and therefore the transfer function $G_{vi}(s)$ can be expressed as

$$G_{vi}(s) = \frac{v_{out}(s)}{v_c(s)} = \frac{R_L}{sC_{out}R_L + 1}. \tag{11}$$

By substituting (11) into (9) and setting $s = 2\pi f_{cV}$ at the target crossover frequency of the outer voltage loop, the proportional gain k_{pV} is given by

$$k_{pV} = \frac{2\pi f_{cV} C_{out}}{K_V K_{A/D} K_{cast} \left(1/K_I K_{A/D}\right)}. \tag{12}$$

From (12), it can be observed that k_{pV} depends on the peripherals gains, the crossover frequency and output capacitor value. A major goal of this study is to avoid the direct extraction of the passive elements. In a similar way as in the extraction of the coefficients in the inner loop, the value of C_{out} is replaced by the following relationship $\Delta v_{out}/\Delta_t = \Delta i_L^*/C_{out}$, where Δi_L^* is the (known) perturbation that is applied by the inner current loop as a current source and Δv_{out} is obtained by measuring the output state-variable [35]. As shown in the tuning flowchart (see Fig. 3), stage II is initiated once the internal current loop is controlled, hence the current compensator is utilized as a current source to perturb the output network (i.e. load steps Δi_L^*) and then measuring the changes at the output voltage (Δv_{out}^*). Therefore, by rearranging (12) and transforming from the continuous-time to the discrete-time domain, k_{pV} can be expressed as

$$k_{pV} = \frac{2\pi f_{cV}}{f_{sw} K_{cast}} \cdot \frac{\Delta i_L[n]}{\Delta v_{out}[n]}. \tag{13}$$

As can be seen from (13), the extraction of the proportional gain k_{pV} primarily depends on the ratio between the crossover frequency and the switching frequency and the measurements of the changes in the output voltage as a result of injecting current perturbations.

IV. Practical Implementation

A. Implementation Issues

In order to implement the auto-tuning on DPWM controlled SMPS there is need to obtain the values of state-variables at sampling events sufficiently away from the switching action, allowing sample with relatively high signal-to-noise ratio. Since perturbation is involved in parts of the tuning process (in particular in Stage II), a compromise must be considered between the amount of deviation that is created (or allowed) in the signal and the accuracy (and resolution) of the perturbation (DPWM unit) and the measurement (ADC). Ideally, the size of the injected perturbation should be kept as small as possible, to guarantee small disturbance at the output voltage, i.e., the operating point will not be moved significantly [23]. However, due to practical limitation of the ADC, the size of the step disturbance designed such that a sufficient change at the output voltage is excited to allow a reliable measurement.

Another noise sources that are not related to the switching action such as quantization or thermal noises may also affect the accuracy of the coefficients extraction. To remedy this, synchronous averaging of samples has been employed to average out misreading of uncorrelated signals. This has been carried out by 32 word-long auto-regressive moving average (ARMA) filter for Stage I (current loop), and a 16 samples ARMA filter has been utilized in stage II (voltage loop). Obviously, this averaging process significantly extends the duration of the tuning routine, which may be traded for accuracy in cases where the specification mandate shorter periods. It should be noted that the accuracy of the compensators in the long-run is not necessarily compromised since the coefficients may be refreshed or updated at any time as it is applicable at any level of the operating conditions.

B. Digital Architecture

Shown in Fig. 1 is a schematic diagram of a buck converter with the implemented digital auto-tuning ACM controller. The controller is based on the architecture presented in [36] and relies on three key building blocks: 1) a dual-channel adaptive 10-bit delay-line (DL) based window-ADC [4], [26], [36]. 2) a 12-bit programmable PI compensators, that have been realized with shared hardware resources for calculations, resulting in reduced power consumption and logic element count. 3) a 12-bit hybrid high-resolution DPWM (HR-DPWM).

Fig. 4 delineates the auto-tuner hardware module as part of the complete block diagram of the digital auto-tuning ACM controller. It can be observed that the auto-tuner module based on several main units:

- Mode selector that is realized by a finite state-machine (FSM), and is responsible for executing the tuning procedure as described in Fig. 3.
- Perturbation logic block that initiates a variation of the current reference of the inner current loop at stage II of the tuning procedure, which eventually results in a mismatch between the inductor current and the load current as described in the design procedure.
- A volatile memory register and a fixed-point arithmetic module, which calculates and stores the extracted coefficients of both the voltage and current compensators.

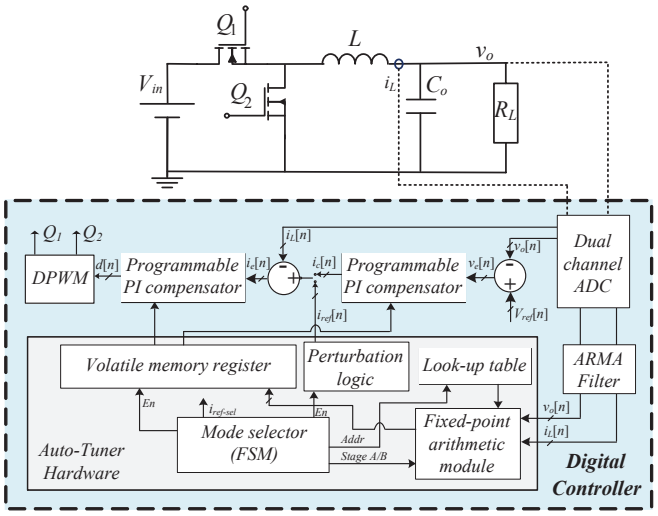

Fig. 4. Full block diagram of the digital auto-tuning ACM controller.

In order to implement a hardware efficient digital auto-tuning system and to simplify the arithmetic operations that calculates the compensators' coefficients according to (4), (8), and (13), in this work the realization of the arithmetic module relies on a simple set of look-up tables (LUTs) [15]. One LUT is responsible for extracting the compensator's zero f_0 according to the desired phase margin φ_m. Another LUT extracts the ratio between the crossover frequency f_c and the switching frequency f_{sw}, for both the inner and outer loops. It should be noted that the LUTs consist of pre-stored values that are selected by the mode selector. Additionally, all other calculations have been performed by one unsigned 16x16 bits multiplier, one signed 16x16 bits multiplier and one unsigned 16-bit divider.

V. Experimental Verification

The auto-tuning algorithm and the control hardware were fully coded in VHDL and implemented on a Cyclone IV FPGA [37], including custom design of an all-digital adaptive 10-bit window delay-line ADC and 12-bit DPWM. The tuning and control VHDL representations were synthesized and implemented using Quartus environment, resulting in approximately 3,000 logic cells. To demonstrate the operation of the auto-tuning algorithm and to validate closed-loop operation of the ACM controller, a 12V-to-1.2V synchronous buck converter prototype has been built and tested. The experimental setup is shown in Fig. 5. The experimental setup comprises of SiC620A DrMos power-stage [38], where the current sensing for the inner loop tuning and regulation is obtained by a series-sense resistor setup [39]. Table I lists the components values and parameters of the experimental prototype.

TABLE I – EXPERIMENTAL PROTOTYPE VALUES

Component	*Value/Type*
Input voltage V_{in}	12V
Nominal output voltage V_{out}	1.2V
Nominal output current I_{out}	8A
Switching frequency f_{sw}	500kHz
Inductor L	1µH, 5mΩ DCR
Capacitor C_{out}	100µF, 5mΩ ESR
Power-stage	SiC620A

Fig. 6 shows the output voltage and inductor current during the tuning soft-start operation, whereas the inductor L=1µH and output capacitor C_{out}=100µF. It can be observed that the while converter's soft-start operation lasts approximately 2ms, the tuning procedure is conducted under than 0.6ms. The dynamic behavior of the tuned controller detonating tightly regulation of the output voltage under load transient events of 5.5A is depicted Fig. 7. For the loading transient event an output voltage undershoot of 110mV has been measured with settling time of 38µs, whereas for the unloading event the output voltage overshoot has been measured to be 140mV and 45µs is the time it takes for the system to set back to steady-state.

To verify the effectiveness of the new auto-tuning ACM controller, the system was tested with several combinations of inductors and output capacitors. The target parameters for the compensators design were f_{cI} = 80kHz, $f_{0,I}$ = 8kHz for the inner current loop and f_{cV} = 40kHz, $f_{0,V}$ = 8kHz for the outer voltage loop, respectively. Table II summarizes the tuning results for inner current and outer voltage loops compensators coefficients extraction for various values of LC filter. It can be observed that, the coefficients extracted by the hardware are found to be in very good agreement with the theoretical results over wide range of operating conditions. The slight discrepancy between the theoretical and experimental results are within the numerical error of the calculation units.

VI. CONCLUSION

A new hardware efficient fully-digital auto-tuning ACM controller has been presented, verified through analysis, simulation and experimental data. The tuning algorithm extracts the loop coefficients based on a sequence of time-domain measurements, applied on each state-variable independently either through the natural changes of the variables or by small perturbations. It is found that information of the change in the state-variables suffice for a successful and accurate closed-loop operation without the need of a detailed extraction of the values of the passive components. The tuning procedure is applicable during converter start-up period, maintaining closed-loop operation of the converter. Very good coefficients extraction accuracy has been demonstrated as well as stability assurance for the entire operation range. The resultant dynamic performance is well compared to any other rapid steady-state linear-type compensation

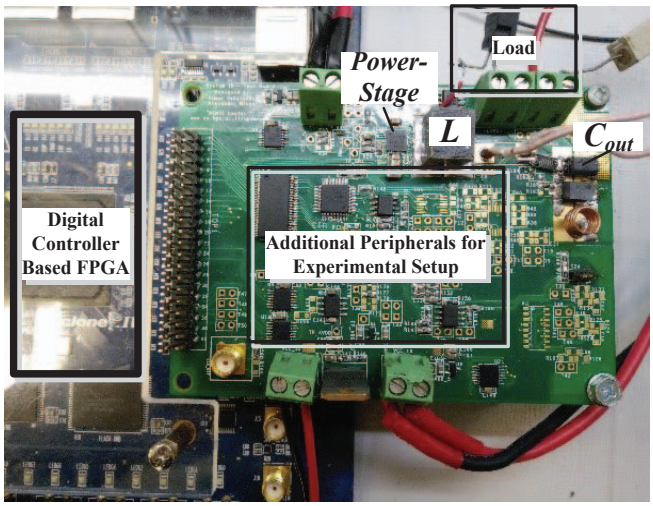

Fig. 5. Experimental prototype for evaluation of the auto-tuning ACM controller. The controller and tuner are realized on FPGA, PCB comprises a synchronous buck converter and additional periphery for signal integrity.

ACKNOWLEDGMENT

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TABLE II – AUTO-TUNING RESULTS WITH DIFFERENT INDUCTORS AND OUTPUT CAPCITORS

		Derived LC		*Current Loop Extracted Coefficients*		*Voltage Loop Extracted Coefficients*	
***L*[µH]**	***C*$_{out}$[µF]**	L[µH]	C_{out}[µF]	a_I	b_I	a_V	b_V
0.5	50	0.528	54.3	0.01382	0.01268	13.65	12.28
1	100	0.978	106	0.0256	0.02349	26.6	23.96
2.2	150	2.3	157	0.06021	0.05523	39.46	35.49

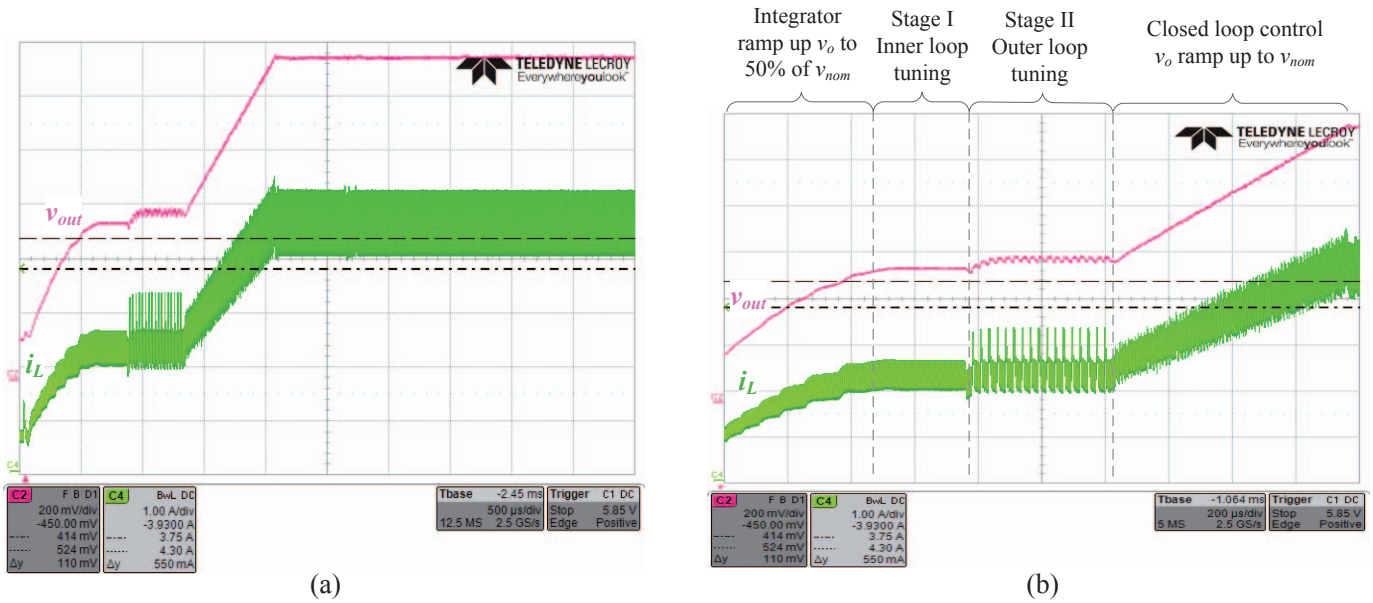

Fig. 6. Experimental results of the soft-start period with auto-tuning: (a) soft-start and regulation, (b) zoom in on the tuning procedure (V_{out} 200mV/div, i_L 1A/div, time scale is 200µs/div).

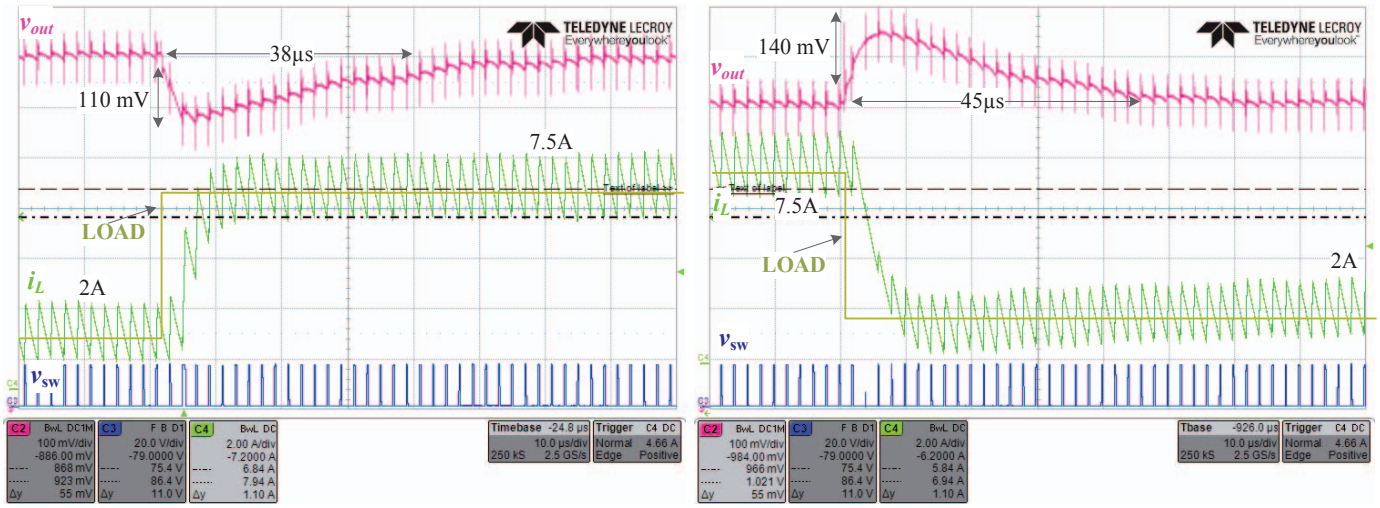

Fig. 7. Experimental load steps of 5.5A with 1µH inductor and 100µF ceramic output capacitor (v_{out} 100mV/div, i_L 2A/div, V_{sw} 20V/div, time scale is 10µs/div).

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