

Digital Self-Tuning Controller for ZCS Resonant Converters Operating in the 10MHz-Range

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Abstract— In this study, a controller for switched-resonator converters operating in the 10MHz range is presented with self-tuning capabilities. The control scheme provides a fast and accurate two-stage lock-in procedure to ensure zero-current switching at high frequencies, maintaining low control workload. The various modules of the controller are detailed, including the self-tuner based on a digital delay-locked loop, and a Rogowski-type on-board zero-current detector. Simulation and experiments were conducted to verify the design of the controller using a gyrator resonant switched-capacitor converter as the switched-resonator power stage.

Keywords—switched-capacitor converters control, system identification, switched-resonator converters, self-tuning control

I. INTRODUCTION

Miniaturization trends in portable electronics and ongoing quests for converters with increased power density have created a growing interest in high-frequency resonant and soft-switching topologies over the last decade [1-5], thus to allow volume reduction while maintaining high efficiency. Switched-resonator converters such as the resonant-switched-capacitor converter (RSCC) [6-11], resonant multi-level binary/Fibonacci converters [12-19] and the gyrator resonant switched-capacitor converter (GRSCC) [20-23] offer potentially higher power density alternatives [20] to switched-inductor converters, with soft-switching capabilities, that in turn, allow higher operating frequencies with reduced loss penalties.

To facilitate precise soft-switching operation, voltage or current sensing is essential, however the straightforward translation of solutions of lower frequencies requires sensor with ultra-high gain-bandwidth product, which finds the applications prohibitive. As a workaround, solutions that observe the zero-crossing point can be employed [24-25], however, there too the sense-to-response latencies prevent continuous cycle-by-cycle signal monitoring for high frequencies. The concept of sampling at turn-off, previously presented for light-load, low-power DCM Buck realizations [26-31], provides binary-type information whether the turn-off is early or late which enables adaptive calibration that

locks into the soft-switching operating point. This solution allows compensation for drifts as a result of component aging or temperature. Realization of high-frequency resonant converters in the 10MHz range has been often facilitated by self-oscillating mechanism so that the soft-switching as well as the drive challenges are resolved [3]. However, in cases when regulation is required, or for the operation of RSCC, natural switching point may not suffice to cover wide operation range. It has become apparent that incorporation of calibration and tuning procedures are mandatory in the advancement of these converters.

In switched-resonator converters, in a similar manner as in the PWM approach, the information of the transistor current polarity around the turn-off instance can be used for trimming and calibration purposes. For example, as illustrated in Fig. 1 the transistors' current at the instance

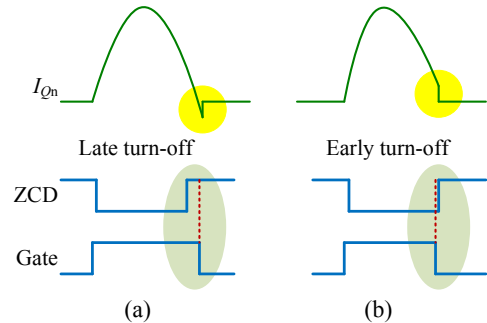


Fig. 1 Zero-cross detection on the current waveform of a resonant circuit switched-off in proximity to half-resonance. (a) late turn-off; (b) early turn-off

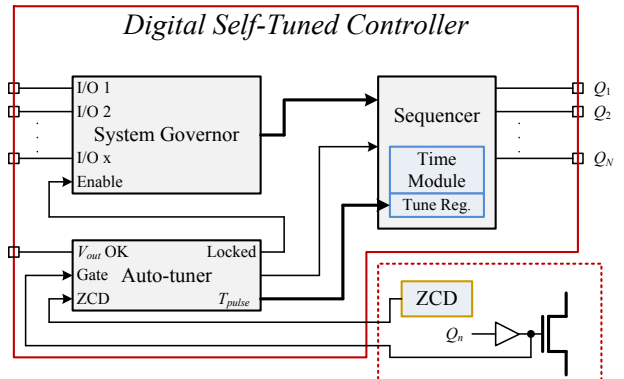


Fig. 2 Block diagram of the controller for switched-resonator converters

prior to turn off will be negative after half-resonance or positive before half-resonance. However, since major portion of the energy is transferred within a switching cycle, the binary-type information may extend the convergence time and increase losses. In addition, as will be detailed in this paper, the current polarity may invert as a result of the switching sequence that is applied on the resonant network.

The objective of this work is to present a tuning procedure and controller architecture (Fig. 2) to efficiently operate a switched-resonator based converter and assure soft-switching operation with a flexible frequency range without sacrificing accuracy. The controller operation is experimentally demonstrated on the GRSCC showing rapid and accurate lock-in capabilities.

The rest of the paper is organized as follows: Section II describes the principle of operation for the controller through the various modules. Section III provides the experimental results. The work is then concluded in Section IV.

II. DIGITAL SELF-TUNED CONTROLLER

The self-tuned controller illustrated in Fig. 2 is described in general form and can be applied to various types of RSCC-based single or multi-stage converters topologies such as the GRSCC, binary/Fibonacci [12] or other [13-19] converters. The description is assisted by a practical case study of a GRSCC [20] realization, illustrated in Fig. 3, that provides very low output impedance emulation for voltage-regulation module (VRM) applications (infinite electronic capacitor, fully published in [23]). The GRSCC shares topological foundations with the RSCC family while its efficiency characteristics and sourcing capabilities resemble a converter of a switched-inductor nature. The controller supports all features of the GRSCC including regulation of the output voltage (by governing the current-flow to the output) and dictates the flow direction. The controller consists of the following modules as depicted in Fig. 2 (described in-detail in the subsections below): a) a system governor to manage, synchronize and dictate the operation mode, b) switching sequencer to generate the required switching scheme, c) a zero-cross detection periphery, and d) self-tuning unit to adjust and calibrate the conduction-time of the switches.

A. System Governor

The *governor* module dictates the desired operation mode of the converter, based on a word dictated by configurable I/O pins (I/O 1 to I/O x in Fig. 2). In the simplistic case of a conventional RSCC, the governor decisions may be limited to whether a single pulse is needed in light load, full mode or none. In multilevel and further complex topologies this module is responsible to determine the optimal target conversion ratio and pass the information to the sequencer. In the case-study of the GRSCC, the governor adjusts the transfer function by pulse-density modulation (PDM) to support voltage regulation. The governor also dictates energy transfer direction to allow for voltage shaping in applications such as envelope-tracking

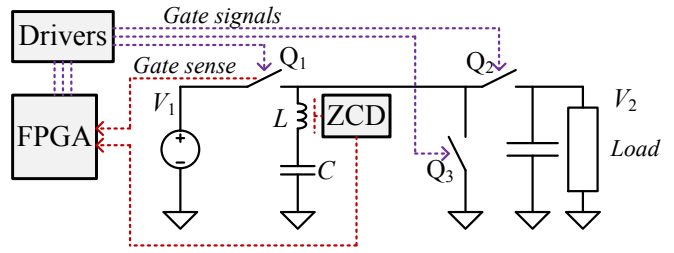


Fig. 3 Simplistic diagram of a basic GRSCC converter

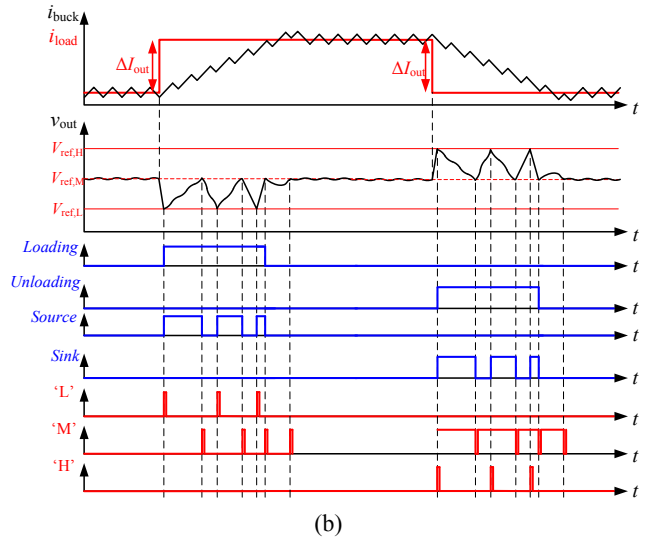
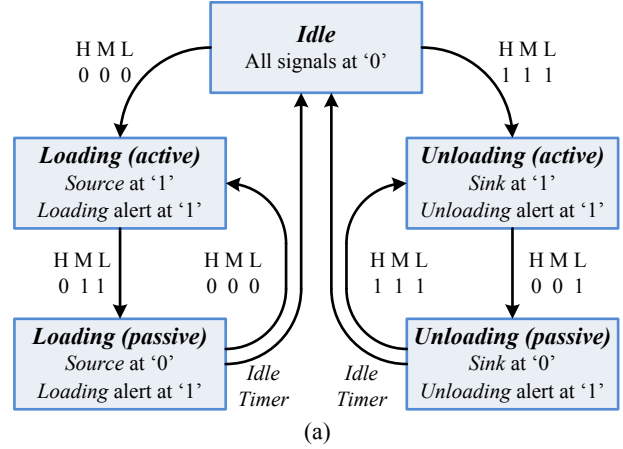


Fig. 4 System governor for a grsc implementation as an infinite capacitor for VRM load-side [23]. (a) State-machine flow-chart; (b) example waveforms.

[22] or mitigation of transient effects on a converter's output voltage [23]. Effectively, the governor is the most variant module and needs to be tailored in to the application.

Fig. 4 describes a simplistic block-diagram of the state machine and explanatory waveforms for a GRSCC realization capable high capacitance emulation. There, three comparators sensing the load-side voltage create virtual voltage boundaries (*H* and *L*), in addition to a center-sense (*M*) that trigger the converter to compensate for any current mismatch between a main (buck) converter and the load. These inputs to the system governor trigger a state machine which consists five states as described in Fig. 4(a): one idle

state, two states which trigger the power stage in the appropriate current sourcing or sinking direction according to the triggering comparator, and two additional states provide indication to any external controller (operating the original power-stage), that a loading / unloading transient has been detected, since the output voltage is now tightly bound, and cannot be used for conventional voltage-mode control anymore. Complete details on the interface with the main buck controller are detailed in [23].

B. Sequencer

The *sequencer* module translates the desired action from the other modules to the correct switching sequence for the power-stage's gates to execute. The module incorporates an internal self-clocked high-resolution timer to ensure correct pulse-length. The timer length is dictated by a register accessible from the calibration module described next. Protection logic and other gating-related features are also incorporated in this module to allow full completion of a sequence and to avoid collision due to conflicts that may arise if data from the activation modules changes or is incorrect.

In the context of the presented case study of a GRSCC, the governor module produces the control commands: *source* signal to transfer energy to the output, a *sink* signal reverse the current, or no signal to allow regulation by adding spacing between pulses or delays, i.e. PDM. Fig. 5 shows a conceptual timing diagram for the operation of the governor and the sequencer modules. Upon a *source* command signal, the module outputs a complete $Q_1 \rightarrow Q_2 \rightarrow Q_3$ sequence (See Fig. 5) which repeats as long as the signal remains high. Upon a *sink* command signal, the module outputs a complete $Q_3 \rightarrow Q_2 \rightarrow Q_1$ sequence. The command signals are internally blanked by the sequencer until the completion of a sequence where the decision is made to whether the sequence should be repeated; hence the operation can be reversed only upon commencing a new sequence. Further protection is embedded in this module, such as dead-time, or special cases, e.g. at transition from source to sink and vice versa, the gate signal that ends the primary sequence will be omitted from the next sequence for correct operation.

C. Zero-cross detector

There are several ways to implement ZCD, IC realization can be obtained by SenseFet, current mirroring or replica [33-35]. This however involves mixed-signal design to facilitate current sensing. Since in this study, the primary focus has been placed on the digital controller, the information of the zero-crossing signal has been designed separately through an on-board solution. The circuitry of the zero-crossing detector is depicted Fig. 6, which shows a variation of Rogowski-type sensor. Here, an open-core inductor with multiple windings operates as a secondary winding to the resonator inductance. The inductor is strategically placed near the resonator's air inductance and captures a portion of the magnetic field through weak coupling [36]. The voltage developed at the terminals of the secondary side connect is clamped by anti-parallel diodes

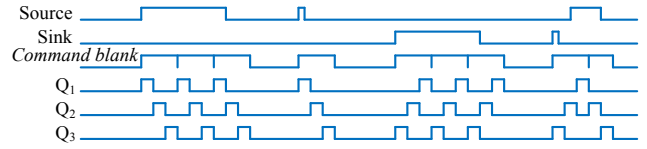


Fig. 5 A GRSCC realization timing diagram for the behavior of the gate signals Q_1 - Q_3 to different command possibilities. 'Command blank' represents an internal signal that masks any change in the sink and source signals during a sequence.

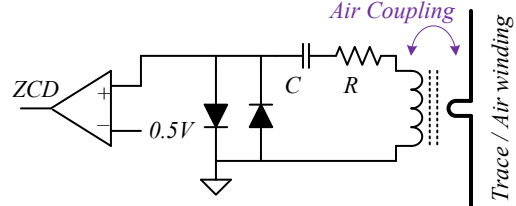


Fig. 6 Schematic of a Rogowski-type ZCD circuit

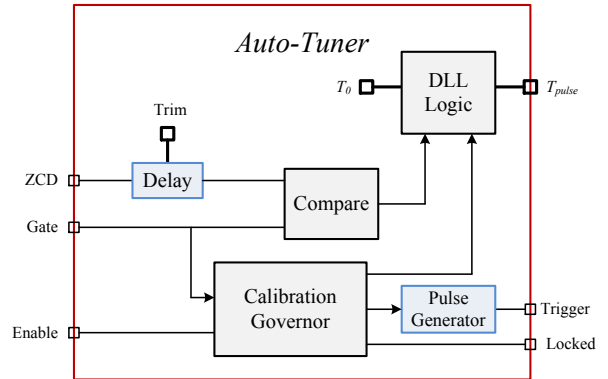


Fig. 7 Internal block-diagram of the auto-tuner module

which then form the output signal. A comparator is then used to translate the information on the diodes to a logic-level ZCD signal. Positive current on the main trace translates to '0' on the ZCD signal; close-to-zero or negative currents translate to '1'. It should be noted that since the current at the primary is clamped by the diodes rather than translated into a voltage representation, the typical integral correction of a Rogowski coil is not required. As will be detailed later by the simulation and experimental results, the information of the zero-crossing point is transferred with negligibly small delay up to frequencies above 10MHz.

D. Auto-tuner

The auto-tuning module consists of several internal units, as shown in Fig. 7. A calibration sub-governor monitors the activity of the sequencer and startup indication (e.g. soft-start signal) if needed, to determine the operation mode of the calibrator. A comparison unit evaluates the ZCD signal to the gate upon which the ZCD is applied to, and determines whether the resonator current is zero when the transistor turns off. The tuning logics applies digital DLL that primarily receives and outputs initial value of the tuned data, then gradually modifies it according to input from the compare module and instructions from the calibration sub-governor.

The auto-tuning module allows flexible choice of the resonant tank values, frequency and current handling capabilities. At power-up a one-time *lock-in* routine is initiated in which the tuner activates the sequencer directly to locate the resonance frequency of the tank. At normal running mode, the module observes the operation of the power-stage and fine-tunes the pulse-length as needed by an *adaptive fine-tuning* routine.

1. Start-up lock-in

The lock-in routine commences at power-up once the voltage levels have reached their operational values (either by soft-start, pre-bias, or by another converter). To allow the lock-in, the calibrator sub-governor initiates a pulsed *source* command to activate the converter at low repetition-rate. This allows the converter to transfer negligible amounts of energy to V_{out} and avoid excess deviations.

In this mode of operation, where the pulse repetition-rate is low, each time converter is triggered, the resonator current fundamentally starts from zero (see Fig. 8). The delay locked-loop then observes the status of the ZCD signal at each falling-edge of the gate-signal. Detection of zero or non-positive current in this case dictates that the gate pulse is too long, leading the modifier logic to coarsely reduce the gates' pulse-length as demonstrated in Fig. 8. In the case that zero-cross is not detected, then the pulse-length is coarsely increased. This procedure is repeated for several sequences (defined by design), then the source command is halted and a READY signal is set, allowing normal operation. Due to the resonant nature of the converter, lock-in can be obtained from an initial period offset of $\pm 100\%$ from the true value. This means for example, that the initial period can be loosely set and soft-switching operation is still assured for any given resonator network.

2. Adaptive fine-tuning

When the converter is in normal running mode, the adaptive fine-tuning module observes the status of the ZCD signal at each falling-edge of the gate-signal as it is being triggered by the main system-governor. Fine-tuning iterations are commenced, updating the timer-length register in the sequencer module once in every several cycles in a similar logic to the lock-in routine but with finer resolution. This allows slow fine-tuning and efficiency improvement over time, yet avoiding interferences which may occur from the tuning itself.

In continuous operation of a switched-resonator converter, it is important to notice that miss-calibration leads the resonator to maintain a non-zero value at the start of a switching state. This may have a cumulative effect the current at the end of the switching state, affecting the calibration as well as the amount of energy that is processed per cycle. Fig. 9 shows simulation results of a conventional RSCC operating with small delay between states versus continuous switching. It can be observed that although the state-time is identical for both cases, the miss-calibration is enhanced in continuous operation. This needs to be taken

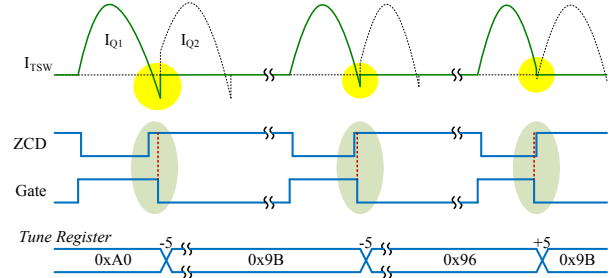


Fig. 8 Example waveforms for three iterations of the lock-in

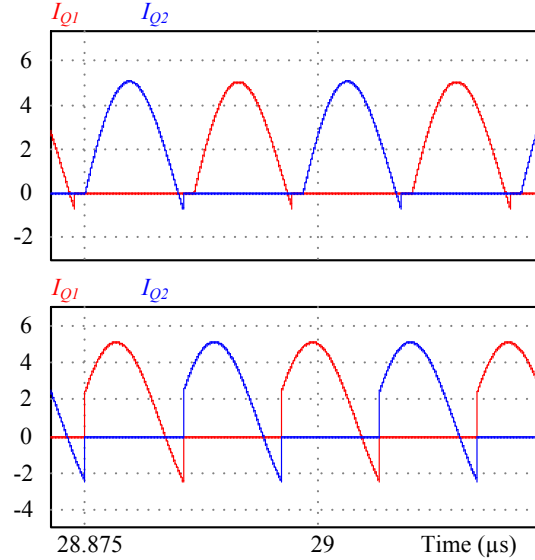


Fig. 9 Simulated current waveforms of late turn-off in a conventional RSCC: (a) when dead-time is applied; (b) without dead-time.

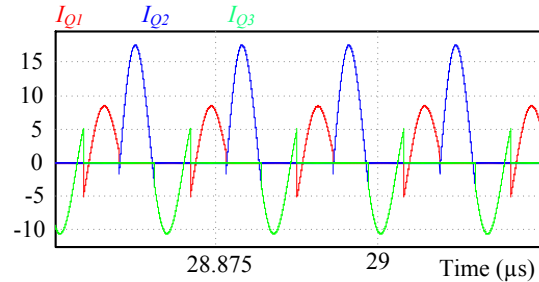


Fig. 10 Simulated current waveforms of late turn-off in a GRSCC without dead-time

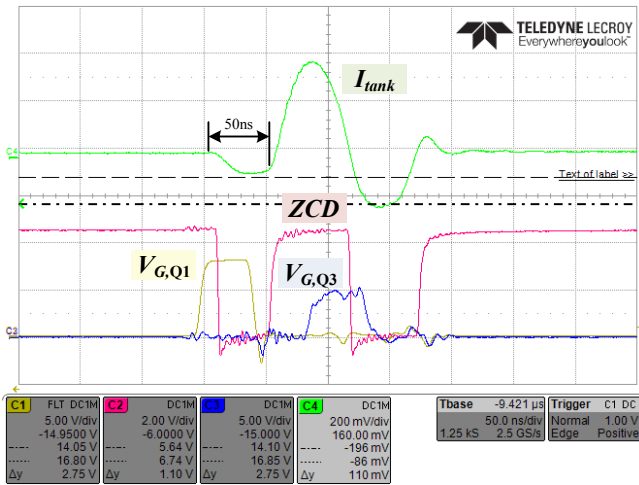
into account in the calibration resolutions chosen for the lock-in and fine-tuning routines.

Fig. 10 demonstrates a similar situation, this time on a GRSCC. In this case, miss-calibration is not enhanced, but it can be seen that the effects of miss-calibration are reversed for Q_1 : even though the state-duration is too long, the current remains positive at turn-off, due to the negative starting-point. If the ZCD is chosen to be applied on Q_1 and compared to its gating signal, then detection of zero or non-positive current dictates that the state-duration is too *short*, leading the modifier logic to *increase* the gates' pulse-length; if zero-cross is not detected, it is should be *decreased*.

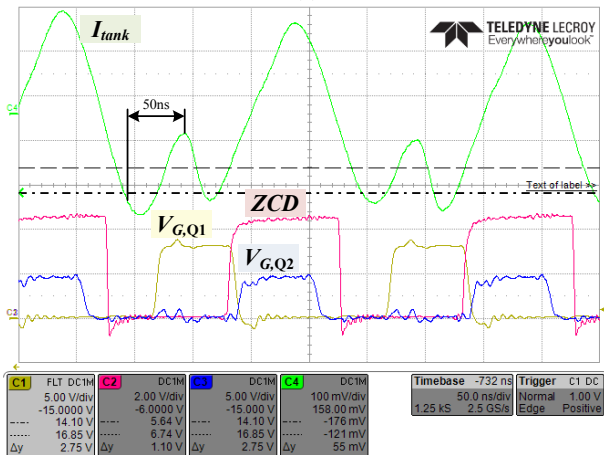
III. EXPERIMENTAL VERIFICATION

An experimental prototype that implements a 6MHz GRSCC (which translates to approximately 18MHz switching frequency per state) using discrete components has been built and tested to verify the operation of the control scheme, with resonator values of $C = 50\text{nF}$ and $L \approx 6\text{nH}$, loop resistance of $R \approx 20\text{m}\Omega$ and peak efficiency of $\eta \approx 80\%$. The controller has been implemented on FPGA (Altera Altera Cyclone IV FPGA development board DE-115) while the ZCD has been constructed on the PCB as described in Section II-C. The controller configured to initiate a 10-iteration for the startup lock-in procedure, and then operate in burst-mode in the ‘normal’ operation, performing a fine-tuning iteration at the 2nd sequence of each burst.

Fig. 11 demonstrates the reverse-logic that is needed to create fine-tuning during continuous operation of a non-calibrated system. This verifies the simulated results in Fig. 8 that predict *early* zero-crossing in the case that the calibrated time is too *short*, which is the opposite of the case of discontinuous mode. Fig. 12(a) shows the change in the register value for the initial calibration sequence. Oscillation



(a)



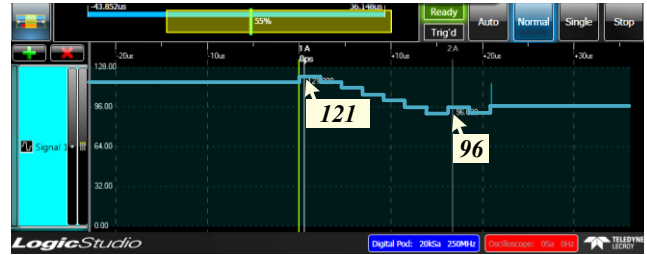
(b)

Fig. 11 Experimental waveforms of a non-calibrated power-stage (short time), demonstrating the current behavior for two cases: (a) during lock-in (b) during steady-state.

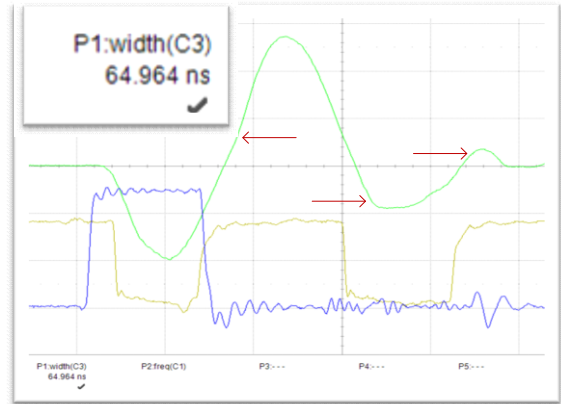
around the correct value can be observed after several iterations, indicating that timing converged to a steady-state point. Fig. 12(b,c), show the current waveforms before and after calibration, verifying the functionality of the lock-in routine.

IV. CONCLUSION

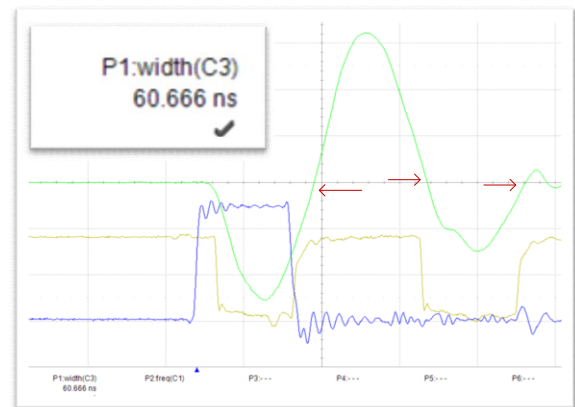
A generalized controller scheme for switched-resonator converters has been presented with adaptive zero-current switching capabilities allowing high variance resonator values of up to $\pm 100\%$ from the initially configured setting point. The controller modules provide a modularity of the units and compatibility of the controller to advanced resonator-based converters such as multi-voltage or multi-stage converters. A two-step approach has been employed



(a)



(b)



(c)

Fig. 12 Experimental waveforms of the Lock-in routine. (a) tune register convergence over time; (b) current and gate signals before lock-in; (c) current and gate signals after lock-in

for adaptive digital delay locked-loop calibration to allow fast convergence time without sacrificing accuracy. First a one-time coarse lock-in routine is implemented to identify the resonant frequency, then an adaptive fine-tuning approach follows throughout the operation of the converter to accurately match the operation frequency, obtain soft-switching, and compensate for any drifts in the resonant parameters either due to biasing, aging or temperature.

The controller has been implemented and verified for governing a 6MHz GRSCC (18MHz switching) showing consistent lock-in capabilities.

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